ACM, a Physical All-Region MOSFET Model: Computer Implementation and Applications

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Chapter 1

Introduction

The modeling of a MOS transistor is a requirement for the design of integrated circuits, since with the representation of its behavior through mathematical expressions we can better design and analyze circuits, not only using computer simulations but also hand calculations.

Given this importance, several MOSFET (Metal Oxide Semiconductor Field Effect Transistor) models have been developed. The Pao-Sah model, which is essentially based on the gradual channel approximation (GCA), is highly physical and is still used as a golden reference for testing accuracy [1]. However, this numerical solution is too involved to be used as a core for compact models. For this reason, other approximations, such as: the charge sheet approximation (CSA), and linearization of the inversion charge, have been employed in the development of new generation compact models, that can be divided into two groups: surface potential (ϕ_s)-based models (SP, PSP, HiSIM and MM11) and charge (Q_I)-based models (ACM, EKV and BSIM5).

The ϕ_s-based models and Q_I-based models were developed to substitute the threshold voltage V_T-based model. The V_T-based models assume that the surface potential is a very simple function of the gate voltage (V_G) resulting in approximate solutions that are only valid in particular regions of operation. This regional approach leads to inaccuracy between regions and consequently this class of models is not accurate enough to represent the moderate inversion region, widely employed in low supply voltage circuits. Despite their limitations such models have been successfully used in numerous design projects over many years [1].

As in the semiconductor industry the time-to-market is crucial, and the electrical simulation consumes a considerable part of the design project, it is essential that a compact model be not only accurate but also efficient. We here present the main equations, computer implementation and simulation

results of the Advanced Compact MOSFET (ACM) model, which is a charge-based model that fulfill these requirements since it is continuous, accurate and has a good speed performance [2].

Chapter 2

Advanced Compact MOSFET Model

The ACM is a charge-based compact model developed by the Integrated Circuits Laboratory at Federal University of Santa Catarina. In the ACM, all the large signal characteristics (currents and charges) and the small signal parameters ((trans) conductances and (trans) capacitances) are given by single-piece expressions for all regions of operation, including accumulation. The ACM model preserves the structural source-drain symmetry of the transistor and uses a reduced number of physical parameters. It is also charge-conserving and has explicit equations for the MOSFET 16 (trans)capacitances.

The model features can be summarized as follows:

- single-piece expressions with infinite order of continuity for all regions of operation;
- source-drain symmetry of the transistor;
- charge-conserving equations;
- physics-based equations for the vertical field dependence of carrier mobility, carrier velocity saturation and saturation voltage;
- geometric dependence of electrical parameters;
- independence of technology;
- easily measurable parameters.

In this chapter, we will summarize the computer implementation, parameters and main equations of the ACM model.

2.1 Computer Implementation

The ACM model was implemented in Eldo, an electrical simulator developed by Mentor Graphics, using the UDM (User Definable Model) tool. The code was written in C language, since the use of a different language would lead to a reduction in the speed performance [3]. The computer implementation of the ACM can be summarized in the flowchart below.

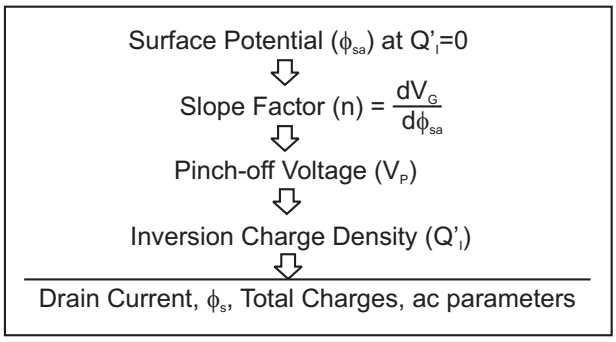

Figure 2.1: Flowchart of Computer Implementation.

2.2 Parameters

As can be observed in Table 2.1, in the ACM model all parameters have a well-known physical meaning. Moreover, this model uses a small set of parameters, 10.

Table 2.1: Parameters of the ACM model.

Parameters	Description	Unit
U0	Carrier mobility	$m^2/(Vs)$
TOX	Gate oxide thickness	m
NSUB	Substrate concentration	cm^{-3}
VFB	Flat-band voltage	V
LAMBDA	Channel length modulation factor	-
ALPHATHETA	Mobility reduction factor	m/V
M	Temperature factor	-
UCRIT	Longitudinal critical field for mobility degradation	V/m
XJ	Junction depth	m
SIGMA	Drain-induced barrier lowering factor	m^2

2.3 Core Model

The ACM is a compact model based on the gradual-channel approximation (GCA) and the charge-sheet approximation (CSA) [4]. The GCA allows the decomposition of the 2-D Poisson equation into two 1-D problems. The CSA assumes that the carriers populate a layer of zero thickness. Furthermore, in the ACM the charge density is linearized with respect to ϕ_{sa}, which is the surface potential calculated disregarding the inversion charge density [5], [6]. The choice of ϕ_{sa} as the linearization point is crucial to preserve the symmetry of the MOSFET. ϕ_{sa} is obtained from

$$(V_G - \mathbf{VFB} - \phi_{sa})^2 = \gamma^2(\phi_t(e^{-\phi_{sa}/\phi_t} - 1) + \phi_{sa}) \tag{2.1}$$

where V_G is the gate voltage, **VFB** [1] is the flat-band voltage and ϕ_t is the thermal voltage. The body effect factor (γ) is given by

$$\gamma = \frac{\sqrt{2q\varepsilon_s \mathbf{NSUB}}}{C'_{ox}} \tag{2.2}$$

where q is the electron charge, ε_s is the permittivity of silicon. The oxide capacitance per unit of area, C'_{ox}, is defined as

$$C'_{ox} = \frac{\varepsilon_{ox}}{\mathbf{TOX}} \tag{2.3}$$

where ε_{ox} is the permittivity of the oxide.

To solve (2.1) and evaluate ϕ_{sa} we used the algorithm presented in [7].

[1] Capital and bold alphanumericals in this work are model parameters described in Table 2.1.

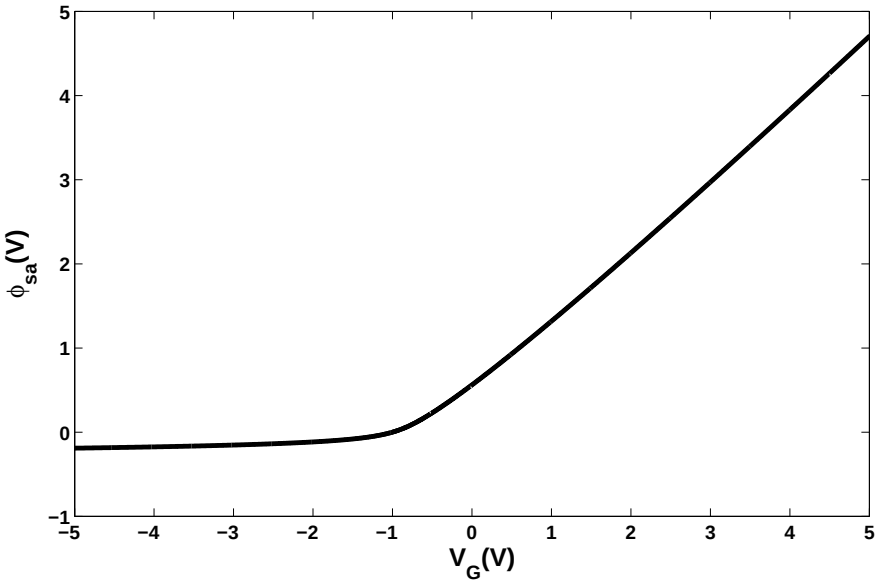

Figure 2.2: Surface potential using (2.1) for **VFB**=-1V.

The error in the evaluation of ϕ_{sa} expressed by

$$f = \frac{(V_G - \mathbf{V_{FB}} - \phi_{\mathbf{sa}})^{\mathbf{2}}}{\gamma^2} - \phi_t(e^{-\phi_{sa}/\phi_t} - 1) - \phi_{sa} \tag{2.4}$$

is shown in Figure 2.3.

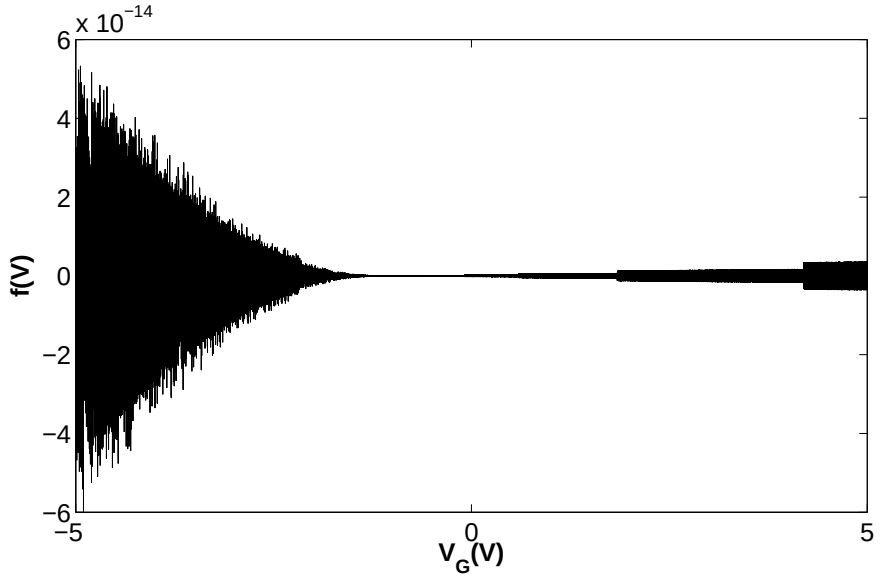

Figure 2.3: Error (2.4) in the evaluation of ϕ_{sa} for **VFB**=-1V.

It is worth mentioning that this high accuracy is essential in order to avoid spikes in the (trans)capacitances calculated via the charge derivative. The figures below illustrate this problem, where it can be observed that for an error less than $10^{-9}V$ the capacitance $C_{gb} = \partial Q_G/\partial V_B$ shows spikes in the region near the flat band voltage.

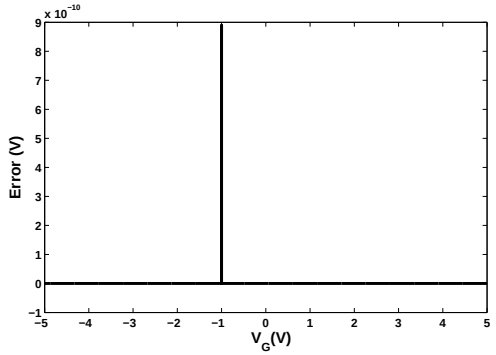

Figure 2.4: Error (2.4) in the evaluation of ϕ_{sa} for **VFB**=-1V.

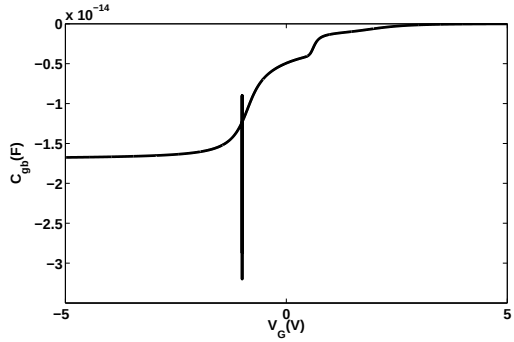

Figure 2.5: Capacitive coefficient C_{gb} in terms of gate voltage for **VFB**=-1V

As is shown in Figure 2.6 for high accuracy the transcapacitance, C_{gb}, presents a smooth transition for $V_G = \mathbf{VFB}$.

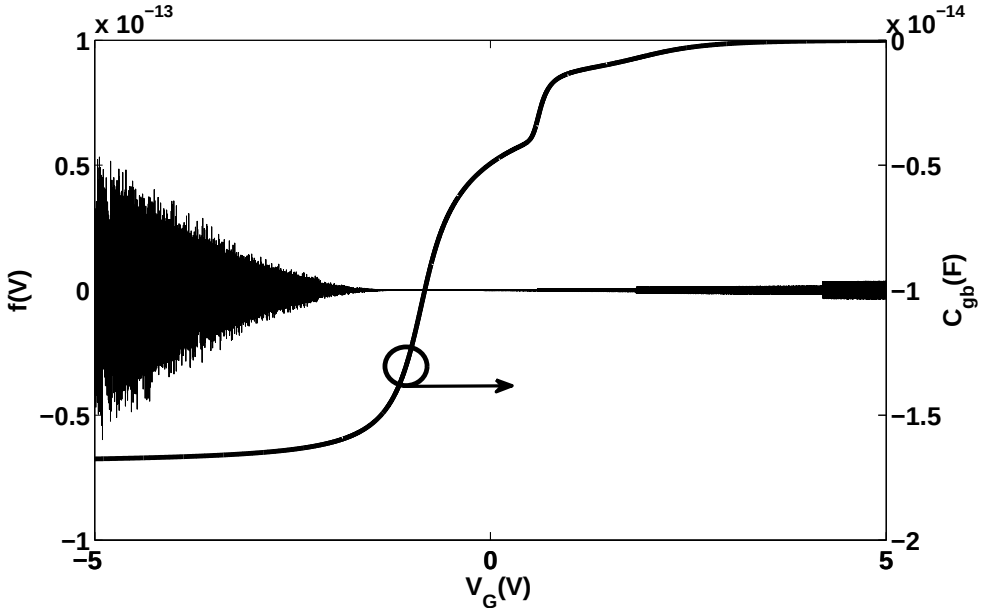

Figure 2.6: Error (2.4) in the evaluation of ϕ_{sa} and capacitive coefficient C_{gb} in terms of gate voltage for **VFB**=-1V

Figure 2.7 shows the number of iterations required to solve ϕ_{sa} with an error less than 10^{-13} V.

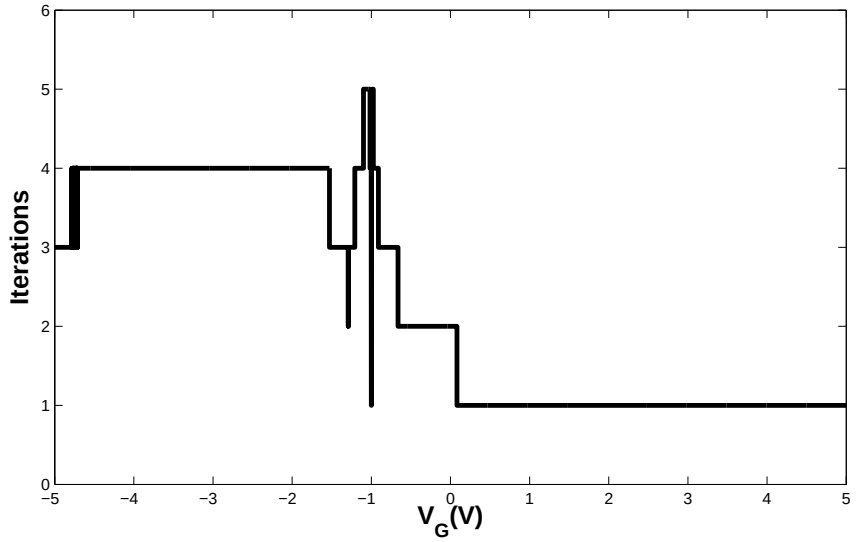

Figure 2.7: Number of iterations to solve (2.1) with error less than 10^{-13}V.

It should be noted that in the common operation region ($V_G > 0$) only one iteration is required.

2.3.1 Slope Factor

Taking the derivative of (2.1) with respect to the surface potential for zero inversion charge density results in

$$n = \frac{dV_G}{d\phi_{sa}} = 1 - \frac{1}{C'_{ox}}\frac{dQ'_B}{d\phi_{sa}} = 1 + \frac{C'_b}{C'_{ox}} \tag{2.5}$$

where C'_b is the bulk capacitance calculated at ϕ_{sa}. In the ACM model, the slope factor n is a function of the gate voltage only [8]

$$n = 1 + \frac{\gamma(1 - e^{-\phi_{sa}/\phi_t})}{2(sign(\phi_{sa}))\sqrt{\phi_{sa} + \phi_t e^{-\phi_{sa}/\phi_t} - \phi_t}}. \tag{2.6}$$

A plot of n vs. V_G is shown in Figure 2.8 . For strong inversion, n is slightly greater than one. On the other hand, in accumulation the bulk charge increases almost linearly with the gate voltage; therefore, the slope factor increases following this same trend, as can be observed in Figure 2.8 .

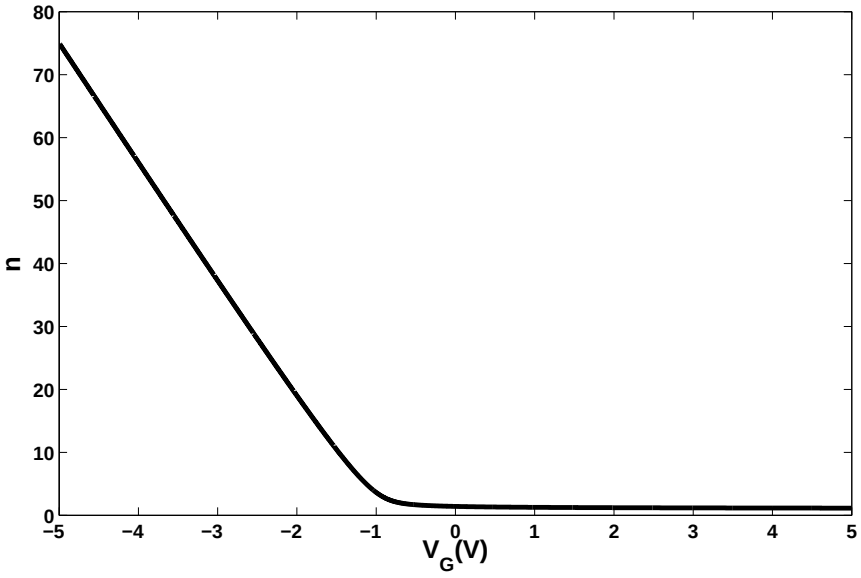

Figure 2.8: Slope factor (2.6) in terms of gate voltage.

2.3.2 Pinch-off Voltage

An important dc parameter of the ACM model is the pinch-off voltage V_P. To be succinct, V_P is the channel potential at which the inversion charge density is equal to the thermal charge $Q'_{IP} = -nC'_{ox}\phi_t$. It is related to ϕ_{sa} by

$$V_P = \phi_{sa} - 2\phi_F - \phi_t \left(1 + ln\left(\frac{n}{n-1}\right)\right) \tag{2.7}$$

where ϕ_F is the Fermi potential. The plot of V_P in terms of the gate voltage is presented in Figure 2.9.

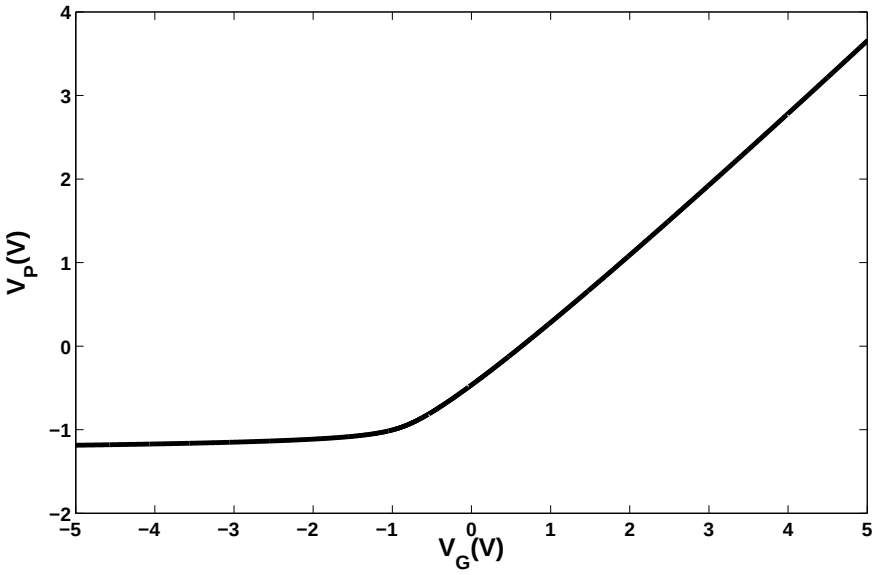

Figure 2.9: Pinch-off voltage (2.7) in terms of gate voltage.

2.3.3 Unified Charge Control Model

To evaluate the inversion charge density, which is the key variable of the ACM, the unified charge control model (UCCM) was used [9]. Combining UCCM and the main approximation of the ACM [10]

$$dQ'_I = nC'_{ox}d\phi_s \tag{2.8}$$

we have

$$V_{P_{DIBL}} - V_{D(S)} = \phi_t \left[\frac{Q'_{IP} - Q'_{ID(S)}}{nC'_{ox}\phi_t} + ln\left(\frac{Q'_{ID(S)}}{Q'_{IP}}\right)\right] \tag{2.9}$$

where $V_{P_{DIBL}}$ is pinch-off voltage including the DIBL effect, defined in (2.17), V_S is the source voltage and V_D is the drain voltage. Q'_{ID} and Q'_{IS} are the inversion charge density at drain and source, respectively.

To solve (2.9) the last algorithm presented in [11], was used, which gives an error (Figure 2.10) smaller than 10^{-7}V over the whole inversion region and only one iteration is required [2], [12].

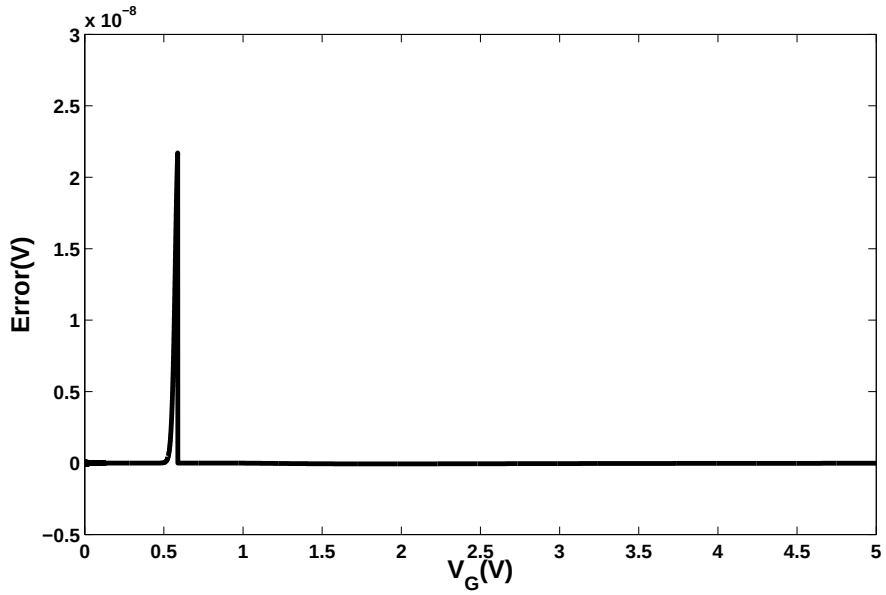

Figure 2.10: Error to evaluate $Q'_{IS(D)}$ using (2.9).

2.4 Channel Length Modulation

The approach employed to find an analytical formulation for the saturation region divides the channel into two sections [4]. Using this formulation, the current can be calculated using the expression derived under the gradual channel approximation but considering the effective channel length of the device to be reduced by the length ΔL of the drain section. In addition, the voltage drop in the drain section must be accounted for to calculate the effective drain-to-source voltage V_{DSeff}. The dependence of the effective channel length on the drain-to-source voltage, which is illustrated in Figure 2.11, is referred to as channel length modulation (CLM) .

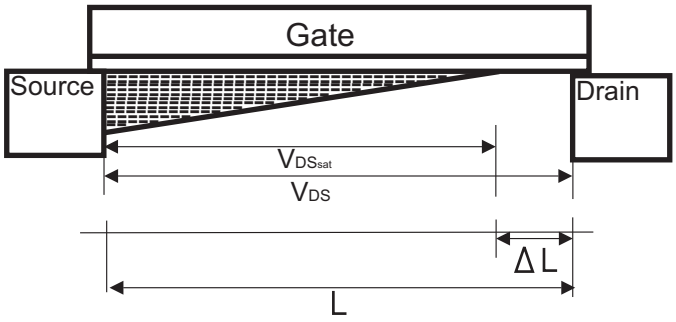

Figure 2.11: Channel Length Modulation.

2.4.1 Effective Length

The effective length is defined as [4]

$$L_{eff} = L - \Delta L \tag{2.10}$$

where the channel length shortening (ΔL) is, according to this model, given by

$$\Delta L = \mathbf{LAMBDA} \cdot L_C \cdot ln\left[1 + \frac{(V_{DS} - V_{DSeff})}{L_C \mathbf{UCRIT}}\right] \tag{2.11}$$

where V_{DSeff} is defined in (2.16) and L_C is

$$L_C = \sqrt{\frac{\varepsilon_s \mathbf{XJ}}{C'_{ox}}}. \tag{2.12}$$

2.4.2 Effective Drain-to-Source Voltage

To evaluate the effective drain-to-source voltage (V_{DSeff}), first we have to calculate the inversion charge density at the drain end of the channel (Q'_{IDsat}) [13]

$$Q'_{IDsat} = Q'_{IS} - nC'_{ox}\phi_t - q_o\left[1 - \sqrt{1 - \frac{2(Q'_{IS} - nC'_{ox}\phi_t)}{q_o} + \frac{(nC'_{ox}\phi_t)^2}{{q_o}^2}}\right] \tag{2.13}$$

where q_o is given by

$$q_o = n \cdot C'_{ox} \cdot L \cdot \mathbf{UCRIT}. \tag{2.14}$$

In the ACM model, the drain-to-source voltage for saturation is given by

$$V_{DSsat} = \phi_t \left(\frac{q'_{IDsat} - q'_{IS}}{nC'_{ox}\phi_t} + ln\left(\frac{q'_{IS}}{q'_{IDsat}}\right)\right) \tag{2.15}$$

where q'_{IS} and q'_{IDsat} are the inversion charge density at source and at the drain end of the channel normalized with respect to Q'_{IP}, respectively. Finally, to obtain the effective drain-source voltage we used the smooth function below [13]

$$V_{DSeff} = \frac{V_{DS}}{\left(1 + \left(\frac{V_{DS}}{V_{DSsat}}\right)^4\right)^{1/4}}. \tag{2.16}$$

2.5 Drain-Induced Barrier Lowering

Reverse bias of the drain junctions creates a field pattern that can lower the potential separating the source from the drain, resulting in increased injection of carriers by the source [4]. This phenomenon is referred to as drain-induced barrier lowering (DIBL) and is included in the ACM model, increasing the pinch-off voltage

$$V_{P_{DIBL}} = V_P + \frac{\mathbf{SIGMA}}{nL_{eff}^2}\left(V_S + V_D\right). \tag{2.17}$$

2.6 Carrier Mobility

The mobility varies with temperature according to the approximate expression

$$\mu = \mathbf{UO}(T/T_o)^{-\mathbf{M}} \tag{2.18}$$

for the temperature range 200-400K. T_0 is the reference temperature and $\mathbf{M}$ lies in the range 1.2-1.4 for p-channel transistors and in the range 1.4-1.6 for n-channel transistors.

The influence of the vertical electric field in the mobility is expressed by

$$\mu_{eff} = \frac{\mu}{1 - \mathbf{ALPHATHETA} \cdot (Q_B + \eta Q_I)} \tag{2.19}$$

where Q_B is the total bulk charge, Q_I is the total inversion charge and η is 1/2 for NMOS transistors and 1/3 for PMOS transistors [4].

To include the effect of velocity saturation the following approximation for the field-dependent mobility was employed on mobility

$$\mu_s = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{v_{lim}} \frac{d\phi_s}{dy}} = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{v_{lim}} \frac{dQ'_I}{nC'_{ox}dy}} \tag{2.20}$$

2.7 Drain Current

Using (2.20) the drain current equation is given by

$$I_D = \frac{\mu_{eff} W}{2nC'_{ox} L_{eff}} \frac{{Q'_F}^2 - {Q'_R}^2}{1 + \frac{\mu_{eff}(Q'_R - Q'_F)}{qo}} \tag{2.21}$$

where

$$Q'_{F(R)} = Q'_{IS(D)} - nC'_{ox}\phi_t \tag{2.22}$$

This equation of the drain current includes, through μ_{eff}, the effects of both longitudinal and vertical electric fields. For the calculation of the drain current, the factor $1+\mu_{eff}(Q'_R - Q'_F)/qo$ in the denominator of equation (2.21) is replaced with a continuous and smooth function to avoid discontinuities in the derivatives of the drain current around $V_{DS} = 0$ [13].

2.8 Total charges

The effect of velocity saturation is included in the total charges using the virtual charge density

$$Q'_{VS(D)} = Q'_{IS(D)} - nC'_{ox}\phi_t + \frac{I_D}{W v_{lim}} \tag{2.23}$$

where $I_D/W v_{lim}$ is the saturation charge, i.e., the minimum amount of carrier charge density required to sustain a channel current equal to I_D [14]. The virtual charge is the real inversion charge plus the pinch-off charge (diffusion increases the current) minus the saturation charge (velocity saturation reduces the current).

The ACM model has compact expressions for total charges valid in all regions. These expressions including both velocity saturation and short-channel effect are summarized in Table 2.2.

Table 2.2: Total Charges

Variable	Expression
α	$\frac{Q'_{VD}}{Q'_{VS}}$
Q_I	$WL_{eff}\left[\frac{2(1+\alpha+\alpha^2)}{3(1+\alpha)}Q'_{VS}+nC'_{ox}\phi_t\right]-\frac{LI_D}{v_{lim}}$
Q_S	$\frac{WL_{eff}^2}{L}\left[\frac{(6+12\alpha+8\alpha^2+4\alpha^3)}{15(1+\alpha)^2}Q'_{VS}-\frac{nC'_{ox}\phi_t}{2}\right]-\frac{LI_D}{2v_{lim}}$
Q_D	Q_I-Q_S
Q_B	$-(\frac{n-1}{n})Q_I+WL_{eff}\left(-sign(\phi_{sa})\gamma C'_{ox}\sqrt{\phi_{sa}+\phi_t(e^{-\phi_{sa}/\phi_t}-1)}\right)$
Q_G	$-Q_B-Q_I$

Figure 2.12 shows the total charges in terms of the gate voltage obtained from simulations using the ACM model implemented in ELDO.

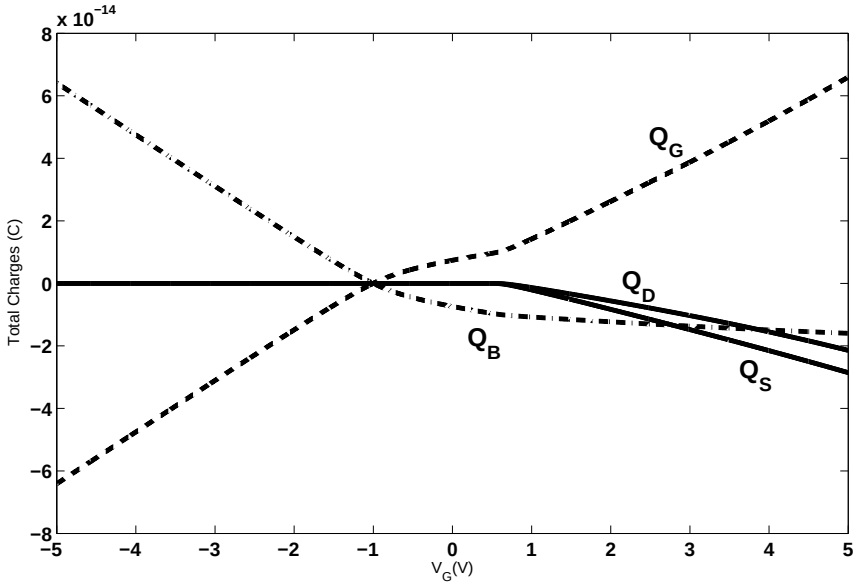

Figure 2.12: Total charges (Q_G, Q_B, Q_D, Q_S) in terms of gate voltage for $V_{DS} = 3V$ and **VFB**=-1V.

2.9 Capacitive Coefficients

The four-by-four matrix of the MOSFET intrinsic capacitances for quasi-static operation is defined according to

$$\begin{pmatrix} dQ_G/dt \\ dQ_S/dt \\ dQ_D/dt \\ dQ_B/dt \end{pmatrix} = \begin{pmatrix} C_{gg} & -C_{gs} & -C_{gd} & -C_{gb} \\ -C_{sg} & C_{ss} & -C_{sd} & -C_{sb} \\ -C_{dg} & -C_{ds} & C_{dd} & -C_{db} \\ -C_{bg} & -C_{bs} & -C_{bd} & C_{bb} \end{pmatrix} \begin{pmatrix} dV_G/dt \\ dV_S/dt \\ dV_D/dt \\ dV_B/dt \end{pmatrix}. \quad (2.24)$$

Only nine out of the sixteen capacitive coefficients in (2.24) are linearly independent, due to charge conservation and charge transfer dependence on voltage differences only [6], [14]. Table 2.3 presents nine capacitive coefficients, including velocity saturation and short-channel effects, calculated as in [4], [14].

Table 2.3: The nine capacitive coefficients

Variable	Expression
$C_{gs}(**)$	$\frac{2}{3}WL_{eff}C'_{ox}\frac{1+2\alpha}{(1+\alpha)^2}\frac{q'_{IS}}{1+q'_{IS}} + \frac{L_{eff}g_{ms}(1-\alpha)^2}{3nv_{lim}(1+\alpha)^2}$
$C_{gd}(**)$	$\frac{2}{3}WL_{eff}C'_{ox}\frac{\alpha^2+2\alpha}{(1+\alpha)^2}\frac{q'_{ID}}{1+q'_{ID}} + \frac{L_{eff}g_{md}(1-\alpha)^2}{3nv_{lim}(1+\alpha)^2}$
$C_{bs}(**)$	$(n-1)C_{gs(d)}$
$C_{gb} = C_{bg}(*)$	$\frac{n-1}{n}\left(C_{ox} - C_{gso} - C_{gdo} - \frac{L_{eff}g_{mg}(1-\alpha)^2}{3v_{lim}(1+\alpha)^2}\right)$
$C_{ds}(**)$	$-\frac{4}{15}nC'_{ox}W\frac{L^2_{eff}}{L}\frac{\alpha+3\alpha+\alpha^2}{(1+\alpha)^3}\frac{q'_{IS}}{(1+q'_{IS})} - \frac{1}{30}\frac{g_{ms}L^2_{eff}}{v_{lim}L}\frac{(3\alpha+7)(1-\alpha)^2}{(1+\alpha)^3}$
$C_m = C_{dg} - C_{gd}$	$\frac{C_{sd}-C_{ds}}{n}$

(*) C_{gso} and C_{gdo} are the first terms in C_{gs} and C_{gd}, respectively.(**) C_{bd} and C_{sd} are obtained from C_{bs} and C_{ds}, respectively, by simply exchanging S↔D and $\alpha \leftrightarrow 1/\alpha$.

Figure 2.13 presents a numerical comparison between C_{gb} and C_{gb}. This comparison shows that the approach $C_{gb} = C_{bg}$ is a good approximation, specially because difference occurs in the region where these capacitive coefficients are small.

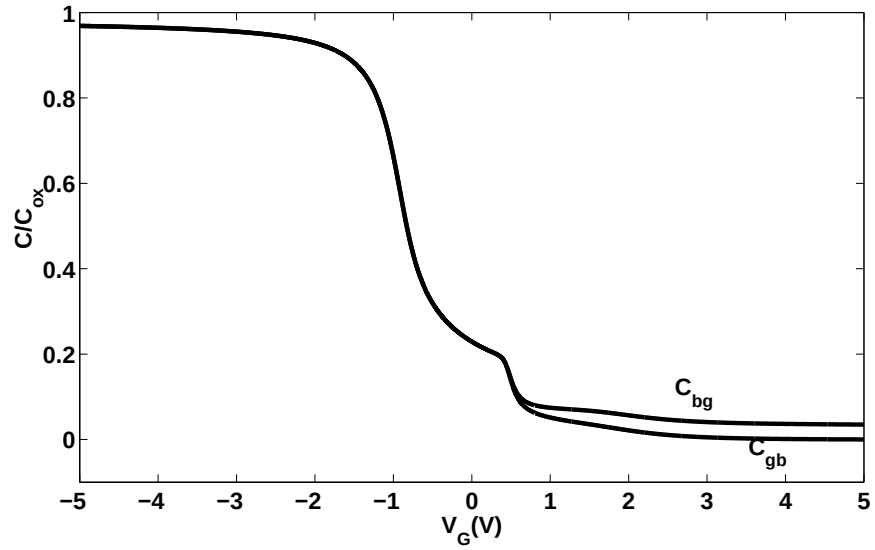

Figure 2.13: Numerical comparison between C_{gb} and C_{bg}.

Figure 2.15 presents a comparison between C_{gb} numerical and C_{gb} obtained from expression shows in Table 2.3.

2.9.1 Simplified small-signal MOSFET model

The schematic of the simplified small-signal MOSFET model is presented in Figure 2.14. This model not only preserves the inherent symmetry of the MOSFET but also represents accurately the MOSFET ac behavior for operating frequencies such $\omega\tau_1 << 1$, where τ_1 is the first-order time constant for non-quasi-static operation [8].

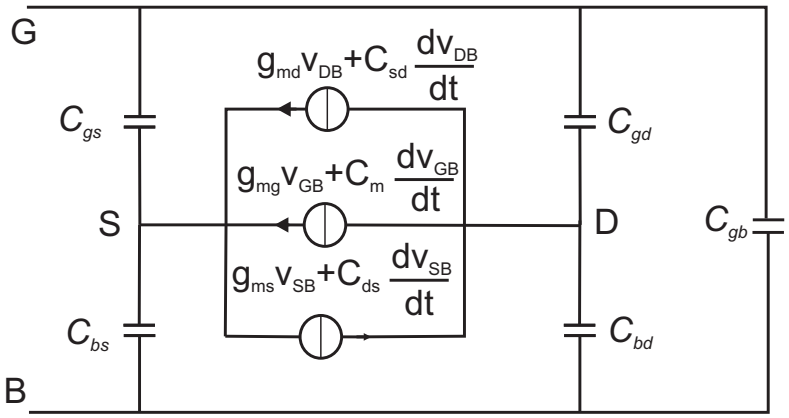

Figure 2.14: Simplified small-signal MOSFET model.

Figure 2.15 shows five capacitances of the simplified small-signal MOSFET model. In this plot, solid lines (——) are the capacitive coefficients obtained via total charge (Table 2.2) derivative and dashed lines (- -) are the coefficients using the expressions from Table 2.3.

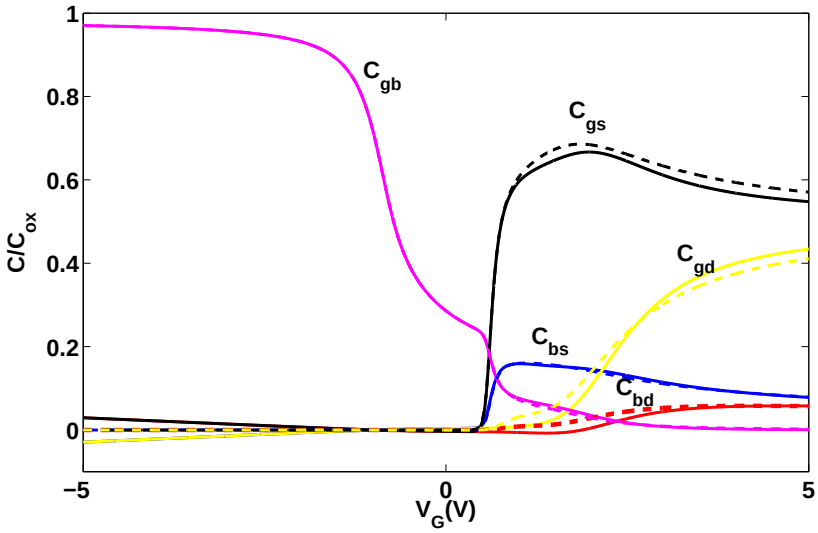

Figure 2.15: Five normalized capacitances of the simplified small-signal MOSFET model for $V_{DS} = 3V$ and $V_{FB} = -1V$.

Figure 2.15 shows a good agreement between the expressions from Table 2.3 (solid lines (——)) and coefficients obtained from the derivative of the total charges (dashed lines (- -)).

Chapter 3

Simulation results

In this chapter, we present results from the ACM model implemented in ELDO and comparison with other compact models [1]. Firstly, we present some benchmark tests and in the following section we present the comparison of simulation time from several compact models.

3.1 Benchmark Tests

Benchmark tests are employed for evaluate the quality of compact models. In this section, we show the Gummel Symmetry Test and the MOSFET current divider [2], [13], [12].

3.1.1 MOSFET Current Dividers

MOSFET current dividers are useful components of analog circuits that can be also be used to test the quality of compact models. Figure 3.1 shows one such divider. In this array, all transistors have the same dimensions and share a common substrate. A first order analysis of this topology shows that the reference current is successively divided by two. In order to reduce deviations from the expected values owing to short-channel effects, long and wide channel devices ($W = 100\mu m$ and $L = W = 20\mu m$) have been employed in the current divider [12].

[1] All simulations used the models implemented in ELDO version 6_6, release 2005_3, with default parameters

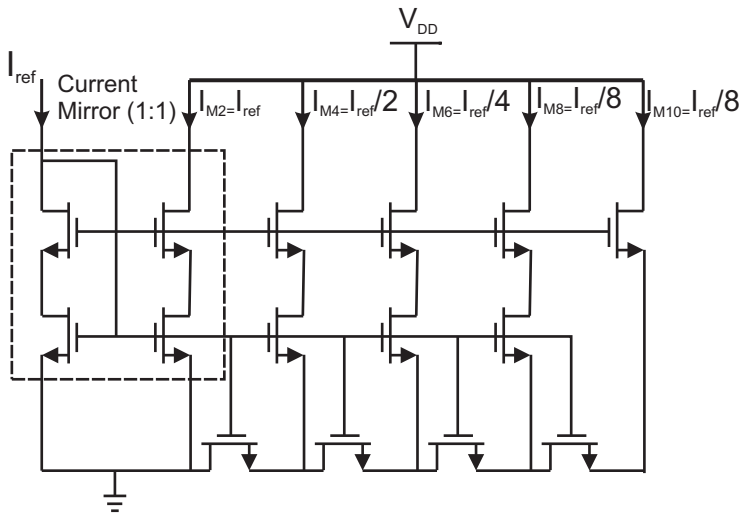

Figure 3.1: M2M network

Figure 3.2 shows that the maximum normalized error using the ACM model does not exceed 0.04% for a 3-decade variation of the input reference current I_{REF}.

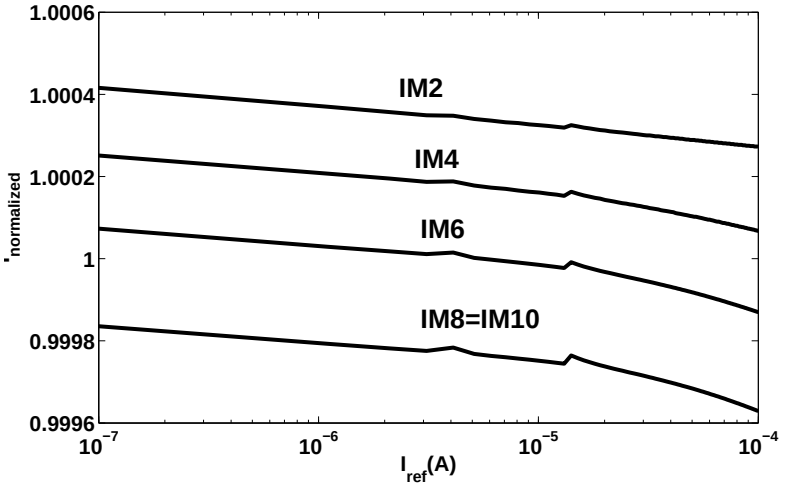

Figure 3.2: Normalized branch currents ($I_{NORMALIZED}$) vs. input current reference (I_{REF}) obtained from simulation of the circuit presented in Figure 3.1 using the ACM model.

On the other hand the simulations carried out using PSP shows high relative error for the current and spikes for the current ratios showing that

PSP, at least this version, is not able to represent consistently the series association of transistors.

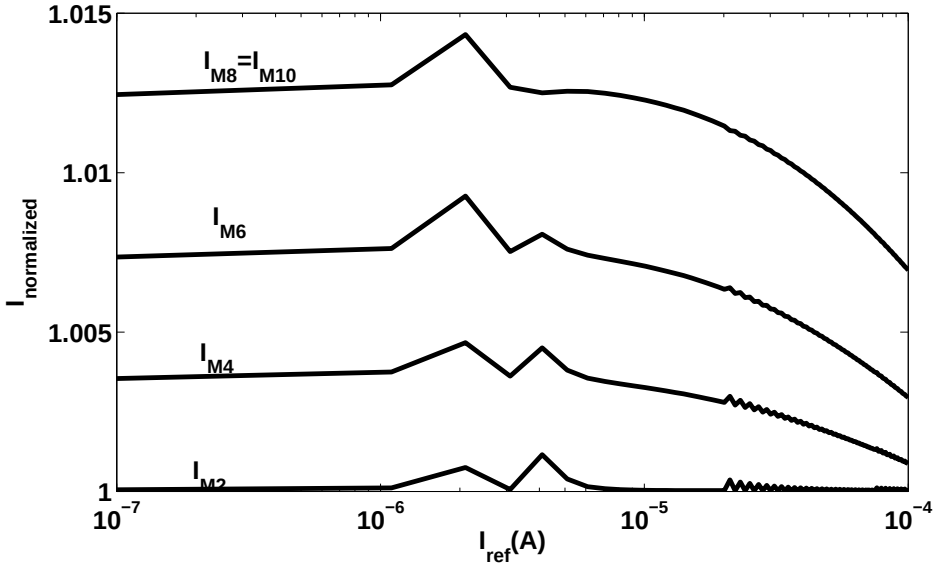

Figure 3.3: Normalized branch currents ($I_{NORMALIZED}$) vs. input current reference (I_{REF}) obtained from simulation of the circuit presented in Figure 3.1 using the PSP model.

3.1.2 Gummel Symmetry Test

The Gummel Symmetry Test (GST) is used to show the symmetry of the forward and reverse models of operation and the continuity, around the origin, of the drain current and charges as well as their derivatives [12]. In this test the drain-to-source voltage is $2V_X$

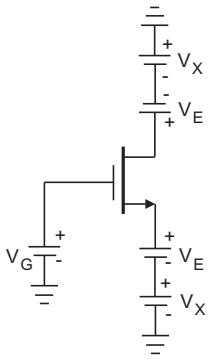

Figure 3.4: Squematic used in the Gummel Symmetry Test.

As it is clear in Figure 3.5, the ACM model shows the expected behavior, the derivatives are continuous and the transition around $V_{DS} = 0V$ is smooth.

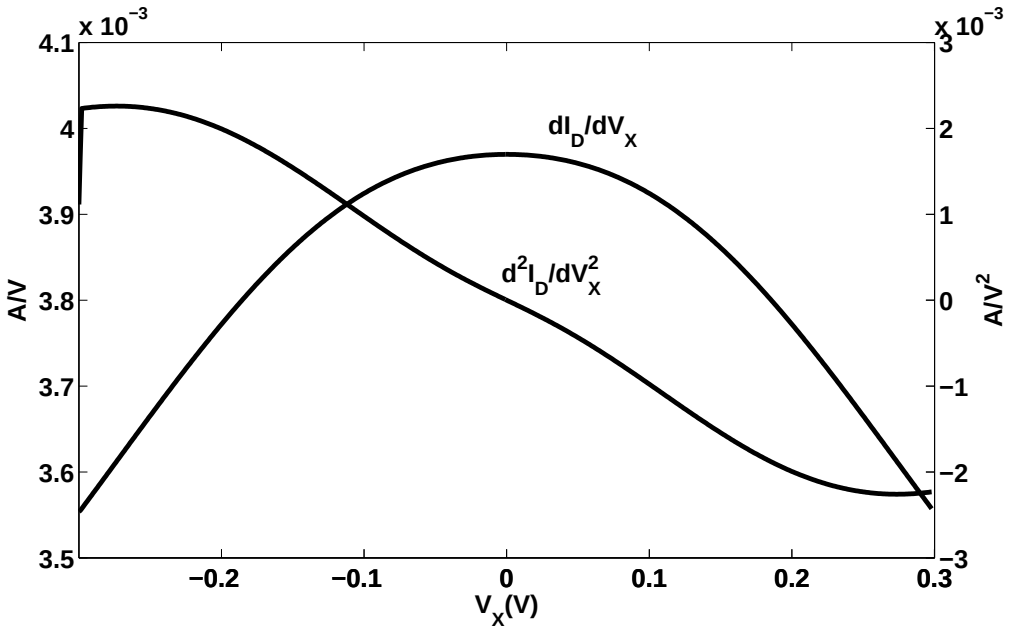

Figure 3.5: Transconductance ($\partial I_D/\partial V_x$) and derivative of transconductance ($\partial^2 I_D/\partial V_x^2$) using the ACM model implemented in ELDO for $V_E = 1V$, $W = 10\mu$ and $L = 10\mu$.

Figure 3.6 shows the result simulated with the PSP model. As the drain current is an odd function of V_X, the second derivative must be zero for $V_{DS} = 0V$ and this passage through zero must be unique, however the simulation using the PSP model presents three passages of the second derivative of the current through zero.

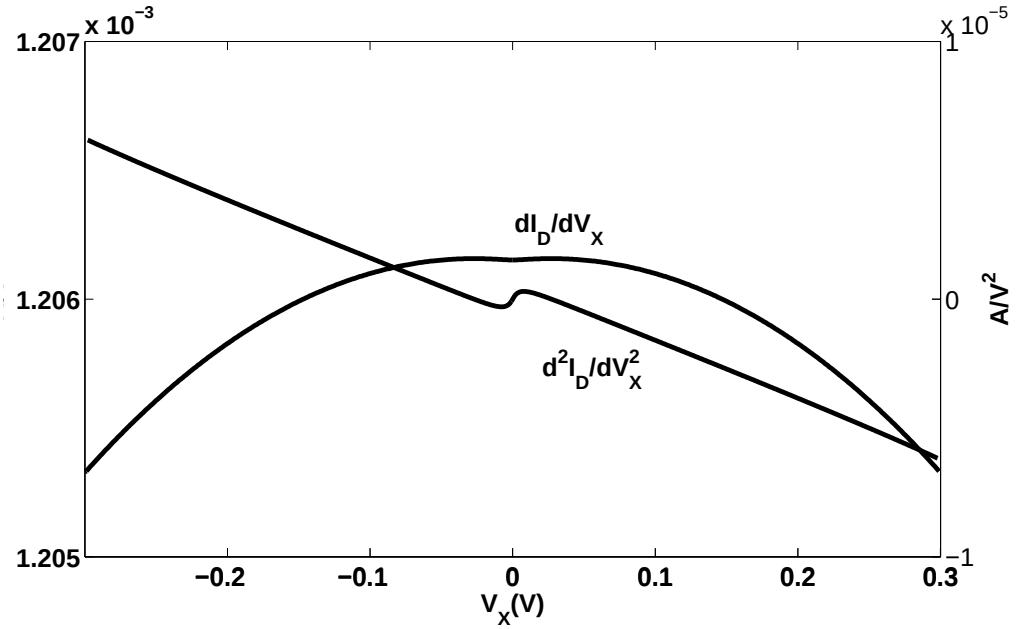

Figure 3.6: Transconductance ($\partial I_D/\partial V_x$) and derivative of transconductance ($\partial^2 I_D/\partial V_x^2$) using the PSP model implemented in ELDO for $V_E = 1V$, $W = 10\mu$ and $L = 10\mu$.

3.2 Simulation Time

In the semiconductor industry the time-to-market is crucial, therefore the compact model must be fast, however this speed can not decrease the accuracy. For this reason, in this section we present a comparison of the simulation time for several compact models.

3.2.1 Circuit description

To evaluate the computer performance we used the 7 different circuits. The circuits are described below

- schmitfast - CMOS Schmitt trigger with large amount of feedback - 6 MOS transistors.
- schmitslow - CMOS Schmitt trigger with small amount of feedback - 8 MOS transistors.
- g1310 - Circuit composed of 14 MOS transistors, 21 capacitors, 28 diodes and 56 resistors.

- hussamp - 3-stage opamp, internally compensated - 16 MOS transistors, 2 capacitors and 1 resistor.
- ab_ac - Class AB opamp - 31 MOS transistors, 22 capacitors and 1 resistor.
- ab_integer - Class AB opamp - 31 MOS transistors, 24 capacitors and 3 resistor.
- cram - Circuit composed of 60 MOS transistors and 42 capacitors.

3.2.2 Simulation Results

In all simulations, we used the same machine (Processor:Pentium 4 1.6 GHz and RAM: 768 MB) and the models implemented in ELDO version 6_6, release 2005_3, with default parameters.

Table 3.1: Simulation results using several compact models.

Circuit	Analysis	ACM	EKV(*)	MM11(*)	PSP(*)	BSIM4(*)	HiSIM(*)
schmitfast	DC	3s775ms	0.522	1.663	1.274	0.968	1.332
schmitslow	DC	5s884ms	0.499	1.414	1.325	0.972	1.201
g1310	TRAN	1s536ms	0.732	1.045	0.898	0.779	0.939
hussamp	TRAN	6s409ms	1.007	1.073	1.064	1.013	1.016
ab_ac	AC	3s100ms	1.066	2.238	1.745	1.193	1.519
ab_integer	TRAN	2s901ms	1.018	1.078	1.114	1.031	1.044
cram	TRAN	1s025ms	0.263	1.902	1.224	1.263	1.454

(*) Simulation times normalized with respect to ACM.

Although the EKV presents the best speed performance, Table 3.1 shows that the ACM model presents in general better speed performance than the surface-based (MM11, PSP, HiSIM) models.

Chapter 4

Design Example

To demonstrate the usefulness of the ACM model, we describe the design project of a folded cascode operational amplifier as presented in [8]. In Figure 4.1 and Figure 4.2 are shown schematics of folded cascode amplifier and bias network, respectively.

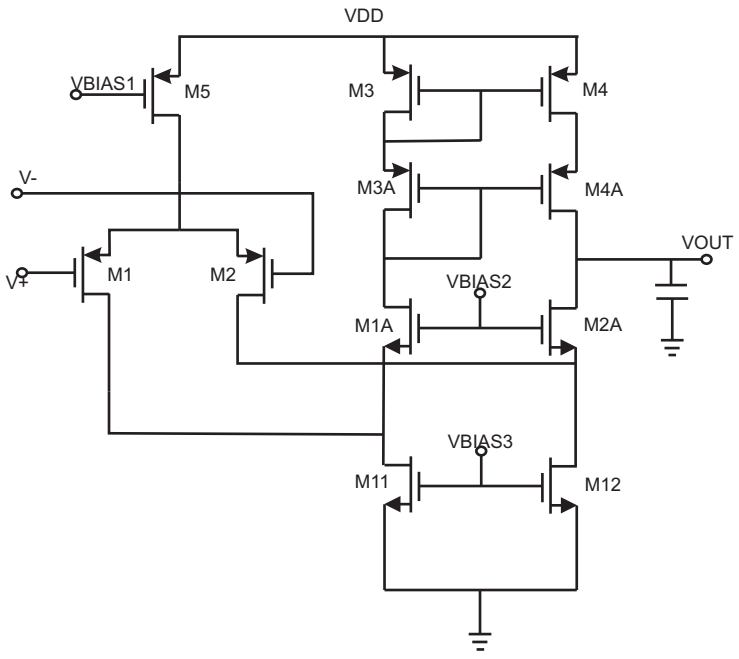

Figure 4.1: Folded Cascode opamp.

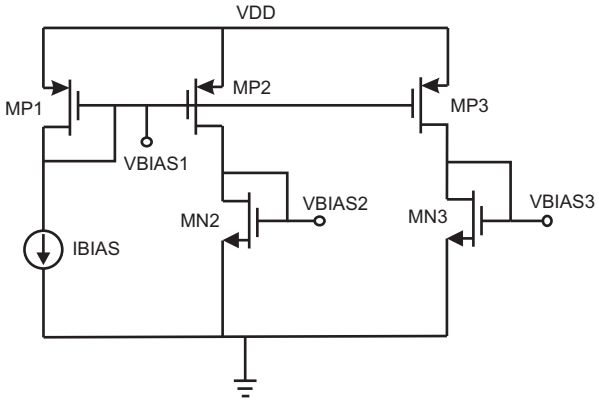

Figure 4.2: Bias Network.

Table 4.1 presents the specifications of the design project.

Table 4.1: Specifications

	Specifications
GBW	10 MHz
A_{VO}	>100 dB
SR	>4 V/μs

4.1 Hand design

In this design, we used the ACM equations for later comparison with simulation results from PSP. Table 4.2 summarizes the expressions used in this design.

Table 4.2: Design-oriented expressions for the long-channel MOSFET in saturation.

Parameter	Expression
if	I_D/I_S
I_S	$\frac{W\mu C'_{ox} n {\phi_t}^2}{L}$
g_{mg}	$\frac{I_D}{n\phi_t}\frac{2}{\sqrt{1+if}+1}$
$\frac{L}{W}$	$\frac{2\mu C'_{ox}\phi_t}{g_{mg}}\left(\frac{I_D}{ng_{mg}\phi_t}-1\right)$
V_{DSsat}	$\phi_t\left(\sqrt{1+if}+3\right)$

The first parameter determined in our design was the transconductance g_{m1} of the input transistors from

$$g_{m1} = 2\pi.GBW.C_L \tag{4.1}$$

which gives g_{m1}= 314 $\mu A/V$. The minimum current that meets the transconductance specification is obtained in weak inversion, i.e., making $if \rightarrow 0$ in the expression of g_{mg}/I_D in Table 4.2. One can easily verify that, for if $if \rightarrow 0$, $g_{mg} \rightarrow I_D/n\phi_t$. Therefore, the minimum current of the input transistors M1 and M2 is I_{D1min}= 9.1 μA (we used n=1.12 and ϕ_t = 25.9 mV). In our design we have chosen the commonly employed relationship between currents $I_{D11} = I_{D12} = I_{D5}/2$. In this way, both the rising and falling slew rates are equal to I_{D5}/C_L. Therefore, to comply with the required slew rate spec

$$SR = \frac{I_{D5}}{C_L} \tag{4.2}$$

we need $I_{D5} = 2I_{D1} > 20\mu A$. We decided to choose the bias current $I_{D5} = 27\mu A$. Using ID1=13.5μA together with gm1= 314 $\mu A/V$ we find the inversion level if≅3. We decided to set the inversion levels of all transistors, except one in the bias network, equal to 3. The advantage of having such a low inversion level is that the saturation voltage of the transistors is around $5\phi_t$ ≅130 mV, a relatively small value. Once we had chosen the drain current of the transistors, we could readily find the aspect ratios using the expression in Table 4.2, which gives L/W as a function of the drain current and transconductance, besides the technological parameters.

Table 4.3: Transistors dimensions

Transistor	L(μm)	W(μm)
M1,M2	0.5	13.5
M11,M12	0.5	27
M3,M4	0.5	13.5
M1A,M2A	0.5	13.5
M3A,M4A	0.5	13.5
M5	0.5	27
MP5	0.5	27
MP1,MP2,MP3	0.5	13.5
MN2	2(4x0.5)	13.5
MN3	0.5	13.5

Transistors M3A, M3, M4A, M4 form a self-biased cascode current mirror, which is generally assumed to be not a good choice for low-voltage circuitry. In our design, however, the gate-to-source voltage of the diode-connected transistors is relatively small due to both the low threshold voltage and low inversion level.

The bias network (Figure 4.2) is driven by a current source IBIAS=13.5 μA. Note that the aspect ratios of MP1 (MP2, MP3) and MN3 are equal to one half the aspect ratios of M5 and M11, respectively. On the other hand, the bias voltage VBIAS2 must be, at least, equal to the gate-to-source voltage of M1A plus the saturation voltage V_{DSsat} of M11 [15], which is approximately equal to $5\phi_t \cong 130$ mV. The inversion level of MN3 must be such that

$$V_{GS(MN3)} = V_{BIAS3} = V_{GS(M1A)} + V_{DSsat(M11)} + \Delta V \tag{4.3}$$

where ΔV is a safety margin which has been included in the design equations to ensure that the drain voltage of M11 is slightly above the drain saturation voltage. This safety margin prevents M11 from operating in the linear region due to either component mismatch and/or to non accurate dc modeling. In our design we chose $\Delta V \cong$40 mV. Using the linearized form of UCCM we find that

$$V_{BIAS3} = V_{T0} + n\phi_t[\sqrt{1 + i_{f(MN3)}} - 2 + ln(\sqrt{1 + i_{f(MN3)}} - 1)] \tag{4.4}$$

The term $V_{GS(M1A)}$ can also be found from the linearized UCCM. Since the inversion level of M1A is 3, we write, for M1A

$$\frac{V_{GB(M1A)} - V_{T0}}{n} - V_{SB(M1A)} = 0 \tag{4.5}$$

where the threshold voltage (V_{T0}) is extracted from the transcondutance-to-current ratio characteristic. As demonstrated in [16], for ($g_{mg}/I_D = (g_{mg}/I_D)/2$) $V_G = V_{T0}$ giving in this case $V_{T0} = 208mV$.

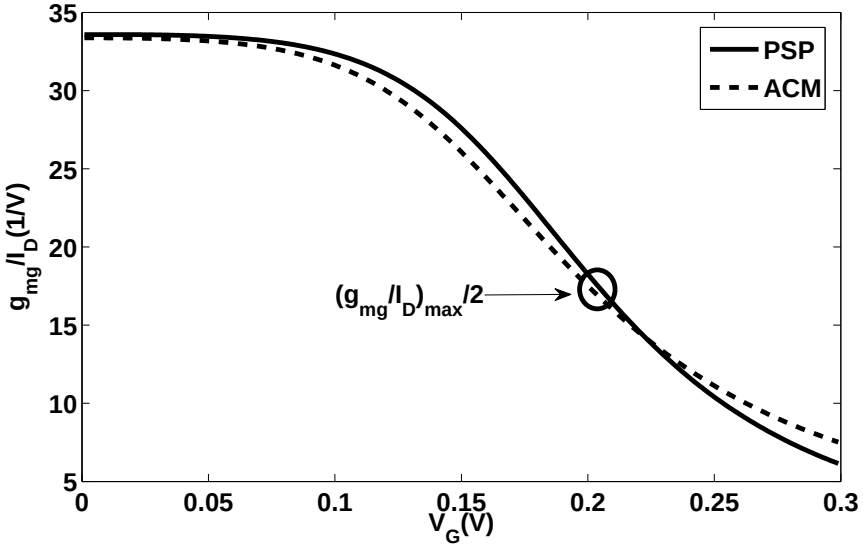

Figure 4.3: Transconductance-to-current characteristic of an NMOS transistor for V_{DS}=1mV.

The combination of the three previous equations allowed us to calculate the inversion level of MN3, which is around 46.

4.2 Simulation results

In this section, we present results obtained from simulation using the PSP model. Figure 4.4 shows that the amplifier fulfilled the gain specification (Gain>100dB) and the gain-bandwidth product simulated is 9.77 MHz.

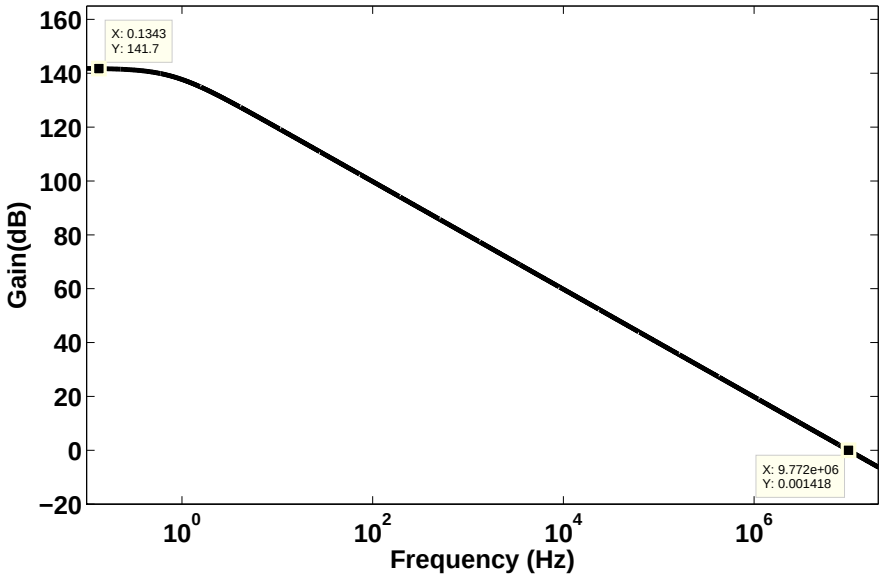

Figure 4.4: Folded cascode frequency response.

The rising (and falling) slew rate is approximately $5V/\mu s$ (Figure 4.5)

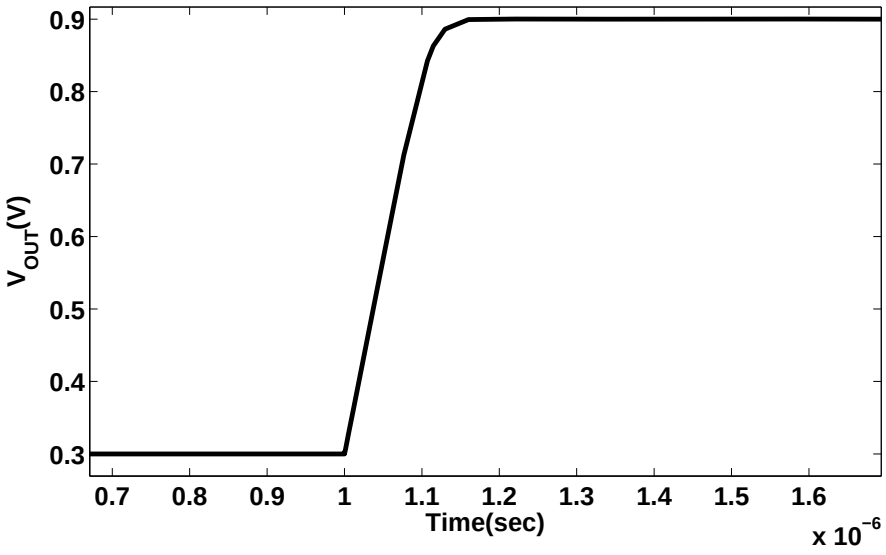

Figure 4.5: Slew rate.

This example shows that design analog circuits using the ACM model is a good choice because it uses a small number of simple and accurate equations.

Chapter 5

Conclusions

In this work, we described the computer implementation of ACM model, which is a charge-based model that has single equations valid in all regions from accumulation to strong inversion, into Eldo.

To demonstrate the quality of the ACM model some simulations were employed to verify the consistency (symmetry and series association) and evaluate the speed performance. These computer simulations and later comparison with other compact models showed that the ACM model is not only a fully consistent model but also has a good speed performance. Also, the core model of the ACM uses a small set of parameters and all parameters have well-known physical meaning.

In summary, the ACM is a powerful tool for analog design that can be used both for electrical simulation and for hand design because it consists of simple, accurate and single equations together with a small number of physical parameters.

Publication List

[1] O. Franca Siebel, "Um modelo eficiente do transistor MOS para o projeto de circuitos VLSI", Master Thesis, Universidade Federal de Santa Catarina (in Portuguese), Mar. 2007. Available online at http://eel.ufsc.br/ lci.

[2] O. Franca Siebel, M. C. Schneider and C. Galup-Montoro, Fundamentals, Computer Implementation and Applications of the Advanced Compact MOSFET (ACM) model, 22nd Symposium on Microelectronic Technology and Devices, (SBMicro 07), Rio de Janeiro, Brazil, pp. 333 - 342, Sep. 2007.

[3] C. Galup-Montoro, M. C. Schneider, A. I. A. Cunha, F. Rangel de Sousa, H. Klimach and O. Franca Siebel, The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design, Proceedings of the IEEE CICC, San Jose, USA, p. 519-526, Sep. 2007.

[4] O. Franca Siebel, C. Galup-Montoro and M. C. Schneider, "An efficient implementation of the ACM MOSFET model in ELDO for VLSI circuit design", University Booth at Design Automation Conference, San Diego, USA, June 2007.

[5] O. Franca Siebel, M. C. Schneider and C. Galup-Montoro, ACM, a Physical All-Region MOSFET Model for Circuit Analysis and Design.Paper submitted to International Symposium on Circuits and Systems (ISCAS) 2008.

Appendix A

The Table below presents the value of ACM parameters used in all simulations.

Parameters	Value	Unit
U0	0.05	$m^2/(Vs)$
TOX	2E-9	m
NSUB	2E-18	cm^{-3}
VFB	-1	V
LAMBDA	0.25	-
ALPHATHETA	1E8	m/V
M	1.2	-
UCRIT	3.5E-6	V/m
XJ	0.25	m
SIGMA	0.3E-15	m^2

The c code of the main function of the ACM computer implementation in Eldo is presented below.

```
/*****************************************
* function mosuser1
*****************************************/
/*Variable definition*/
void mosuser1 (MOSARGU)

double v1,v2,vg,vg1,vds,vs,vd,vdssat,vdsl,vsb1,vdb1,vp,vp1,mu;
double vgs,vsb,vdb,vfb,alpha,phit,phisa,xis,auxphisat,phisat,gate_charge;
```

```
double ypisilon,e2,f,f1,fprime,ftwoprime,iterations,ug,phisa1,signphisa,signphisa2;
double phif,erro_algo,teste,phisa2,alpha1,qba,erro_phisa,phisa3,signphisa3;
double uf,qf,qis,ur,qr,qid,qmin,qo,epsilon,ucrit,n,ncoxphit;
double delta_l,leq,vdssatleq,epsilona,qa,qminleq,vdleq,qidleq;
double xi1,xi2,qrleq,beta,qi,q1,q2,qb,qg,qd,qs,x,xx1,sigma,mueff,betaeff,aplhatheta,current1;
double gamma,phis,x1,temp2,vdsnovo,u2,x2;
double current,wn2,zn2,temp32,temp22,en2,y22;
double u1,wn1,zn1,temp3,y2,en1,k,q1q1,q2q2,q1q1q1,q2q2q2,qd1,qd2,qd3;

register struct S_tytra *T = &(trans[itra]) ;
register struct S_tygeo *TY = &(trageo[itra]) ;
register struct S_tymod *M = &(modmos[T->imo]) ;

/*Voltage acquisition*/
if (M->noup == 'P' )
{
/* PMOS */
vg = vvb - vvg; v1 = vvb - vv1; v2 = vvb - vv2;
}
else
{ /* NMOS */
vg = vvg - vvb; v1 = vv1 - vvb; v2 = vv2 - vvb;
}
vds = fabs ( v2 - v1 ) ; /* the Drain-source voltage */
vs = v1;
if (v1 > v2 ) vs = v2; /* the source-bulk voltage*/

/*Voltage Bias Definition*/
vd = vds + vs;
vgs = vg - vs;
vsb = vs;
vdb = vd;

/*Changing the variable p3 e p2 for gamma and phis*/
gamma=M->p3;
vfb=M->p13;
phit=M->mktsurq;

/*Algorithm for evaluate phisa*/
iterations=1;
alpha=-gamma*sqrt(phit);
```

```
phisa=0;
ug=vg-vfb;

if (ug==0) phisa=0;

else
{

if (ug<alpha) phisa=-2*phit*log(ug/alpha);

if (ug>phit)
{
auxphisat=1+4*(ug-phit)/(gamma*gamma);
phisat=ug+(gamma*gamma/2)*(1-sqrt(auxphisat));
phisa=phisat;
}

}

if (ug>0) phisa = ug<phisa ? ug : phisa;

else phisa = phisa>ug ? phisa : ug;

gate_charge=(ug-phisa);
e2=0;
ypisilon=-phisa/phit;

if (ypisilon>-30) e2=exp(ypisilon); //avoid underflow

f=gate_charge*gate_charge/(gamma*gamma)-phit*(e2-1)-phisa;

fprime=e2-2*gate_charge/(gamma*gamma)-1;

ftwoprime=2/(gamma*gamma)-(e2)/(phit);

phisa=phisa-f/(fprime-(f*ftwoprime)/(2*fprime));

// /*Iterative loop:repeat until abs(f)<10raise to -12*/
while (fabs(f) >= 0.000000000001)
{
gate_charge=(ug-phisa);
```

```
e2=0;
ypisilon=-phisa/phit;
iterations=iterations+1;

if (ypisilon>-30) e2=exp(ypisilon);

f=gate_charge*gate_charge/(gamma*gamma)-phit*(e2-1)-phisa;
fprime=e2-2*gate_charge/(gamma*gamma)-1;
ftwoprime=2/(gamma*gamma)-(e2)/(phit);
phisa=phisa-f/(fprime-(f*ftwoprime)/(2*fprime));

}

signphisa = phisa>0 ? 1: -1/*signal of phisa*/
if (phisa==0) signphisa=0;

phisa2=fabs(phisa);
/*Slope factor*/
if (phisa2<=0.00008)

{
phisa2=-0.00002008;
signphisa2 = phisa2>0 ? 1: -1;
if (phisa2==0) signphisa2=0;
n=1+(gamma*(1-safexp(-(phisa2)/phit)))/(2*signphisa2*safesqrt((phisa2)+phit*(safexp(-
(phisa2)/phit))-phit));

}
else
{
n=1+(gamma*(1-safexp(-(phisa)/phit)))/(2*signphisa*safesqrt((phisa)+phit*(safexp(-
(phisa)/phit))-phit));

}

/*Pinch-off voltage*/
phif=M->p5;
vp = phisa-2*phif-phit*(1+log(n/(n-1)));

/*DIBL coeficient - SIGMA*/
sigma = M->p4/T->ld/T->ld;
```

```
vp = vp + sigma / n * (vd + vs);

/*Definition of pinch-off charge - ncoxphit*/
ncoxphit = n * M->cox *phit;

/*Source Charge Calculation (Algorithm to solution of the transcendental
equation)*/
u1 = (vp - vs)/M->mktsurq + 2;

if (u1 <-30)
{
u1 = -30;
wn1 = 1e-10;
}

else if (u1 <= 0.6)
{
x1 = exp(u1-1);
wn1 = x1 * (1 + 4 * x1 / 3) / (1 + x1 * (7 / 3 + 5 * x1 / 6));
}
else
{
wn1 = (u1-1) - 24 * (((u1-1) + 2) * (u1-1) - 3) / ((7 * (u1-1) + 58) * (u1-1)
+ 127);
}
/*iteration ONE*/
zn1 = (u1-1) - wn1 - log(wn1);
temp3 = 1 + wn1;
y2 = 2 * temp3 * (temp3 + 2 * zn1/3) - zn1;
en1 = zn1 * y2 / (temp3 * (y2 - zn1));
wn1 = wn1 * (1 + en1);

teste = wn1+1;
qf = wn1+1;
/*qf = forward inversion charge density*/
qf = -qf * ncoxphit;

/*qis = source inversion charge density*/
qis = qf + ncoxphit;
```

```
/*Charge Algorithm accuracy*/
erro_algo=phit*((-ncoxphit-qis)/ncoxphit+log(qis/(-ncoxphit)))-vp+vs;


/*Longitudinal critical field calculation*/
ucrit = M->p12 / M->mu0;/*p12 is vmax*/

/*qo calculation*/
qo = n * M->cox * T->ld * ucrit;

epsilon = ncoxphit/qo;

/*Minimum charge = inversion density at the drain end of the channel*/
qmin = 2 * epsilon * qis * (1 - qis / (2 * epsilon * qo)) / (1 - (qis - ncoxphit) /
qo + safesqrt(1 - 2 * (qis-ncoxphit) / qo + (ncoxphit / qo) *(ncoxphit / qo)));

/*Saturation Voltage*/
vdssat = M->mktsurq * ((qmin - qis)/ncoxphit + safelog(qis / qmin));

/*Calculation of effetive drain voltage*/
vdsnovo = (vds)/(pow(1+pow(vds/vdssat,4),1/4));

/*Equivalent channel*/

delta_l = M->lambda * M->p10 * log(1 + (vds - vdsnovo) / (M->p10 *
ucrit));/*p10 eh lc*/
leq = T->ld - delta_l;

/*Drain Charge Calculation*/ u2 = (vp - vdsnovo - vs) / M->mktsurq + 2;
if (u2 <-30)
{
wn2=1.0e-10;
u2=-30;
}

else if (u2 <= 0.6)
{
x2 = exp(u2-1);
wn2 = x2 * (1 + 4 * x2 / 3) / (1 + x2 * (7 / 3 + 5 * x2/6));
}
```

```
else
{
wn2 = (u2-1) - 24 * (((u2-1) + 2) * (u2-1) - 3) / ((7 * (u2-1) + 58) * (u2-1)
+127);
}

/*iteration ONE*/
zn2 = (u2-1)- wn2 - log(wn2);
temp32 = 1 + wn2;
y22 = 2 * temp32 * (temp32 + 2 * zn2/3)-zn2;
en2 = zn2 * y22 / (temp32 * (y22 - zn2));
wn2 = wn2 * (1+en2);

qrleq = wn2+1;
/*qrleq = reverse inversion charge density*/
qrleq = -qrleq * ncoxphit;
/*qidleq = drain inversion charge density*/
qidleq = qrleq + ncoxphit;
/*end of drain charge calculation*/

/* TOTAL CHARGES WITHOUT EFFECTS*/
alpha1=qrleq/qf;

qi=T->wd*leq*((2*(1+alpha1+alpha1*alpha1))*(qis-ncoxphit)/(3*(1+alpha1))+ncoxphit);
qd=T->wd*leq*((4+8*alpha1+12*alpha1*alpha1+6*alpha1*alpha1*alpha1)*(qis-
ncoxphit)/(15*(1+alpha1)*(1+alpha1))+ncoxphit/2);
qs=T->wd*leq*((6+12*alpha1+8*alpha1*alpha1+4*alpha1*alpha1*alpha1)*(qis-
ncoxphit)/(15*(1+alpha1)*(1+alpha1))+ncoxphit/2);

qba=(signphisa)*T->wd*leq*(-gamma*M->cox*safesqrt(phisa+phit*(safexp(-
phisa/phit)-1)));
qb=-((n-1)/(n))*qi+qba;
qg=-qi-qb;

/*Drain Current */

xi1 = (qf * qf - qrleq * qrleq) / (2 * n);
/*To avoid descontinuity to Vds=0 */
xi2 = 1/(1 + sqrt((qf - qrleq)*(qf - qrleq)+ (qo/10)*(qo/10))*(1/qo));
mueff=M->mu0/(1-M->p17*(qb+0.5*qi));//APLHATHETA is p17
betaeff = (mueff * T->wd) / (M->cox * leq);
```

```
current = (betaeff * xi1 * xi2);

/*Conversionlectrical-topological*/
/*NMOS*/
if (M->noup=='N')
{
if (v2>v1)
{
courant = current*1.0e3;/*value in mA*/
courbs = 0;
courbd = 0;
}
else
{
courant = -current*1.0e3;/*value in mA*/
courbs=0;
courbd=0;
}
}
/*PMOS*/
if (M->noup=='P')
{

if (v1>v2)
{
courant = current*1.0e3;/*value in mA*/
courbs = 0;
courbd = 0;
{
else
{
courant = -current*1.0e3;/*value in mA*/ courbs=0;
courbd=0;
}
}
}
if (M->xqc <= d0p5 )
{
x = current / (T->wd * M->p12) ;/*p12 is vmax*/
xx1 = (T->ld*current) / (M->p12) ;/*p12 is vmax*/
```

```
q1 = qf + x;
q2 = qrleq + x;
q1q1=q1*q1;
q2q2=q2*q2;
q1q1q1=q1q1*q1;
q2q2q2=q2q2*q2;

/*Inversion Charge*/
qi = T->wd * leq * ((2*(q1q1+q1*q2+(q2q2))/(3*(q1+q2)))+ncoxphit) -
xx1;

/*Bulk Charge equation*/
qb = ((-n + 1) * qi)/n + qba;

/*Drain Charge equation*/
qd1=T->wd*(leq*leq/T->ld);
qd2=6*(q2q2q2)+12*(q2q2)*q1+8*q2*(q1q1)+4*(q1q1q1);
qd3=(15*(q1+q2)*(q1+q2));
qd=qd1*(qd2/qd3+ncoxphit/2)-xx1/2;

/* Source Charge*/
qs = qi-qd;
/*Gate Charge equation 3.73*/
qg=-qb-qi;

/*Charge - Conversion electrical-topological*/
/*NMOS*/
if (M->noup=='N')
{
if (v2>v1)
{
/*Case of Charge control */
TY->q11 =1.0e+12 * qs ;/*charge attached to node n1 in pC*/
TY->q22 =1.0e+12 * qd ;/*charge attached to node n2 in pC*/
TY->qg =1.0e+12 * qg;/*charge attached to node ng in pC*/
cg1 = dzero; cg2 = dzero; c1b = dzero; c2b = dzero; cgb = dzero;
}
else
{
/*Case of Charge control */
TY->q11 =1.0e+12 * qd ;/*charge attached to node n1 in pC*/
```

```
TY->q22 =1.0e+12 * qs ;/*charge attached to node n2 in pC*/
TY->qg =1.0e+12 * qg;/*charge attached to node ng in pC*/
cg1 = dzero; cg2 = dzero; c1b = dzero; c2b = dzero; cgb = dzero;
}
}

if (M->noup=='P')
{
if (v2>v1)
{
/*Case of Charge control */
TY->q11 =-1.0e+12 * qs ;/*charge attached to node n1 in pC*/
TY->q22 =-1.0e+12 * qd ;/*charge attached to node n2 in pC*/
TY->qg =-1.0e+12 * qg;/*charge attached to node ng in pC*/
cg1 = dzero; cg2 = dzero; c1b = dzero; c2b = dzero; cgb = dzero;
}
else
{
/*Case of Charge control */
TY->q11 =-1.0e+12 * qd ;/*charge attached to node n1 in pC*/
TY->q22 =-1.0e+12 * qs ;/*charge attached to node n2 in pC*/
TY->qg =-1.0e+12 * qg;/*charge attached to node ng in pC*/
cg1 = dzero; cg2 = dzero; c1b = dzero; c2b = dzero; cgb = dzero;
}

}
}

}
```

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