Ultra-Low Voltage CMOS Logic Circuits

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***Abstract*— The operation of digital circuits from power supply voltages of the order of 200 mV or less imposes that, in general, MOSFETs are biased in the subthreshold regime, characterized by the exponential relation between the control voltages and the current. In this tutorial paper we analyze some of the basic building blocks of digital circuits operating in the subthreshold region. We analyze the basic CMOS inverter as regards the voltage transfer characteristic, dynamic behavior, and power dissipation. To reduce the dependence of the drain current on the process parameters we show some compensation circuits that adjust the body voltage, with a small silicon area penalty. Some properties of the static random access memory (SRAM) are reviewed. Finally, the Schmitt Trigger inverter, which is well suited to replace the standard inverter as a basic building block for ultra-low-voltage operation, is briefly analyzed.**

***Index Terms*—Ultra-low voltage logic, subthreshold, low power, VLSI, static CMOS, SRAM, Schmitt Trigger.**

I. Introduction

In recent years, significant advances toward ultra-low voltage have been achieved, aimed at applications that are energy autonomous or rely solely on small batteries. Examples of these applications include cell phones, laptops, handheld and infotainment systems, sensor networks, wearable computing, and biomedical systems [1], [2]. All of these applications must save energy while providing intelligence and better performance for costly infrastructure and support in places with difficult access, such as inside the human body. Moreover, in the future most electronic devices will include a wireless connection, leading to millions of connected devices [3]. All of these devices must capture their own energy, since it is not feasible to use batteries in all of them; nature would simply be unable to absorb all of these batteries after their disposal.

In this regard, a reduction in the supply voltage is the most important action required to increase autonomy. The fundamental limit of the supply voltage in CMOS digital circuits is 36mV at 300K, as determined in [4], [5]. One of the challenges associated with lowering the supply voltage of digital circuits is to compensate for the variation in the technological parameters, mainly the threshold voltage, V_T, of the transistors. Threshold voltage spreading from wafer to wafer in a given technology can lead to large variations in the drain current [6]. As a result, the performance of a digital gate can be severely degraded.

Body biasing has been applied to digital circuits in an attempt to approach the limit of supply voltage and also, to some extent, to compensate for the spreading of process parameters from wafer to wafer. It has been demonstrated that digital circuits can operate from supply voltages of 100 mV, 50 mV, and 85 mV in [6], [7], and [8], respectively. In [9], a 62mV supply voltage is applied to a multiplier based on Schmitt Trigger (ST) structures.

This tutorial is organized as follows. The standard CMOS inverter is analyzed in Section 2. In Section 3, this analysis is extended to the NAND gate. Three circuits for proper body biasing to compensate for variations in the technological parameters are described in Section 4. In Section 5 we briefly analyze the SRAM memory while in Section 6 the application of the Schmitt Trigger inverter for logic circuits is discussed. Conclusions are drawn in Section 7.

II. The CMOS Inverter

A. Static Analysis

As the supply voltage is reduced to values lower than the threshold voltage, V_T, of the NMOS and PMOS transistors, the transistors are biased in the subthreshold or weak inversion regime of operation. This regime is characterized by the exponential dependence of the drain current on the gate, drain and source voltages [10], given by (1).

$$I_{DN(P)} = I_{ON(P)} \cdot e^{\frac{V_{GB(BG)} - |V_{TN(P)}| - n_{N(P)} \cdot V_{SB(BS)}}{n_{N(P)} \cdot \phi_t}} \cdot \left(1 - e^{-\frac{V_{DS(SD)}}{\phi_t}}\right) \quad (1)$$

$I_{ON(P)}$ is a current scaling factor which is dependent on the technology and the geometric parameters. V_{GB} and V_{SB} are the gate and source voltages referenced to the bulk and V_{DS} is the drain-source voltage. ϕ_t is the thermal voltage and n is the slope factor. The strength or current capability of the transistor is given by

$$I_{N(P)} = I_{ON(P)} \cdot e^{\frac{-|V_{TN(P)}|}{n_{N(P)} \cdot \phi_t}} \quad (2)$$

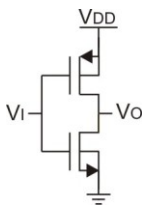

Fig.1: Static CMOS inverter.

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Considering the standard CMOS inverter in Fig. 1, the voltage transfer characteristic (VTC) can be determined from (1). For the sake of simplicity let $n_N=n_P=n$. The static transfer function of the inverter is obtained from

$$I_{DN} = I_{DP} \tag{3}$$

$$I_{ON}\cdot e^{\frac{V_I-V_{TN}}{n\cdot\phi_t}}\cdot\left(1-e^{-\frac{V_O}{\phi_t}}\right)=I_{OP}\cdot e^{\frac{V_{DD}-V_I-|V_{TP}|}{n\cdot\phi_t}}\cdot\left(1-e^{-\frac{V_{DD}-V_O}{\phi_t}}\right) \tag{4}$$

$$V_I=\frac{V_{DD}}{2}+\frac{V_{TN}-|V_{TP}|}{2}+\frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{I_{OP}}{I_{ON}}\right)+\frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{1-e^{-\frac{V_{DD}-V_O}{\phi_t}}}{1-e^{-\frac{V_O}{\phi_t}}}\right) \tag{5}$$

The VTC characterized by equation (5) is dependent on the supply voltage, the imbalance of the transistor threshold voltages and the ratio between the scaling currents. In the ideal case of transistors with the same strength, *i.e.*, $I_{ON}=I_{OP}$ and $V_{TN}=|V_{TP}|$, the VTC reduces to that given by equation (6).

$$V_I=\frac{V_{DD}}{2}+\frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{1-e^{-\frac{V_{DD}-V_O}{\phi_t}}}{1-e^{-\frac{V_O}{\phi_t}}}\right) \tag{6}$$

The inverter threshold voltage, V_M, is defined as the voltage, such that $V_I=V_O$. A first order approximation of V_M derived from (5), given in (7), shows linear dependence of V_M on the threshold voltage mismatch and a logarithmic dependence on the transistors current ratio. In cases where the transistors have the same strength ($I_N=I_P$), $V_M=V_{DD}/2$. If the NMOS transistor is stronger than the PMOS transistor, then $V_M<V_{DD}/2$ and, if the PMOS transistor is stronger than the NMOS transistor, then $V_M>V_{DD}/2$. From (7), it can be noted that a mismatch in the threshold voltages can be compensated for by properly sizing PMOS-NMOS transistors, to obtain $V_M=V_{DD}/2$.

$$V_M\approx\frac{V_{DD}}{2}+\frac{\frac{V_{TN}-|V_{TP}|}{2}+\frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{I_{OP}}{I_{ON}}\right)}{1+\left|\frac{dV_I}{dV_O}\right|_{V_O=\frac{V_{DD}}{2}}} \tag{7}$$

$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}}=\frac{e^{\frac{V_{DD}}{2\cdot\phi_t}}-1}{n} \tag{8}$$

The dependence of V_M on the technological parameters is attenuated by the denominator in (7) which has a term that is dependent on the supply voltage according to expression (8). For n=1, the denominator in (8) is only 1.02 for V_{DD}=200 mV, but it is 1.62 for V_{DD}=50 mV. Thus, as the supply voltage is reduced the influence of the process parameters on V_M is also reduced. For $V_{DD}>4\phi_t$, V_M can be rewritten as

$$V_M=\frac{V_{DD}}{2}+\frac{V_{TN}-|V_{TP}|}{2}+\frac{n\cdot\phi_t}{2}\cdot\ln\left(\frac{I_{OP}}{I_{ON}}\right) \tag{9}$$

The current through the inverter, I_{SC}, can be calculated from (1) and (5) for any input voltage, giving (10) as a result. In particular, the maximum current, $I_{SC\,MAX}$, is given in (11) when the input voltage is equal to the logic gate threshold voltage, *i.e.*, $V_I=V_M$.

$$I_{SC}=\sqrt{I_{ON}\cdot I_{OP}}\cdot e^{\frac{V_{DD}-V_{TN}-|V_{TP}|}{2\cdot n\cdot\phi_t}}\cdot\sqrt{\left(1-e^{-\frac{V_O}{\phi_t}}\right)\cdot\left(1-e^{-\frac{V_{DD}-V_O}{\phi_t}}\right)} \tag{10}$$

$$I_{SC\,MAX}=\sqrt{I_{ON}\cdot I_{OP}}\cdot e^{\frac{V_{DD}-V_{TN}-|V_{TP}|}{2\cdot n\cdot\phi_t}}\cdot\left(1-e^{-\frac{V_{DD}}{2\cdot\phi_t}}\right) \tag{11}$$

Figure 2 shows the VTC and the drain current of the inverter for different supply voltages, $I_{ON}=I_{OP}$=1nA, n=1 and $V_{TN}=|V_{TP}|$=0.3V. It can be noted that as the supply voltage is reduced, the output of the inverter does not fully reach the supply rails. As an example, for V_{DD}=50mV, the output is 46.6mV when the input is 0V and it is 3.4mV when the input is 50mV. Practical values can be even lower since the slope factor of the transistors, n, is generally greater than unity.

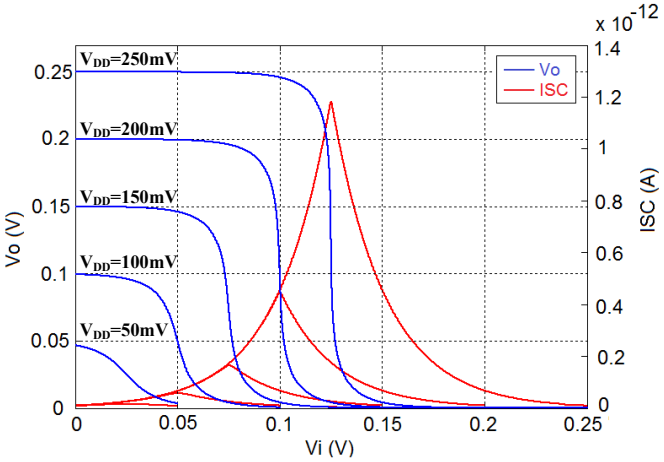

Fig. 2: Inverter voltage and current transfer characteristics.

The minimum operating supply voltage of the inverter and any CMOS static logic gate must be at least equal to unity, *i.e.*,

$$\left|\frac{dV_O}{dV_I}\right|_{V_O=\frac{V_{DD}}{2}}=1 \tag{12}$$

for correct binary signal interpretation [4]. Using (12) together with (8) for n=1, we can readily find that

$$V_{DD\min}=2\phi_t\ln(2)=36\text{mV at 300K} \tag{13}$$

which is the result presented in [4] and [5].

B. *Dynamic Analysis*

The rise and fall times of the inverter, T_{LH} and T_{HL}, respectively, are determined from the circuits shown in Fig. 3. $T_{LH(HL)}$ is the time needed to charge (discharge) the output node between 10% and 90% (90% and 10%) of V_{DD}. Applying a step to the input, the values of T_{HL} and T_{LH} are [11]

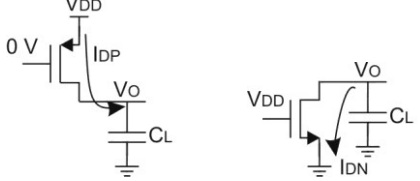

Fig. 3: (a) Charging C_L; (b) Discharging C_L.

$$I_{DN(P)} = \mp C_L \cdot \frac{dV_O}{dt} \tag{14}$$

$$I_{ON(P)} \cdot e^{\frac{V_{DD}-|V_{TN(P)}|}{n_{N(P)}\cdot\phi_t}} \cdot \left(1 - e^{-\frac{V_O}{\phi_t}}\right) = \mp C_L \cdot \frac{dV_O}{dt} \tag{15}$$

$$t_{HL(LH)} = \frac{0.8 \cdot V_{DD} + \phi_t \cdot \ln\left(\frac{1 - e^{-\frac{0.9\cdot V_{DD}}{\phi_t}}}{1 - e^{-\frac{0.1\cdot V_{DD}}{\phi_t}}}\right)}{I_{ON(P)} \cdot e^{\frac{V_{DD}-|V_{TN(P)}|}{n_{N(P)}\cdot\phi_t}}} \cdot C_L \tag{16}$$

C. Power Dissipation

Generally, the power dissipation in a circuit can be divided into dynamic and short-circuit power, both being dependent on the switching frequency, and static power, which is independent of the frequency.

The dynamic power is associated with the energy dissipated in the transistors to charge and discharge the load capacitance. It is calculated as the average energy transferred from the power supply to the load, in a full switching cycle, T. In the first half-cycle, a charge Q, equation (17), provided by the supply is used to raise the output capacitor voltage, through the PMOS transistor, as shown in Fig. 3 (a). In the second half-cycle, the capacitor is discharged through the NMOS transistor, as seen in Fig. 3 (b). The result is an average current, I_{AVG}, through the power supply, as given by (18). The dynamic power, P_{DYN}, is then calculated as the product of the average current and supply voltage, from (17) to (19), and is valid for the case in which the capacitor is fully charged to V_{DD} and discharged to GND, which is a rough approximation for very low supply voltages.

$$Q = C_L \cdot V_{DD} \tag{17}$$

$$\frac{Q}{T} = I_{AVG} = C_L \cdot V_{DD} \cdot f \tag{18}$$

$$P_{DYN} = I_{AVG} \cdot V_{DD} = C_L \cdot V_{DD}^2 \cdot f \tag{19}$$

The short-circuit power, P_{SC}, is due to the simultaneous conduction of the PMOS and NMOS transistors during a transition. The short-circuit current, I_{SC}, given by (10) for any voltage, as shown in Fig. 4, is at its maximum when $V_I = V_M$. The short-circuit power P_{SC} is given by

$$P_{SC} = V_{DD} \cdot \frac{1}{T} \cdot \int I_{SC} \cdot dt \tag{20}$$

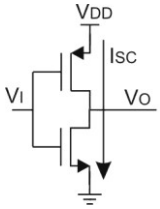

Fig. 4: Short-circuit current

The static power, P_{ST}, in (21) is due to the dissipation of the transistors when they are supposedly in the off state. Even when the transistors are off, a small leakage current, $I_{LKN(P)}$, flows,as shown in Fig.5. I_{LK}, derived from (1), is given in (22).

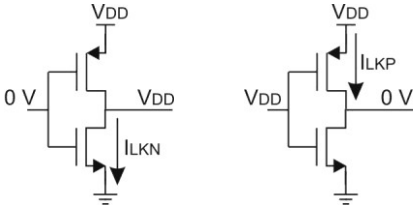

Fig.5: (a) NMOS leakage; (b) PMOS leakage.

$$P_{STN(P)} = I_{LKN(P)} \cdot V_{DD} \tag{21}$$

$$I_{LKN(P)} = I_{ON(P)} \cdot e^{\frac{-|V_{TN(P)}|}{n_{N(P)}\cdot\phi_t}} \tag{22}$$

In all cases, the dynamic power, short-circuit power and static power, which are of major concern in low power circuits, are greatly reduced with a lowering of the supply voltage. Dynamic power is the most affected since it is dependent on the square of V_{DD}.

III. THE NAND GATE

The analysis carried out for the inverter input-output relation, which resulted in (5) and (7), can be extended to more complex logic gates such as the NAND gate, which is shown in Fig.6. The output changes state for one of the two following events. In the first case, labeled as (a) in (23), one of the inputs, *e.g.*, V_A, changes whereas the other is held constant at (or close to) V_{DD}. In the second case, labeled as (b) in (23), both inputs vary simultaneously, *i.e.*, $V_A \equiv V_B$. In this case, the NAND gate is equivalent to an inverter with a P-channel transistor equivalent to the parallel association of P_1 and P_2 and an NMOS transistor equivalent to the series association of N_1 and N_2. The equivalent strength, I_{EQ}, of the series/parallel associations of the NAND transistors is given in (23).

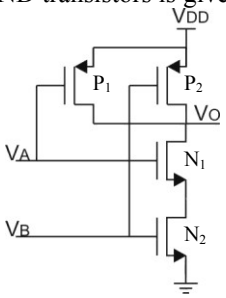

Fig. 6: The 2-input NAND gate.

$$\left.\begin{aligned} I_{EQ,P} = I_P \text{ and } I_{EQ,N} = I_N \quad &\text{(a)} \\ I_{EQ,P} = I_P \cdot 2 \text{ and } I_{EQ,N} = I_N/2 \quad &\text{(b)} \end{aligned}\right\} \tag{23}$$

The relations in (23) reveal that the threshold V_M of the logic gate is dependent on whether one input varies alone or both vary together. Figure 7 shows the VTC of the NAND gate obtained from equation (5) with conditions (a) and (b) in (23) for V_{DD}=150mV.

The series/parallel association of transistors can be extended to logic gates with more inputs without any degradation in the output voltage due to the transistor stacking.

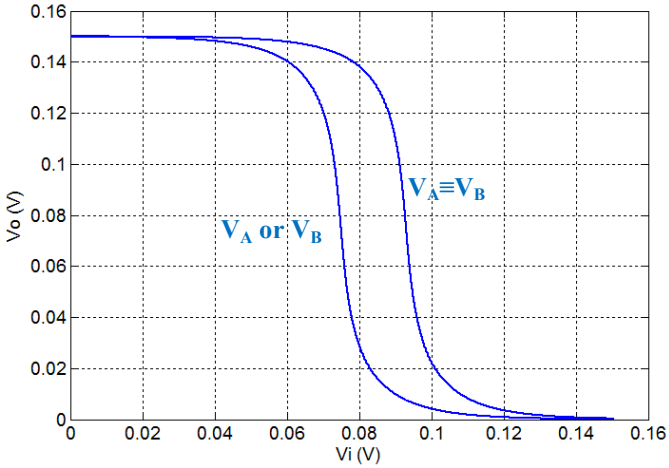

Fig.7: NAND VTC when only one input varies (V_A or V_B) or when both vary together ($V_A \equiv V_B$).

IV. Body Bias Compensation

The transistor drain current in the subthreshold region, equation (1), is very sensitive to V_T. Typical variations of V_T from batch to batch can lead to considerable current variation. Figure 8 shows the simulation of the typical current $I_{DN(P)}$ transfers versus the gate-to-source voltage with nominal threshold voltages close to 500mV and ±30mV variations, for a 180nm technology. The current can vary by as much as a factor of five in the exponential region.

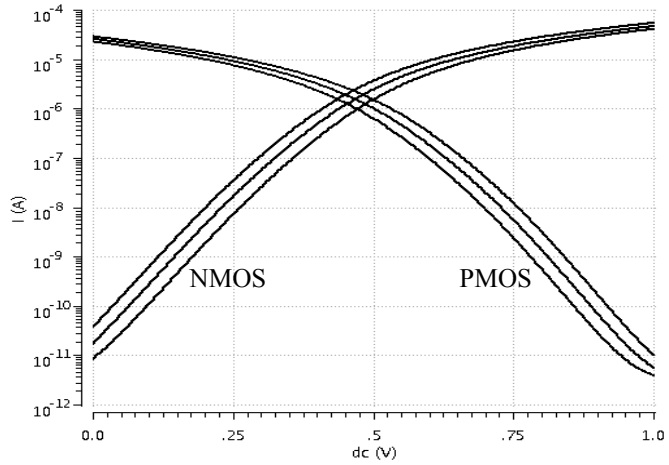

Fig. 8: NMOS and PMOS drain current.

Variations in the process parameters result in shifts in the voltage transfer characteristic (VTC) of a CMOS inverter, as can be inferred from (7). If the PMOS transistor and the NMOS transistor are well matched, $V_M = V_{DD}/2$. For fast NMOS (lower V_T) and slow PMOS (higher V_T) transistors $V_M < V_{DD}/2$ and, conversely, for slow NMOS (higher V_T) and fast PMOS (lower V_T) transistors $V_M > V_{DD}/2$. This is exemplified in Fig. 9, assuming that the threshold voltages can vary by ±30mV around the typical (TT) value. In Fig. 9, the supply voltage is 150mV, FS stands for fast NMOS and slow PMOS transistors, while SF stands for slow NMOS and fast PMOS transistors.

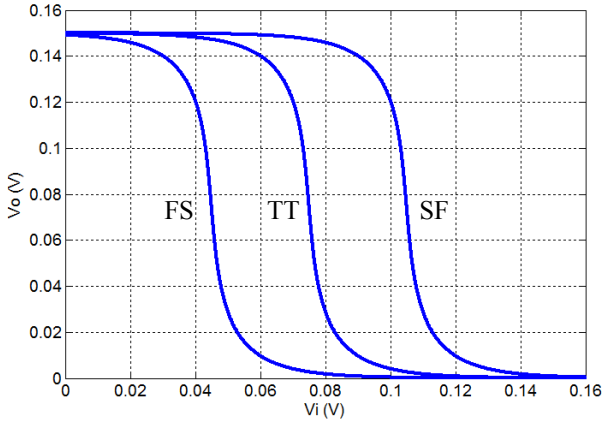

Fig. 9: Inverter VTC under the influence of a variation in the process parameters.

A variation in the process parameters also affects the rise and fall times of the inverter, as equation (16) shows. Variations of an order of magnitude in the NMOS or PMOS drain currents result in rise and fall times that also differ by an order of magnitude. This represents a waste of energy since the maximum operating frequency is mostly determined by the highest sum of the expected fall and rise times. Therefore, proper techniques must be applied in order to compensate, to some extent, for the large variations in the drive currents and, consequently, avoid wasting of energy. Figure 10 shows the transient simulation of the charge and discharge of a load capacitor, C_L=50fF, driven by an inverter with different NMOS and PMOS drain current capabilities, for a supply voltage of 200 mV. The rise and fall times are clearly very different due to the slow NMOS and fast PMOS transistors.

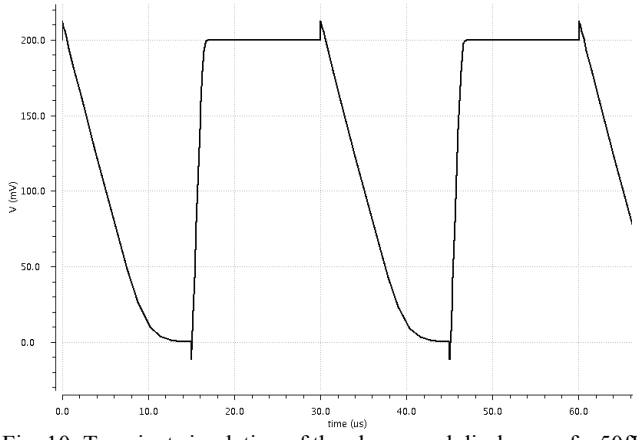

Fig. 10: Transient simulation of the charge and discharge of a 50fF load capacitor by an unbalanced CMOS inverter.

Expression (1) also shows that a variation in the source-to-body voltage, V_{SB}, of the transistor affects the drain current. With a proper body voltage, mismatches in the drive current in the NMOS and PMOS can be reduced regardless of their sizes and technological parameters. Reverse body biasing (RBB) is a technique in which the body-bias voltage is higher than V_{DD} for the P transistor and lower than GND for the N transistor. This technique is good for leakage current reduction, but has

the great inconvenience of the need for bias voltages higher than V_{DD} and lower than GND. Forward body biasing (FBB) is another technique in which the body voltages are between GND and V_{DD}. An inverter with body-bias voltages V_{BN} and V_{BP} is shown in Fig. 11.

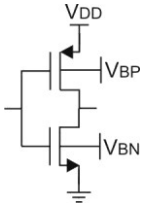

Fig. 11: Inverter with body bias.

In Fig. 12, three bias circuits that can be used to compensate for process variations by providing an appropriate forward body-bias voltage, V_W, are shown. V_W is a common voltage applied to both NMOS and PMOS transistors of a logic gate and, in the three circuits, is the result of the equalization of the NMOS and PMOS currents. Note that both source-to-bulk parasitic diodes are forward body biased, so V_{DD} is limited to sub-1V voltages. Low voltage operation is also recommended to avoid latch-up. The circuit in Fig. 12 (a) was proposed in [6] to equalize the "off" currents of the complimentary devices. Two derivations of this circuit were proposed in [11]: the circuit in Fig. 12 (b) compensates for the "on" or driving currents of the MOSFETs, while that in Fig. 12 (c) compensates for the currents when the input is equal to the gate threshold.

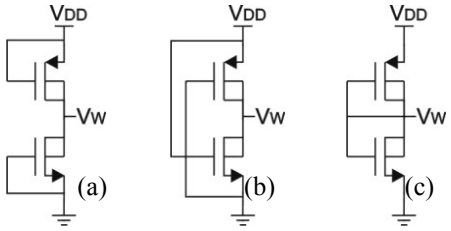

Fig. 12: Body-bias compensation circuits
(a) "off" circuit; (b) "on" circuit; (c) "midway" circuit.

The analysis of the circuits in Fig.12 is straightforward. Noting that

$$I_{DP} = I_{DN} \tag{24}$$

the value of V_W for the circuit in Fig. 12 (c) can be determined from (1), resulting in

$$I_{OP} \cdot e^{\frac{0-|V_{TP}|-n_P\cdot(V_W-V_{DD})}{n_P\cdot\phi_T}} = I_{ON} \cdot e^{\frac{0-V_{TN}-n_N\cdot(0-V_W)}{n_N\cdot\phi_T}} \tag{25}$$

Solving (25) for V_W gives:

$$V_W = \frac{V_{DD}}{2} + \frac{V_{TN}}{2\cdot n_N} - \frac{|V_{TP}|}{2\cdot n_P} + \frac{\phi_T}{2}\ln\left(\frac{I_{OP}}{I_{ON}}\right) \tag{26}$$

The body-bias compensation voltage, V_W, given in (26) is similar to the threshold voltage V_M of the inverter given by (9). This is due to the fact that the inverter shown in Fig. 1 and the circuit in Fig. 12 (c) are similar. This similarity comes from the fact that the inverter threshold voltage is determined by making V_I=V_O, *i.e.*, by shorting the output and input nodes, exactly as in Fig. 12 (c). The main difference between the inverter and the circuit in Fig. 12 (c) is that the bodies of the MOSFETs in the latter case are connected to the drain, whereas in the former case they are connected to the source.

As an example of the effect of the bias voltage, a comparison between the transient simulations of an inverter without body bias (NBB) and of one with forward body bias (FBB) compensation from the circuit in Fig. 12 (c) is shown in Fig. 13 for a supply voltage of 200mV. Clearly, the rise and fall times of the inverter with body bias are closer than those of the inverter without body bias. The simulation also shows another benefit of the FBB: the rise and fall times are faster than without body bias, leading to improved performance at the same supply voltages; thus, for the same static power dissipation faster clocks can be used.

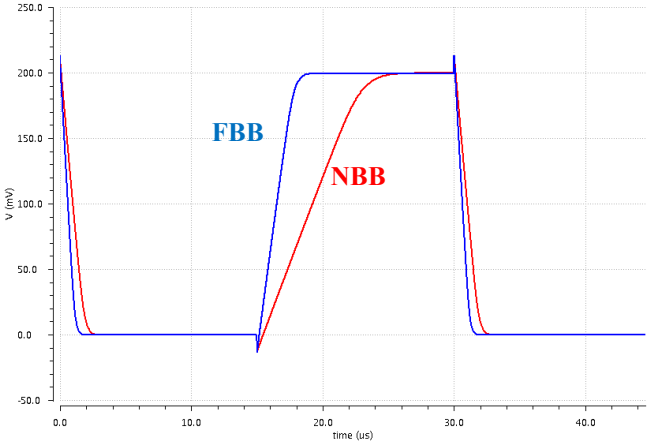

Fig.13: Inverter transient with (FBB) and without (NBB) body biasing.

V. THE SRAM

The six-transistor cell composed of 2 cross-coupled inverters, the so-called bistable latch, and 2 switches, as shown in Fig. 14, is the standard SRAM bitcell. Each bitcell is selected by its corresponding wordline (WL). The requirement of this cell is such that the resistance of the pass transistors connected to the bitlines BL and BR must be sufficiently low to allow correct writing but high enough to avoid the flipping of stored data during reading mode. For example, during a read operation, the stored data can flip from '0' to '1' due to the voltage divider formed by the pass transistor and the NMOS transistor of the inverter, since both bitlines are precharged to V_{DD}. With proper sizing this can be avoided, but under process, voltage and temperature (PVT) variations, this requirement may be challenging and can result in different failure modes, such as read, hold, write and access time failures. Additionally, the SRAM is much more prone to failures in the case of low supply voltages.

The VTC of the first inverter of the SRAM latch in Fig. 14 and the inverted VTC of the second inverter, when the horizontal and vertical axes are permuted, form the butterfly plots shown in Fig. 15 for three different supply voltages. For higher voltages, the curves intercept at two stable points (open circle), V_H and V_L, and one metastable point (closed circle). On lowering the supply voltage, and thus the maximum gain of the inverters, the two stable points become closer to the metastable point and can even become indistinguishable from

it, resulting in low output voltage swing (given by the difference between V_H and V_L) and logic failure [13]. Figure 16 shows the values of V_H and V_L as a function of the supply voltage for the case where the PMOS and NMOS transistors have the same strength, with n=1.5. In this case, there is only one stable point for V_{DD}<50 mV, *i.e.*, the SRAM is ineffective. For higher supply voltages, there are two stable points, V_H and V_L, and one metastable point, V_M. In this case, the SRAM is effective as long as V_H and V_L can be distinguished by the read circuit.

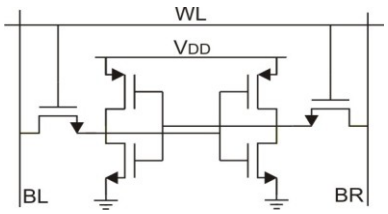

Fig. 14: Classical 6T SRAM.

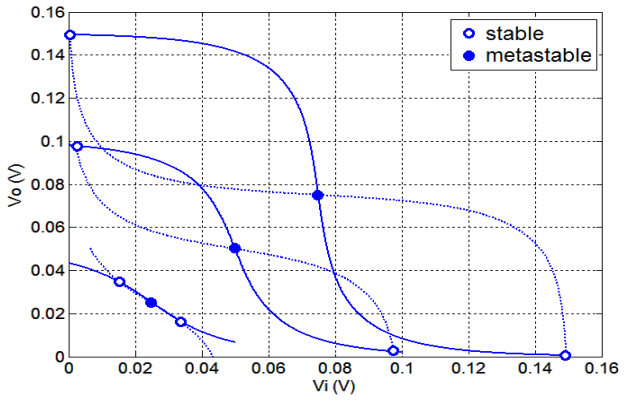

Fig. 15: SRAM latch butterfly plot – n=1.5.

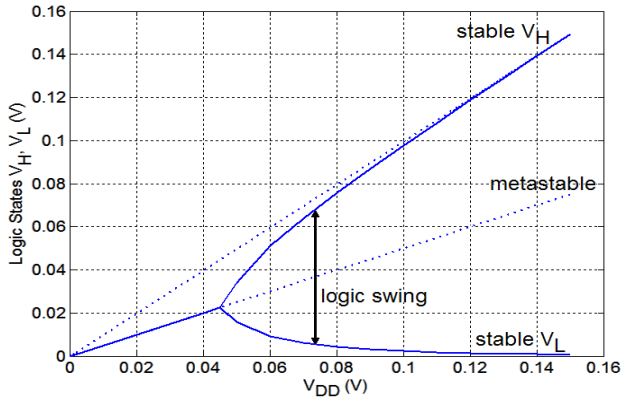

Fig. 16 SRAM latch output logic states – n=1.5.

VI. Schmitt Trigger-Based Logic

The classical six-transistor Schmitt Trigger (ST) inverter shown in Fig. 17(a), is a common digital circuit that can be used either as an input filter to de-bounce signals or in SRAM memories, as shown in Fig. 17(b) [12], or as part of analog oscillators due to the hysteresis effect. Although the ST operation has been analyzed for strong inversion [14], [15], little effort has been directed toward modeling it in weak inversion. In [9], an analytical expression of the internal node potential, V_X, is derived to compare the leakage currents of the ST and the standard inverter.

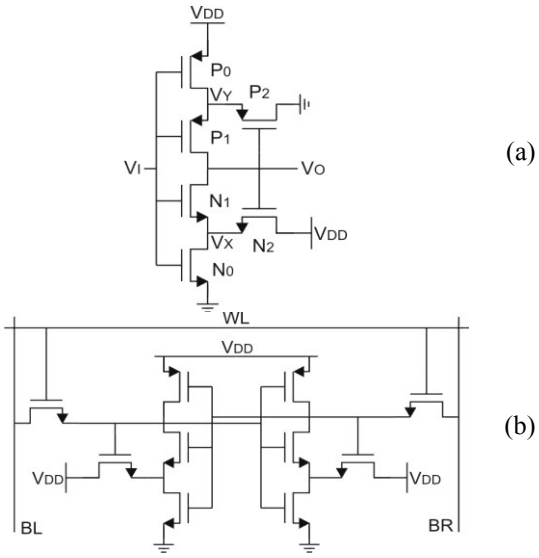

Fig. 17: (a) 6-T Schmitt Trigger; (b) SRAM based on the ST [12].

The main topological difference of the ST as compared to the conventional CMOS inverter is the inclusion of two internal nodes in the NMOS and PMOS networks, which are connected to the positive feedback transistors P_2 and N_2 controlled by the output voltage, V_O. These transistors are responsible for the hysteresis effect when operated with supply voltages higher than around 100mV [9]. For supply voltages below this level, hysteresis is not present. Actually, a lack of hysteresis is preferable for V_{DD} minimization [7], [12] in order to maximize the static noise margin (SNM). The VTC for a supply voltage of 120mV is shown in Fig. 18. One of the benefits of the ST is that, although it does not reduce leakage, it shifts the leakage path so that the output voltage is not loaded [9]. Therefore, when the input is at GND and the output is high, N_2 pulls V_X to a high potential. Thus, the gate-to-source voltage of N_1 becomes negative and its drain to source voltage is close to zero. For the two reasons above, the current flowing in N_1 is greatly reduced and the output voltage deviation is lower [9].

For an optimized behavior [8], the corresponding PMOS and NMOS transistors must have the same current strength. Thus, N_0 and P_0, N_1 and P_1, and N_2 and P_2 in Fig. 17(a), labeled as I_0, I_1 and I_2, respectively, have the same current strength. The node voltages, V_Y, V_X and V_O are determined by the KCL and the application of (1) to the pull-up and pull-down networks gives

$$I_{DN0} = I_{DN1} + I_{DN2} \tag{27}$$

$$I_0 \cdot e^{\frac{V_I}{\phi_t}} \cdot \left[1 - e^{-\frac{V_X}{\phi_t}}\right] = I_1 \cdot e^{\frac{V_I}{\phi_t}} \cdot \left[e^{-\frac{V_X}{\phi_t}} - e^{-\frac{V_O}{\phi_t}}\right] + I_2 \cdot e^{\frac{V_O}{\phi_t}} \cdot \left[e^{-\frac{V_X}{\phi_t}} - e^{-\frac{V_{DD}}{\phi_t}}\right] \tag{28}$$

Solving (28) for V_X results in

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 \cdot e^{-\frac{V_O}{\phi_t}} + I_2 \cdot e^{\frac{V_O - V_I}{\phi_t}} \cdot e^{-\frac{V_{DD}}{\phi_t}}} \tag{29}$$

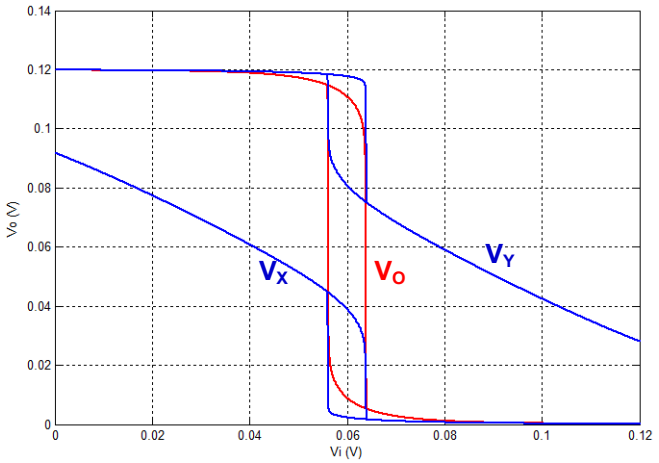

Fig. 18: ST VTC for V_{DD}=120mV.

The Schmitt Trigger (ST)-based SRAM in Fig. 17(b) requires no architectural changes and shows better read static noise and built-in process variation tolerance [12] compared to the SRAM based on the conventional inverter. The ST inverter increases or decreases the trip point of the cell, due to the hysteresis effect of the ST, depending on the direction of the input transition, resulting in higher SNM. Thus, the ST is used to reduce unexpected flips in the stored data.

VII. Conclusions

In this tutorial, the basic logic gates aimed at ultra-low voltage operation working principles were summarized. These gates need additional schemes to compensate for variations in the process parameters, the application of a body-bias voltage being one of the most commonly used compensation methods. As an alternative, the Schmitt Trigger inverter was reviewed and interesting aspects of its operation in weak inversion were shown. Due to its features, the Schmitt Trigger is a promising circuit for a broad range of ultra-low-voltage applications.

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