Limits for Low Supply Voltage Operation of a 5 GHz VCO to Drive a 4-Path Mixer

Mariana Siniscalchi
Instituto de Ingeniería Eléctrica
Universidad de la República
Montevideo, Uruguay
msiniscalchi@fing.edu.uy

Carlos Galup-Montoro
Electrical and Electronics Engineering Department
UFSC
Florianópolis, Brazil
carlosgalup@gmail.com

Sylvain Bourdel
TIMA
Grenoble INP
Grenoble, France
sylvain.bourdel@grenoble-inp.fr

Fernando Silveira
Instituto de Ingeniería Eléctrica
Universidad de la República
Montevideo, Uruguay
silveira@fing.edu.uy

2022 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI) | 978-1-6654-8128-1/22/$31.00 ©2022 IEEE | DOI: 10.1109/SBCCI55532.2022.9893254

***Abstract*—The design and simulation results of a cross-coupled LC VCO in 28 nm FD-SOI for the 4.8 - 5 GHz band are presented. Following a previous work, it is predicted that 0.26 V is the minimum supply voltage of this VCO. It was verified through simulations that the VCO can operate with 0.25 V supply, consuming 90 µW and has a phase noise of -90.2 dBc/Hz at 1 MHz, while complying with the requirements of the following stage. As a consequence of operating at frequencies above the transition frequency of the transistors, the predictions based on the previous study, are less accurate but still provide a good starting point for the design. Moreover, lifting the previous study hypothesis of having an oscillation frequency at least a decade below the transition frequency of the transistors has allowed to further lowering the minimum supply voltage.**

***Index Terms*—Low-Voltage, Low-Power Electronics, RF, FD-SOI**

I. Introduction

PREVIOUSLY, it was studied the limits for lowering the supply voltage in an LC VCO operating at 2.4 GHz [1]. Here, the results are extended to the particular case of a real application, in the band of 4.8 to 5 GHz.

A voltage controlled oscillator (VCO) is designed in a 28 nm FD-SOI process to be the local oscillator (LO) of an RF receiver. A four path mixer is used so that the baseband signal contains fewer harmonics [2]. Thus, the LO must provide four signals with a 90° phase shift from one another and such that the duty-cycle is 1/4. The frequency of these four signals must be tuned in the range from 4.8 GHz to 5.0 GHz with the lowest power consumption possible. Thus, the intermediate frequency f_{IF} is zero. The phase noise should be lower than -88 dBc/Hz at 1 MHz offset frequency, to prove useful according to the standard IEEE 802.15.4 [3].

In the ultra low voltage context, it proves difficult to generate phase and quadrature signals, due to the lack of a well functioning current source, as it is one of the building blocks of this kind of circuits [4]. For this reason, a known alternative approach will be used [4]. A VCO operating at the double of the nominal frequency will be connected to a frequency divider, to obtain the phase and quadrature signals at the nominal frequency. The block diagram is shown in Fig. 1.

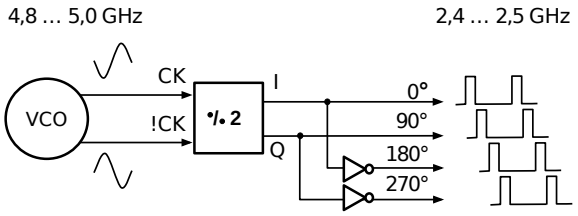


Fig. 1. Block diagram of the local oscillator, including the VCO and the divide by two, to obtain the four signals with 90° phase shift.

The frequency divider is implemented by means of an asynchronous state machine. The logic gates loading the VCO are inverters biased with a supply voltage of 0.5 V and a symmetric back-plane voltage of $V_{BPn} = 2$ V and $V_{BPp} = -2$ V, to minimize power consumption at 5 GHz [5]. The low-Vt transistors sizes are: $L = 30$ nm, $W_N = 80$ nm and $W_P = 260$ nm. To comply with the input voltage of this logic gates, the output of the VCO must swing from 0 V to 0.5 V.

Even though the back-plane voltages are out of the range defined by the supply voltage of the inverters, the current drawn on the back plane bias voltage is very small since the nodes are only capacitively loaded and have a fixed dc voltage. Thus, these dc voltages can be obtained by means of a charge pump voltage step-up.

II. Design of the VCO

Figure 2 shows the circuit schematic of the VCO.

This voltage biased topology is more suitable for ultra low voltage operation than a current biased topology, since the transistors in the tail current source would not saturate. In addition, the voltage biased topology is useful in the ultra low voltage context, since the circuit is only connected to the supply voltage, V_{DD}, through the inductor. Therefore, full advantage is taken from the dc voltage by supplying it directly to the transistors and having an output that may swing well above V_{DD} [6].

In the following we summarize the results of [1] that allows to define the required supply voltage, current and transistor

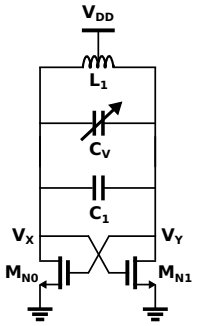


Fig. 2. Circuit schematic of the LC cross-coupled voltage controlled oscillator.

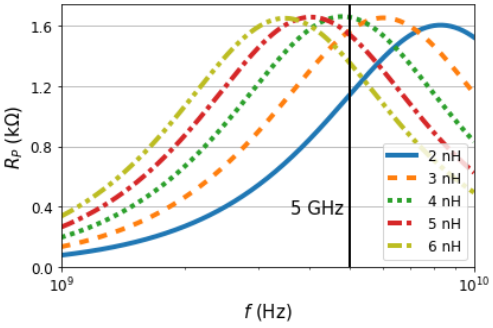


Fig. 3. Parasitic parallel resistor R_P as a function of frequency of a given inductor of the library of nominal value L_n showed in the legend.

size. The Barkhausen oscillation condition reduces to

$$g_m \geq \frac{2}{R_P} + g_o, \tag{1}$$

where R_P is equivalent parallel resistor of the inductor and g_m and g_o are the transconductance and the output conductance of either transistor, respectively, which are extracted through simulations at the dc operating point $V_{GS} = V_{DS} = V_{DD}$. Thus, the oscillation condition depends on the supply voltage V_{DD} through the parameters g_m and g_o.

Both transistors are implemented with N fingers of width W_u and length L_u. As a consequence, the total width is $W = N \times W_u$ and the drain current is

$$I_D = N \times I_{D\,u}, \tag{2}$$

where $I_{D\,u}$ is the drain current through a single finger.

(1) simplifies to a condition on the drain current

$$I_D \geq \frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{g_o}{I_D}}, \tag{3}$$

where g_m/I_D and g_o/I_D as a function of V_{DD} are looked up in a table. This lookup table (LUT) must be filled in advance by means of dc simulations of a single finger.

From (2) and (3), it follows that there is a minimum number of fingers N, given by

$$N_{min} = \left(\frac{1}{I_{D\,u}}\right)\left(\frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{g_o}{I_D}}\right). \tag{4}$$

Therefore, to obtain the lowest power consuming VCO, the library inductor with the highest R_P must be selected. Figure 3 shows the value of R_P as a function of frequency, for the inductors available in the library that have the widest coil (11 µm) to maximize R_P.

In the band from 4.8 to 5 GHz, the inductor with the highest R_P is the inductor with nominal value of $L_n = 4\,\mathrm{nH}$, equivalent parallel inductance $L_P = 5.4\,\mathrm{nH}$ and $R_P = 1.6\,\mathrm{k\Omega}$. The variations of R_P with frequency within the 4.8 to 5 GHz band are negligible.

To achieve a power efficient design, the transistors should be designed to have a high g_m/I_D, according to (3). Increasing the length of the transistor increases g_m/I_D with a small penalty on the parasitic capacitances, because, in the

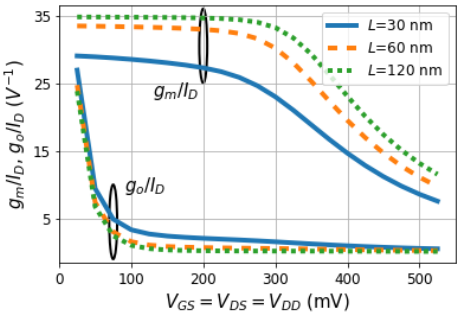


Fig. 4. Simulation results of g_m/I_D and g_o/I_D dependence on VDD for several values of channel length L, with W = 160 nm and VBP = 0 V.

subthreshold regime and for advanced technologies, these are mostly dominated by fringing capacitances which are almost independent on the transistor length, as shown in [7]. Figure 4 shows the simulation results, in the typical case, of the ratios g_m/I_D and g_o/I_D of a transistor, depending on the voltage biasing and the channel length L. The impact of process variations are taken into consideration in Section III. Thus, the length of the unit transistor is chosen to be 60 nm, as g_m/I_D is already significantly higher than that of a minimum channel length transistor ($L = 30\,\mathrm{nm}$) while avoiding a bigger penalty in parasitic capacitances [7].

Thus, both transistors are implemented with N fingers of width $W_u = 160\,\mathrm{nm}$ and length $L_u = 60\,\mathrm{nm}$. As a consequence, the total width is $W = N \times W_u$.

According to (4), if $g_m/g_o > 1$, there is an N large enough to satisfy (4). However, increasing N increases the parasitic capacitances of the transistors. This is a problem if the equivalent parasitic capacitance is greater than C_{tot}, where

$$C_{tot} = \frac{1}{(2\pi f_{osc})^2 L_P}, \tag{5}$$

because in this case the desired oscillation frequency cannot be tuned by means of adjusting the MoM capacitor C_1 and the varactor C_V. Thus, as shown in [1],

$$C_1 + C_V = C_{tot} - N\left(\frac{C_{gs}+C_{gb}+C_{sd}+C_{bd}}{2} + 2C_{gd}\right) \geq 0, \tag{6}$$

where C_{ij} are the capacitances of a single finger loaded from the LUT.

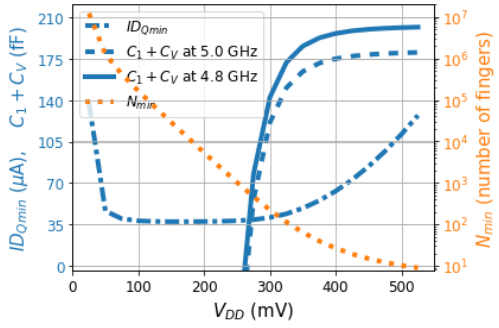


Fig. 5. Results predicted by (3), (4) and (6) and the LUT for the minimum current and number of fingers of each transistor for oscillation in the band from 4.8 to 5 GHz, and the necessary capacitor $C_1 + C_V$ for oscillation at 4.8 GHz and 5.0 GHz, as a function of V_{DD} with $V_{BP} = 0$ V.

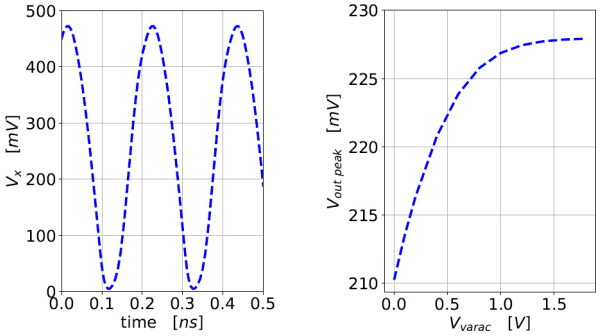
Figure 5 shows the results predicted by (3), (4), which apply to the band from 4.8 to 5 GHz, provided that the dependence of R_P on the frequency within the band is negligible.

The capacitance $C_1 + C_V$ needed to tune the oscillation frequency to 4.8 GHz and 5 GHz, is also shown in Figure 5. As a result, the minimum supply voltage is $V_{DD} = 260$ mV in all the tuning range, since this is the minimum voltage that allows to comply with (6). The minimum drain current in this case is $I_D = 39$ μA and is obtained with a number of fingers of N =670.

This design point is not a practical solution but a boundary for the design space. Practical designs should include an over-compensation factor in (1) to ensure oscillation even with additional losses due to interconnections [4].

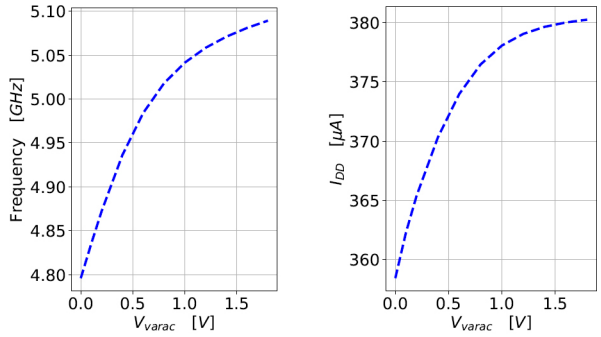
Simulations of the circuit were carried out to further reduce the supply voltage to 0.25 V and to ensure a differential output voltage of 0.5 V peak to peak, in order to provide a proper input for the frequency divider presented in the diagram in Fig. 1. The size of a single finger ($W_u/L_u = 160\,\text{nm}/60\,\text{nm}$) and the inductor (4 nH nominal) are unchanged during these simulations. Only the number of fingers of the transistors and the capacitances C_1 and C_V are modified. Also, the oscillation frequency must be tuned within the range from 4.8 to 5.0 GHz by means of the differential varactor.

As a result, the transistors are built of 500 fingers. The capacitor C_1 and the varactor C_V are implemented using cells available in the kit library. As a result, C_1 = 4.4 fF implemented with a metal-oxide-metal (MoM) capacitance and C_V is implemented with 6 fingers of 1 μm of length and 1.87 μm width. This very small C_1 value is considered as a limit case in order to assess the minimum supply voltage. Improving the design for yield might lead to a higher C_1, and hence a higher supply voltage. From Fig. 5 it can be seen that this value can be increased with negligible penalty in V_{DD}. The control voltage of the varactor varies from 0 V to 0.7 V to tune the frequency. The current supplied to the varactor from the 0.7 V source is very small and the variations required are very slow. Thus, it can be handled in the same way as the back-plane voltage supply of the frequency divider in Fig. 1.



(a) (b)

Fig. 6. Simulation results of the output voltage of the VCO: (a) transient results for $V_{varac} = 0$ V and (b) amplitude of the output voltage (V_x), as a function of V_{varac}.



(a) (b)

Fig. 7. Simulation results of (a) the oscillation frequency and (b) the current consumption, as function of V_{varac}.

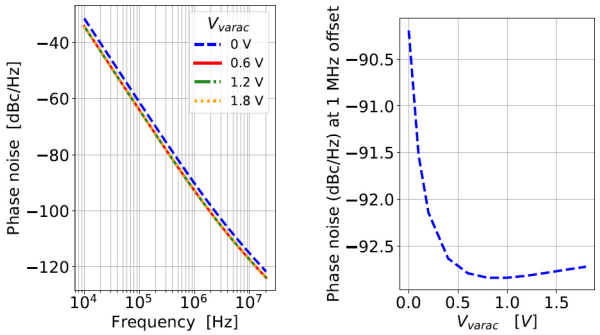
III. Results and Discussion

Figure 6a shows the transient simulation results of the output voltage at node V_x of the oscillator, with the control voltage of the varactor connected to ground, this is $V_{varac} = 0$ V. This results show that the oscillator starts as expected and provides a peak to peak amplitude of 470 mV. The amplitude of the first harmonic of the output voltage V_x (which is the same as V_y) is depicted in Fig. 6b as a function of V_{varac}. Therefore, to achieve a robust design, 40 mV and 460 mV must be valid low and high input levels of the frequency divider. The frequency divider was designed and verified that, with the VCO driving it, it properly provides the signals required in the intended application.

The frequency tuning range is depicted in Fig. 7a, where it is seen that, by setting V_{varac} = from 0 V to 0.7 V, the oscillation frequency is tuned from 4.8 GHz to 5 GHz.

Figure 8 shows the simulation results of the phase noise of the VCO. The phase noise at 1 MHz offset frequency is presented in Fig. 8b, showing that the phase noise is below -90 dBc/Hz in the whole frequency range.

The minimum operating voltage is slightly lower than the one predicted by the method in [1]. A difference between this work and [1] is that the hypothesis of the transition



(a) (b)

Fig. 8. Simulation results of the phase noise of the VCO (a) over frequency, for several values of the voltage control of the varactor, V_{varac}, and (b) at 1 MHz offset, as a function of V_{varac}.

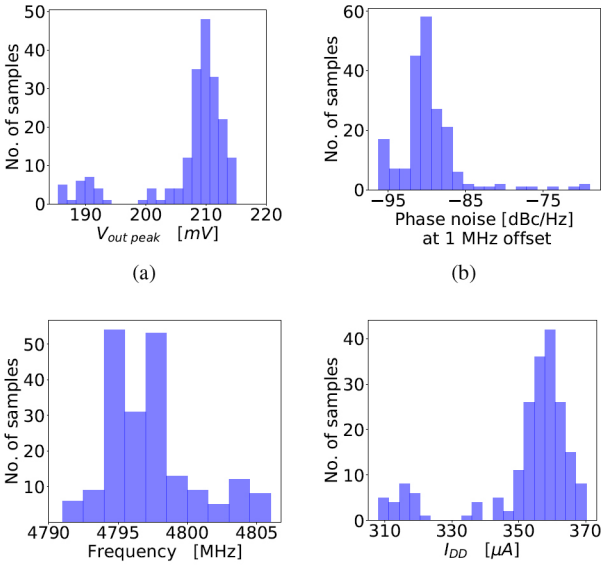
frequency, f_T, being at least 10 times greater than the oscillation frequency, f_{osc}, is not fulfilled. Therefore, removing this constraint allows to reduce the minimum supply voltage. In this case $f_{osc} = 5\,\text{GHz}$ while $f_T = 3\,\text{GHz}$. Therefore, the transistor is operating at a frequency between f_T and f_{max} (the maximum oscillation frequency) [8].

A question that may arise is whether the simulation results properly account for non-quasistatic effects. To verify this, the ac simulations of g_m and g_o are conducted in two test benches. The first test bench consists of two transistors of 30 nm length and 160 nm width, connected in series without extrinsic parasitics in the interconnecting node. The second test bench consists of a single transistor of 60 nm length and 160 nm width. In both test benches the bias voltage is such that the transistors have the same bias current. The results of the simulations of the two test benches agree, consistent with no non-quasistatic effects left unaccounted for.

An additional question is whether the simulation parameters of the technology kit properly model the reality under these particular conditions of operation above f_T with very low bias voltage. In order to check this, experimental validation is required.

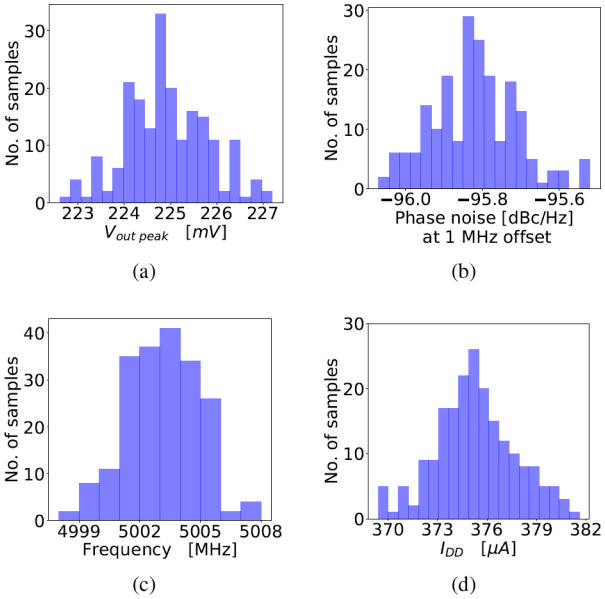
A. Montecarlo simulations of the VCO

Montecarlo simulations were run to account for jointly both process and mismatch variations in all of the circuit components. The results are shown in Fig. 9 for $V_{varac} = 0$ V to obtain an oscillation frequency of 4.8 GHz. For $V_{varac} = 0.7$ V to obtain an oscillation frequency of 5 GHz, the results are shown in Fig. 10. As expected from the simulations in the typical corner, the performance enhances and the current consumption increases at higher frequencies. However, the current consumption is at most 382 µA in the worst case within the 200 samples at 5 GHz. The amplitude of the output voltage of the VCO is in most of the samples over 200 mV, according to Figs. 9a and 10a. Therefore, 50 mV and 450 mV must be valid low and high input levels of the frequency divider, which is adequate for the 0.5 V power supply of this block.



(a) (b) (c) (d)

Fig. 9. Montecarlo simulation results for 200 samples of (a) the amplitude of the output voltage, (b) the phase noise at 1 MHz offset, (c) the oscillation frequency and (d) the current consumption, with $V_{varac} = 0$ V.



(a) (b) (c) (d)

Fig. 10. Montecarlo simulation results for 200 samples of (a) the amplitude of the output voltage, (b) the phase noise at 1 MHz offset, (c) the oscillation frequency and (d) the current consumption, with $V_{varac} = 0.7$ V.

TABLE I
STATE-OF-THE ART OF LOW-POWER LC VCOS

	[9] *	[10] **	[11] ***	[12] *	[13] *	This work **
Frequency range (GHz)	5.14-5.44	2.35-2.37	6.98-6.54	1.55-1.67	2.8-5.8	4.80-5.00
Supply (V)	0.39	0.41	0.35	0.6	0.9	0.25
Power (mW)	0.468	0.1	3.4	1.32	3.6	0.09
Phase noise (dBc/Hz) at 1 MHz offset	-104.41	-107.2	-108.1	-118.6	-110	-90.2
Process (nm)	130	130	130	40	28	28

* Measurements, ** simulations and ***post-layout simulations results.

B. Comparison of the designed VCO to prior works

Table I summarizes the key parameters of the two lowest power VCOs in the state of the art to operate at frequencies close to 4 to 5 GHz (to make a fair comparison), these are [9] and [10].

In addition, Table I includes two low power quadrature VCOs, [11] and [12], which provide phase and quadrature outputs as is the case of the VCO presented herein cascaded with the frequency divider.

Finally, it is included in Table I a low voltage VCO implemented in the same process as the present work [13]. The power consumption and phase noise results are for 5.8 GHz.

The lowest power consumption is that of the VCO presented herein, although the results in [10] are very close. The high power consumption of [11] and [12] is mainly due to the wide tuning range and low phase noise.

On the other hand, the phase noise is significantly higher when compared to the state of the art.

If the application requires lower phase noise, the circuit design may be modified to this aim in trade of current consumption. To reduce the phase noise by 3 dB in all the tuning range, the number of transistor fingers should be increased from 500 to 700 and the MoM capacitor C_1 further reduced to 2 fF, according to the simulations. This results in an increase of 21% in the worst case consumption within the tuning range and an increase of 30 mV in the peak output amplitude. Further decrease of the phase noise would require to consider alternative VCO architectures, such as the cross-coupled topology with a tail current source [4], but these are out of the scope of this paper.

It was also verified through simulations that further lowering the phase noise is not possible by means of adding more fingers to the transistors while keeping the same supply voltage. Moreover, the design space is limited in the direction of adding fingers since soon the parasitic capacitances dominate and the tuning range starts narrowing.

IV. CONCLUSION

The design and simulation results of a cross-coupled LC VCO in 28 nm FD-SOI for the 4.8 - 5 GHz band were presented. The VCO is loaded with a frequency divider to supply four signals with 90° phase shift to drive a 4-path mixer.

Following a previous work, it was predicted that 0.26 V is the minimum supply voltage of this VCO. Through simulations it was verified that the VCO can operate with 0.25 V supply, consuming 90 µW while complying with the requirements of the frequency divider. The VCO has a phase noise of -90.2 dBc/Hz, fulfilling the requirements of the application.

The oscillation frequency is higher than the transition frequency of the transistors f_T. As a consequence, the predictions are not as accurate but provide a good starting point for the design. Moreover, lifting the previous study hypothesis of having an oscillation frequency at least a decade below f_T has allowed to further lowering the minimum supply voltage.

ACKNOWLEDGMENT

The authors would like to acknowledge project STIC-AmSud O2ERF, and CAP and CSIC Universidad de la República, Uruguay.

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