Low-Power & Low-Voltage Analog Integrated Circuits

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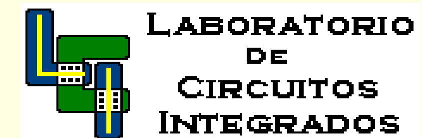
http://www.eel.ufsc.br/~lci/

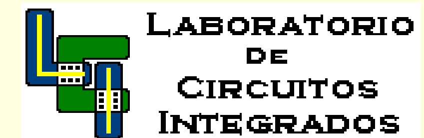
Universidade Federal de Santa Catarina



Acknowledgments

Ana Isabela A. Cunha

Universidade Federal da Bahia



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1. Why low-power & low-voltage
2. Fundamental limitations in analog integrated circuits
3. Components of the CMOS technology
4. MOSFET modeling
5. The basic gain stage
6. The current mirror
7. A self-biased current source

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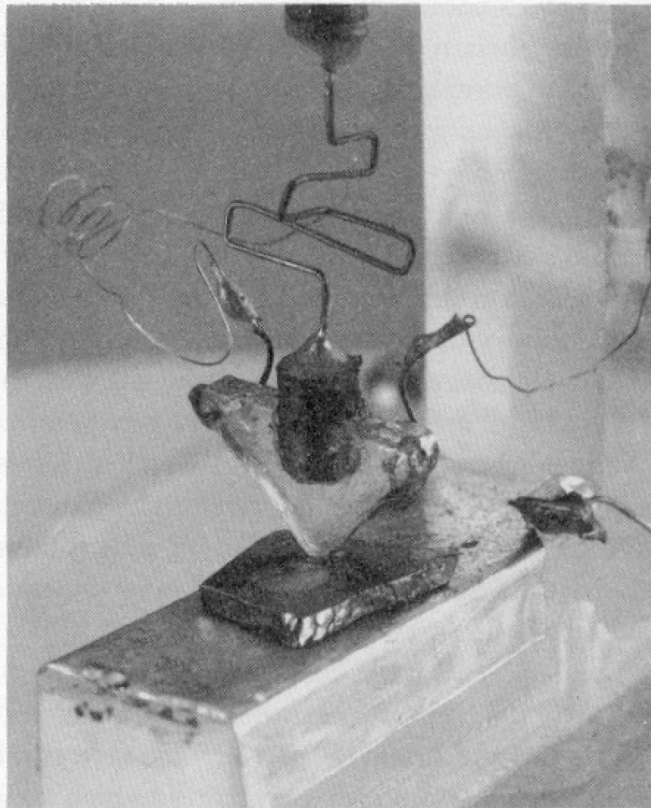
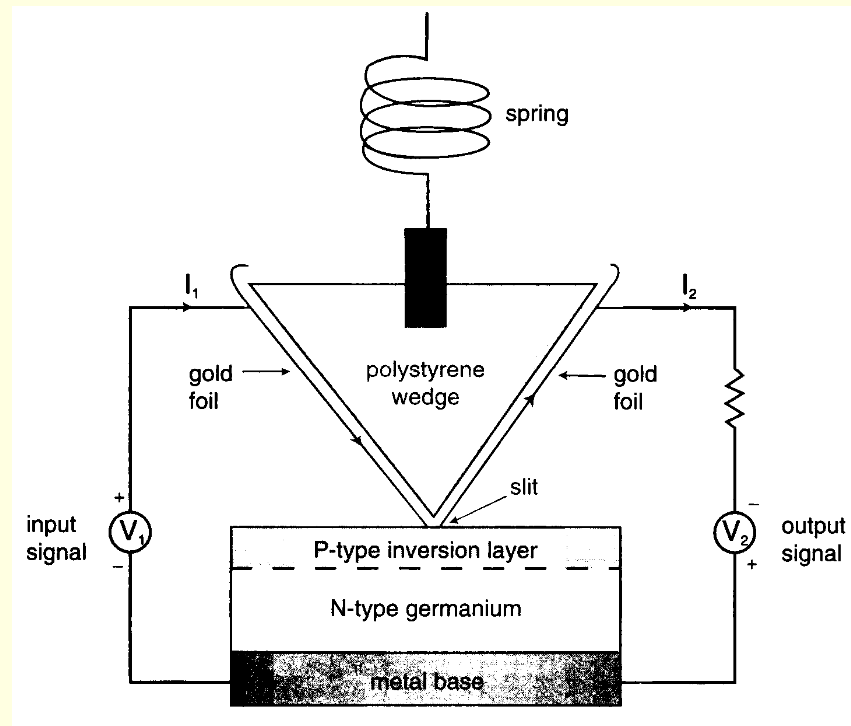
1.1. The Microelectronics Revolution

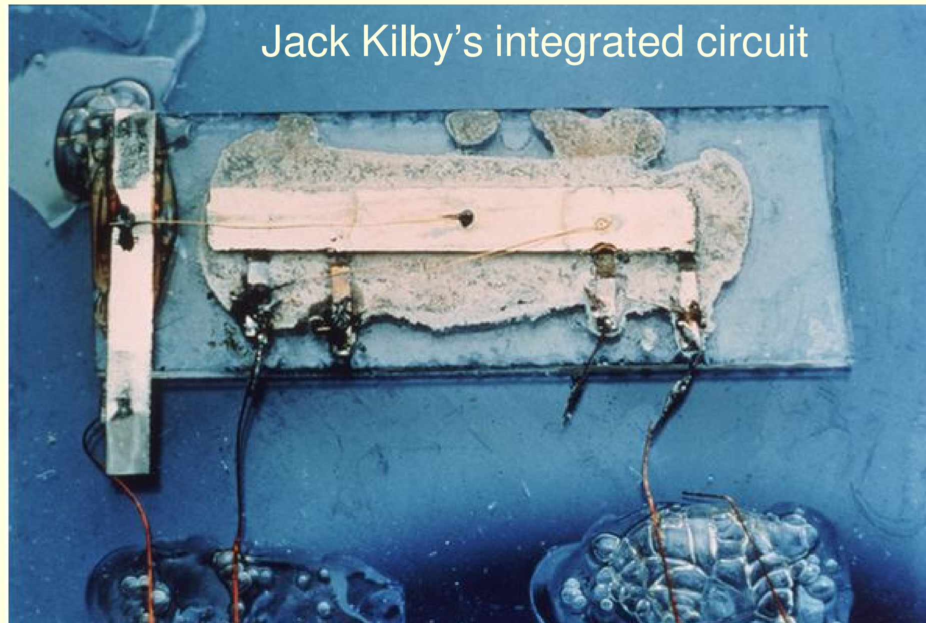


The invention of the transistor (1947)



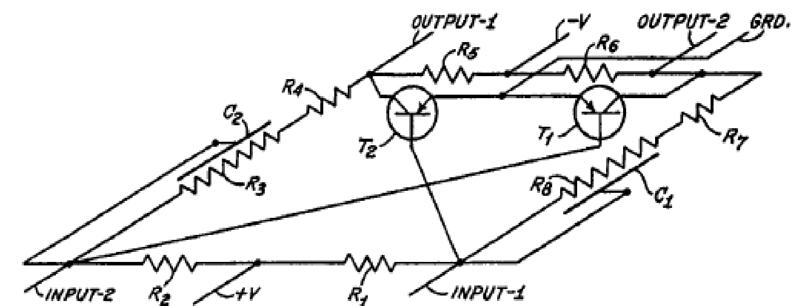
Source: Wikipedia

1.1. The Microelectronics Revolution



Source: Wikipedia

The invention of the integrated circuit (1958-1959)



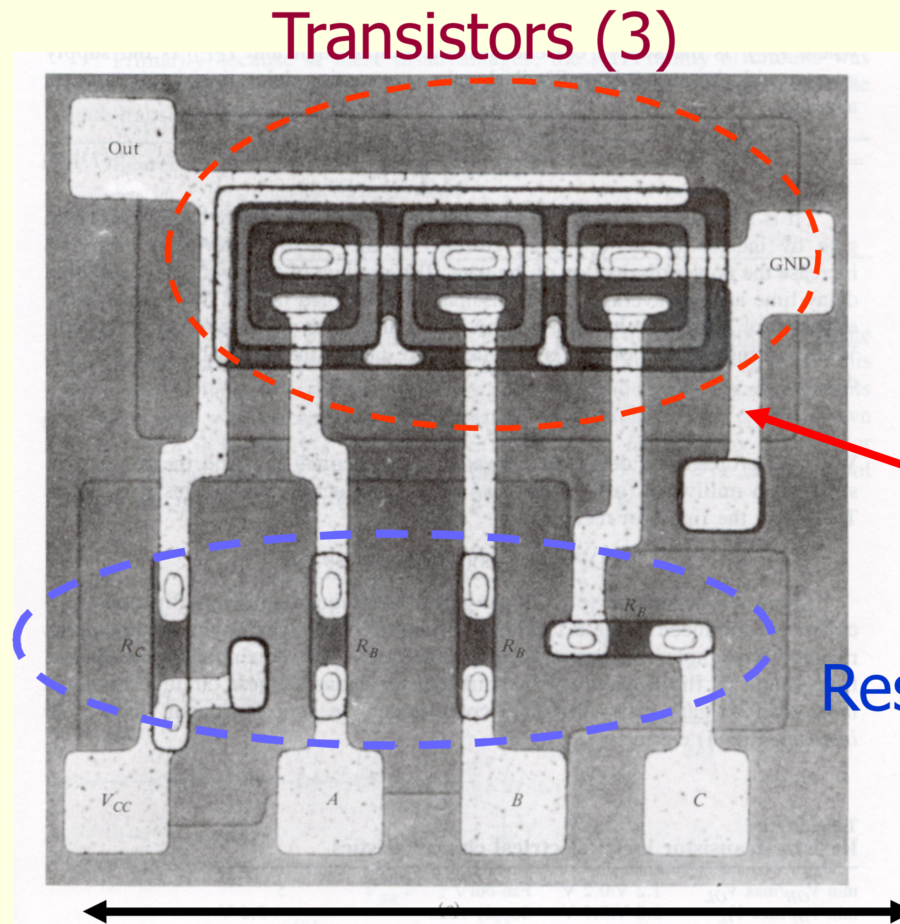
Source: R. Jaeger, Microelectronic Circuit Design, McGraw-Hill, 1997

Jack Kilby (Texas Instruments) – 1958

Robert Noyce (Fairchild Semiconductor) - 1959

1.1. The Microelectronics Revolution

Transistors (3)



~ 1 mm

The first commercial IC: 3-input NOR gate – RTL **Fairchild (1961)**

Connection metal

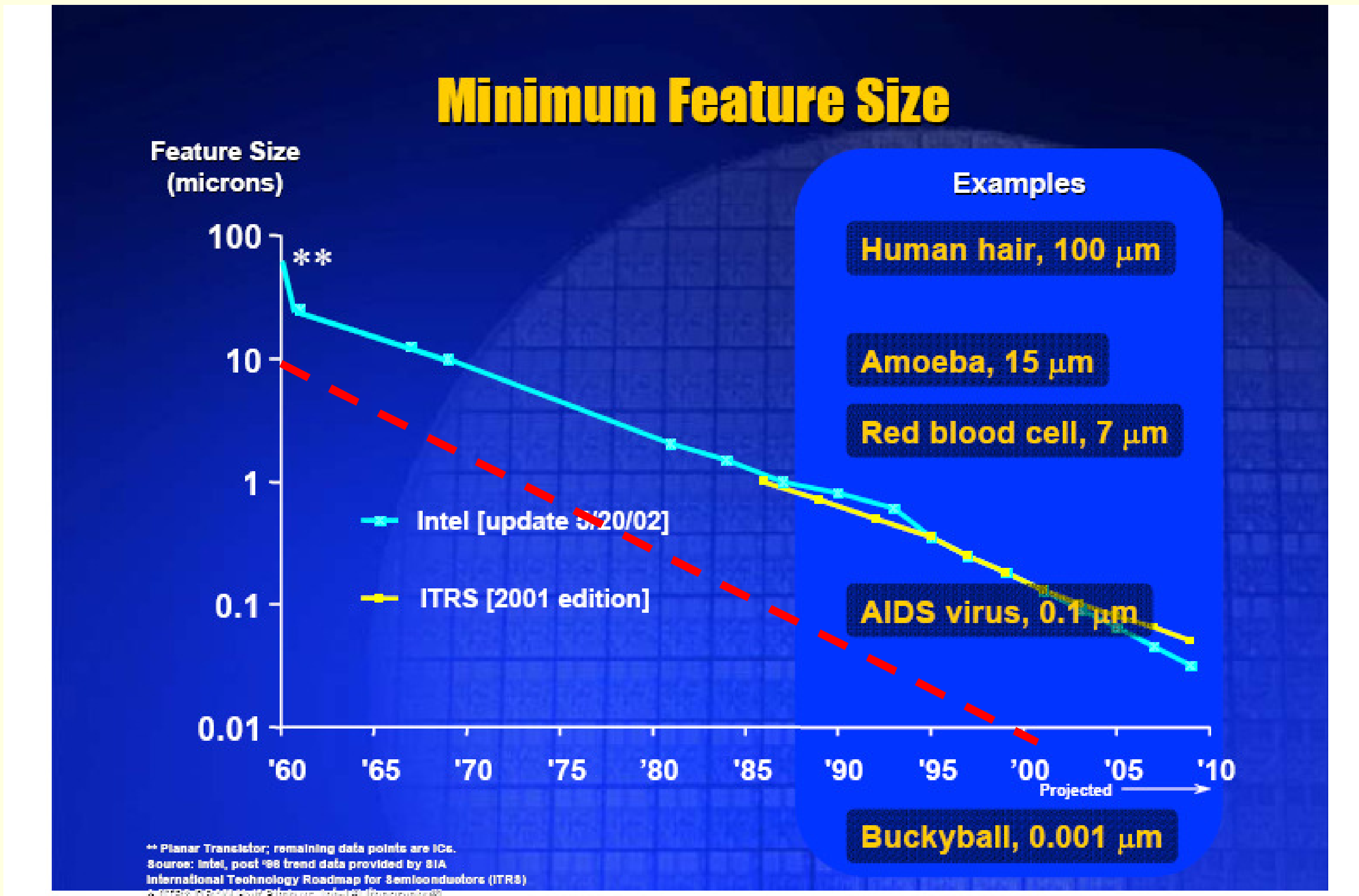
Resistors (4)

1.1. The Microelectronics Revolution

Moore's law

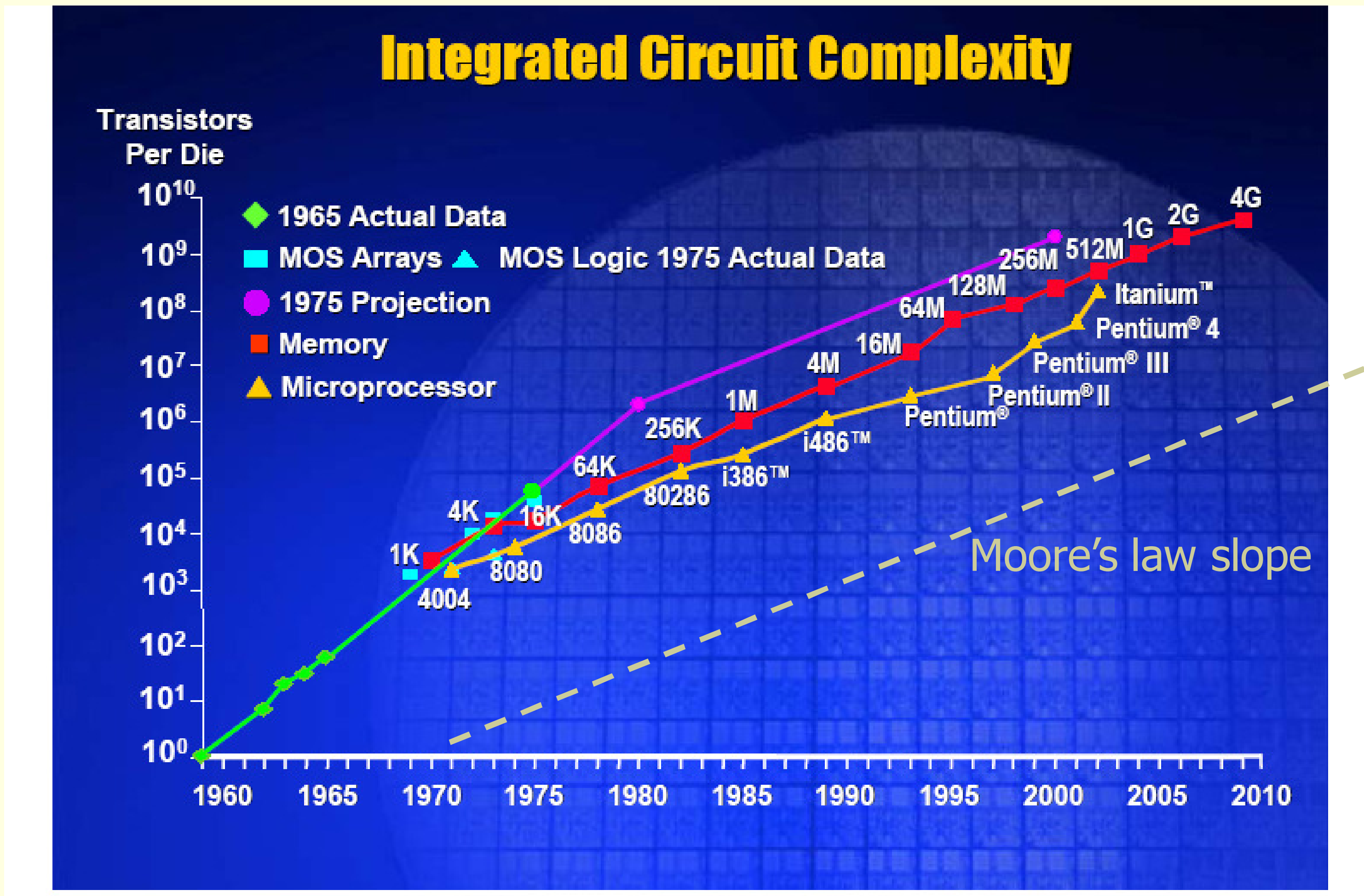
The number of transistors on integrated circuits doubles every two years

1.1. The Microelectronics Revolution



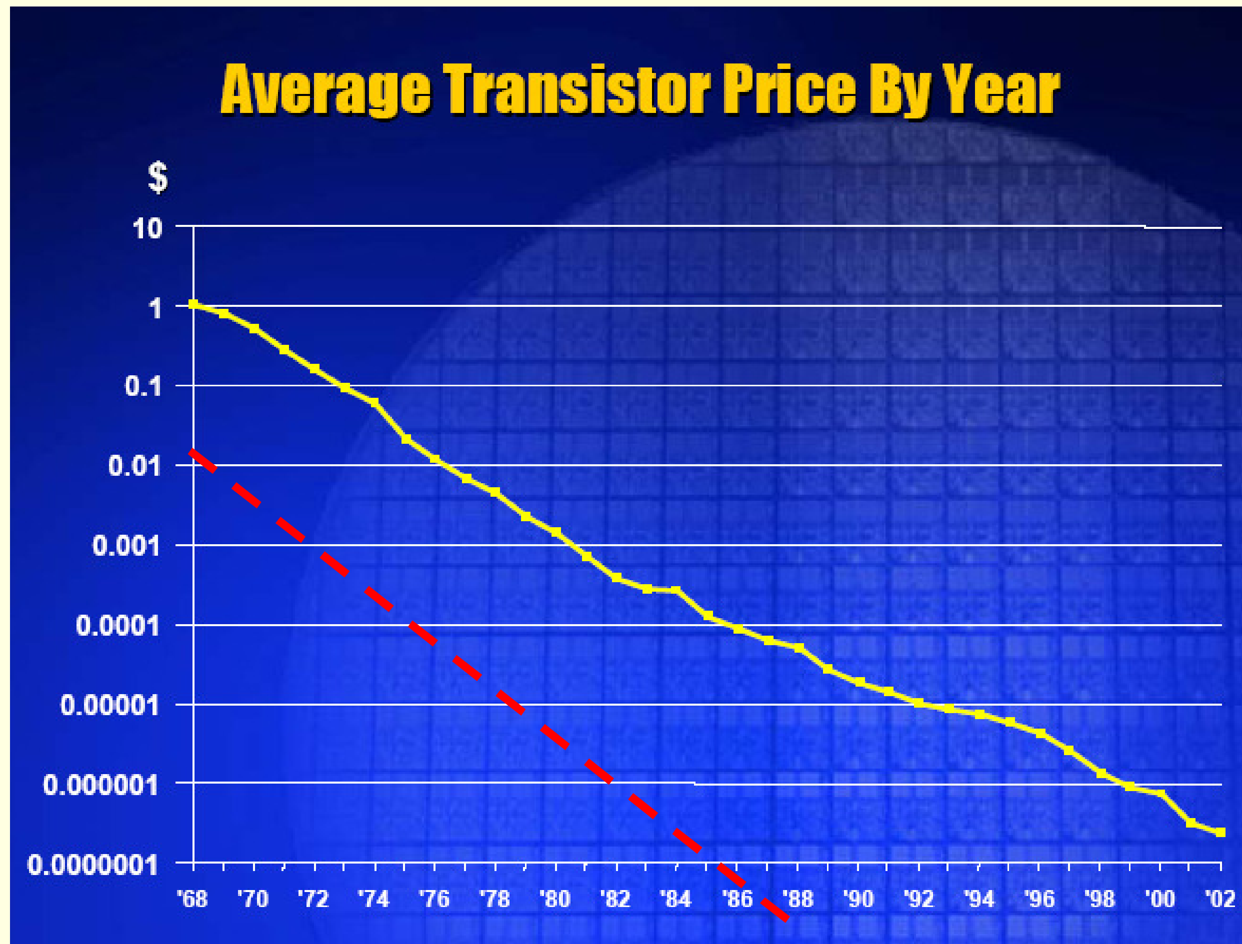
Source: Intel

1.1. The Microelectronics Revolution



Source: Intel

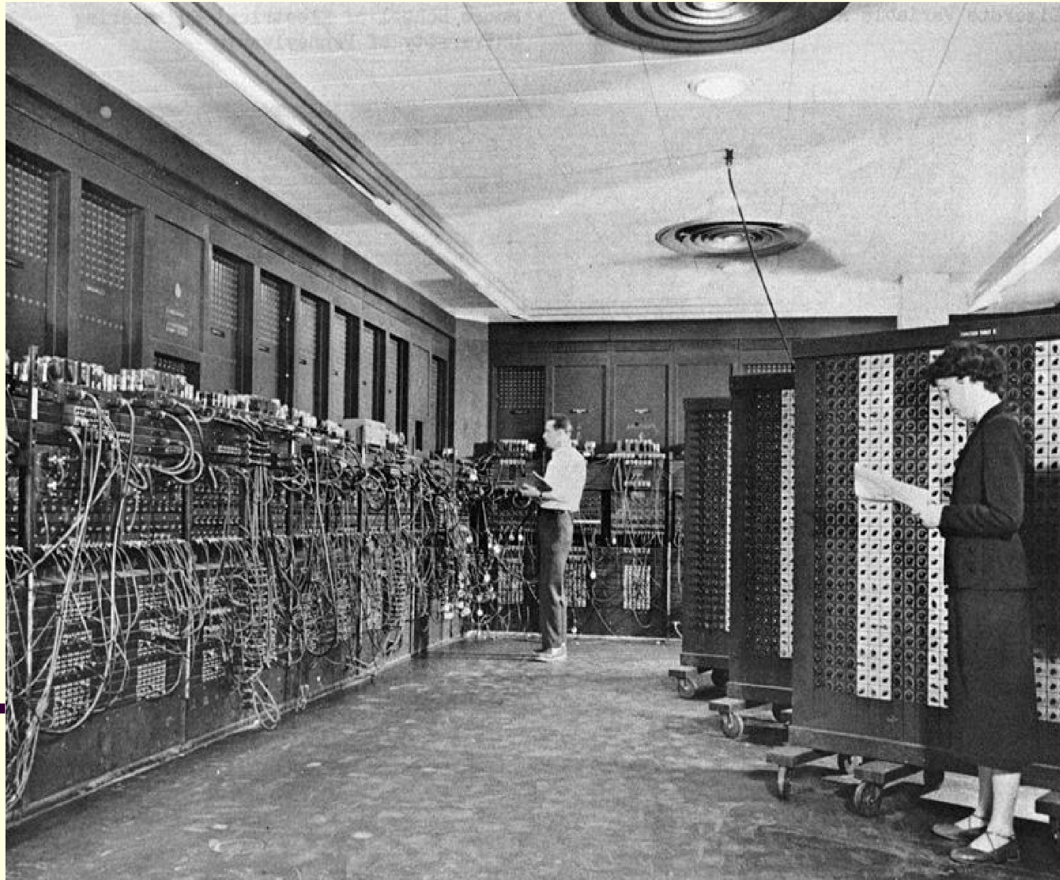
1.1. The Microelectronics Revolution



Source: Intel

1.2. Low Power Microelectronics

The early electronic computers



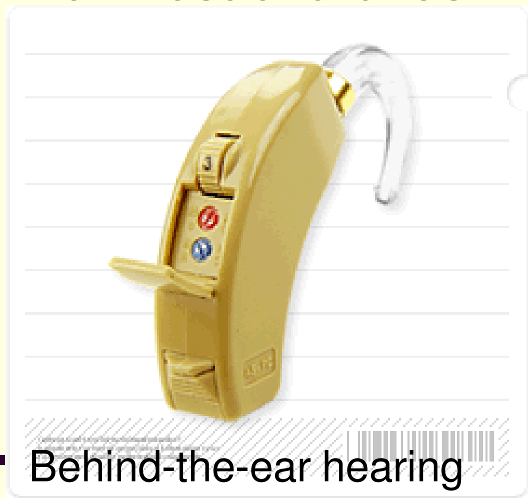
ENIAC (1946)

17.468 vacuum tubes
7.200 diodes
1.500 relays
70.000 resistors
10.000 capacitors
Weight: 27 ton
Dimensions: 2.6 m×0.9 m× 26 m (60 m^3)
Power: 150 kW

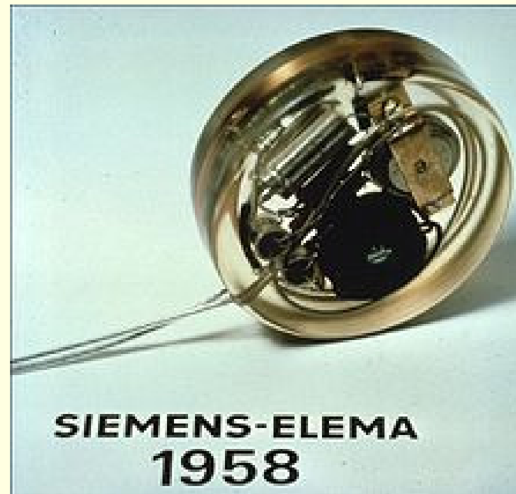
Source: Wikipedia

1.2. Low Power Microelectronics

Historically demanding applications of LP microelectronics (long-life autonomous portable equipment): wrist watches, hearing aids, implantable cardiac pacemakers, pocket calculators, pagers. Until the early 90's, power was not an issue for most of the ICs.



Behind-the-ear hearing aid – Amplivox

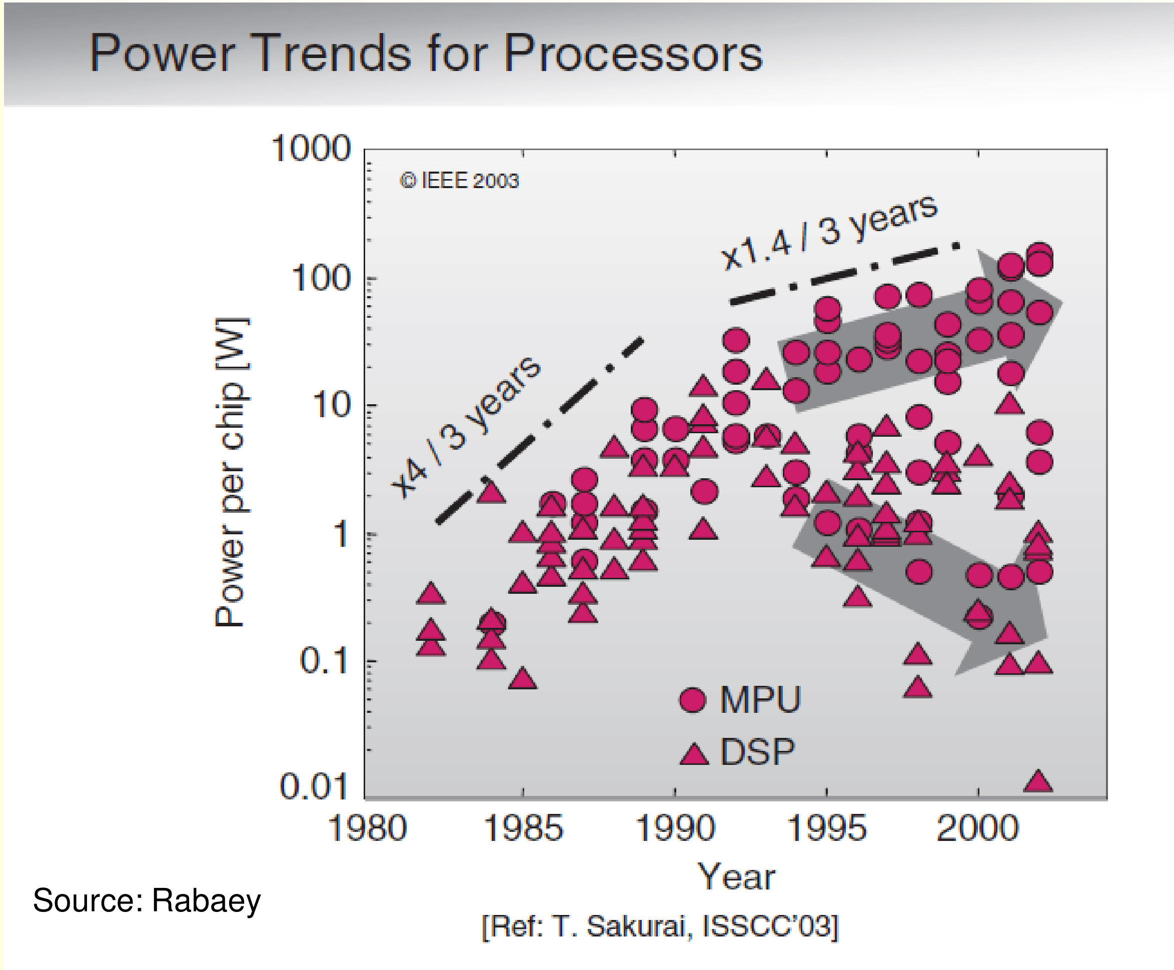


The first implantable pacemaker

Artificial pacemaker with electrode for transvenous insertion.

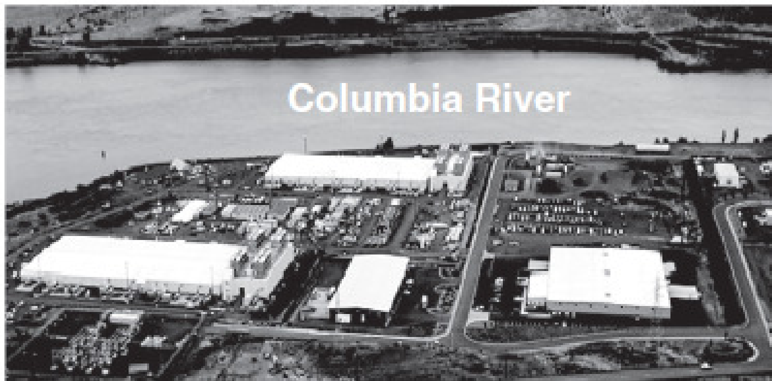
Source: Wikipedia

1.2. Low Power Microelectronics



1.2. Low Power Microelectronics

Cost of large data centers solely determined by power bill …

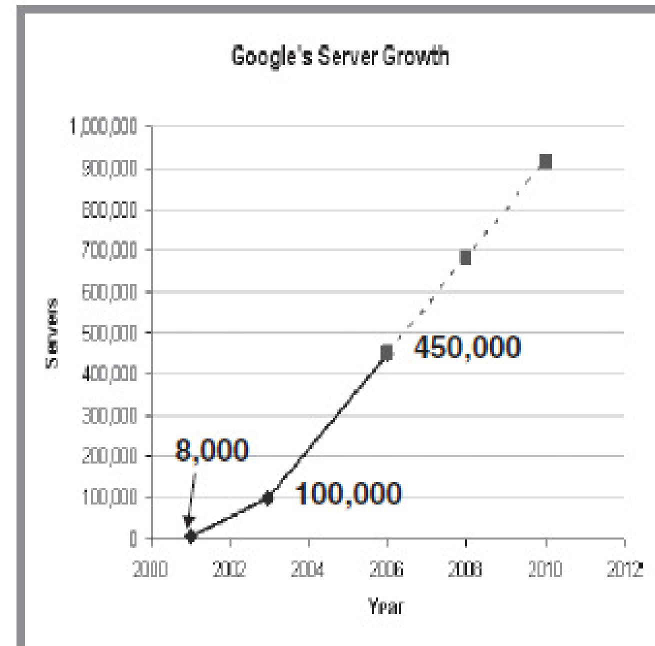


Google Data Center, The Dalles, Oregon

- 400 Millions of Personal Computers worldwide (Year 2000)
  - -Assumed to consume 0.16 Tera (10^{12}) kWh per year
  - -Equivalent to 26 nuclear power plants
- Over 1 Giga kWh per year just for cooling
  - -Including manufacturing electricity

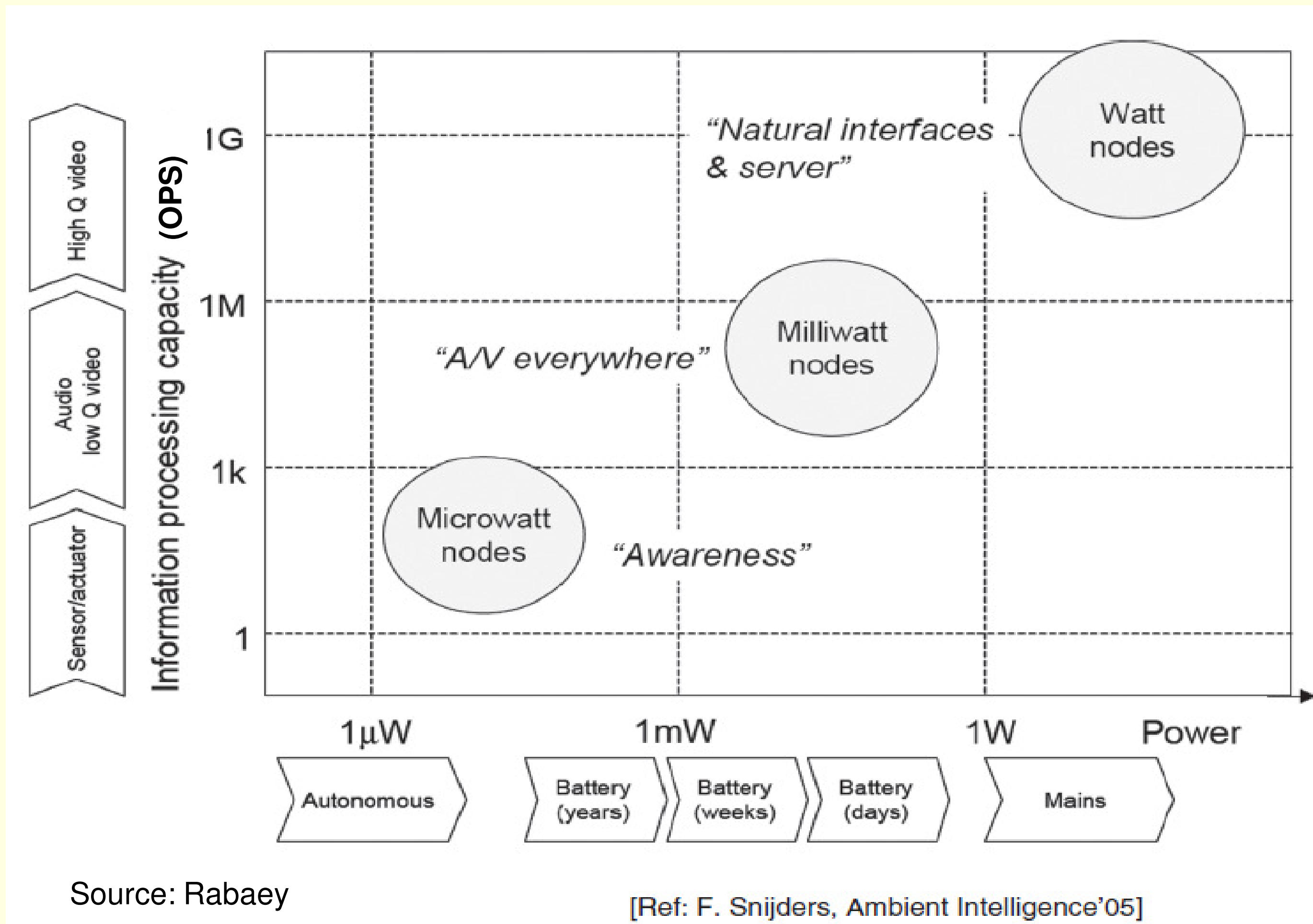
[Ref: Bar-Cohen et al., 2000]

NY Times, June 06



Source: Rabaey

1.2. Low Power Microelectronics



Source: Rabaey

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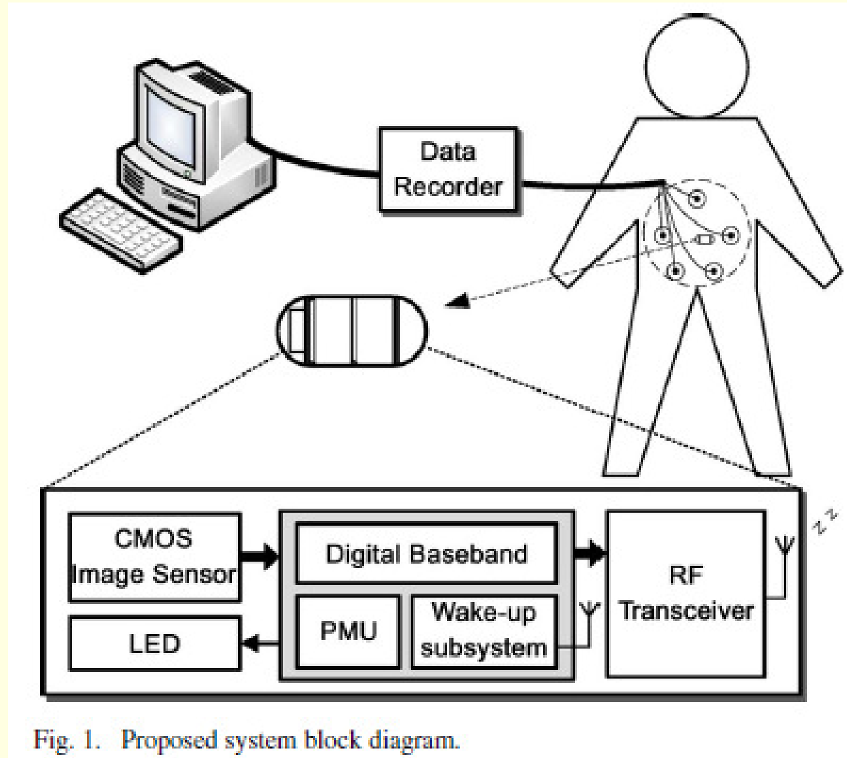
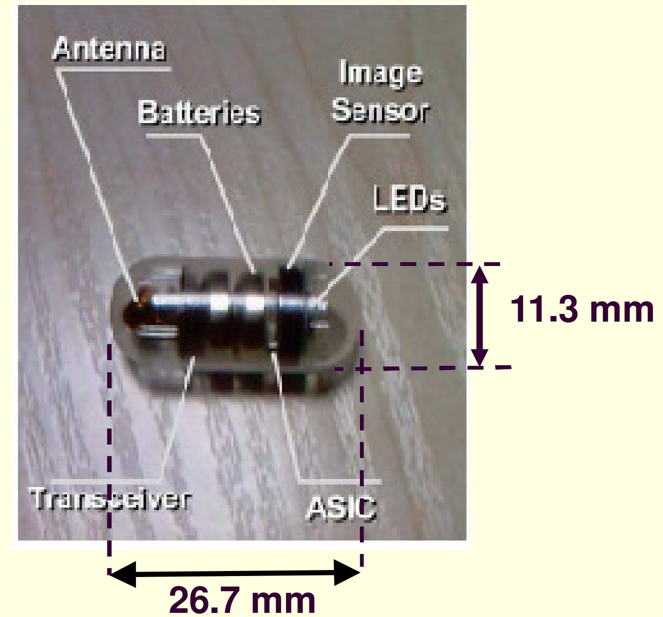
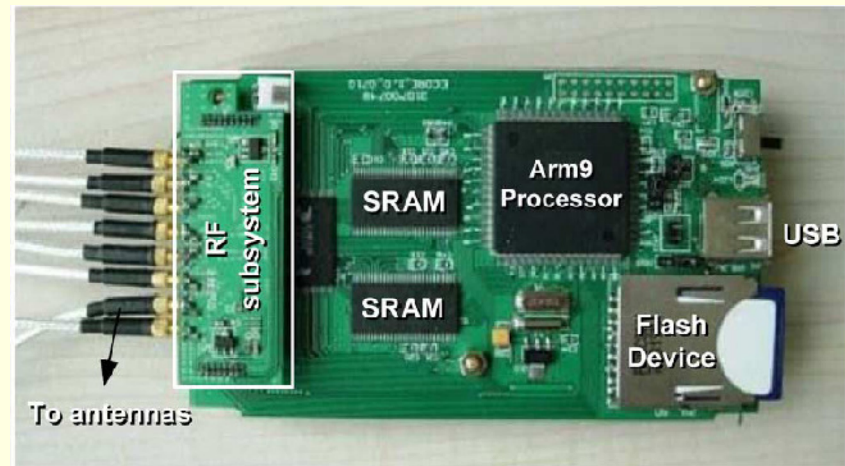


Fig. 1. Proposed system block diagram.





X. Chen et al, IEEE Trans. Biomedical Circ. And Syst., vol. 3, no. 1, Feb 2009

1.Why low-power & low-voltage

J. Rabaey, *Low Power Design Essentials*, Springer, 2009.

C. Piguet (ed.), *Low-Power Electronics Design*, CRC Press, 2005

J. D. Meindl, “Low Power Microelectronics: Retrospect and Prospect,” *Proc. of the IEEE*, vol.83, no.4, pp. 619-635, Apr. 1995.

J. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits – A Design Perspective, Prentice-Hall, 2003.

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2.1 Design specifications

Digital Design:

Time Delay or Frequency, Power, Energy/operation, Reliability, Robustness, Cost

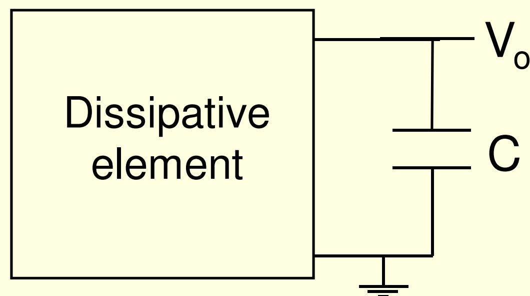
Analog Design:

Noise, Linearity, Bandwidth (Frequency), Power, Supply Voltage, Gain, Accuracy, Robustness, Cost

2.2 Noise and Distortion

Thermal noise:

Energy equipartition principle: In thermal equilibrium the mean thermal energy per degree of freedom is (1/2)kT, where k is the Boltzmann constant and T is the absolute temperature.



Noise energy in C= $$\frac{C\overline{v_{o,n}^2}}{2} = \frac{kT}{2} \Rightarrow \overline{v_{o,n}^2} = \frac{kT}{C}$$

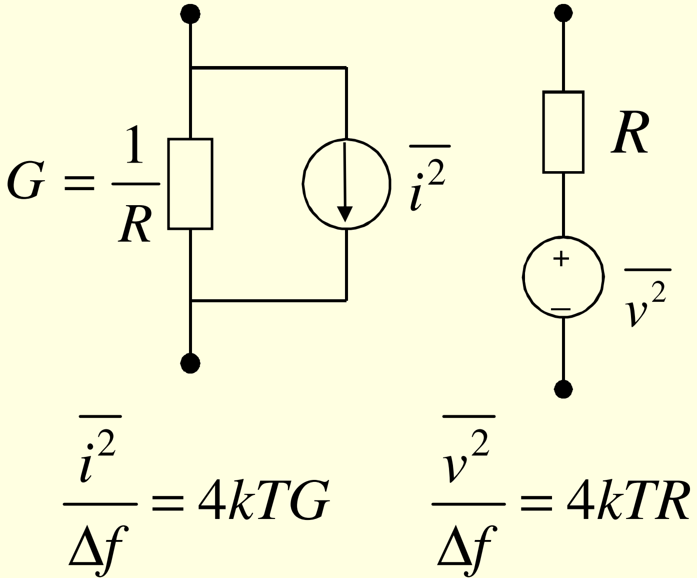
Assume that $$V_{o,s} = V_P \sin \omega t$$

Signal energy in C= $$\frac{C\overline{v_{o,s}^2}}{2} = \frac{CV_P^2}{4}$$

The signal-to-noise ratio is $$S/N = \frac{V_P^2/2}{kT/C}$$

2.2 Noise and Distortion

Thermal noise :



$$\frac{\overline{i^2}}{\Delta f} = 4kTG \qquad \frac{\overline{v^2}}{\Delta f} = 4kTR$$

Norton and Thevenin equivalent circuits of a real (noisy) resistor

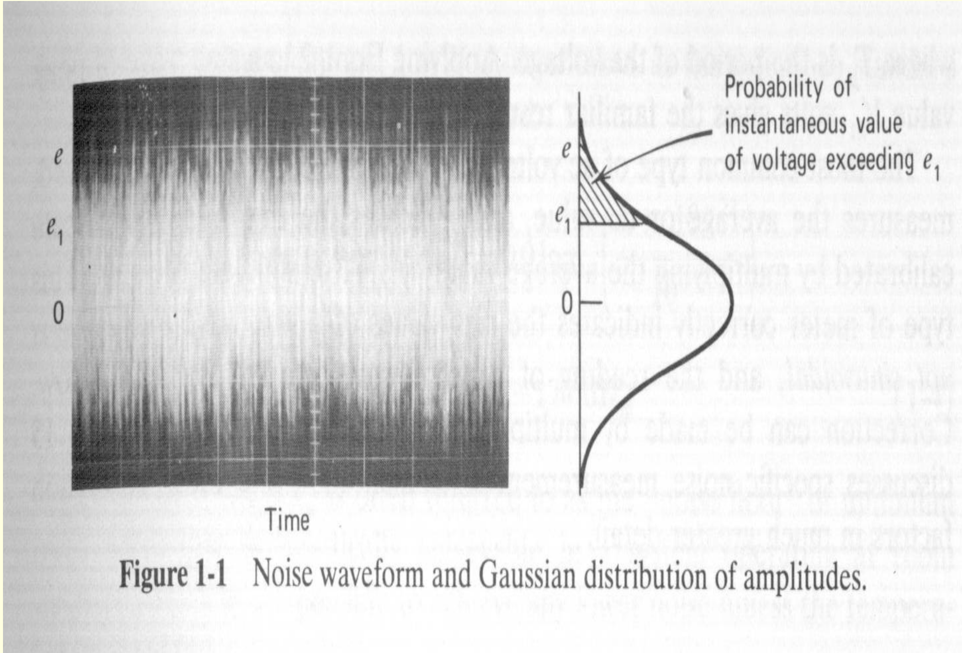
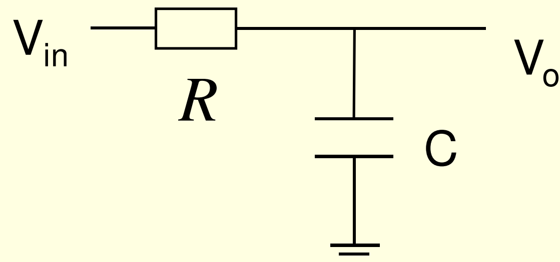


Figure 1-1 Noise waveform and Gaussian distribution of amplitudes.

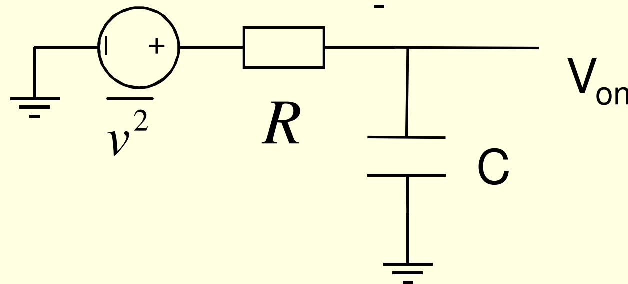
Source: Motchenbacher

2.2 Noise and Distortion

kT/C noise



$$\frac{V_o}{V_{in}} = H(j\omega) = \frac{1}{1 + j\omega RC}$$



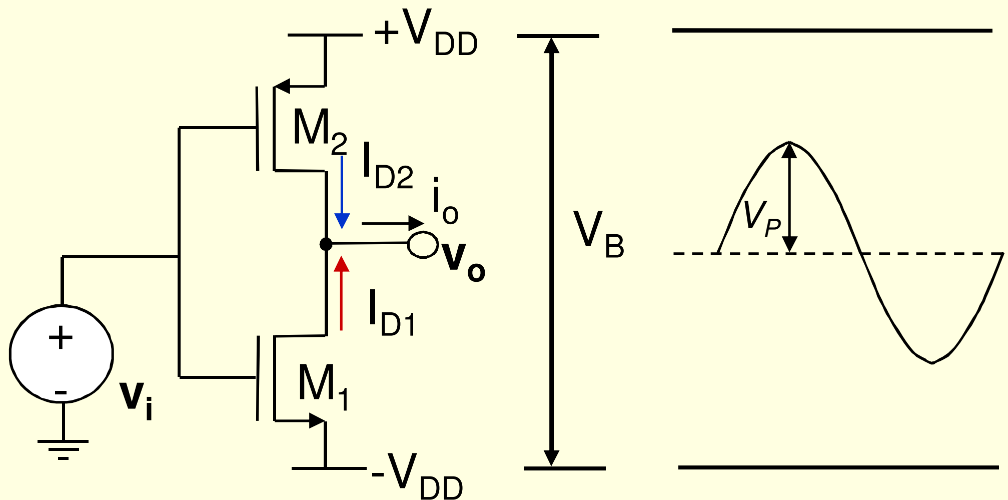
$$\frac{V_{on}}{V} = H(j\omega) \qquad \frac{\overline{v_{on}^2}}{\Delta f} = \left|H(j\omega)\right|^2 \frac{\overline{v^2}}{\Delta f}$$

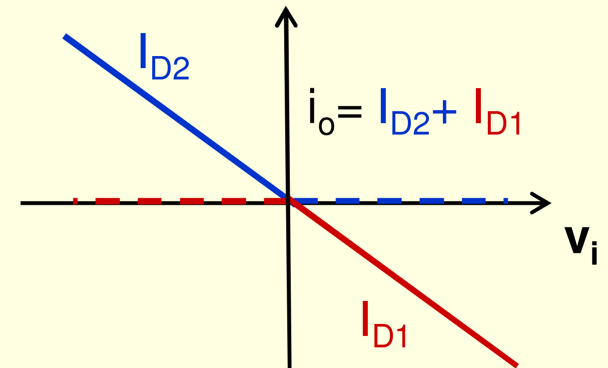
$$\overline{v_{on}^2} = \int_0^\infty \frac{1}{1+(\omega RC)^2} 4kTR \frac{d\omega}{2\pi} = \frac{kT}{C}$$

As stated by thermodynamics (*energy equipartition principle*).

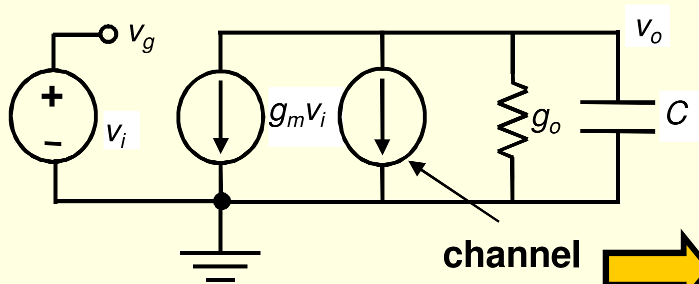
2.2 Noise and Distortion

Power vs. signal-to-noise ratio



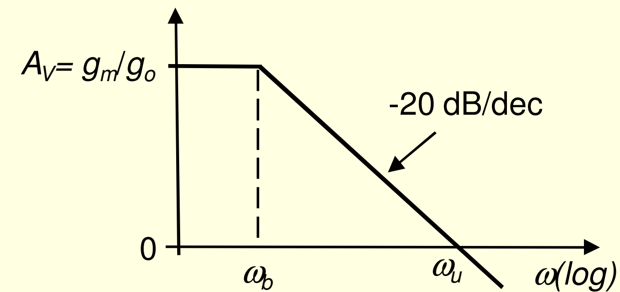


"Idealized" class-B transconductor



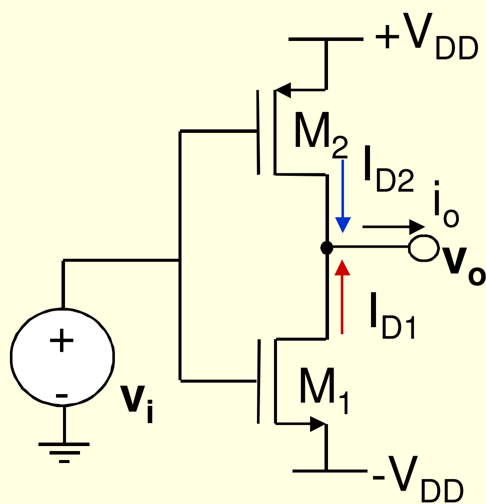
channel noise

$$\frac{\overline{i_n^2}}{\Delta f} = 4\gamma k T g_m$$



2.2 Noise and Distortion

Power vs. signal-to-noise ratio



Output noise voltage $$\overline{v_{o,n}^2} = \gamma \frac{kT}{C} \frac{g_m}{g_o} \quad \textbf{(i)}$$

Output signal voltage $$\overline{v_{o,s}^2} = \frac{V_P^2}{2} \quad \textbf{(ii)} \qquad v_o = V_P \sin \omega t$$

Power delivered by the supplies is $$P = \frac{V_B V_P}{\pi} g_o \quad \textbf{(iii)}$$

From (i) – (iii): $$P = 4\gamma \frac{V_B}{V_P} \frac{g_m}{g_o} \left(kT \cdot \Delta f \cdot S / N \right)$$

with $$\Delta f = \frac{g_o}{2\pi C}$$

2.2 Noise and Distortion

Distortion – The output signal is limited by the maximum acceptable nonlinearity. In the previous case, $V_P/V_B<0.5$

Dynamic range: Usually defined as the $(S/N)_{max}$, with the maximum signal defined as that for which the distortion is acceptable.

2.3 Parasitic capacitors

Power consumption increases due to parasitic capacitors:

- **More transconductance (and current) is needed for keeping the speed;**
- **Phase shift introduced by parasitic capacitances may require compensation capacitance (and more current to reach the gain-bandwidth product)**

2.4 Mismatch & 1/f Noise

Both mismatch and 1/f noise are ~ proportional to the inverse of the gate area.

If both mismatch (to improve dc accuracy) and 1/f noise (to improve S/N ratio) are reduced through an area increase, parasitic capacitances also increase, giving rise to increased current consumption to reach the required speed.

& Charge Injection for switched-capacitor circuits

2. Fundamental limitations in analog integrated circuits

E. Sánchez-Sinencio and A. G. Andreou (eds.), *Low-Voltage/ Low Power Integrated Circuits and Systems*, IEEE Press, New York, 1999.

J. D. Meindl, "Low Power Microelectronics: Retrospect and Prospect," *Proc. of the IEEE*, vol.83, no.4, pp. 619-635, Apr. 1995.

SSCS News, Summer 2008, vol. 13, no. 3 (Issue on the work and impact of *Prof. Eric Vittoz*).

C. Toumazou, G. Moschytz, and B. Gilbert (eds.), *Trade-offs in Analog Circuit Design – The Designer's Companion*, Kluwer, 2002 (see the excellent Chapter 10, by E. A. Vittoz and Y. P. Tsividis).

R. Cavin and W. Liu, Emerging Technologies – Designing Low Power Digital Systems, Tutorial for 1996 ISCAS**,** (see Chapter 1.2, by C. C. Enz and E. A. Vittoz).

http://www.mead.ch/ (courses on Low-power & Low-voltage)

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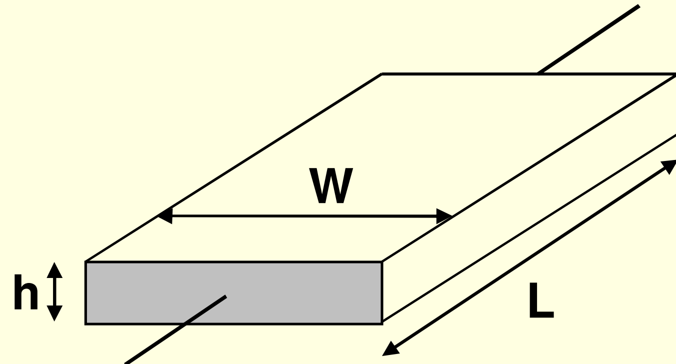
3.1. Resistors



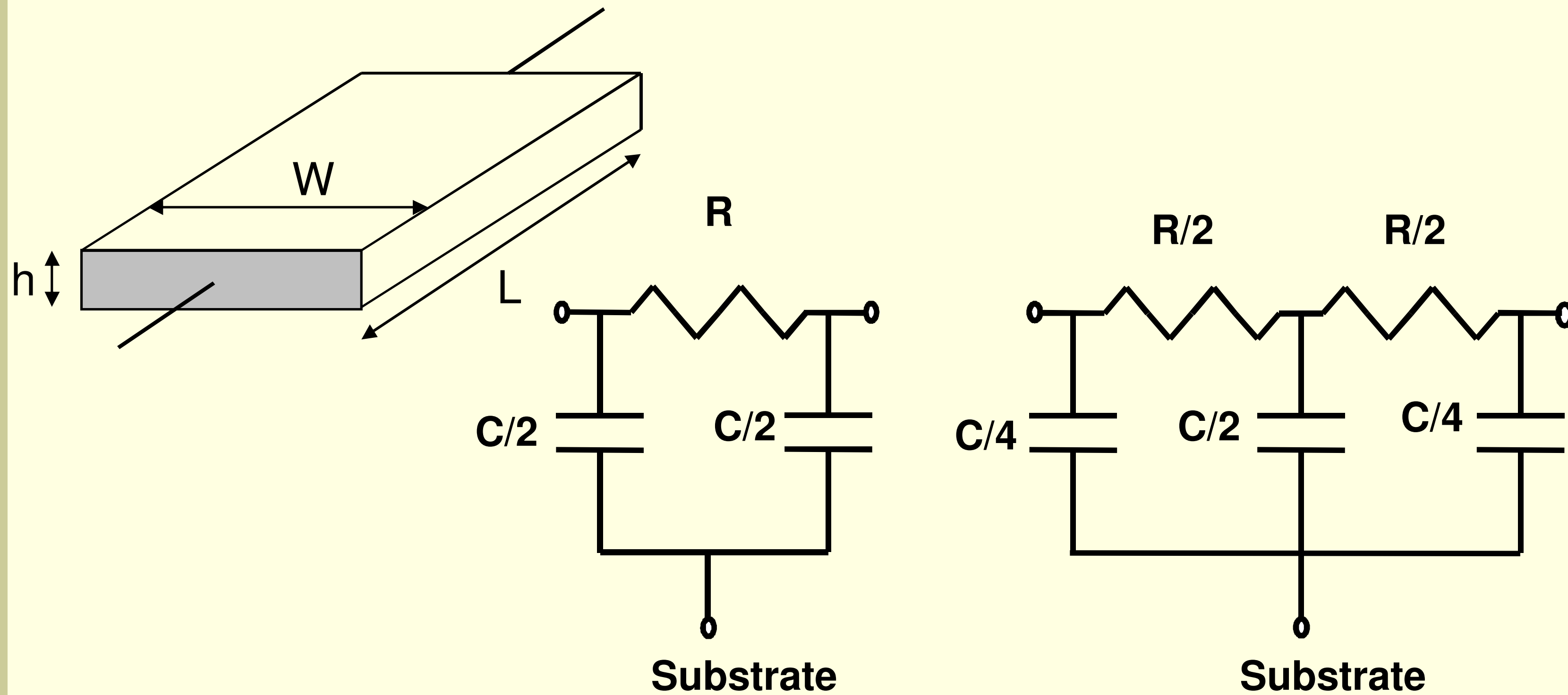
$$R = \rho \frac{L}{hW} = \frac{L}{W}\left(\frac{1}{hq\mu n}\right) = \frac{L}{W} R_{SH}$$

$$TCR = \left(d\rho / \rho\right) / dT\Big|_{T=T_a}$$

$$VCR = \left(d\rho / \rho\right) / dV\Big|_{V=V_{ref}}$$

Resistor type	R_{SH} (Ω/sq)	TCR (ppm/°C)	VCR (ppm/V)
n^+ Polysilicon	100	-800	50
p^+ Polysilicon	200	200	50
n^+/ p^+ Polysilicon (silicided)	5		
n^+ Diffusion	50	1500	500
p^+ Diffusion	100	1500	500
n-Well	1000	2500	10000

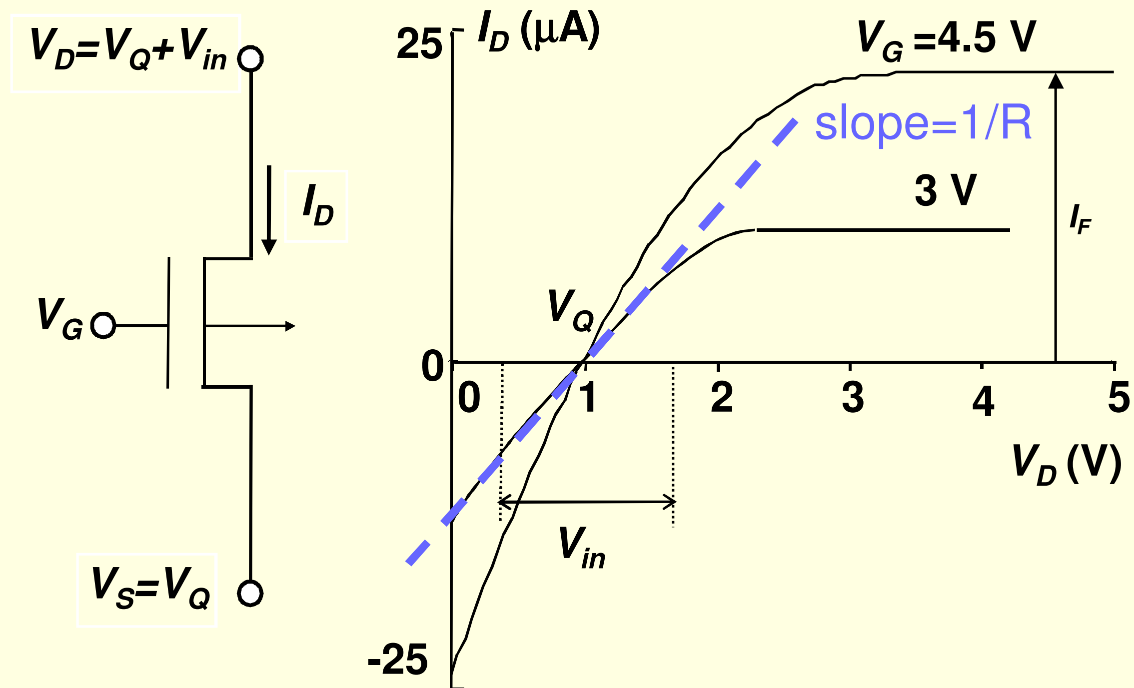
3.1. Resistors



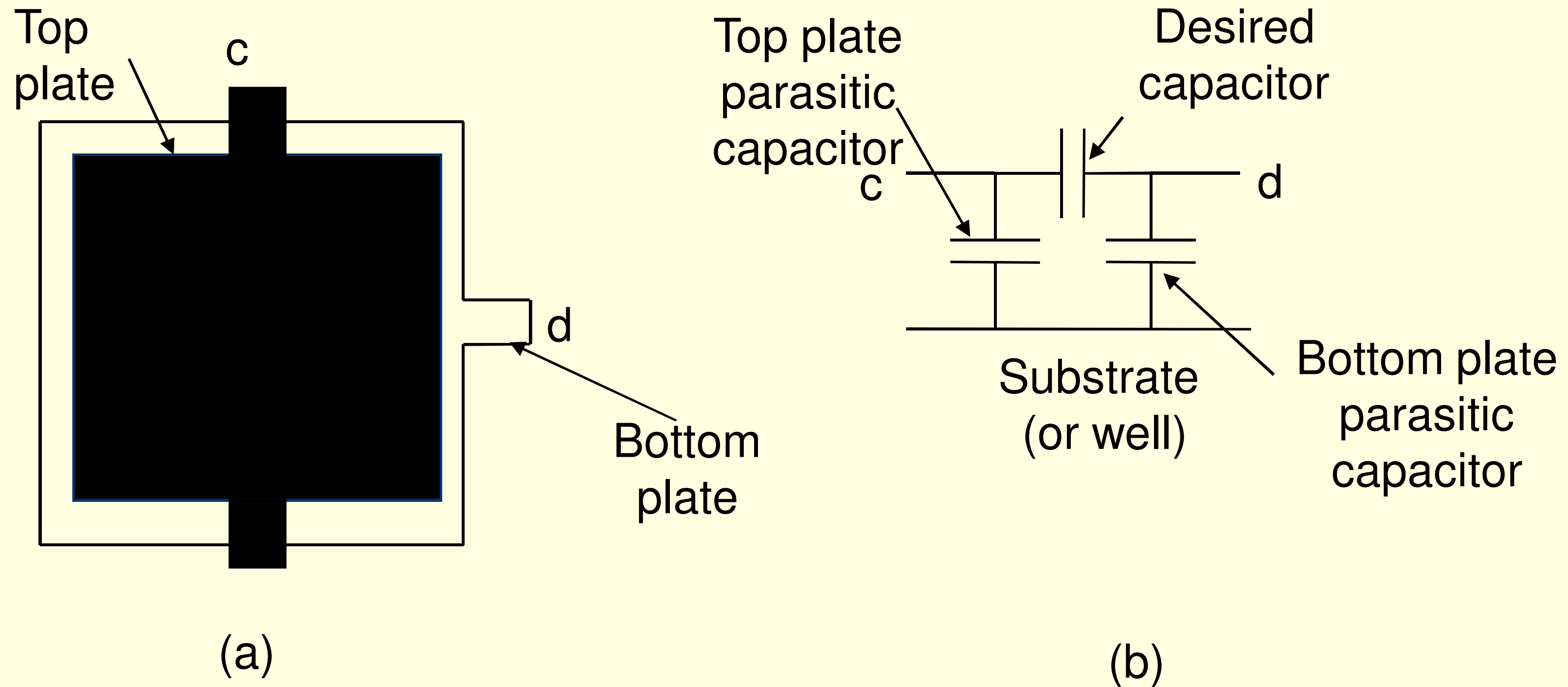
Single-π and double-π equivalent circuits for a polysilicon resistor

3.1. Resistors

The MOSFET as a voltage-controlled resistor $R=R(V_G)$



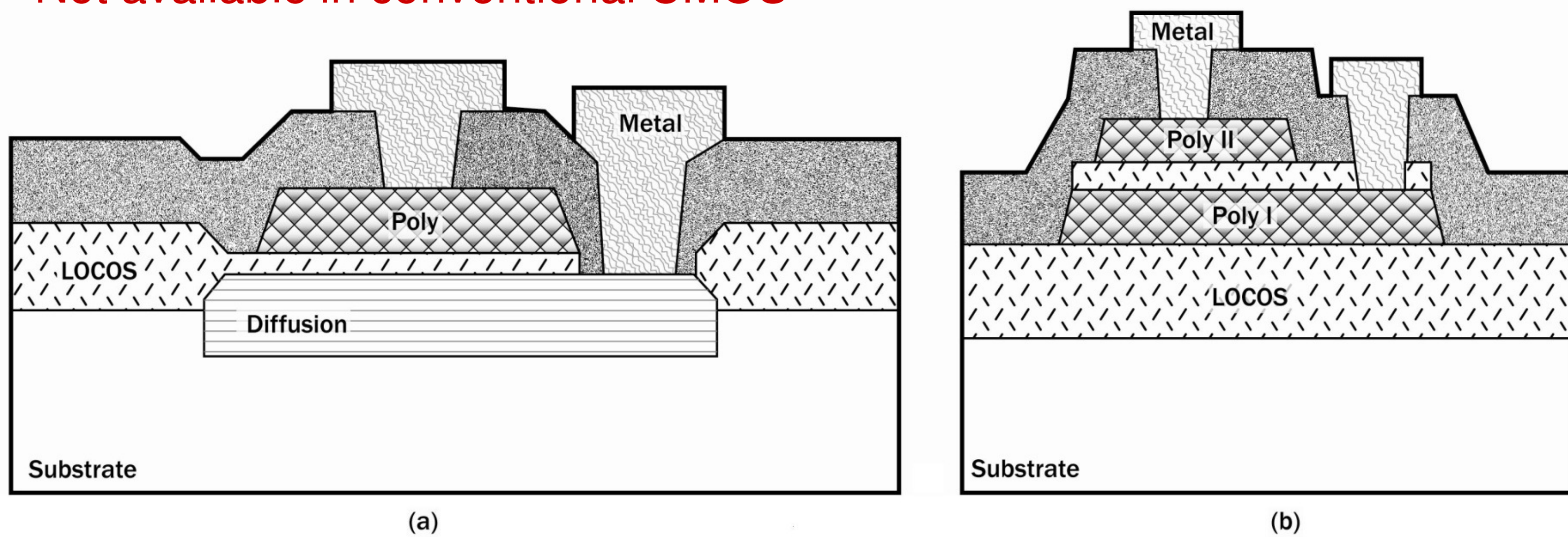
3.2. Capacitors



Integrated parallel plate capacitor (a) Simplified structure; (b) equivalent circuit.

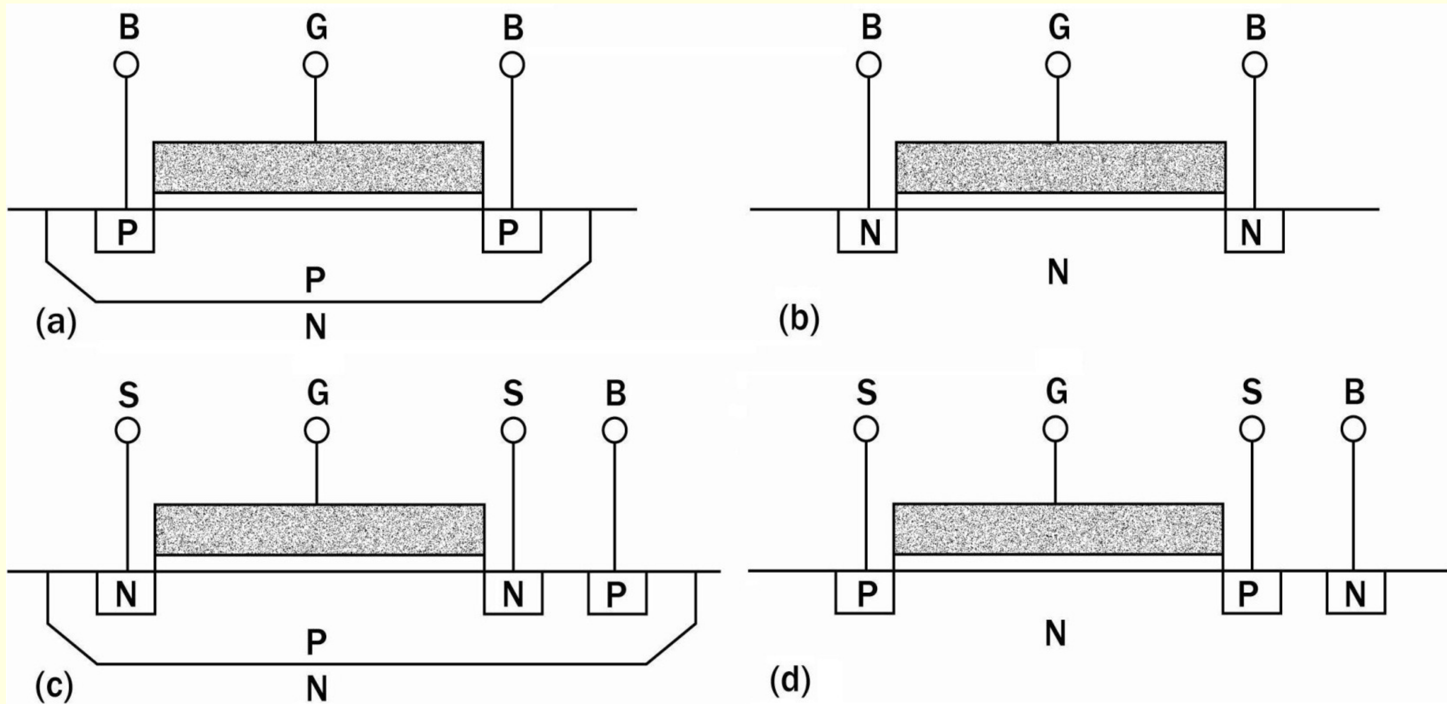
Warning: The integrated capacitor is an RC line

3.2. Capacitors



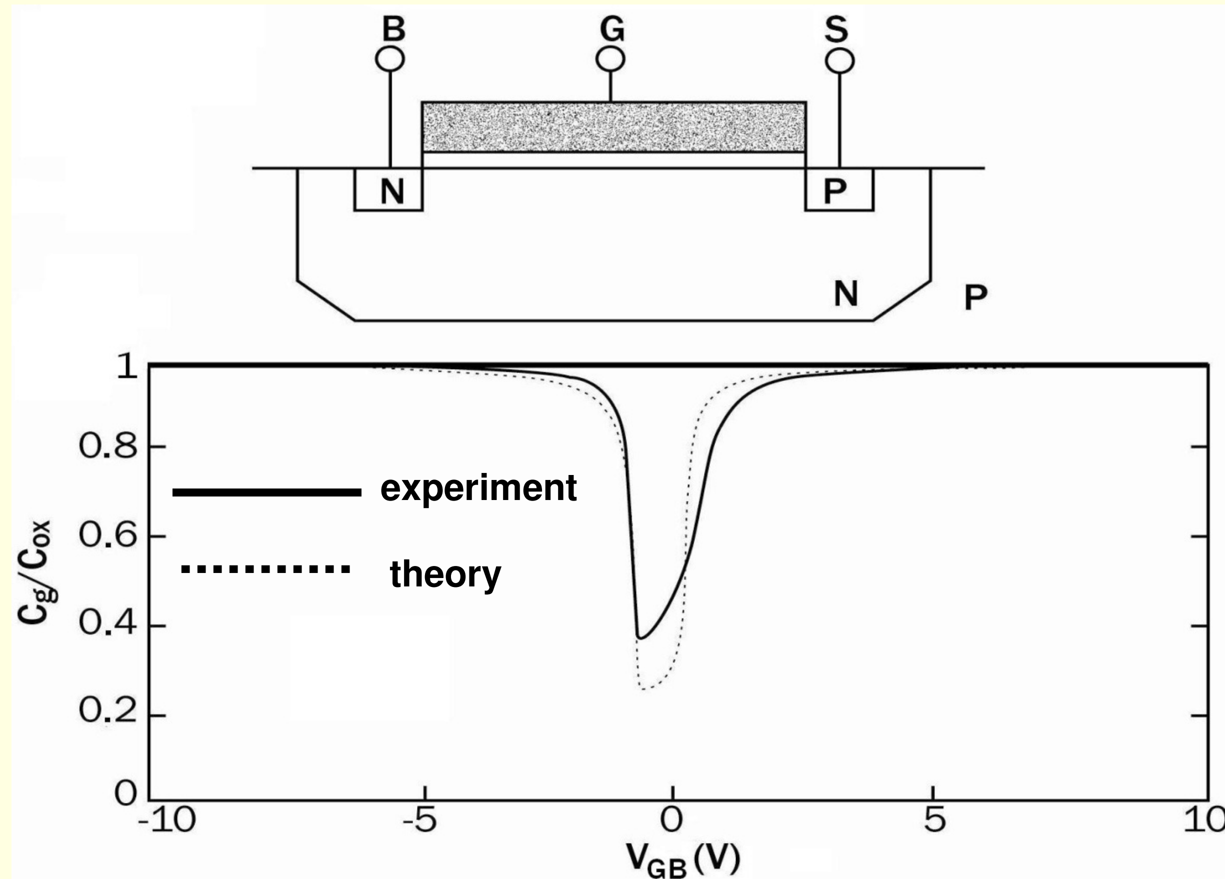
(a) Poly-semiconductor and (b) poly-poly capacitors

3.2. Capacitors



Gate capacitors in a p-well CMOS technology

3.2. Capacitors

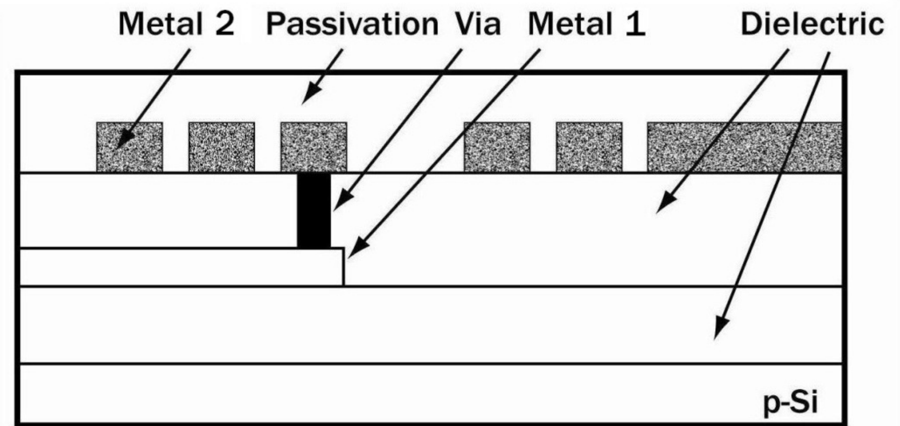


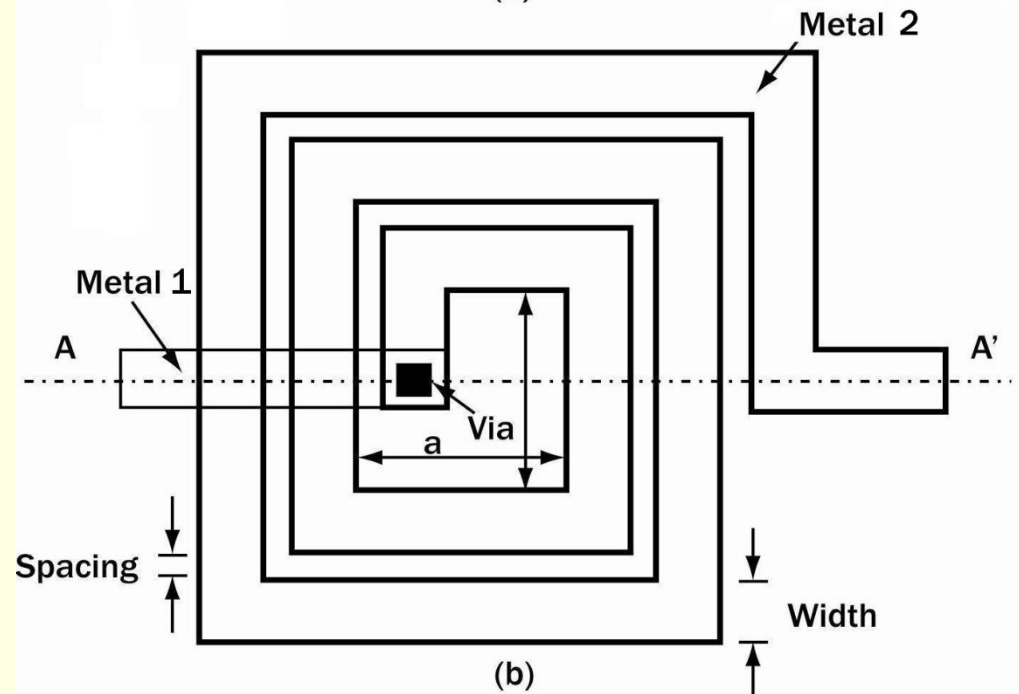
Capacitor in n-well CMOS technology and its corresponding gate capacitance for V_{BS}=0.

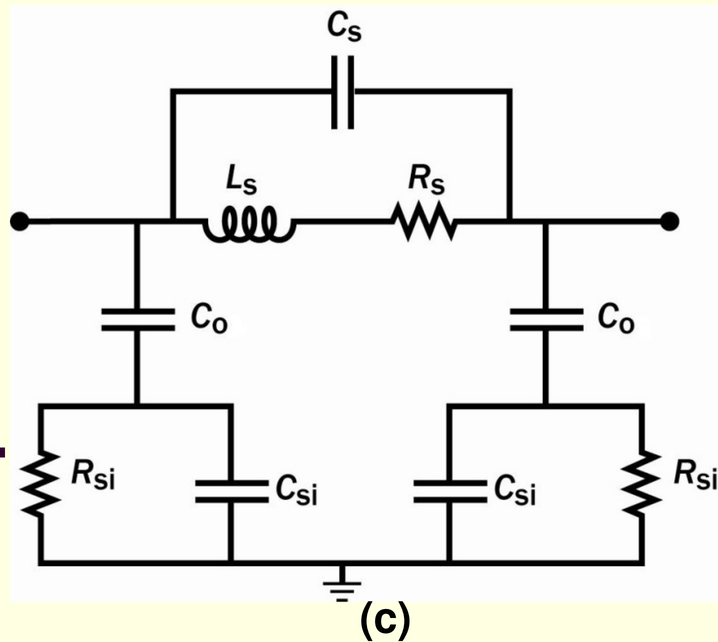
3.3. Inductors

Either bond wires or planar spirals

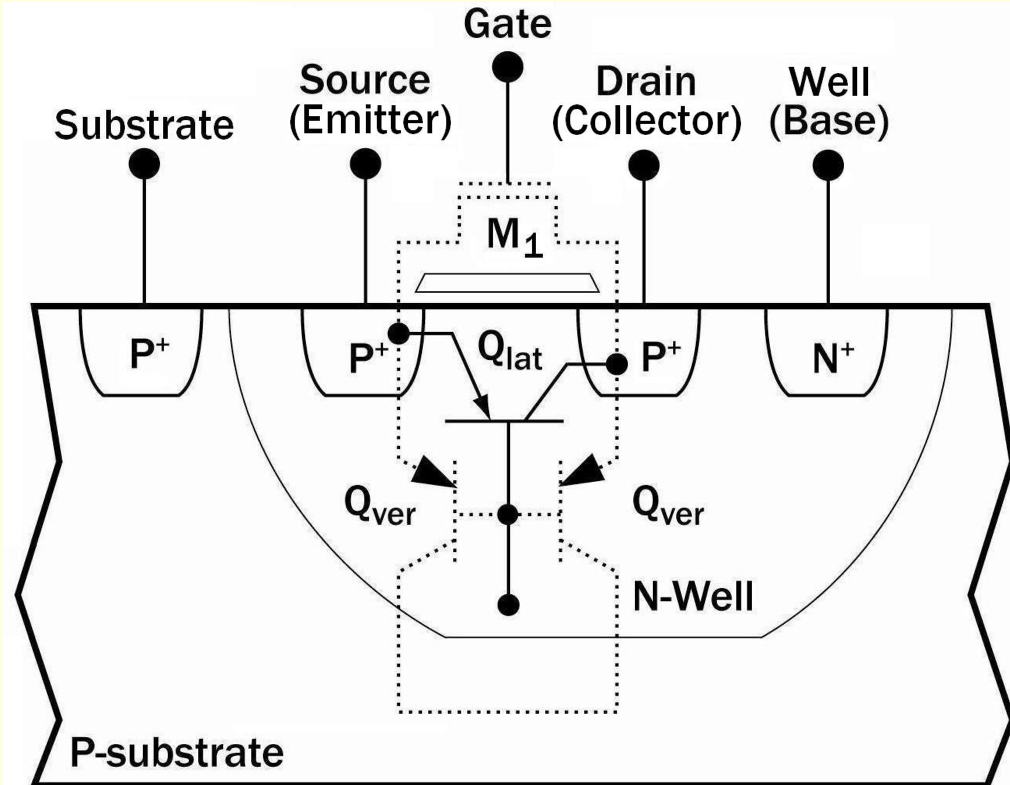
(a) Cross section, (b) top view and (c) lumped model of a planar spiral inductor







3.4. Bipolar Transistors

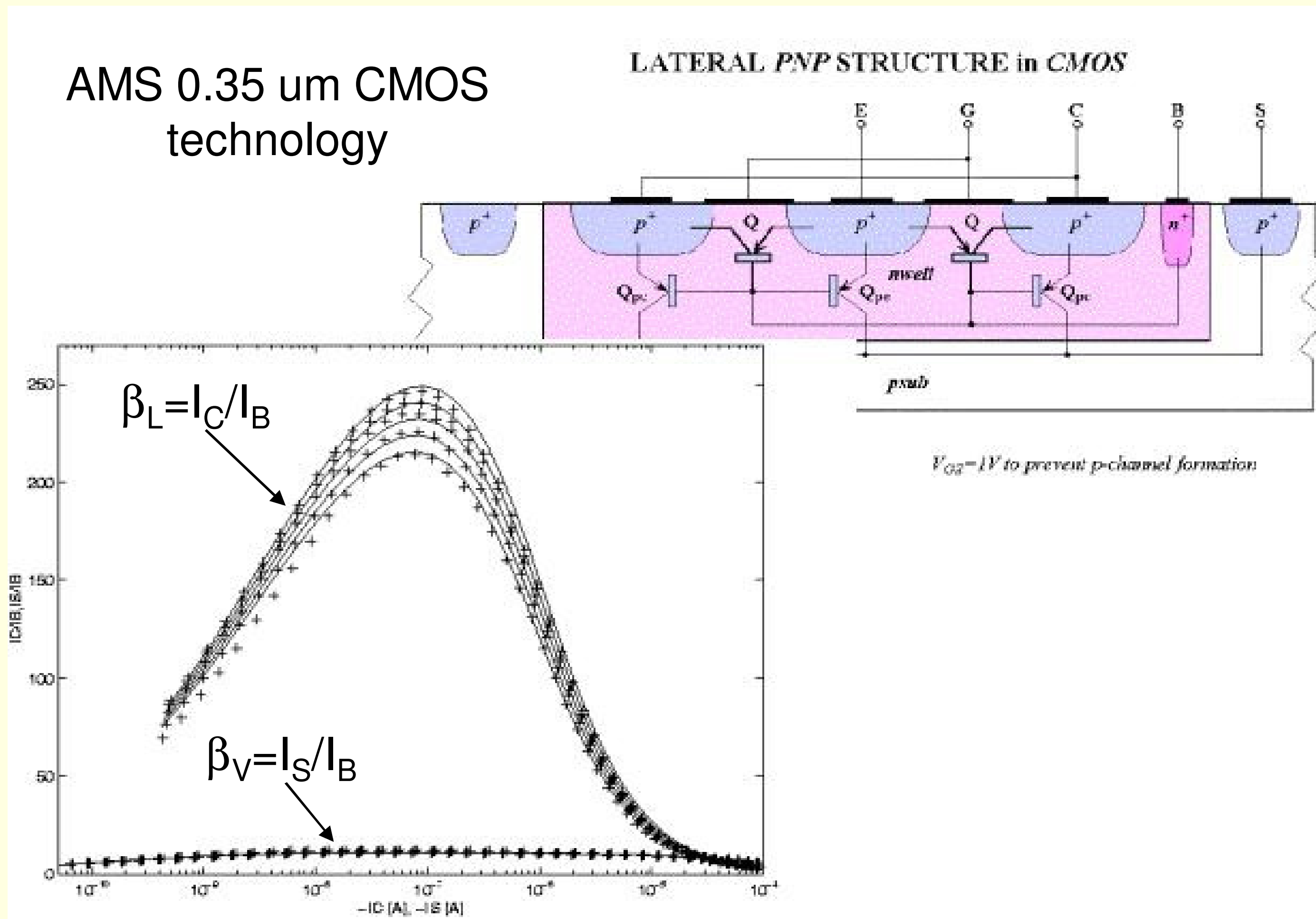


Cross section of bipolar lateral and vertical (substrate) devices in CMOS technology

CMOS-compatible bipolar transistors

P. R. Gray, P. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th. Edn., Wiley, New York, 2001.
E. A. Vittoz, Micropower Techniques, Chapter 3 in Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing, J. E. Franca and Y. Tsividis (eds.), Prentice-Hall, 1994

3.4. Bipolar Transistors



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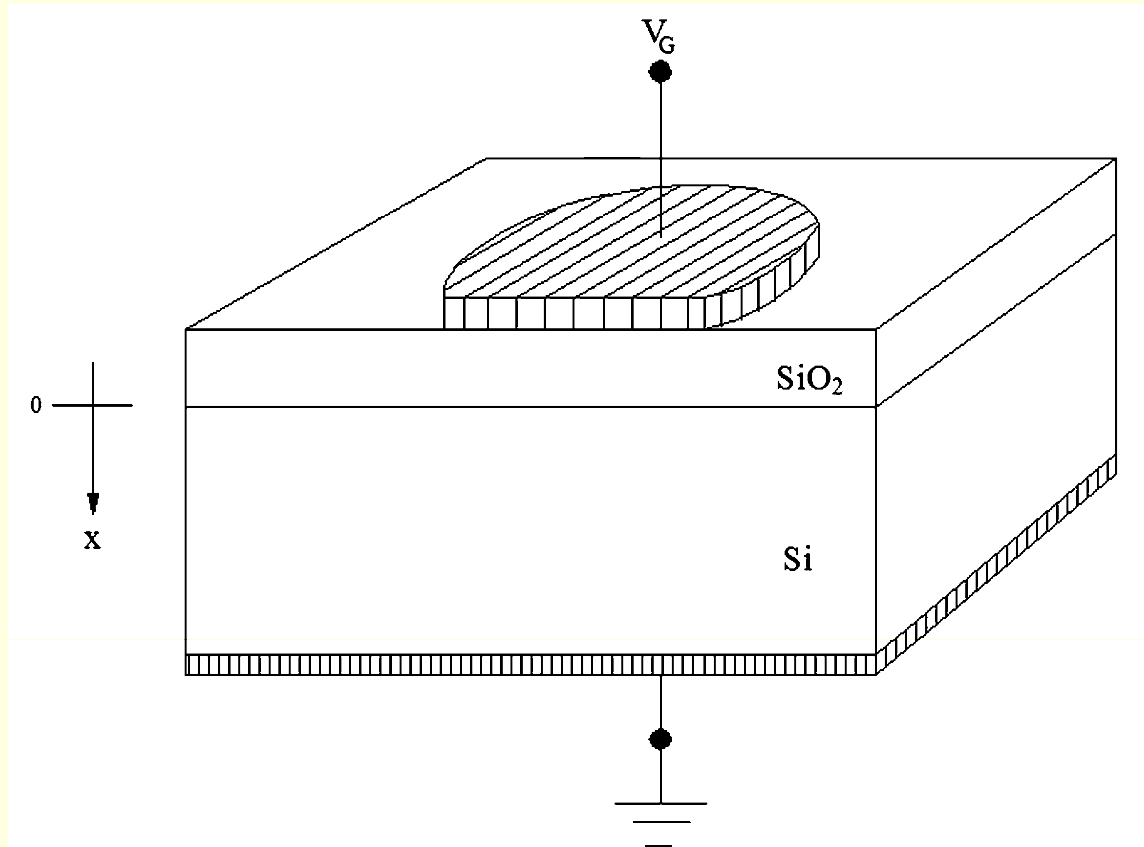
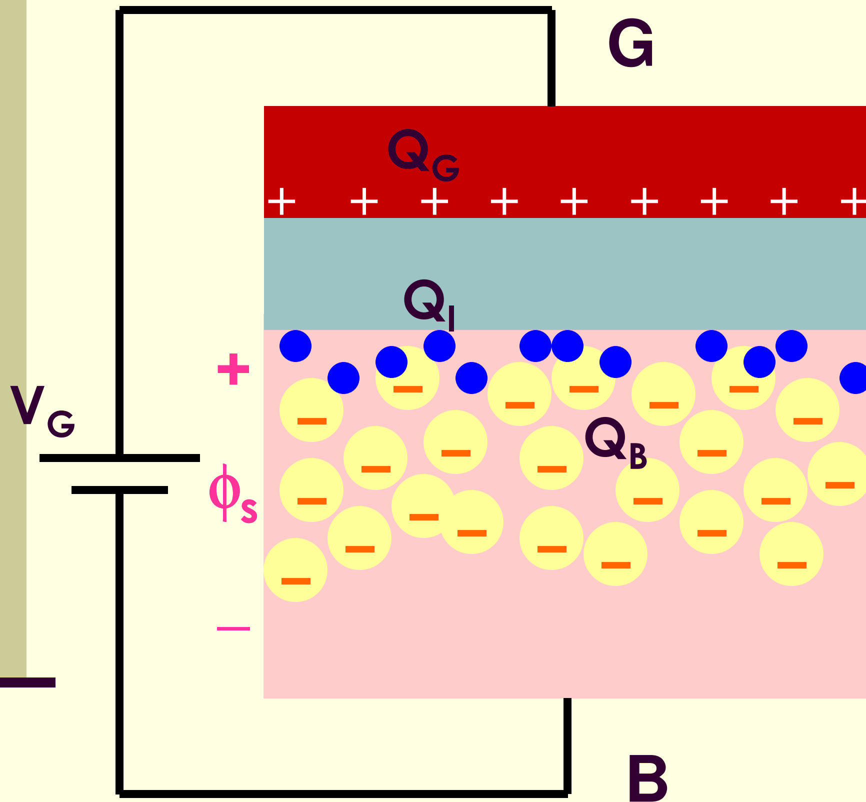
4.1 The two-terminal MOS structure



4.1 The two-terminal MOS structure



V_G gate-to-bulk voltage

C'_{ox} oxide capacitance per unit area

ϕ_s surface potential

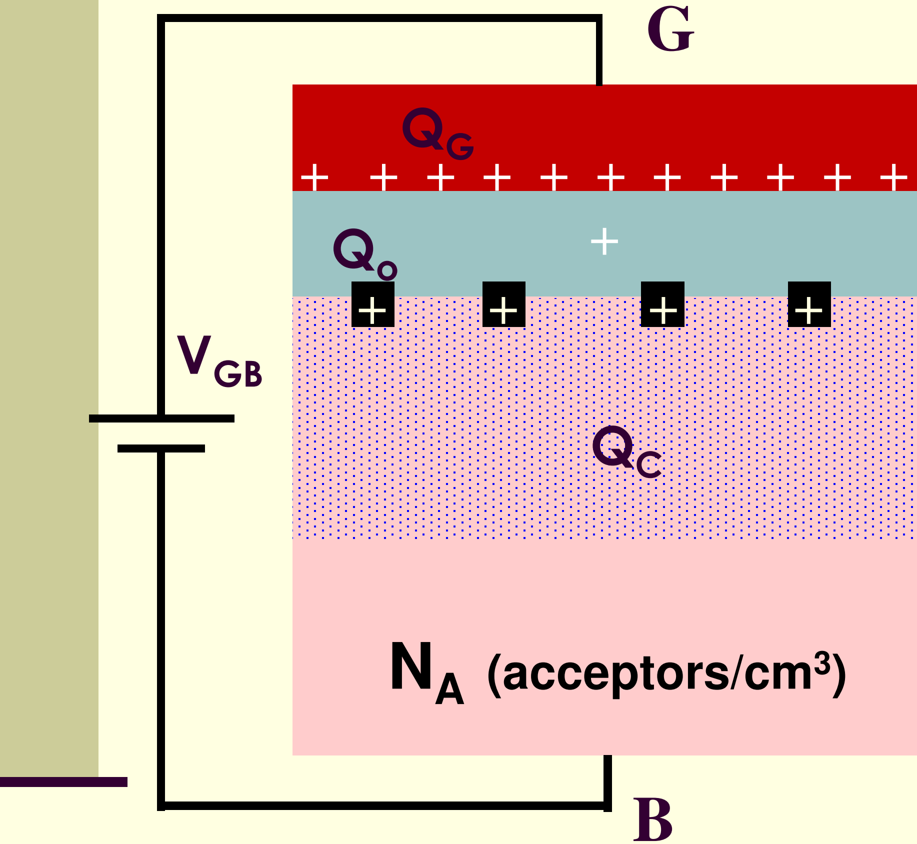
Q'_I inversion charge per unit area

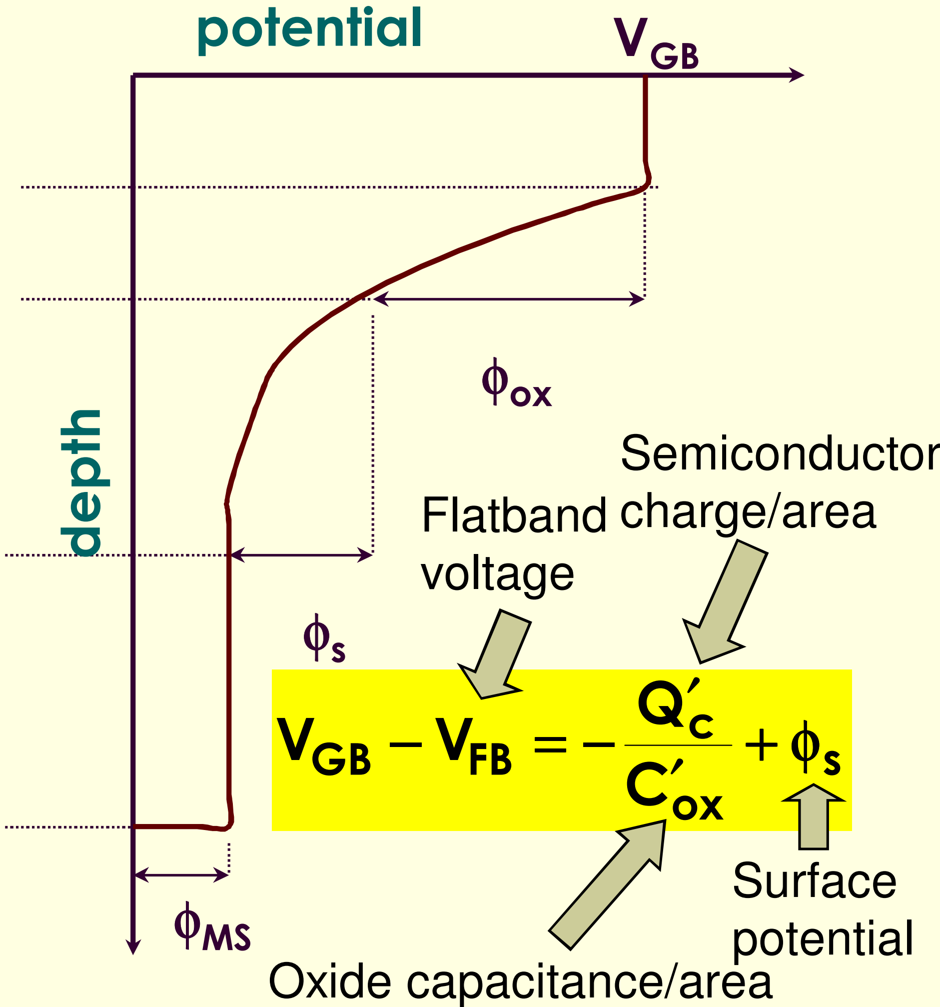
Q'_B bulk charge per unit area

V_{FB} flat-band potential

$$Q'_G = C'_{ox}\left(V_G - V_{FB} - \phi_s\right) = -(Q'_I + Q'_B)$$

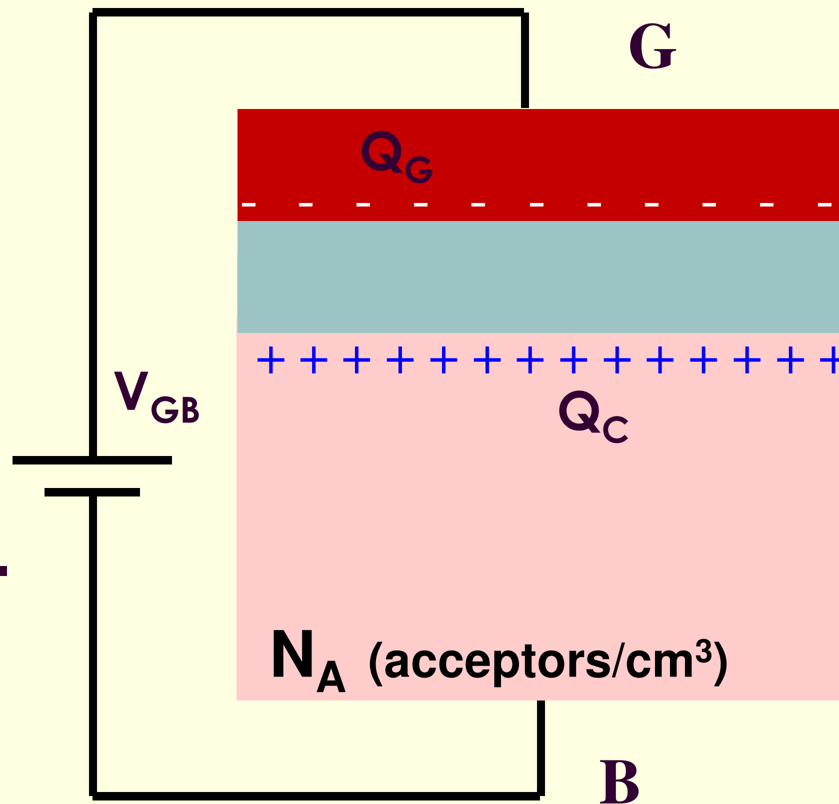
4.2 MOS capacitor voltage balance





4.3 Operation regimes

Accumulation



$V_{GB} < V_{FB}$

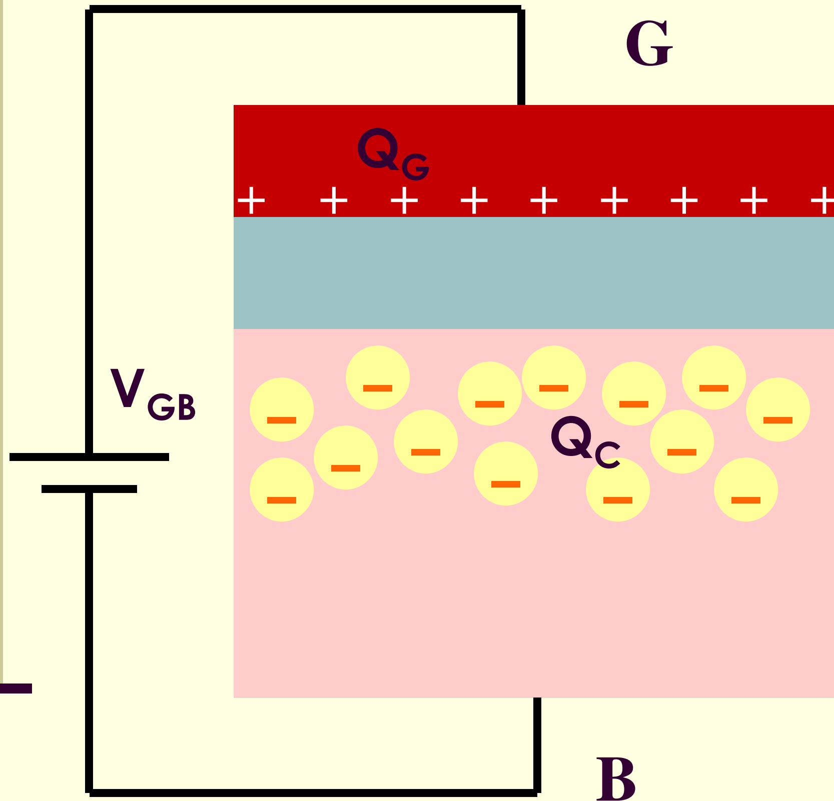
$Q'_C > 0$

$\phi_s < 0$

Holes + accumulate in the P semiconductor surface

4.3 Operation regimes

Depletion



$V_{GB} > V_{FB}$

$Q'_C < 0$

$0 < \phi_s < \phi_F$

Holes evacuate from the P semiconductor surface and acceptor ion charges – become uncovered

ϕ_F = Fermi potential $\cong \phi_t . \ln(N_A/n_i)$

N_A = acceptor concentration

n_i = intrinsic concentration

ϕ_t = thermal voltage = KT/q

4.3 Operation regimes

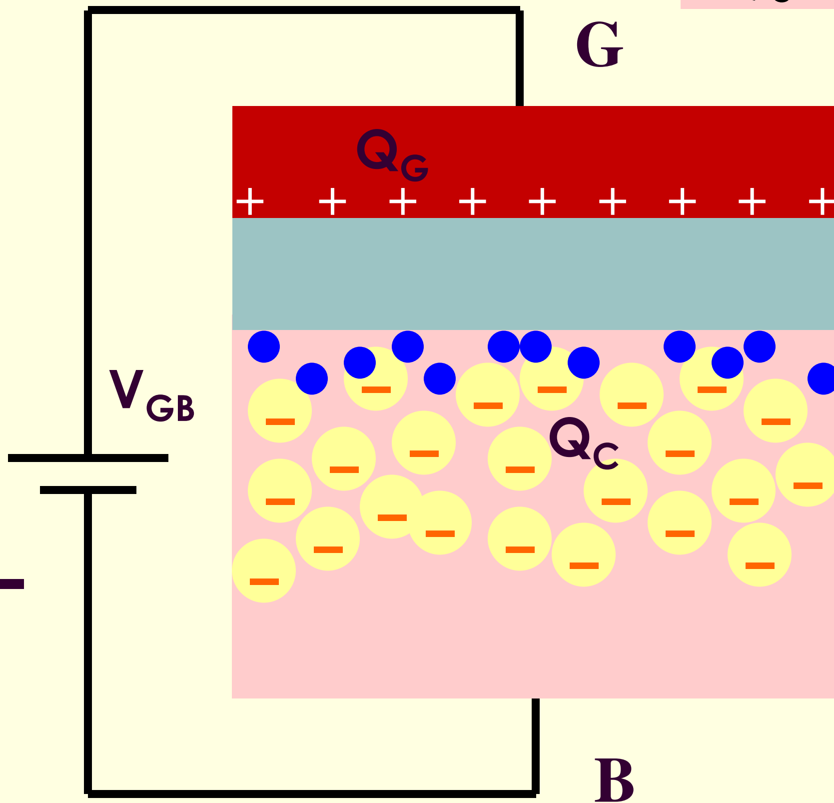
Inversion

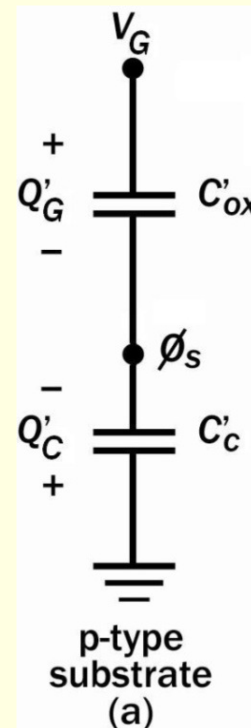
$V_{GB} > V_{FB}$

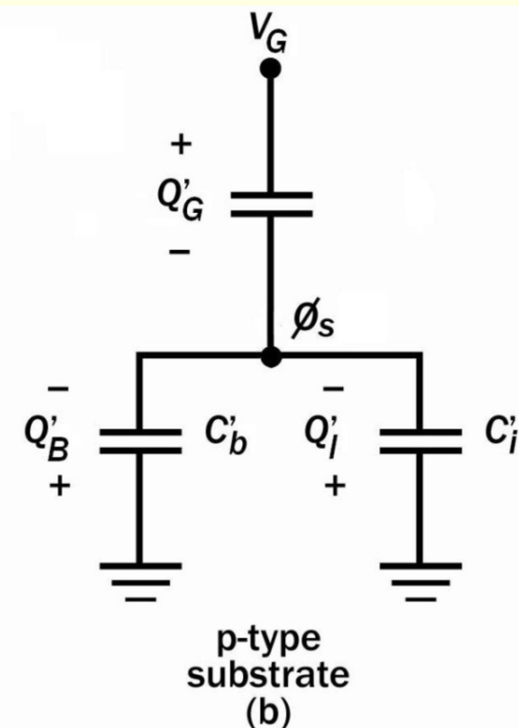
$Q'_C < 0$

$\phi_s > \phi_F$

electrons ● approach the surface!







4.4 MOS capacitor small-signal equivalent circuit

$$C'_{gb} = \frac{dQ'_G}{dV_G}$$

$$C'_{gb} = \frac{1}{\frac{1}{C'_c} + \frac{1}{C'_{ox}}}$$

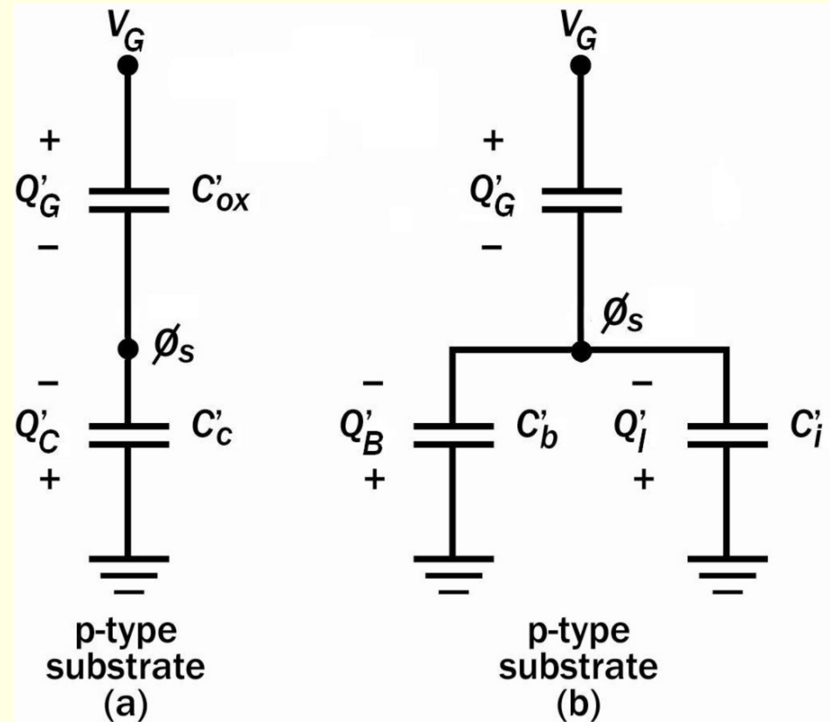
$$C'_c = C'_b + C'_i$$

$$C'_i = -\frac{dQ'_I}{d\phi_s} \cong -\frac{Q'_I}{\phi_t}$$

$$\phi_t = \frac{kT}{q}$$ thermal voltage (26 mV @ 300K)

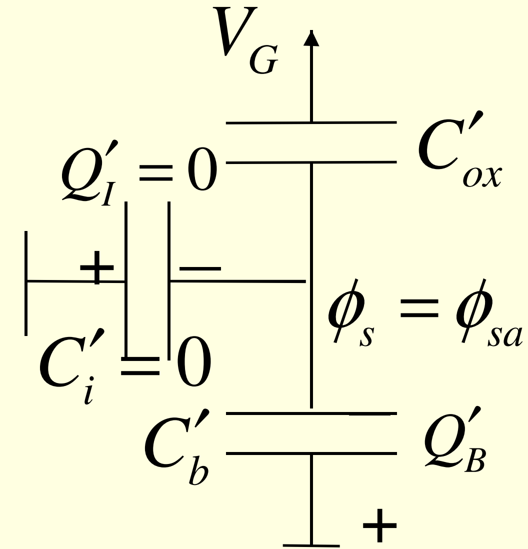
$$C'_b \cong \frac{\gamma C'_{ox}}{2\sqrt{\phi_s - \phi_t}}$$

γ body-effect coefficient



4.5 The linearization surface potential

Determination of $\phi_{sa} = \phi_s \big|_{Q_I'=0}$

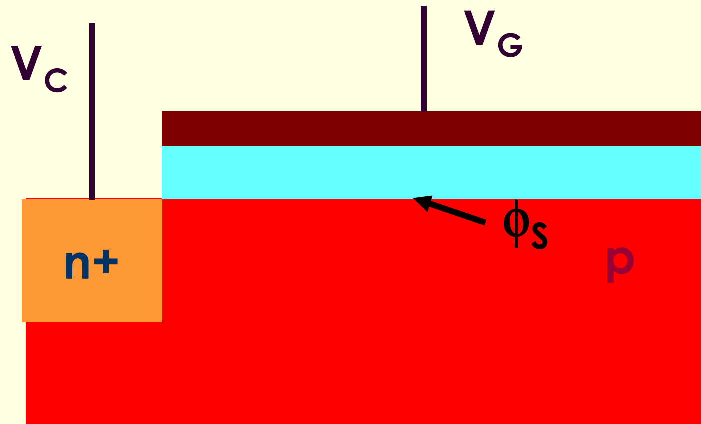


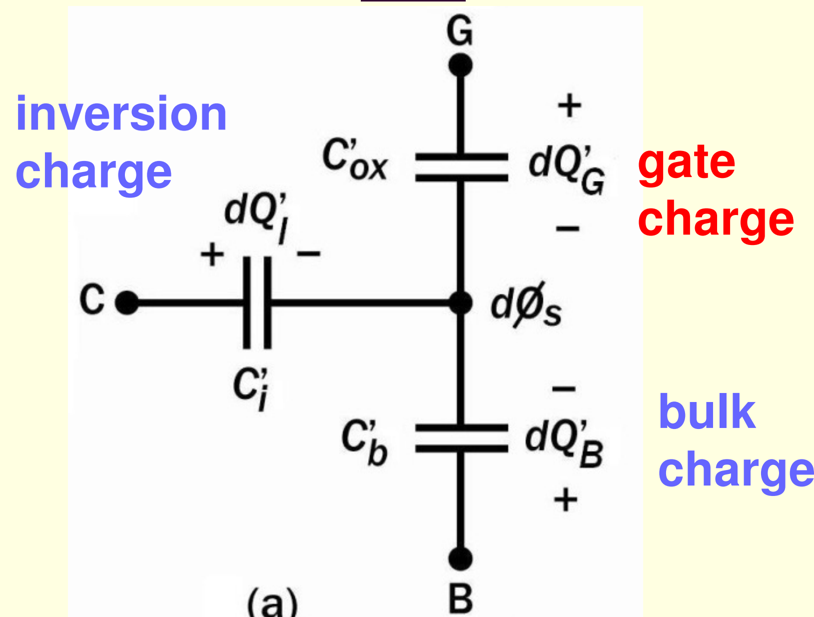
Potential balance

$$V_G - V_{FB} = \phi_{sa} + sgn(\phi_{sa})\gamma\sqrt{\phi_{sa} + \phi_t\left(e^{-\phi_{sa}/\phi_t} - 1\right)}$$

$$\frac{dV_G}{d\phi_{sa}} = n = 1 + \frac{C_b'}{C_{ox}'} = 1 + \frac{\gamma\left(1 - e^{-\phi_{sa}/\phi_t}\right)}{2\,\mathrm{sgn}\left(\phi_{sa}\right)\sqrt{\phi_{sa} + \phi_t\left(e^{-\phi_{sa}/\phi_t} - 1\right)}}$$

4.6 The three-terminal MOS structure





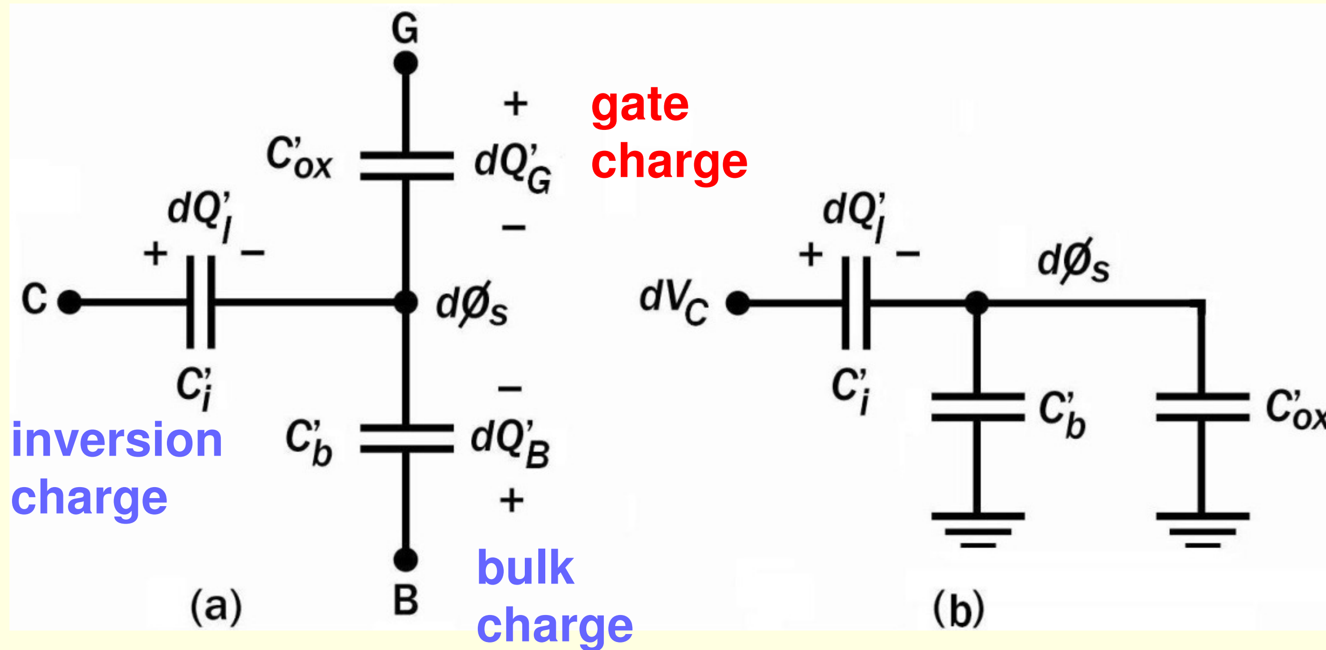
Carrier concentrations in Si substrate follow Boltzmann's law:

$$n, p \propto \exp(-Energy/kT)$$

$$n = n_o \exp[(\phi - V_C)/\phi_t]$$

$$n_o = n_i^2/N_A$$

4.6 Small-signal equivalent capacitive circuit



$$C_i' = -\left.\frac{\partial Q_I'}{\partial \phi_s}\right|_{V_C}$$ **Inversion capacitance/area**

$$C_b' = -\left.\frac{\partial Q_B'}{\partial \phi_s}\right|_{V_C}$$ **Bulk capacitance/area**

Compact MOSFET models are essentially based on how the nonlinear capacitances

C_b' **&** C_i'

are approximated in terms of voltages

4.7 The pinch-off charge density

The channel charge density corresponding to the effective channel capacitance times the thermal voltage, or thermal charge, defines pinch-off

$$Q'_{IP} = -(C'_{ox} + C'_b)\phi_t = -nC'_{ox}\phi_t$$

The name pinch-off is retained herein for historical reasons and means the channel potential corresponding to a small (but well-defined) amount of carriers in the channel.

4.7 The pinch-off voltage V_P

The channel-to-substrate voltage (V_C) for which the channel charge density equals the pinch-off charge density is called the pinch-off voltage V_P.

in weak inversion ⇒ $$-Q'_I = C'_b \phi_t e^{(\phi_{sa} - 2\phi_F - V_C)/\phi_t} = C'_{ox}(n-1)\phi_t e^{(\phi_{sa} - 2\phi_F - V_C)/\phi_t}$$

$$Q'_I = Q'_{IP} = -nC'_{ox}\phi_t \quad \Rightarrow \quad V_C = V_P$$

$$V_P = \phi_{sa} - 2\phi_F - \phi_t \left[1 + \ln\left(\frac{n}{n-1}\right)\right]$$

$$V_P \cong \phi_{sa} - 2\phi_F$$

4.8 The threshold voltage V_{T0}

Equilibrium threshold voltage V_{T0}, for V_C=0,
gate voltage for which $Q'_I = Q'_{IP} = -nC'_{ox}\phi_t$

(gate voltage for which V_P=0)

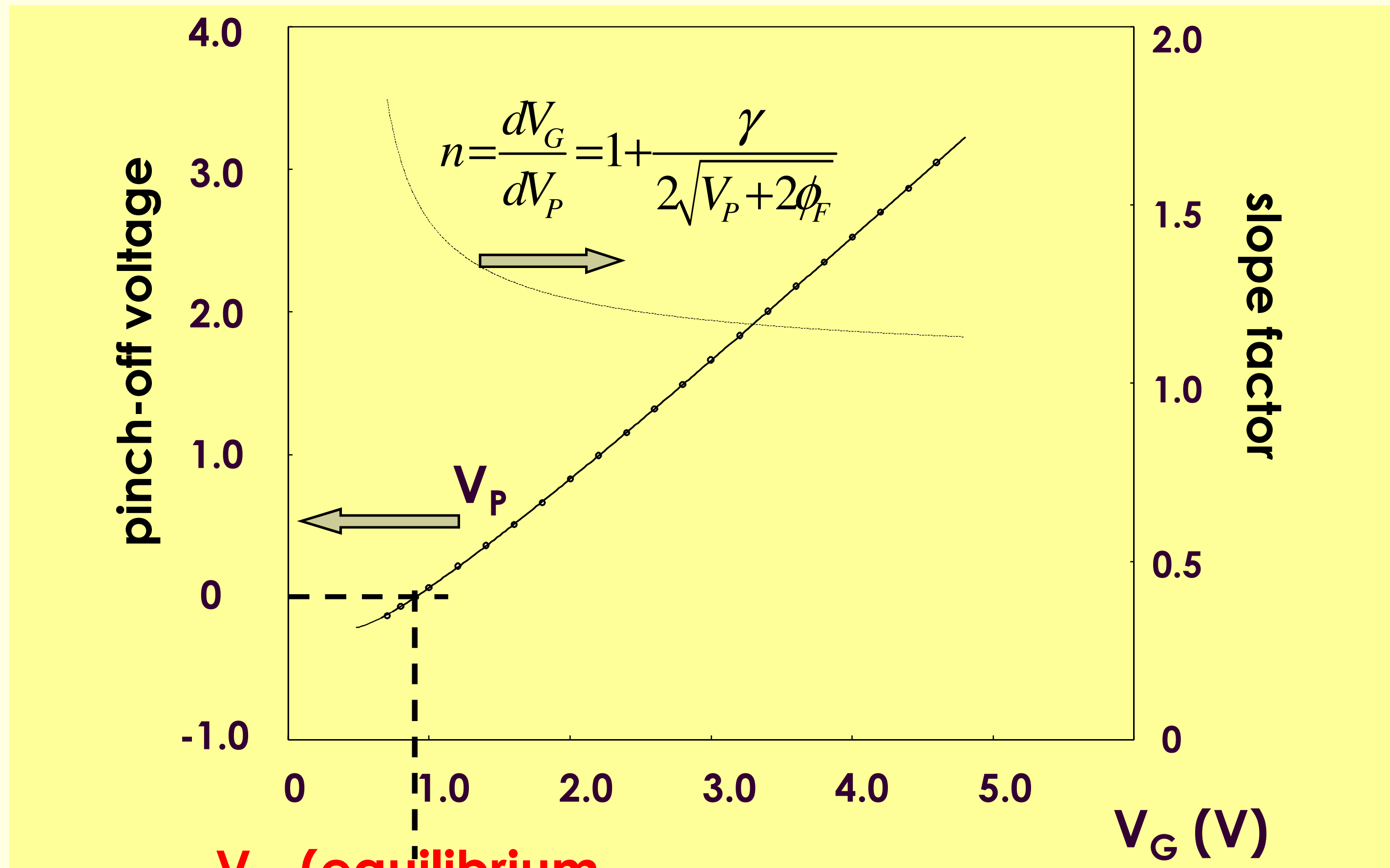
Recalling that

$$\begin{cases} V_P \cong \phi_{sa} - 2\phi_F \\ V_G - V_{FB} = \phi_{sa} + \gamma C'_{ox}\sqrt{\phi_{sa} - \phi_t} \end{cases}$$

it follows that

$$V_{T0} \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

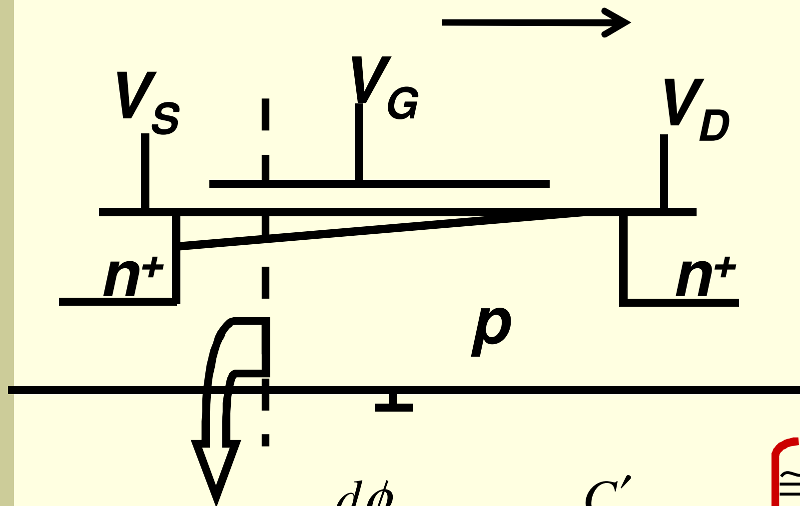
Pinch-off voltage and slope factor vs gate voltage



V_{T0} (equilibrium threshold voltage)

Useful approximation: $V_P \cong \frac{V_G - V_{T0}}{n}$

4.9 Unified charge control model (UCCM) - 1



Basic approximations:

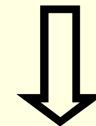
$$C'_{ox} + C'_b = nC'_{ox}$$

$$n = n(V_G)$$

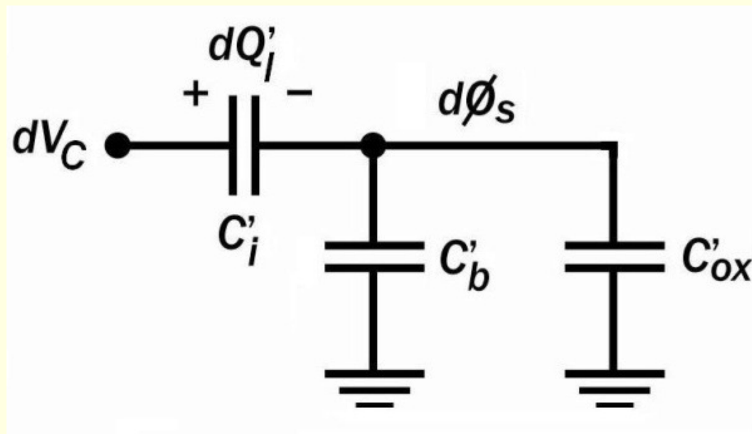
$$dQ'_I = nC'_{ox}d\phi_s$$

$$\frac{d\phi_s}{dV_C} = \frac{C'_i}{C'_i + C'_{ox} + C'_b} \begin{cases} \cong -\dfrac{Q'_I}{nC'_{ox}\phi_t} < 1 & \text{WI} \\ \cong 1 & \text{SI} \end{cases}$$

$$C'_i = -\frac{Q'_I}{\phi_t}$$



$$dV_C = dQ'_I\left(\frac{1}{nC'_{ox}} - \frac{\phi_t}{Q'_I}\right)$$



$$V_S \le V_C \le V_D$$

4.9 Unified charge control model (UCCM) - 2

Integrating $dV_C = dQ_I'\left(\frac{1}{nC_{ox}'} - \frac{\phi_t}{Q_I'}\right)$ between V_C and V_P yields UCCM

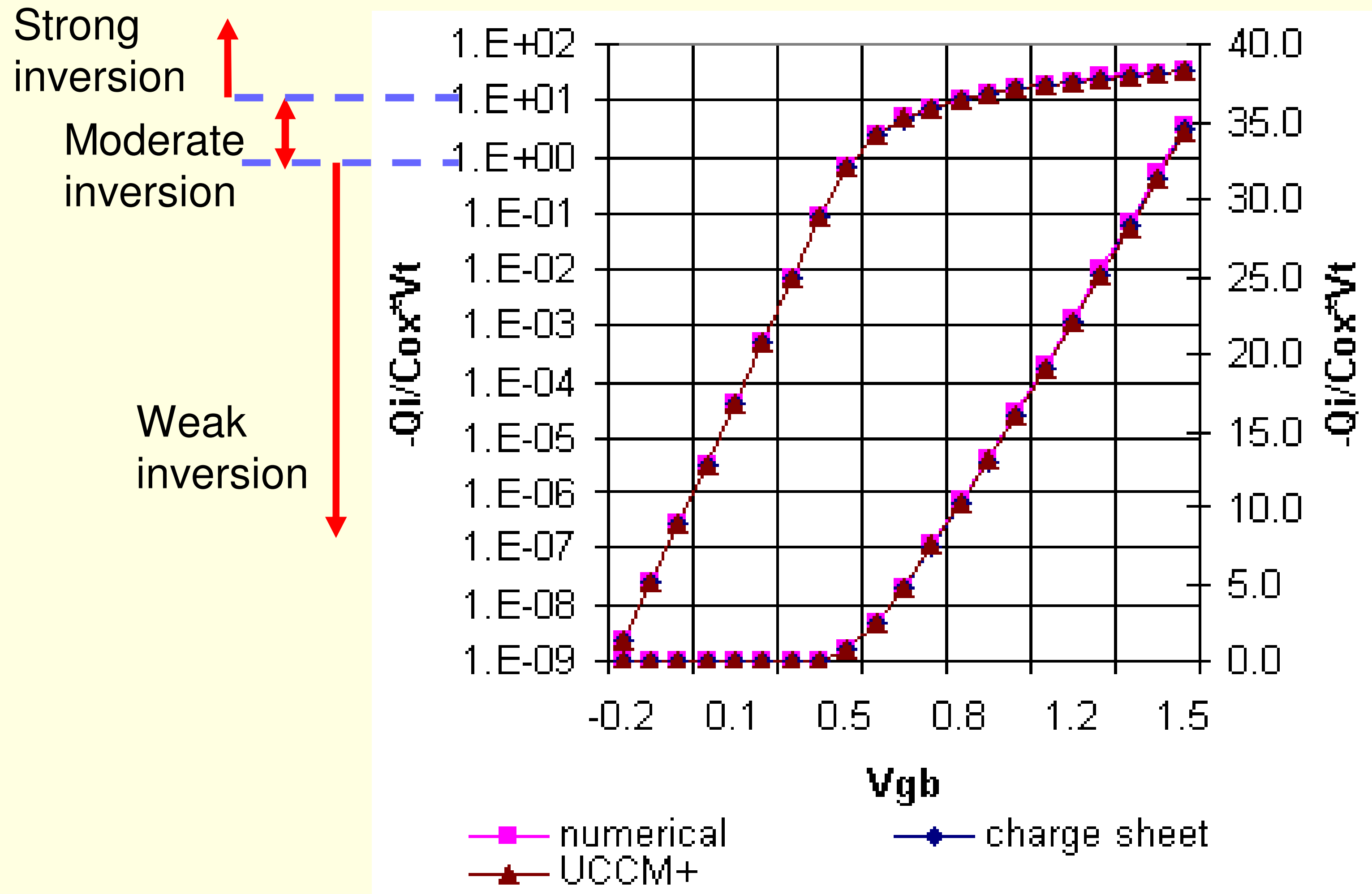
$$V_P - V_C = \frac{Q_{IP}' - Q_I'}{nC_{ox}'} + \phi_t \ln\left(\frac{Q_I'}{Q_{IP}'}\right)$$

$Q_{IP}' = -nC_{ox}'\phi_t$ Thermal (pinch-off) charge

$q_I' = \frac{Q_I'}{-nC_{ox}'\phi_t}$ Normalized inversion charge density

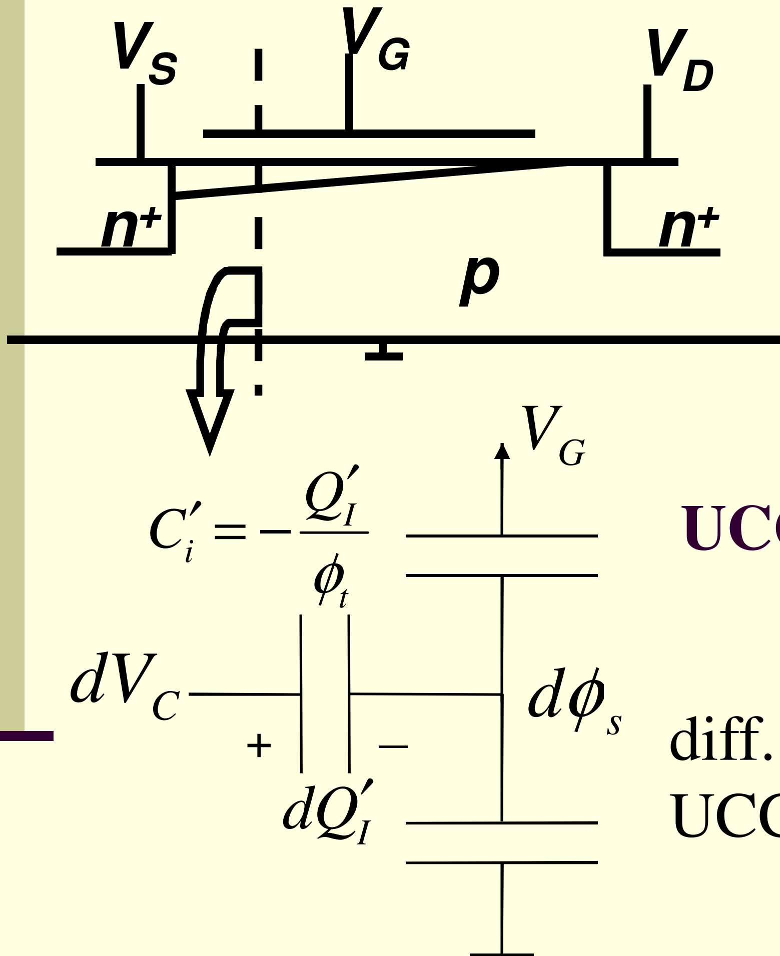
Normalized UCCM $$V_P - V_C = \phi_t (q_I' - 1 + \ln q_I')$$

Inversion charge density



4.10 The four-terminal MOS structure

The drain current -1



The Pao-Sah equation

$$I_D = -\mu_n W \left(-q \int_0^{x_i} n dx \right) \frac{dV_C}{dy} = -\mu_n W Q'_I \frac{dV_C}{dy}$$

$$I_D = -\mu_n \frac{W}{L} \int_{Q'_{IS}}^{Q'_{ID}} Q'_I \frac{dV_C}{dQ'_I} dQ'_I$$

UCCM

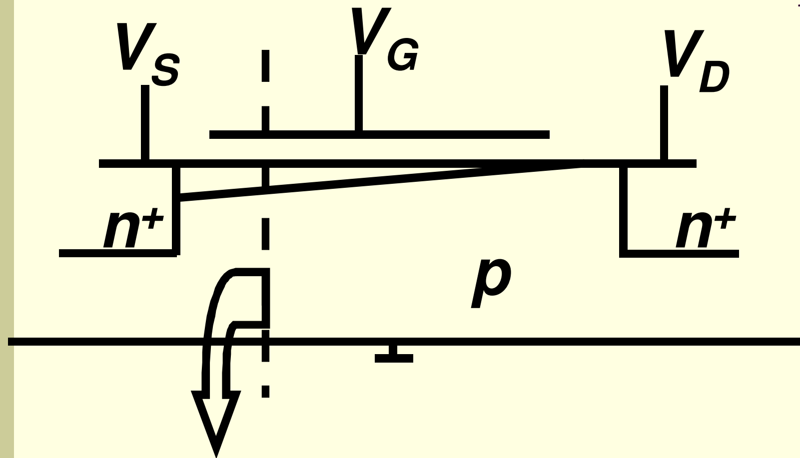
$$\frac{Q'_{IP} - Q'_I}{nC'_{ox}} + \phi_t \ln\left(\frac{Q'_I}{Q'_{IP}} \right) = V_P - V_C$$

diff. UCCM

$$dQ'_I \left(1/nC'_{ox} - \phi_t / Q'_I \right) = dV_C$$

4.10 The four-terminal MOS structure

The drain current -2



The Pao-Sah equation & UCCM

Integrating between source & drain

$$I_D = \frac{\mu_n W}{L}\left[\frac{Q_{IS}'^{\,2} - Q_{ID}'^{\,2}}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right] = \mu_n W\left[\frac{Q_{IS}' + Q_{ID}'}{2} - nC_{ox}'\phi_t\right]\left(\frac{Q_{IS}' - Q_{ID}'}{nC_{ox}' L}\right)$$

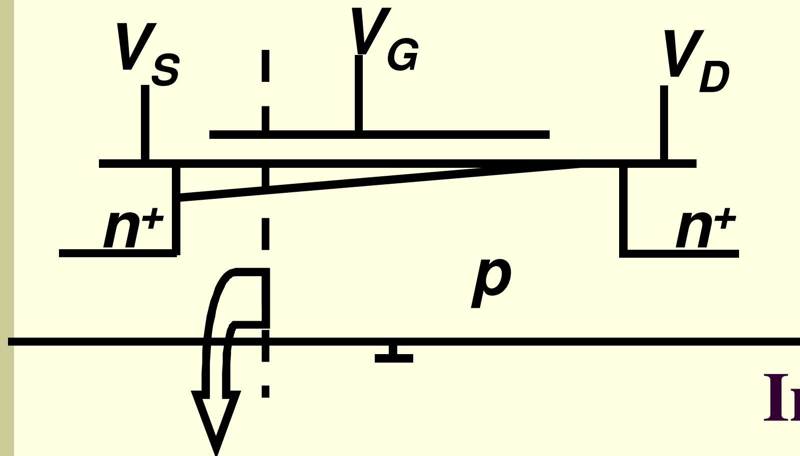
drift + diffusion

average charge

average field

4.10 The four-terminal MOS structure

The drain current -3



The charge-sheet model

drift diffusion

$$I_D = -\mu W Q_I' \frac{d\phi_s}{dy} + \mu W \phi_t \frac{dQ_I'}{dy}$$

$$dQ_I' = nC_{ox}' d\phi_s$$

Integrating between source & drain

$$I_D = \frac{\mu_n W}{L}\left[\frac{{Q_{IS}'}^2 - {Q_{ID}'}^2}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]$$

drift + diffusion

4.10 The four-terminal MOS structure

The drain current - 4

$$I_D = \frac{\mu W}{L}\left[\frac{Q_{IS}'^{\,2} - Q_{ID}'^{\,2}}{2nC_{ox}'} - \phi_t\left(Q_{IS}' - Q_{ID}'\right)\right]$$

Aspect ratio $S = \frac{W}{L}$

Normalization (specific) current $I_S = \mu C_{ox}' n \frac{\phi_t^2}{2} S$

Sheet normalization (specific) current $I_{SH} = \mu C_{ox}' n \frac{\phi_t^2}{2}$

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right] = SI_{SH}\left[i_f - i_r\right]$$

4.11The unified current control model (UICM)

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$V_P - V_{S(D)} = \phi_t\left[q'_{IS(D)} - 1 + \ln q'_{IS(D)}\right]$$

Normalized UCCM

$$q'_{IS(D)} = \frac{Q'_{IS(D)}}{-nC'_{ox}\phi_t}$$

$$i_{f(r)} = {q'_{IS(D)}}^2 + 2q'_{IS(D)} \Rightarrow q'_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1$$

$$i_{f(r)} = \frac{I_{F(R)}}{I_S}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L}$$

$$V_P - V_{S(D)} = \phi_t\left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)\right]$$

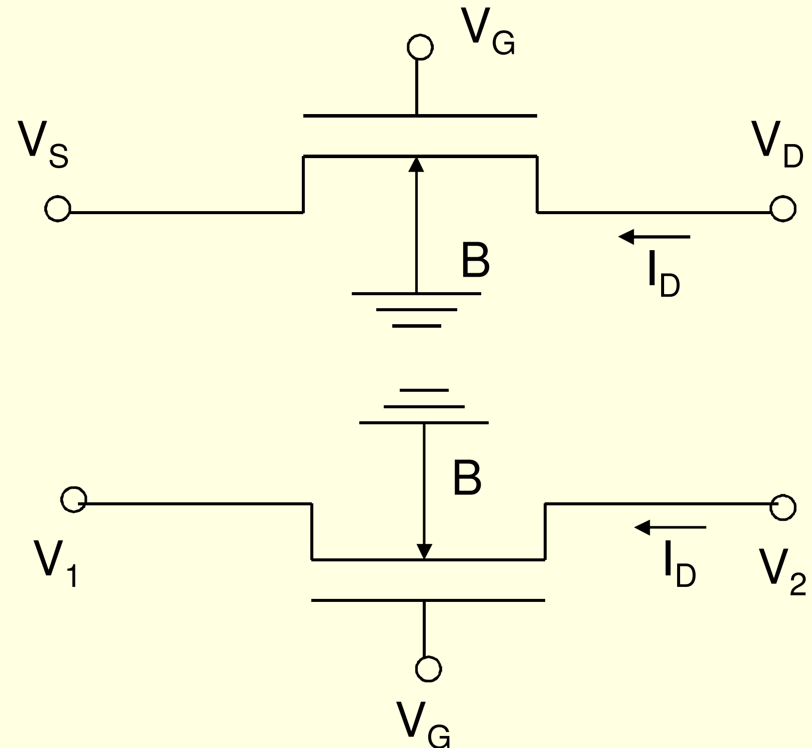
Normalized UICM

Review: The four-terminal MOS structure

1. $I_D = I_D(V_G, V_S, V_D)$

Voltages referenced to local substrate:

$V_G \rightarrow V_{GB} \quad V_S \rightarrow V_{SB} \quad V_D \rightarrow V_{DB}$



2. Symmetry

$$I_D(V_G, V_1, V_2) = -I_D(V_G, V_2, V_1)$$

Review: The four-terminal MOS structure

Normalization

3. For a long-channel MOSFET

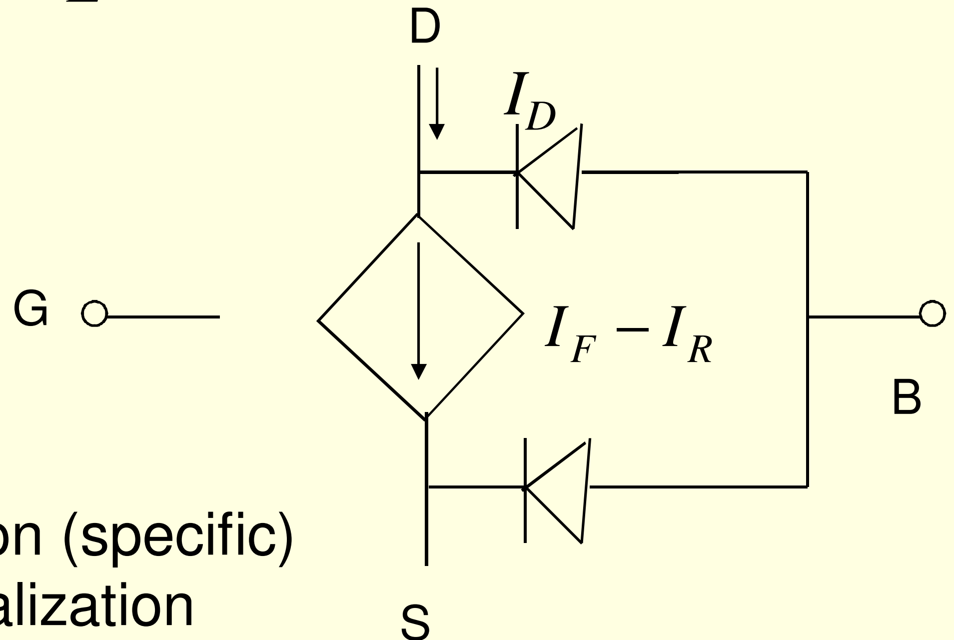
$$I_D = I_F - I_R = I_S\left[i_f - i_r\right] = I_{SH}\frac{W}{L}\left[f\left(V_G, V_S\right) - f\left(V_G, V_D\right)\right]$$

$$I_{F(R)} = I_S\left[q'^{\,2}_{IS(D)} + 2q'_{IS(D)}\right]$$

$$q'_{IS(D)} = Q'_{IS(D)} / \left(-nC'_{ox}\phi_t\right)$$

$$i_{f(r)} = I_{F(R)} / I_S$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SH}\frac{W}{L}$$



I_S and I_{SH} are the normalization (specific) current and the “sheet” normalization current, slightly dependent on bias.

Review: The four-terminal MOS structure

Forward (I_F) and Reverse (I_R) currents

Long-channel MOSFET $I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D)$

(Forward) Saturation

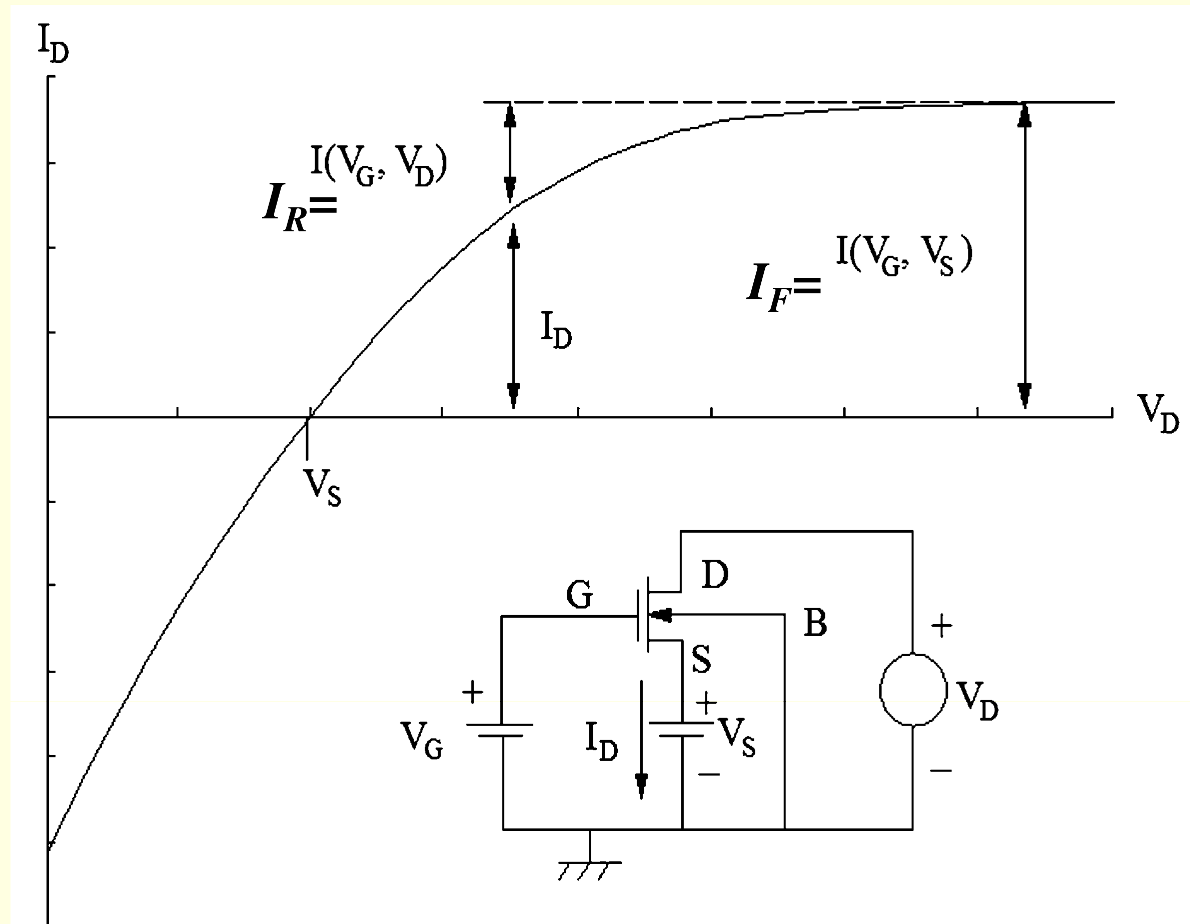
$$I_D = I_F - I_R \cong I_F$$

Triode

$$I_D = I_F - I_R$$

Triode for $V_{DS} \to 0$

$$I_F \cong I_R; \quad I_D = I_F - I_R << I_F$$



Review: The four-terminal MOS structure

Specific current

The specific (normalization) current

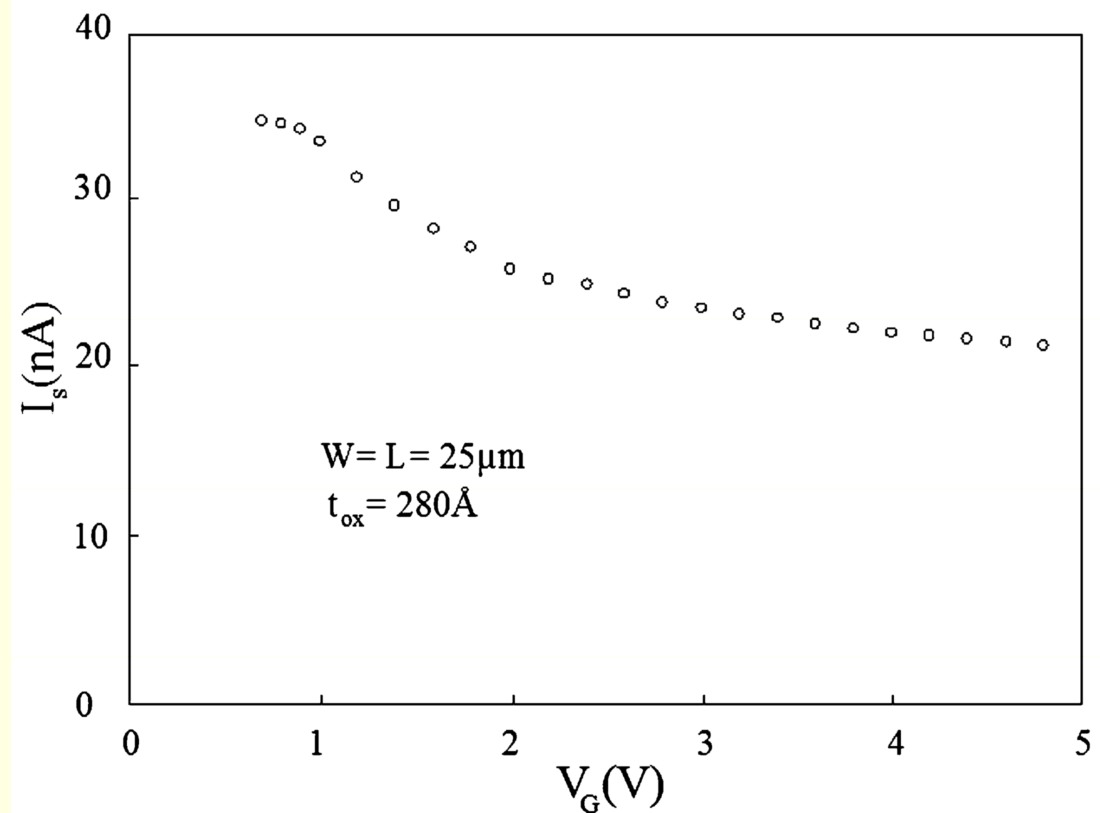
$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L}$$

I_{SH}: design parameter slightly dependent on V_G

$I_{SH} \approx 25$ nA (p-channel)

$I_{SH} \approx 75$ nA (n-channel)

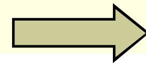
in 0.35 μm CMOS



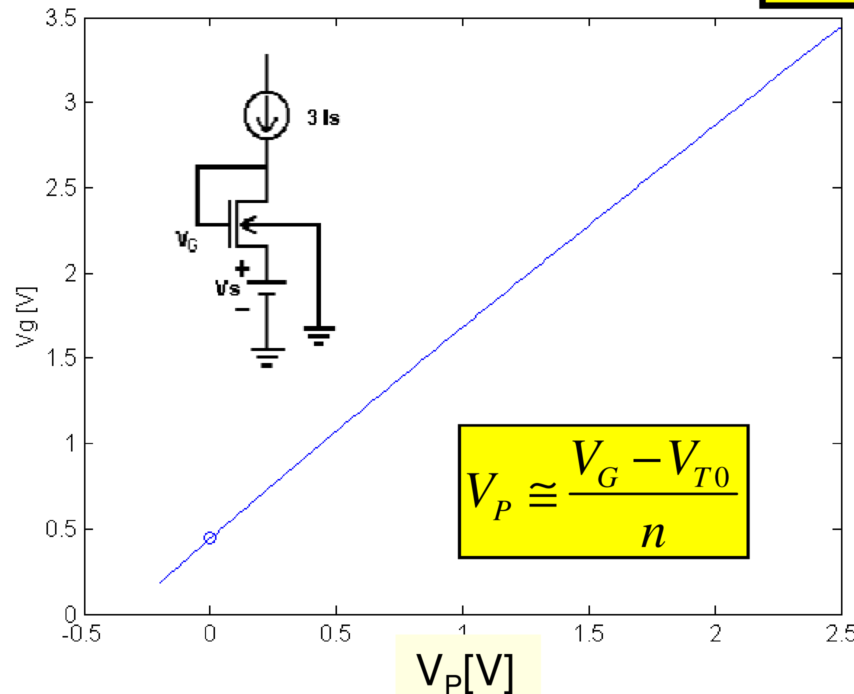
Review: The four-terminal MOS structure

Pinch-off voltage and slope factor

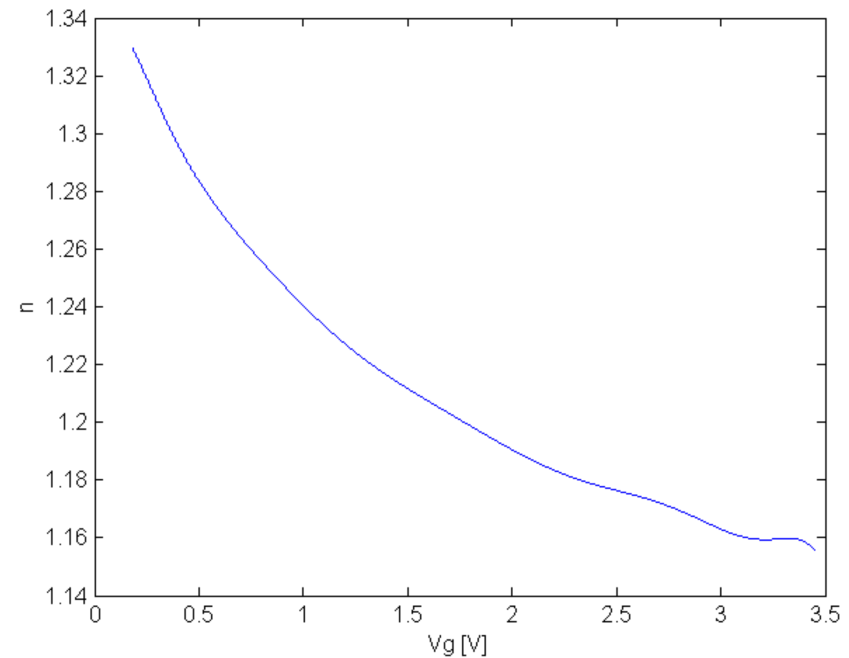
$i_f=3$ at pinch-off



$$V_P - V_S = 0 = \left[\sqrt{1+3} - 2 + \ln\left(\sqrt{1+3} - 1\right)\right]$$



$$V_P \cong \frac{V_G - V_{T0}}{n}$$

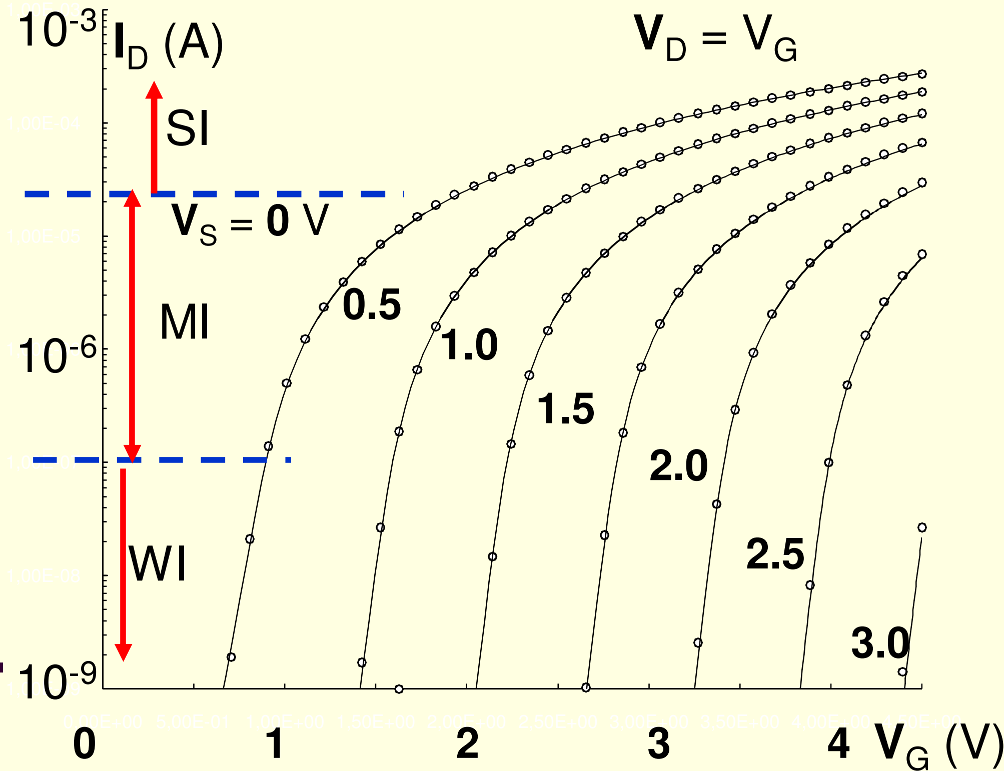


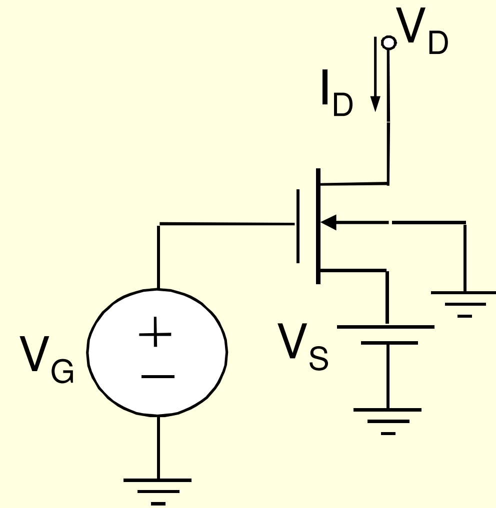
Pinch-off voltage and slope factor as functions of V_G. NMOS transistor W=20 µm, L=2 µm, 0.18 µm CMOS technology.

Experimental results

The I-V Relationship(UICM)

$$V_P - V_S = \phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right]$$





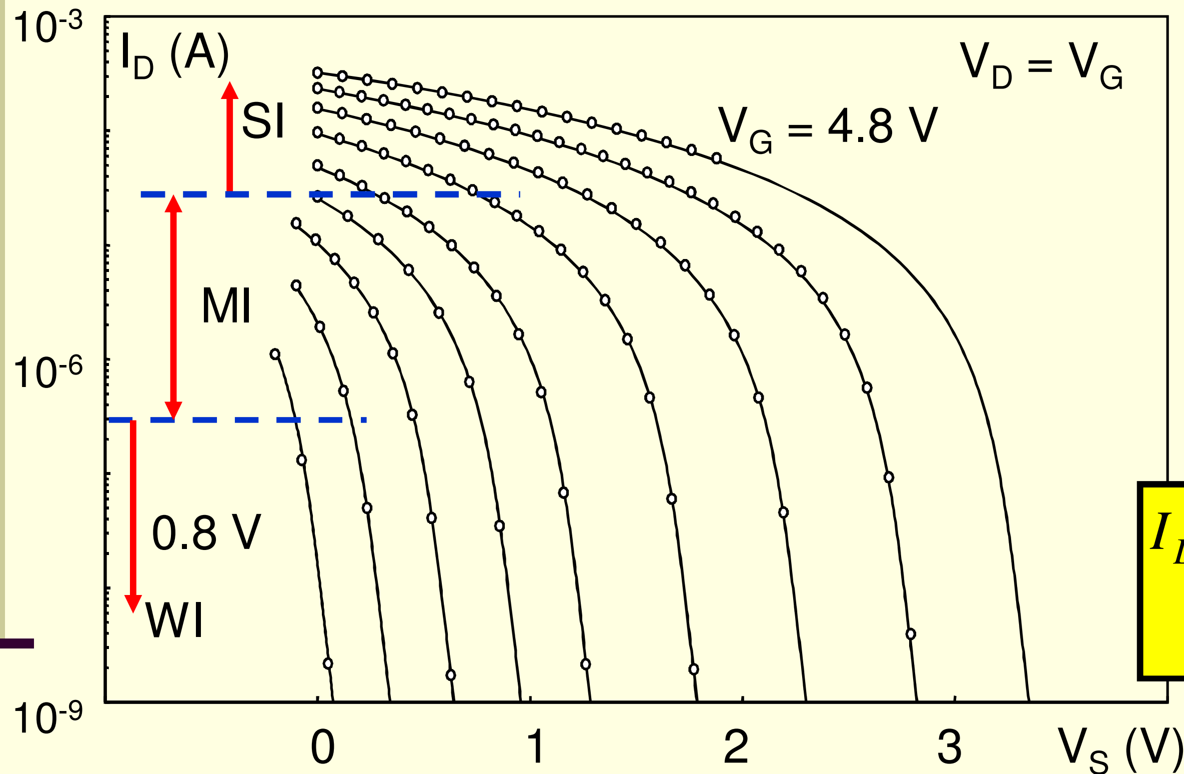
$$I_D = I_F - I_R = I_S\left[i_f - i_r\right] \cong I_S i_f \quad \text{since} \quad i_f >> i_r$$

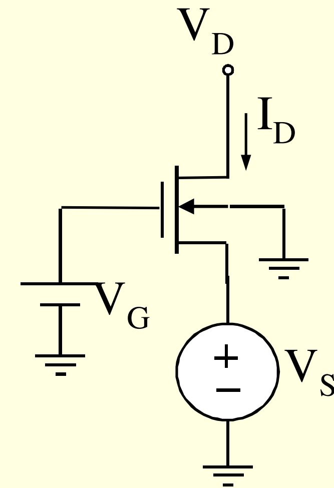
Common-source characteristics

Experimental results

The I-V Relationship (UICM)

$$V_P - V_S = \phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right]$$





$$I_D = I_F - I_R = I_S\left[i_f - i_r\right] \cong I_S i_f \quad \text{since} \quad i_f >> i_r$$

Common-gate characteristics

V_G=0.8, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2, and 4.8 V

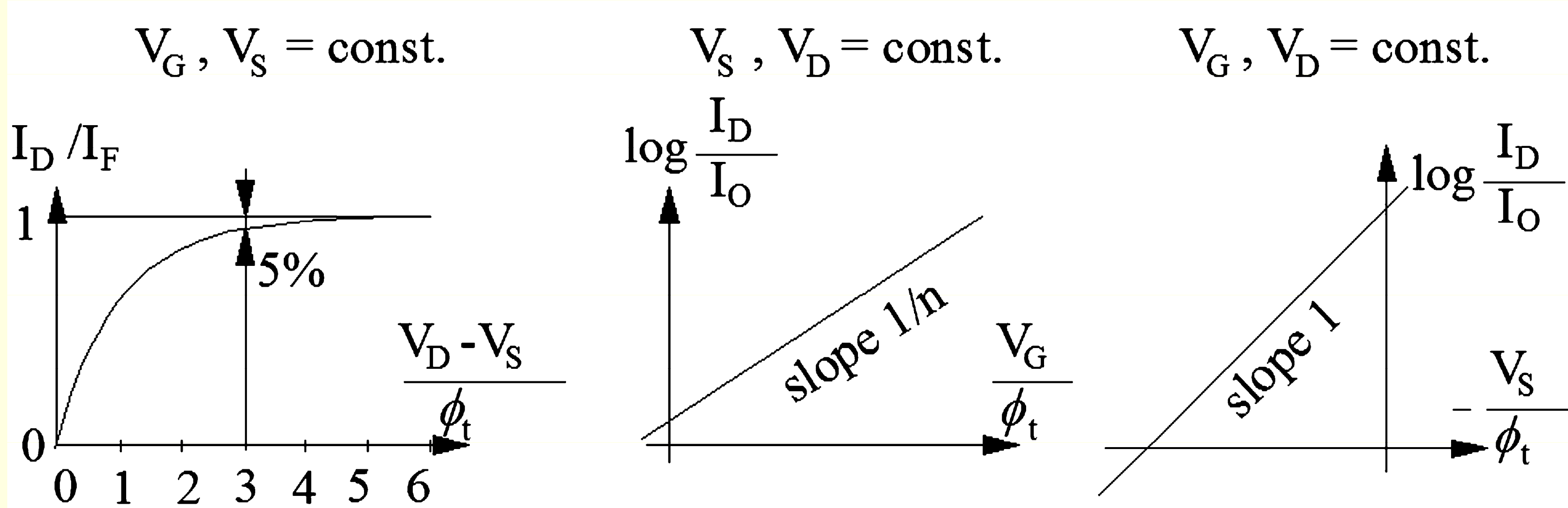
4.12 Weak inversion model

Weak inversion

$i_{f(r)}<1$

$$\frac{V_G - V_{T0}}{n} - V_{S(D)} = \phi_t \left[\underbrace{\sqrt{1+i_{f(r)}} - 2}_{-1} + \ln\left(\underbrace{\sqrt{1+i_{f(r)}} - 1}_{i_{f(r)}/2} \right) \right]$$

$$I_D = I_0 e^{\left(\frac{V_G - V_{T0}}{n} - V_S\right)/\phi_t} \left[1 - e^{-V_{DS}/\phi_t}\right] \qquad I_0 = \mu_n \frac{W}{L} n C'_{ox} \phi_t^2 e^1 = 2 I_S e^1$$

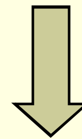


4.13 Strong inversion model - 1

$$\frac{V_G - V_{T0}}{n} - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \right]$$

Strong inversion
$i_{f(r)} >> 1$

$$\frac{V_G - V_{T0}}{n} - V_{S(D)} \cong \phi_t \sqrt{i_{f(r)}} = \phi_t \sqrt{I_{F(R)} / I_S}$$

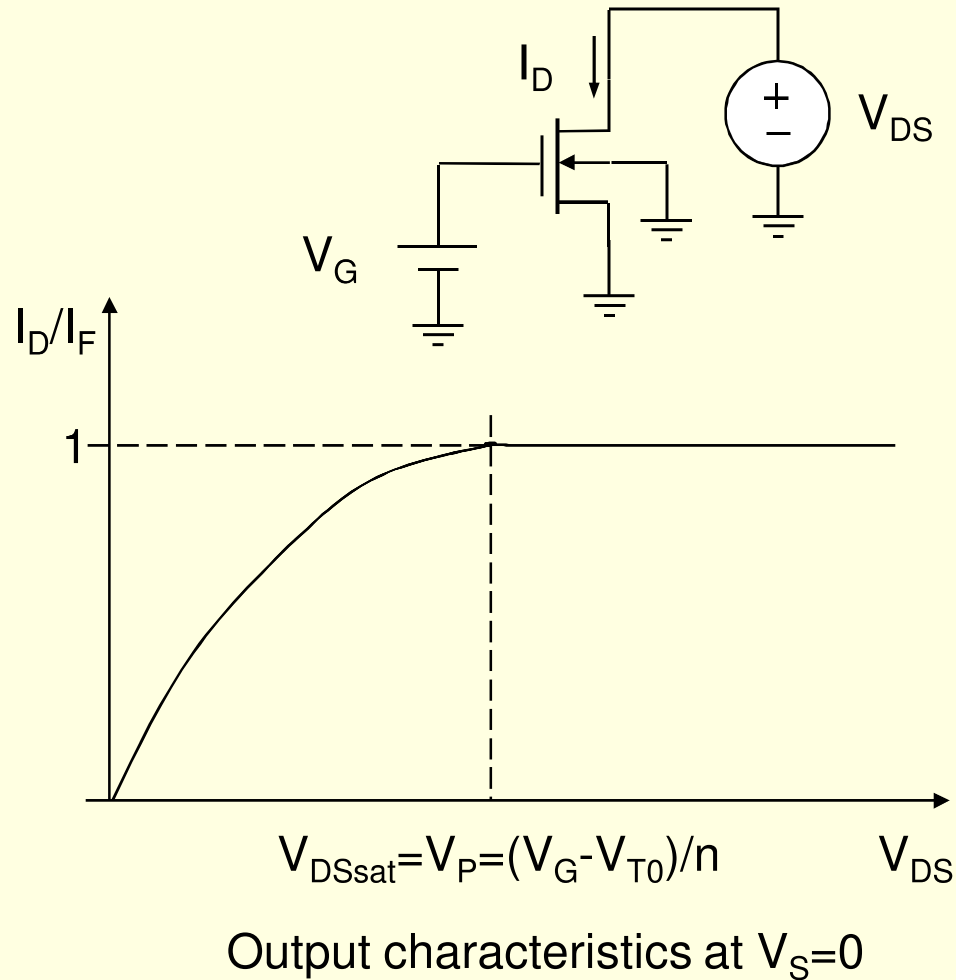


$$I_D = I_F - I_R \cong \mu_n C'_{ox} \frac{W}{2nL} \left[\left(V_G - V_{T0} - nV_S\right)^2 - \left(V_G - V_{T0} - nV_D\right)^2 \right]$$

Moderate inversion
$1 < i_{f(r)} < 100$

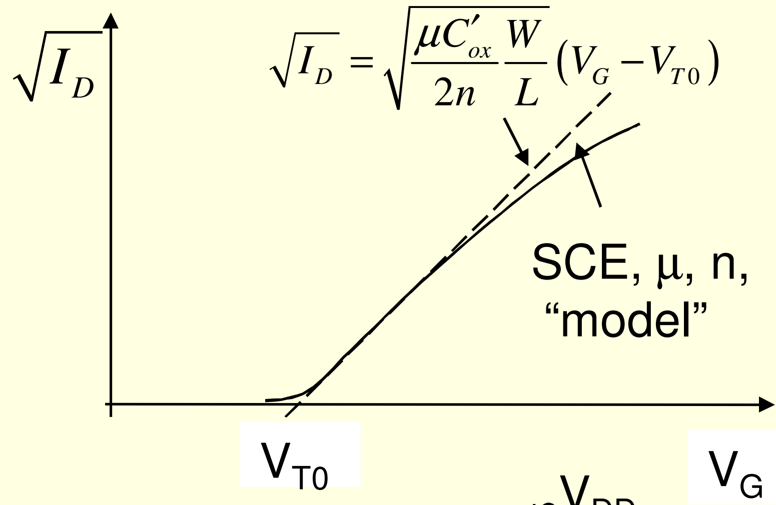
Both sqrt(.) and ln(.) terms are important

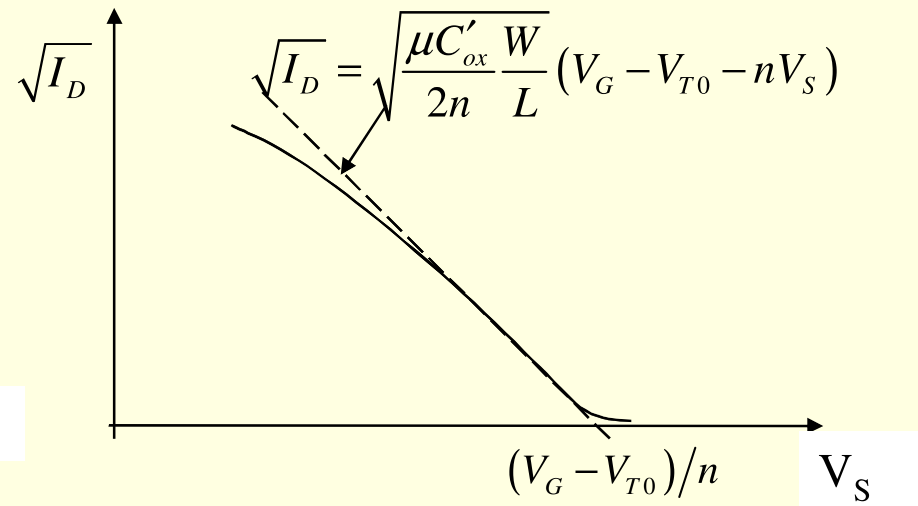
4.13 Strong inversion model - 2

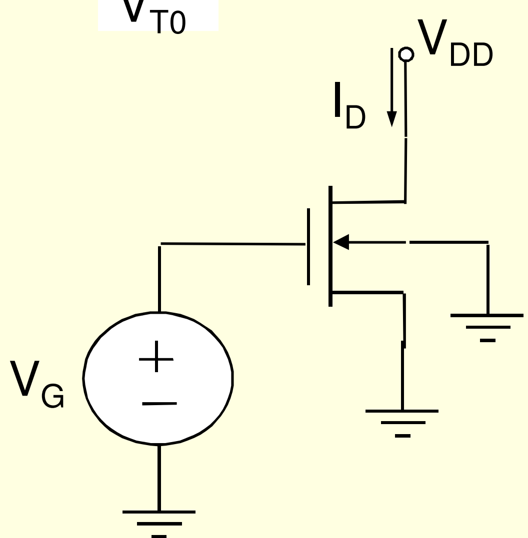


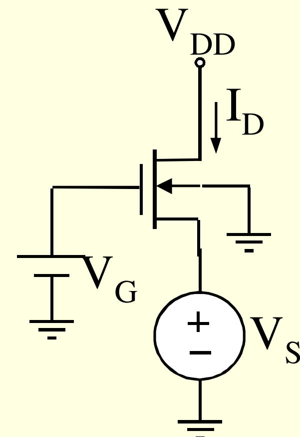
Output characteristics at $V_S=0$

4.13 Strong inversion model - 3



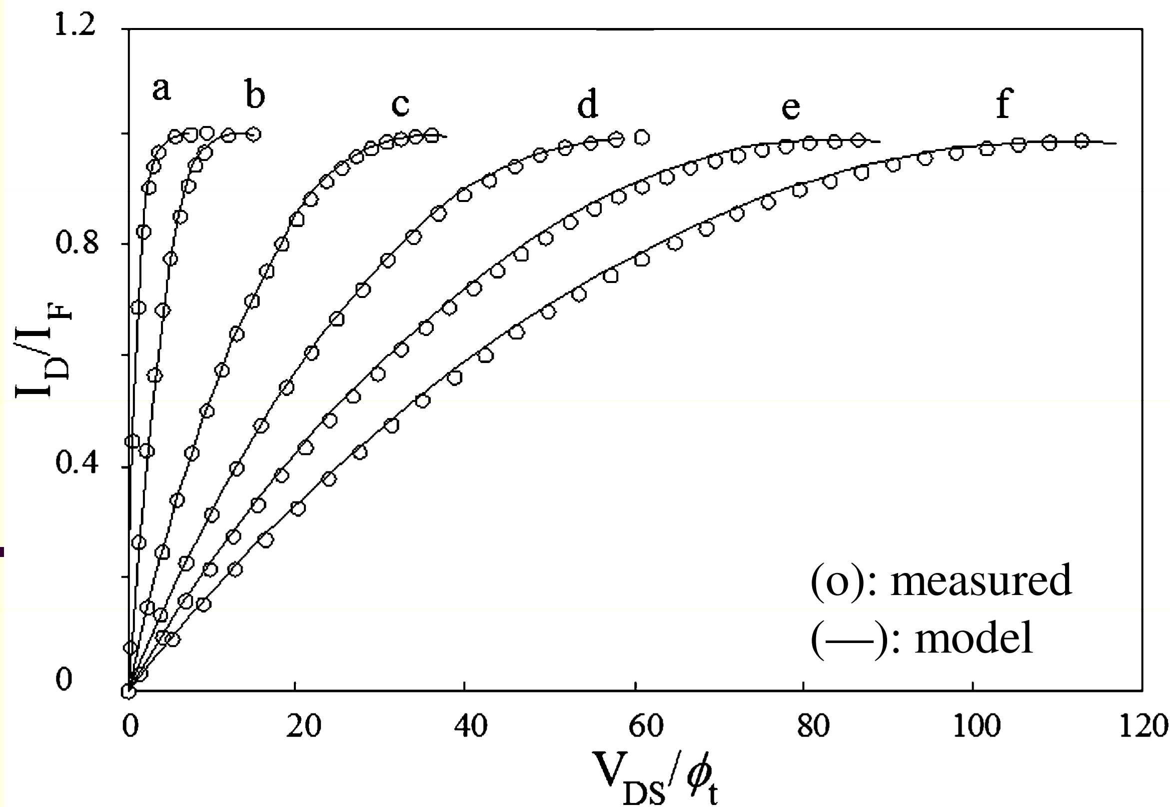






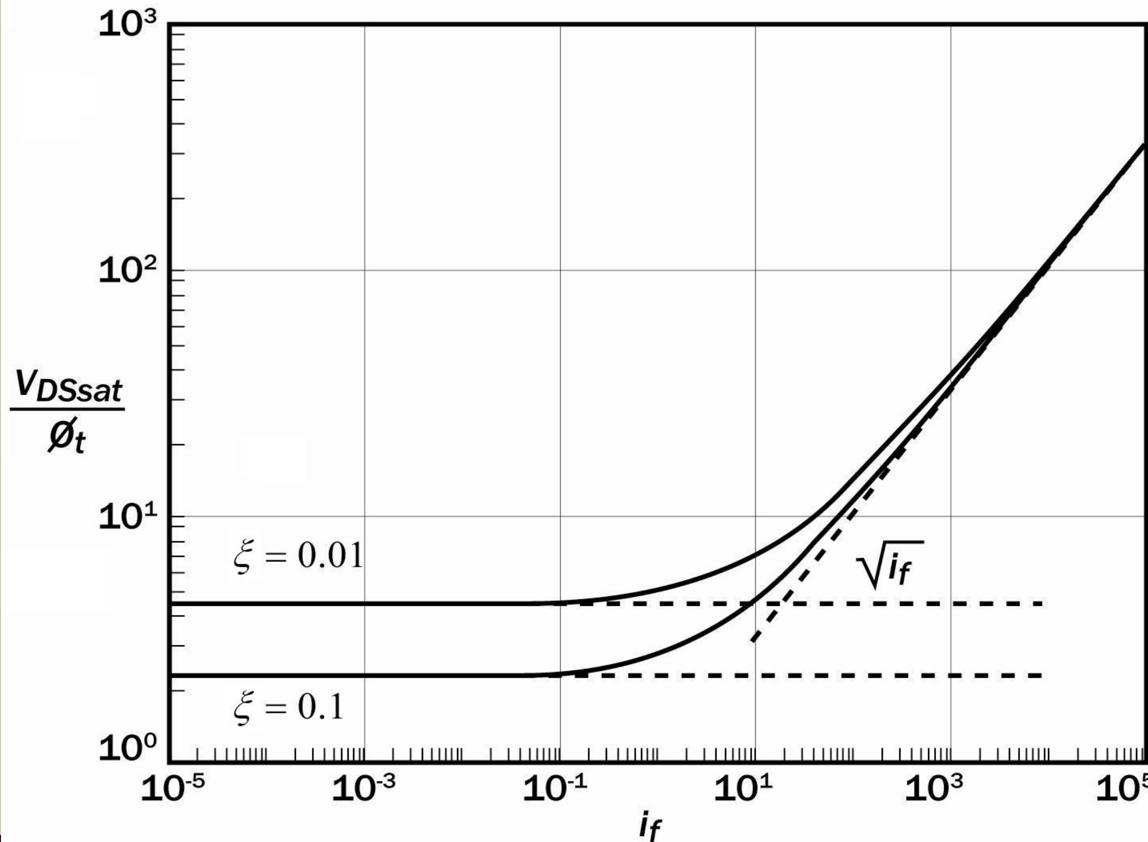
4.14 Universal output characteristics

$$\frac{V_{DS}}{\phi_t} = q'_{IS} - q'_{ID} + \ln\left(\frac{q'_{IS}}{q'_{ID}}\right) = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)$$



(a) i_f= 4.5x 10^{-2} (V_G=0.7 V).
(b) i_f= 65(V_G= 1.2 V).
(c) i_f= 9.5x10^2 (V_G= 2.0 V).
(d) i_f= 3.1x 10^3 (V_G= 2.8 V).
(e) i_f= 6.8x 10^3 (V_G= 3.6 V).
(f) i_f= 1.2x 10^4 (V_G= 4.4 V).

4.15 Saturation voltage



Saturation voltage versus inversion level

Saturation voltage (V_{DSsat}): V_{DS} at which the ratio

$$q'_{ID}/q'_{IS} = \xi$$

$$V_{DSsat} \cong \phi_t \left[\sqrt{1+i_f} + 3 \right]$$

$$V_{DSsat} = \phi_t \left[\ln\left(\frac{1}{\xi}\right) + (1-\xi)\left(\sqrt{1+i_f} - 1\right) \right]$$

$(1-\xi)$ **is the saturation level**

4.16 Transconductances - 1

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B$$

$$g_{mg} = \frac{\partial I_D}{\partial V_G}, g_{ms} = -\frac{\partial I_D}{\partial V_S}, g_{md} = \frac{\partial I_D}{\partial V_D}, g_{mb} = \frac{\partial I_D}{\partial V_B}$$

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0$$

Calculation of g_{ms}

$$I_D = I_F - I_R = I_S\left[i_f - i_r\right]$$

$$g_{ms} = -\frac{\partial\left(I_F - I_R\right)}{\partial V_S} = -\frac{\partial I_F}{\partial V_S} = -I_S\frac{di_f}{dV_S}$$

$$g_{ms} = -\mu\frac{W}{L}Q'_{IS} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f} - 1\right)$$

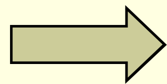
4.16 Transconductances - 2

$$g_{md} = -\mu \frac{W}{L} Q'_{ID} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_r} - 1\right)$$

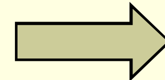
Only in triode region

$$g_{mg} = I_S \frac{\partial (i_f - i_r)}{\partial V_G}$$

UCCM



$$\begin{cases} \dfrac{\partial i_f}{\partial V_G} = -\dfrac{\partial i_f}{n \partial V_S} \\[2ex] \dfrac{\partial i_r}{\partial V_G} = -\dfrac{\partial i_r}{n \partial V_D} \end{cases}$$



$$g_{mg} = \frac{g_{ms} - g_{md}}{n}$$

$$g_{mg} = \frac{g_{ms}}{n} \longrightarrow \text{in saturation}$$

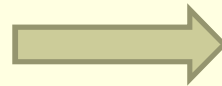
4.16 Transconductances - 3

$$g_{md} = -\mu \frac{W}{L} Q'_{ID}$$

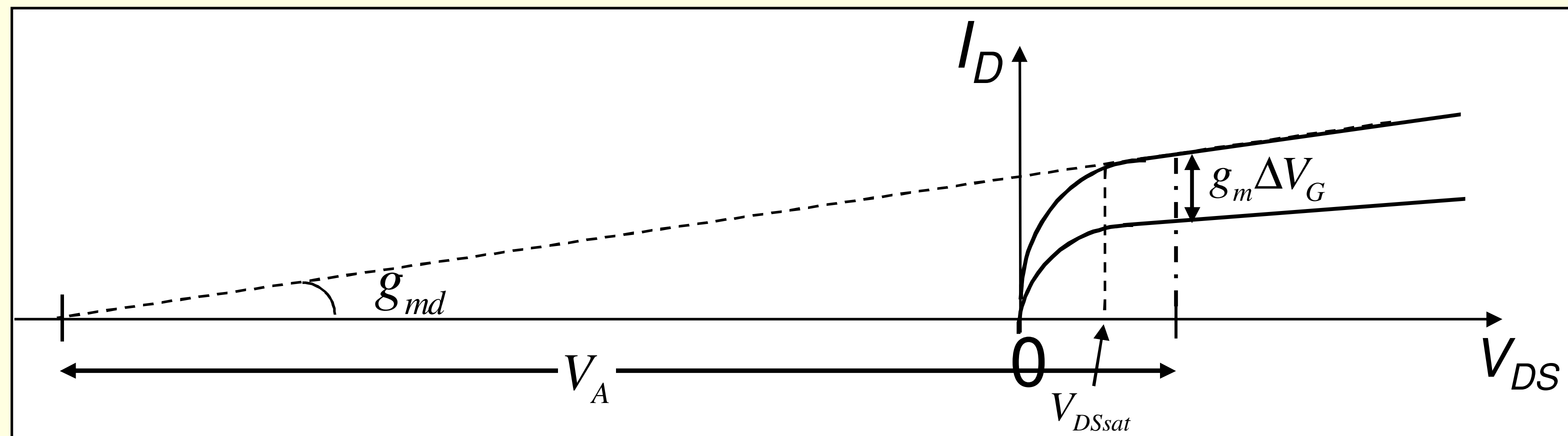
Only in triode region

In saturation, g_{md} is determined by short-channel effects

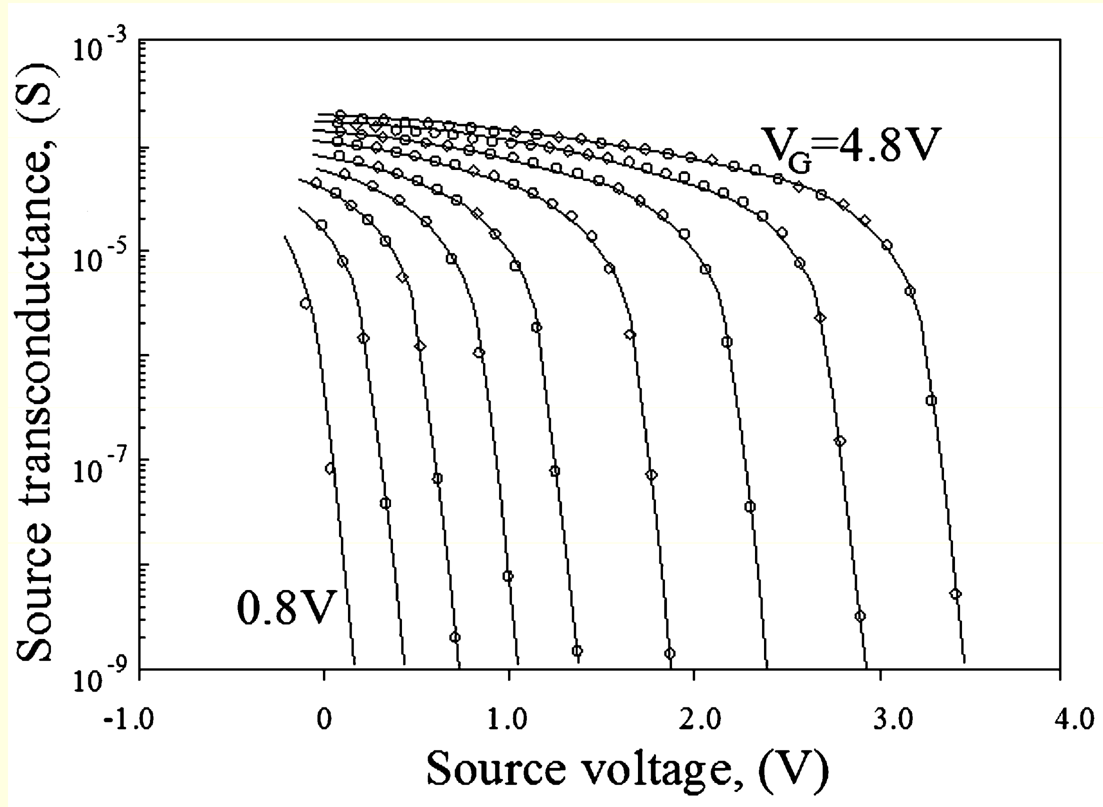
$$g_{md}(g_{ds}) \cong \frac{I_D}{V_A}; \quad V_A \cong V_E L$$

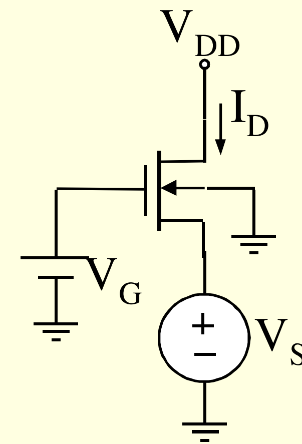


Saturation



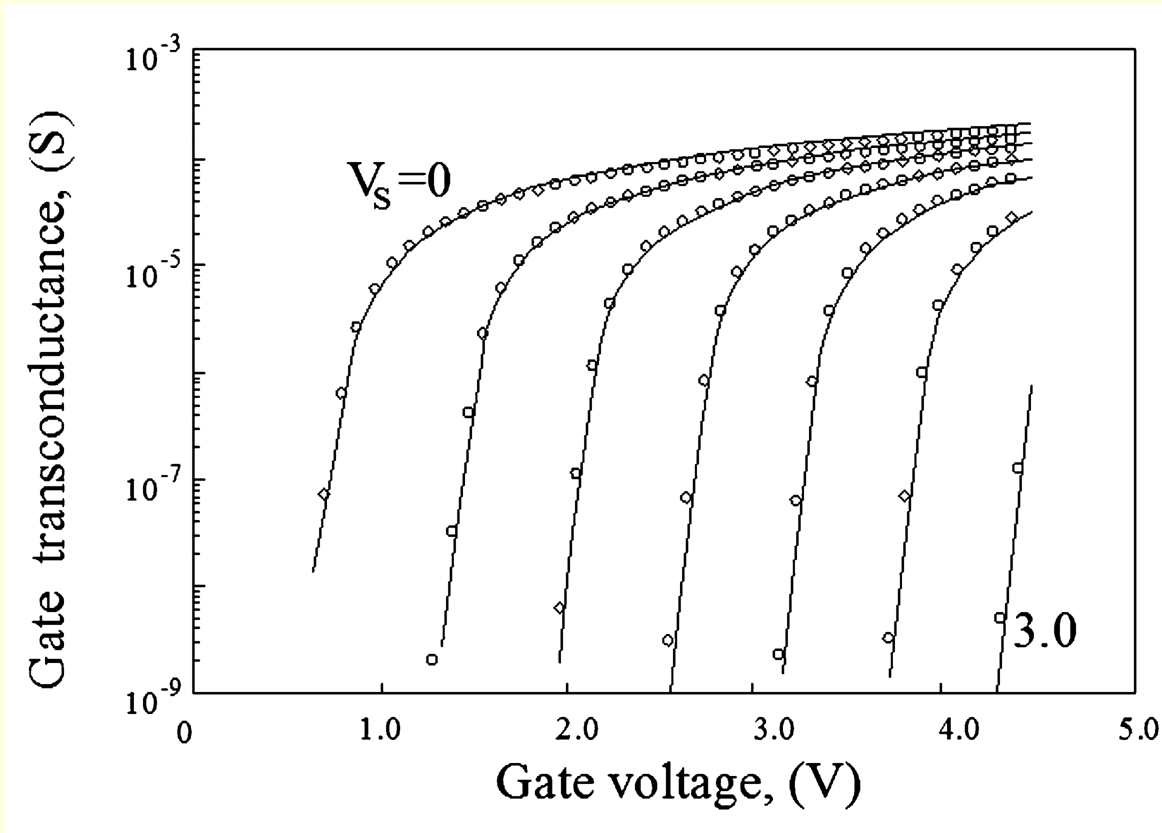
4.16 Transconductances - 4

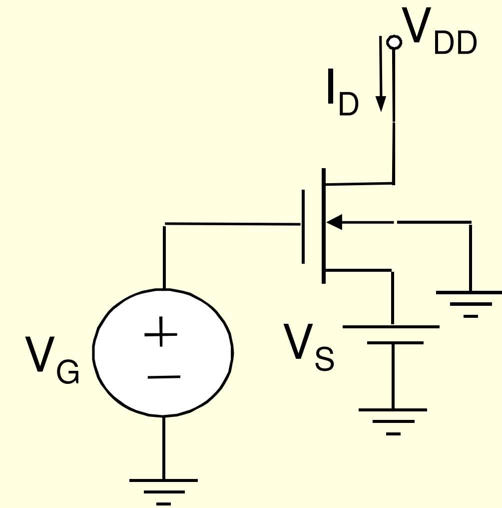




Source transconductance V_G= 0.8, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2, and 4.8 V (W=L=25 μm, tox=280 Å)

4.16 Transconductances - 5





Gate transconductance V_S= 0, 0.5, 1.0,1.5, 2.0, 2.5, and 3.0 V
W=L=25 µm, tox=280 Å

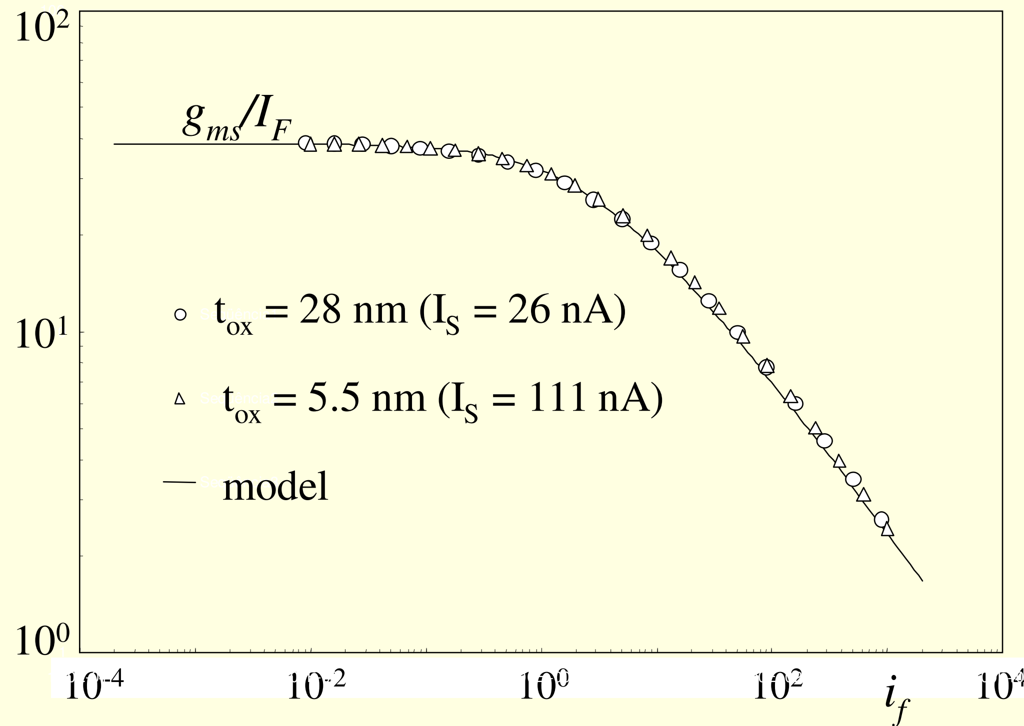
4.17 The transconductance-to-current ratio - 1

Transconductance -to-current ratio

$$\frac{g_{ms(d)}\phi_t}{I_{F(R)}} = \frac{2}{\sqrt{1+i_{f(r)}}+1}$$

$\cong 1 \longrightarrow$ WI ($i_f<1$)

$\cong \frac{2}{\sqrt{i_{f(r)}}} \longrightarrow$ SI ($i_f>>1$)



W=25 μm

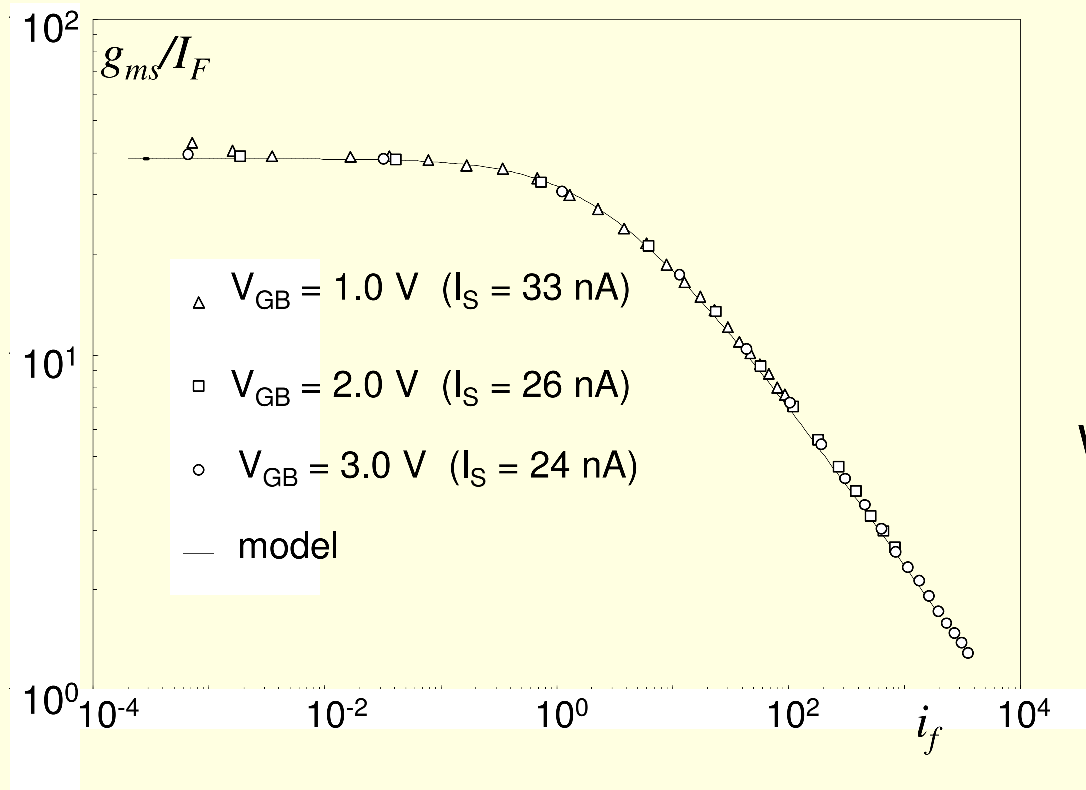
L=25 μm, t_{ox}= 280 Å

L=20 μm, t_{ox}= 55 Å

4.17 The transconductance-to-current ratio - 2

Transconductance -to-current ratio

$$\frac{g_{ms(d)}\phi_t}{I_{F(R)}} = \frac{2}{\sqrt{1+i_{f(r)}}+1} \quad \begin{cases} \cong 1 \longrightarrow \text{WI } (i_f<1) \\ \cong \dfrac{2}{\sqrt{i_{f(r)}}} \longrightarrow \text{SI } (i_f>>1) \end{cases}$$



W=L=25 µm, t_{ox}= 280 Å

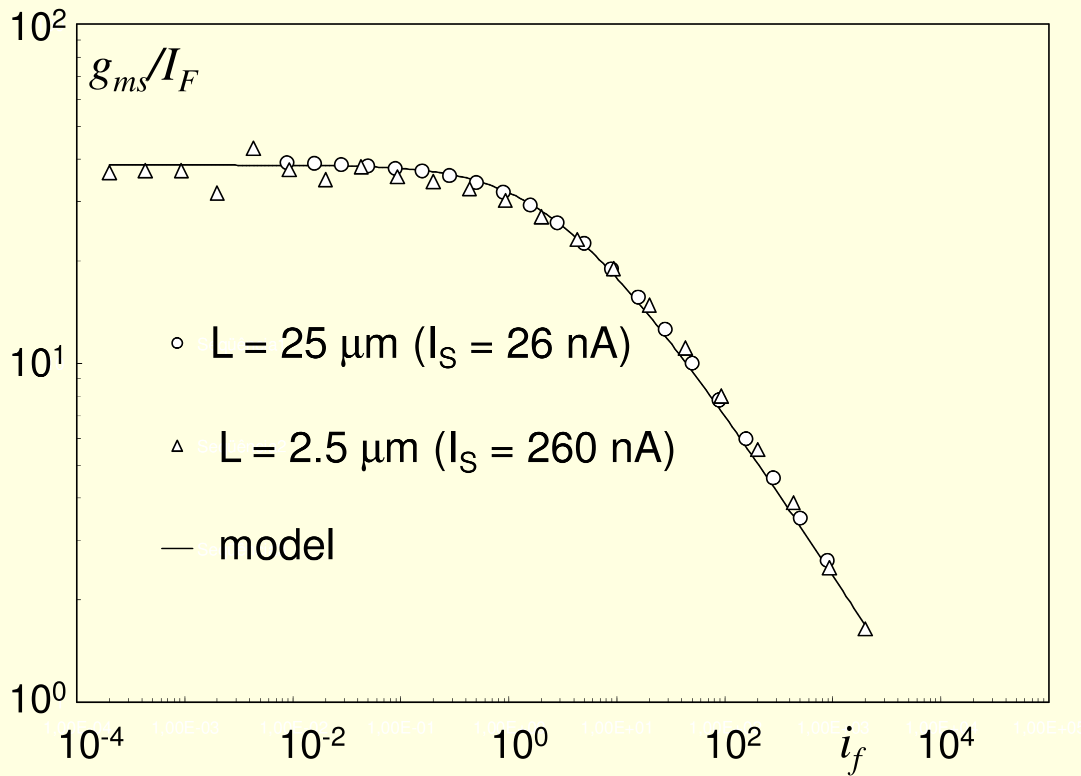
4.17 The transconductance-to-current ratio - 3

Transconductance -to-current ratio

$$\frac{g_{ms(d)}\phi_t}{I_{F(R)}} = \frac{2}{\sqrt{1+i_{f(r)}}+1}$$

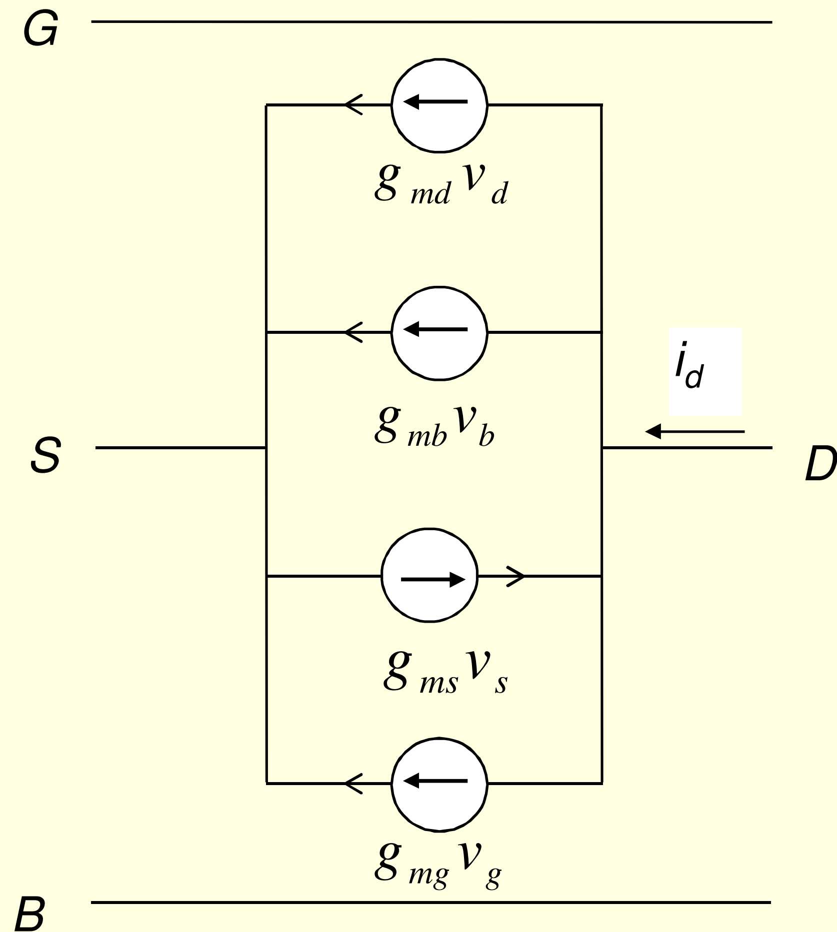
$\cong 1 \longrightarrow$ WI ($i_f < 1$)

$\cong \frac{2}{\sqrt{i_{f(r)}}} \longrightarrow$ SI ($i_f >> 1$)

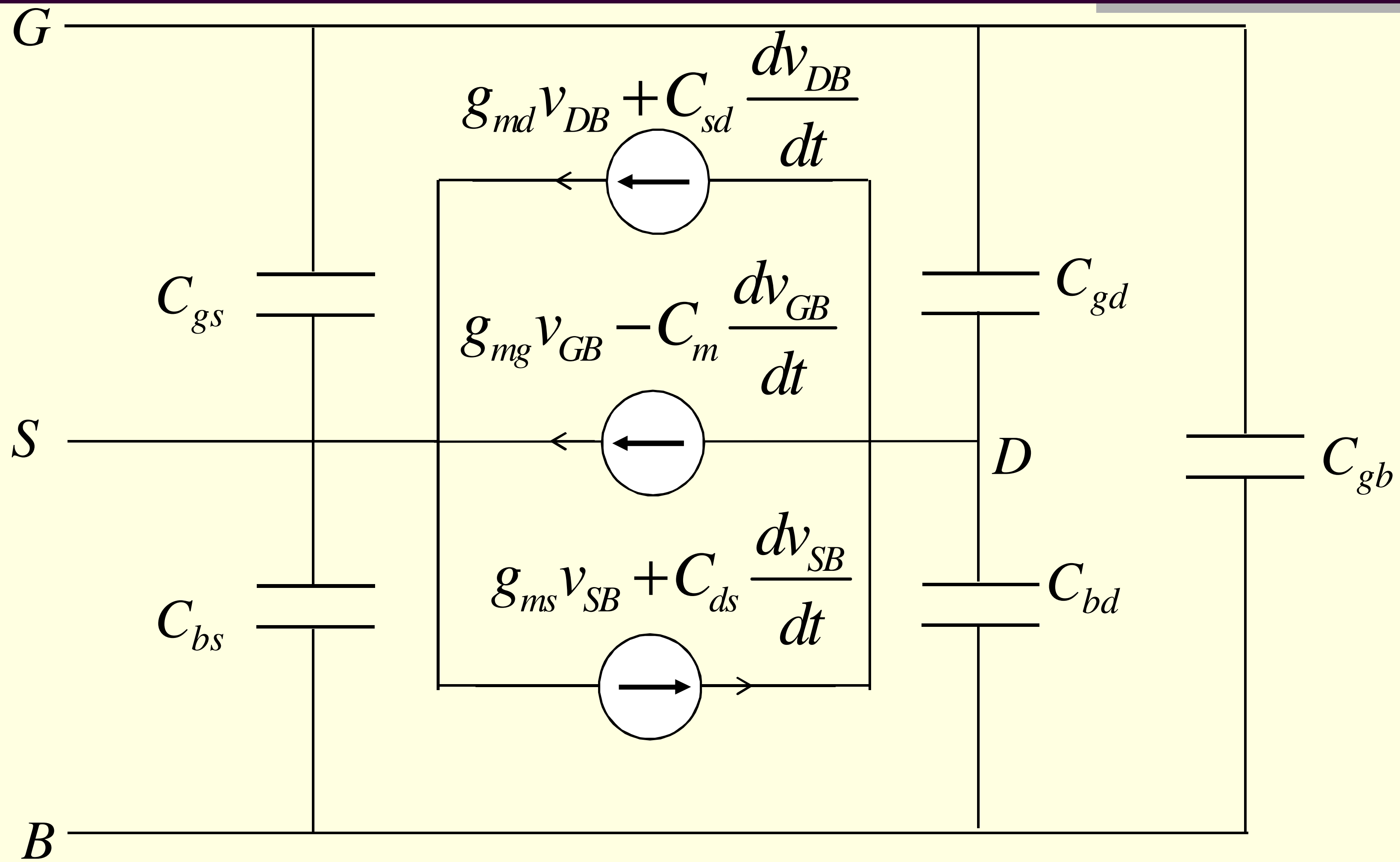


W=25 µm, t_{ox}= 280 Å

4.18 The low-frequency small-signal model

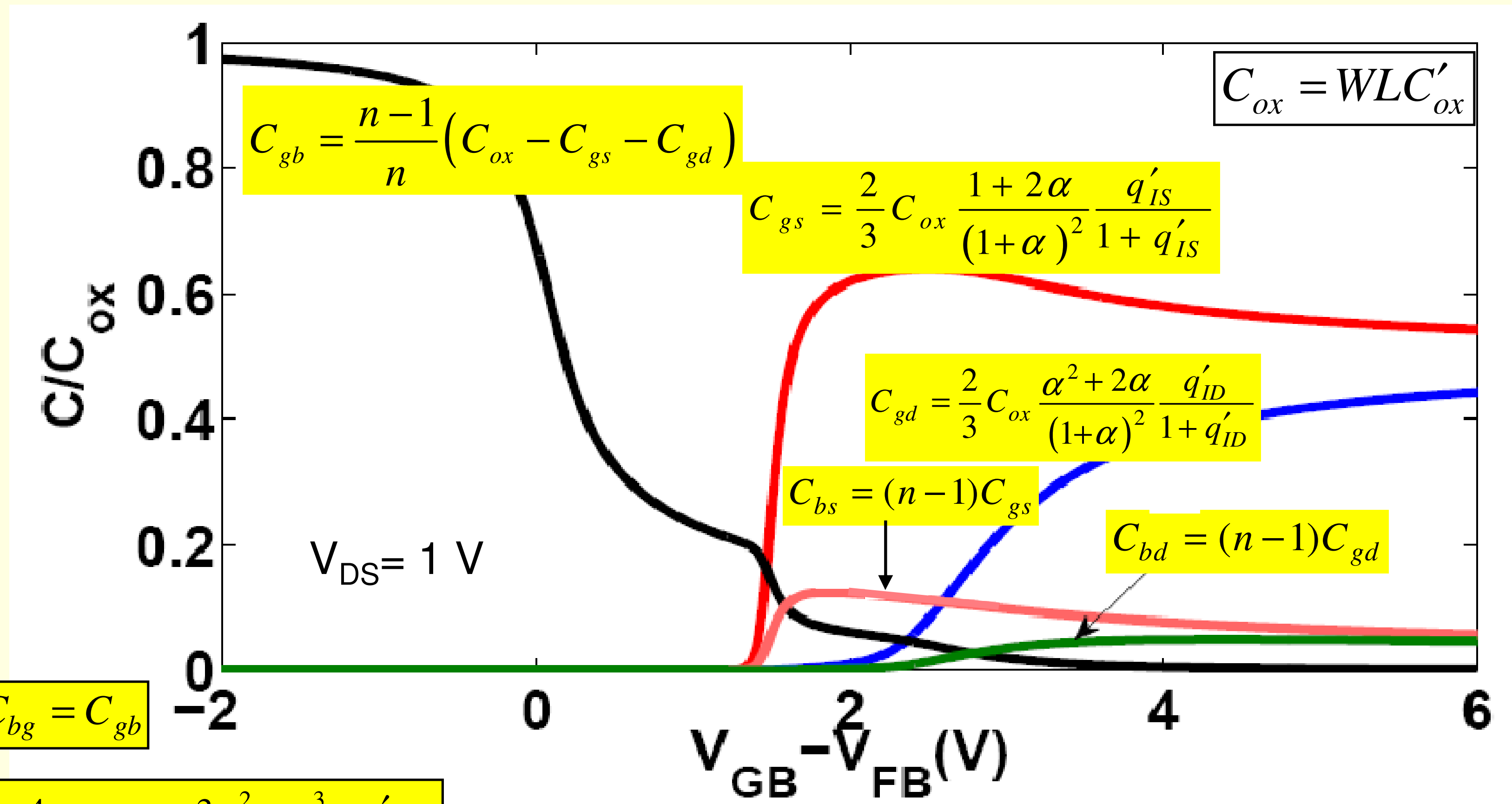


4.18 Small-signal MOSFET model



$$C_{dg} - C_{gd} = C_m = (C_{sd} - C_{ds})/n$$

4.18 Intrinsic capacitances



$$C_{bg} = C_{gb}$$

$$C_{sd} = -\frac{4}{15} n C_{ox} \frac{\alpha + 3\alpha^2 + \alpha^3}{(1+\alpha)^3} \frac{q'_{ID}}{1+q'_{ID}}$$

$$C_{ds} = -\frac{4}{15} n C_{ox} \frac{1 + 3\alpha + \alpha^2}{(1+\alpha)^3} \frac{q'_{IS}}{1+q'_{IS}}$$

$$C_{dg} - C_{gd} = C_m = (C_{sd} - C_{ds}) / n$$

$$\alpha = \frac{1+q'_{ID}}{1+q'_{IS}}$$

⟹ Channel linearity factor

4.19 Noise & Mismatch

- Predicting accuracy (mismatch & noise) is fundamental in analog and digital IC design
- Besides DC and AC models, system designers need information on accuracy $\Rightarrow$ proper matching and noise models are required.
- Simple one-equation models provide a useful tool for hand design also, rather than being restricted to computer simulation.

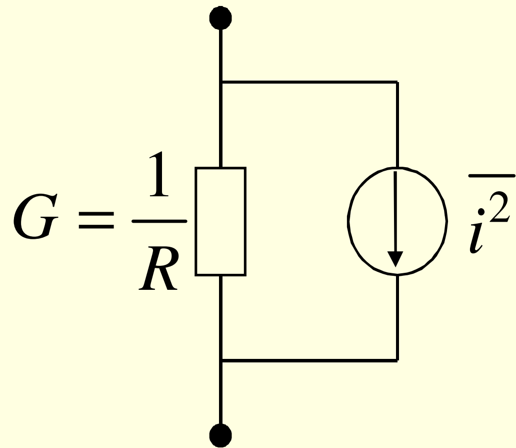
4.19 Noise & Mismatch

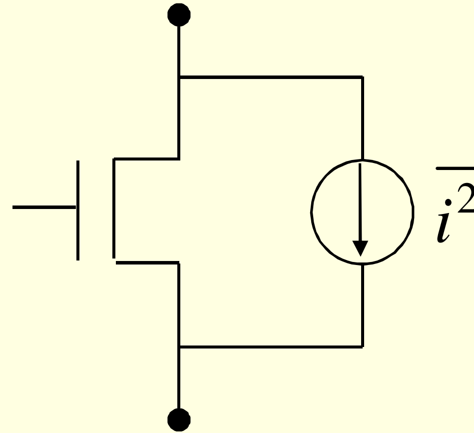
- The spontaneous fluctuations over time of the current and voltage inside a device, which are basically related to the discrete nature of electrical charge, are called electrical noise.
- Time-independent variations between identically designed devices in an integrated circuit due to the spatial fluctuations in the technological parameters and geometries are called mismatch.
- Mismatch (spatial fluctuation) and noise (temporal fluctuation) are similar phenomena, both being dependent on the process, device dimensions, and bias.

4.19 Noise

- **NOISE means spontaneous fluctuations in charge, current or voltage generated in a component.**
- **NOISE is related to the discrete nature of carriers.**
- **Fundamental physical concepts behind noise are simple BUT expressions to compute noise are often obscure.**
- **NOISE sets lower limits to the strength of signals that can be processed.**
- **The understanding of noise is a key factor in low-power/low-voltage designs.**

4.19 Thermal noise of resistor/MOSFET





$$\frac{\overline{i^2}}{\Delta f} = 4kTG$$

$$\frac{\overline{i^2}}{\Delta f} = 4\gamma kTg_{ms}$$

Bias-dependent factor ≈1

4.19 Flicker noise (1/*f*)

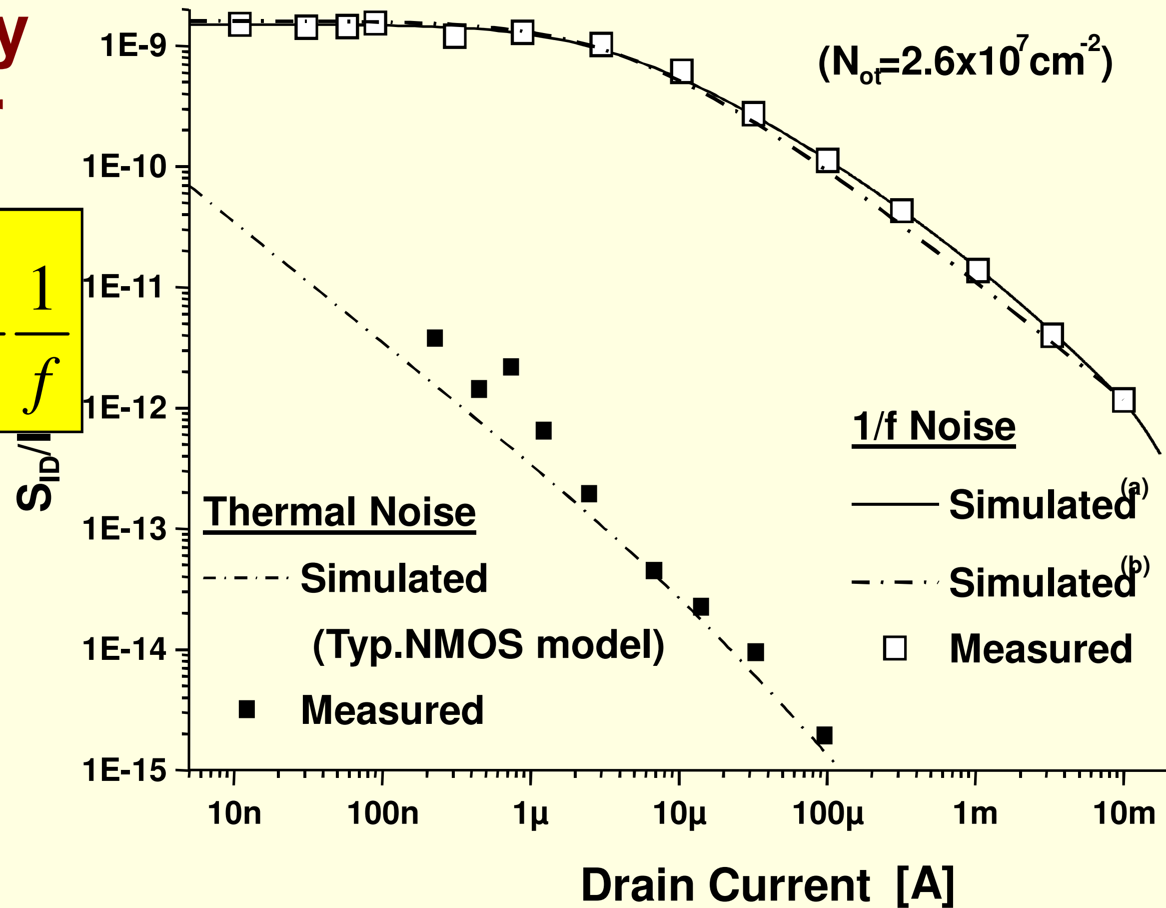
- **Power spectral density (PSD):** $S(f) = K / f^{\beta} \qquad \beta \cong 1$
- **Mainly generated by fluctuations in number of carriers and mobility due to random trapping-detrapping of carriers near the surface of the semiconductor.**
- **Exact mechanism and statistics of resulting noise current, and correlation with technological parameters are not yet clear.**

4.19 Flicker noise

Technology parameter

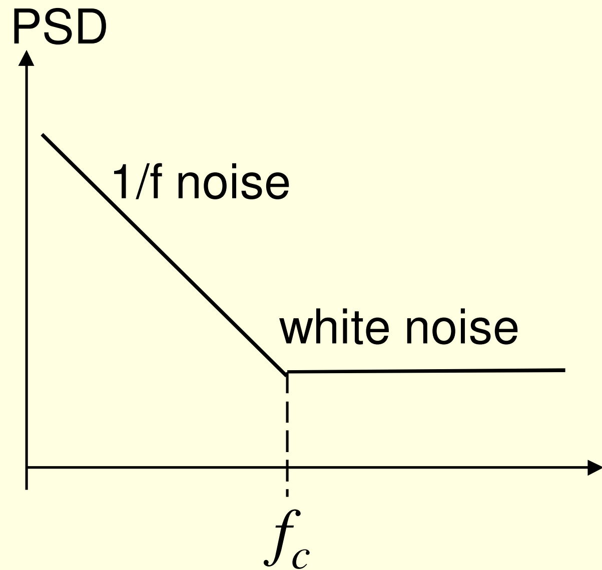
$$\frac{\overline{i^2_{ch(\text{flicker})}}}{\Delta f} \cong \frac{K_F g_m^2}{WLC'_{ox}} \frac{1}{f}$$

Gate area



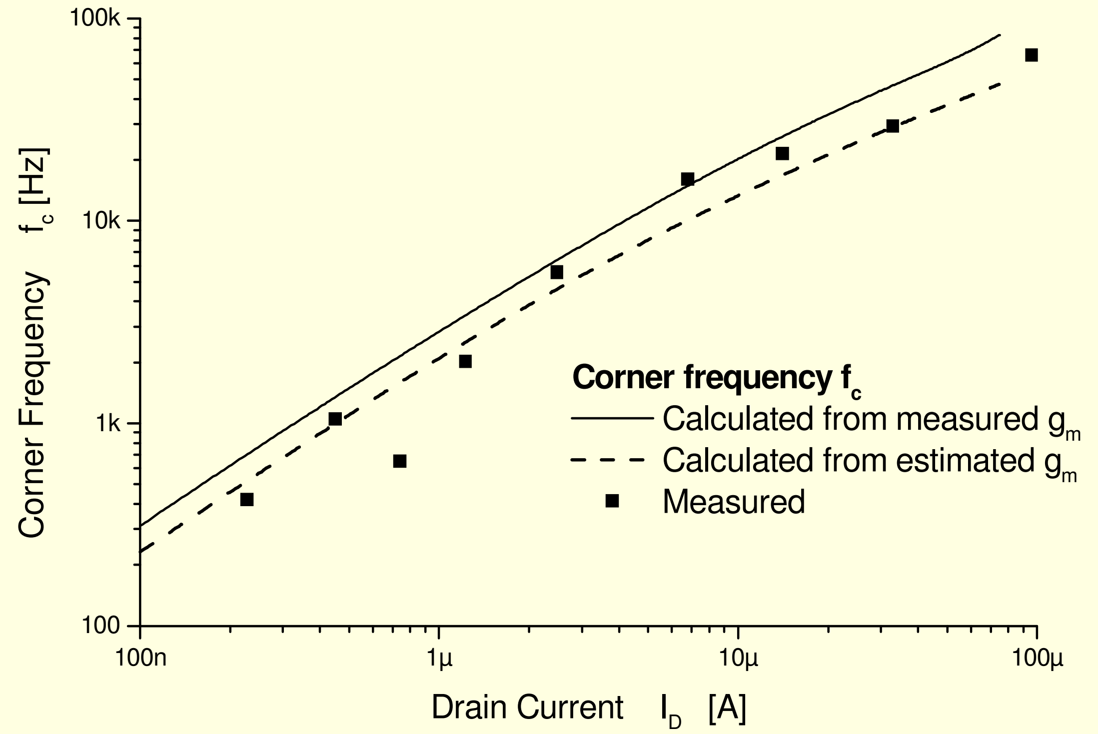
Normalized flicker and thermal PSD at f=1Hz for saturated NMOS-T (W/L=200/5)

4.19 Corner frequency



$$f_c \cong \frac{\pi}{2}\frac{K_F}{nq\phi_t} f_T$$

f_T: MOSFET transition frequency

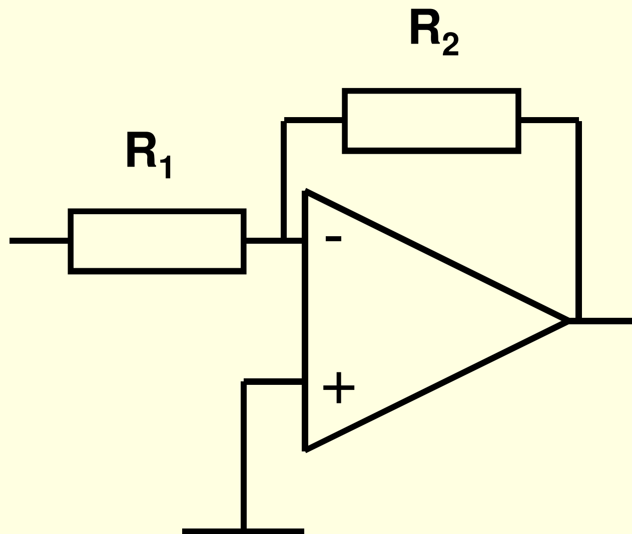


$$f_c \cong \frac{f_T}{2000}$$ → **0.35 um CMOS technology**

4.20 Mismatch

- Mismatch: differences between identically designed devices.
- Performance of many analog and also digital circuits is based on how closely matched components are.
- Consequences of mismatch: offset voltage, current mirror error, variable gate delay, lower resolution of converters, deviations in frequency response,…..
- Lower supply voltages contribute to increase the impact of process fluctuations on electronic systems.

4.20 Mismatch



$A_V = -R_2/R_1$: gain depends on ratio (rather than on absolute values of R's); the relative values of R's must be matched for accurate gain.

4.20 Dealing with mismatch

- GLOBAL variation $\Rightarrow$ total variation of a parameter over a wafer (or batch) caused by equipment variations & spatial drift, e. g.
  - Dimensional errors (photo-mask sizes, lens aberrations)
  - Photo-resist thickness variations
  - Mechanical strain variation
- Because GLOBAL variations are correlated across die, they are minimized by design tricks:
  - common centroid components
  - distance reduction between identically designed pairs
  - same orientation, etc.

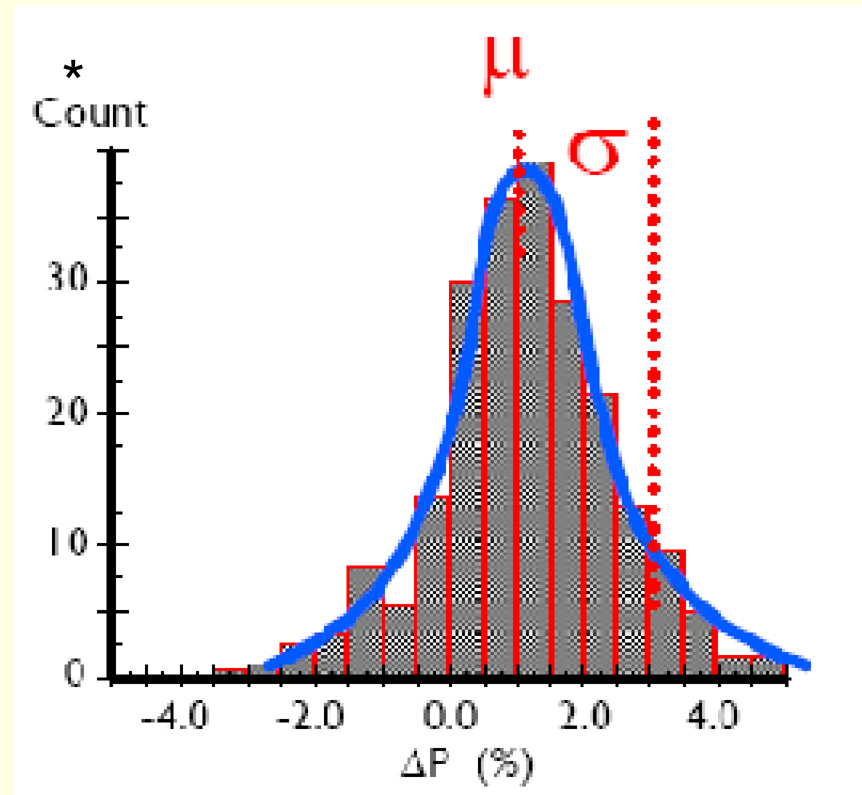
4.20 Dealing with mismatch

- LOCAL variation $\Rightarrow$ variation in a component with respect to an identical adjacent component, caused by atomistic stochastic effects
- Designers must understand the limitations imposed by LOCAL variations on performance.

4.20 Mismatch

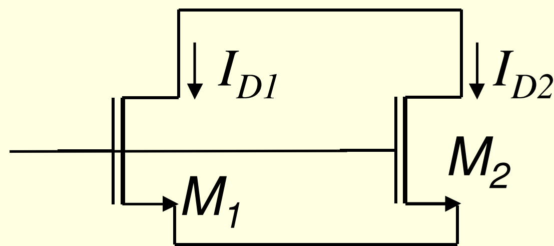
Identically designed resistors

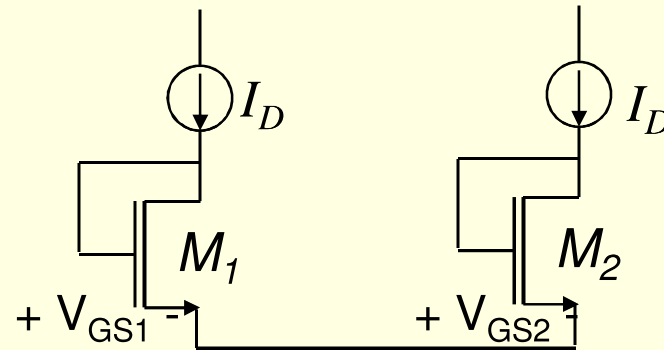
$$\frac{R_2}{R_1} = \frac{R_2 - R_1 + R_1}{R_1} = 1 + \frac{\Delta R}{R}$$



* http://www.essderc2002.deis.unibo.it/ESSDERC_web/Session_D02/D02_1.pdf

4.20 Mismatch





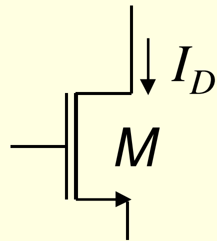
$M_1 \equiv M_2$ but $I_{D1} \neq I_{D2}$ for the same set of voltages

$M_1 \equiv M_2$ but $V_{GS1} \neq V_{GS2}$ for the same current

Fluctuations in doping, polysilicon granularity, interface traps, channel length & width & oxide thickness roughness,

4.20 A simple mismatch model

Mismatch in current



First order model (Vittoz): mismatch is caused by fluctuations in specific current and threshold voltage

$$I_D = I_S f\left(V_G - V_T, V_S, V_D\right)$$ Long-channel MOST

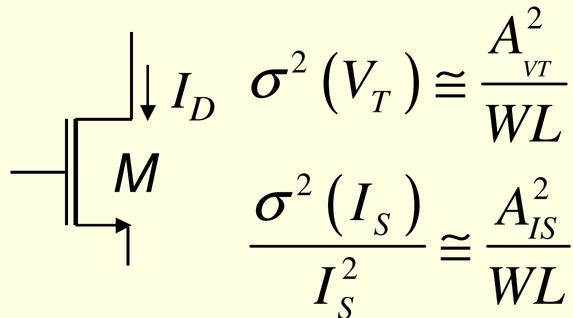
$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta I_S}{I_S} - \frac{g_m}{I_D}\Delta V_T$$

Uncorrelated (?) mismatch sources: $$\frac{\sigma^2(I_D)}{I_D^2} \cong \frac{\sigma^2(I_S)}{I_S^2} + \left(\frac{g_m}{I_D}\right)^2 \sigma^2(V_T)$$

Recall that, in saturation $$\frac{g_m}{I_D} = \frac{2}{n\phi_t}\frac{1}{\sqrt{1+i_f}+1}$$

What about $\sigma^2(I_S)$ and $\sigma^2(V_T)$?

4.20 A simple mismatch model



$$\sigma^2(V_T) \cong \frac{A_{VT}^2}{WL}$$

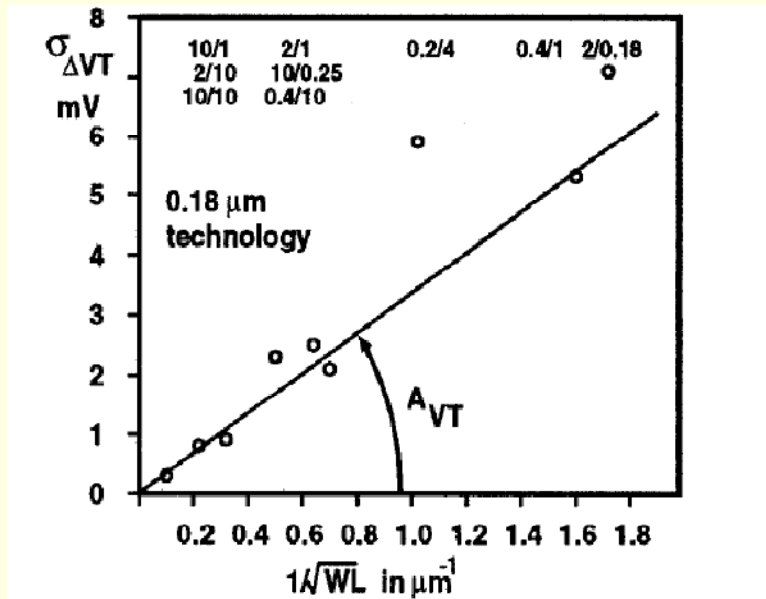
$$\frac{\sigma^2(I_S)}{I_S^2} \cong \frac{A_{IS}^2}{WL}$$

M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G.Welbers, “Matching properties of MOS transistors,” *IEEE JSSC*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.

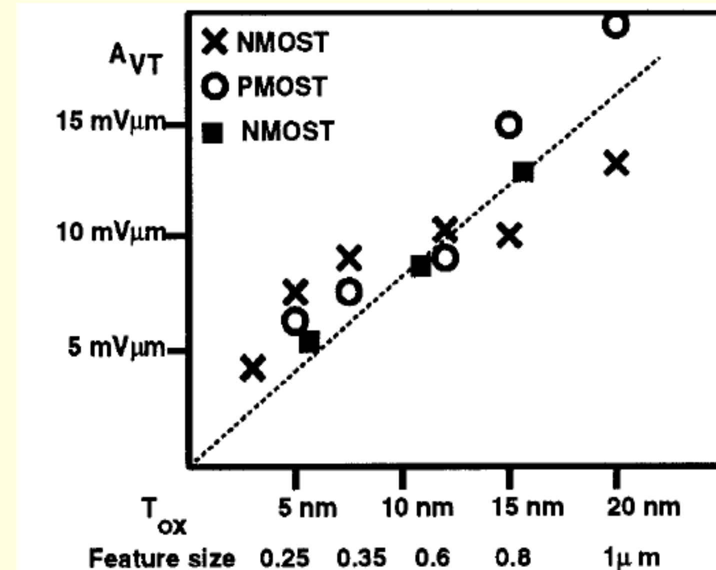
0.35 µm n-well technology

Parameter	NMOST	PMOST	Unit
A_{VT}	9	9	mV·µm
A_{IS} (A_{β})	1.9	2.25	% µm

4.20 A simple mismatch model



2. The standard deviation of the NMOST threshold versus the inverse square root of the area, for a 0.18 μm (3.3-nm gate oxide) process.

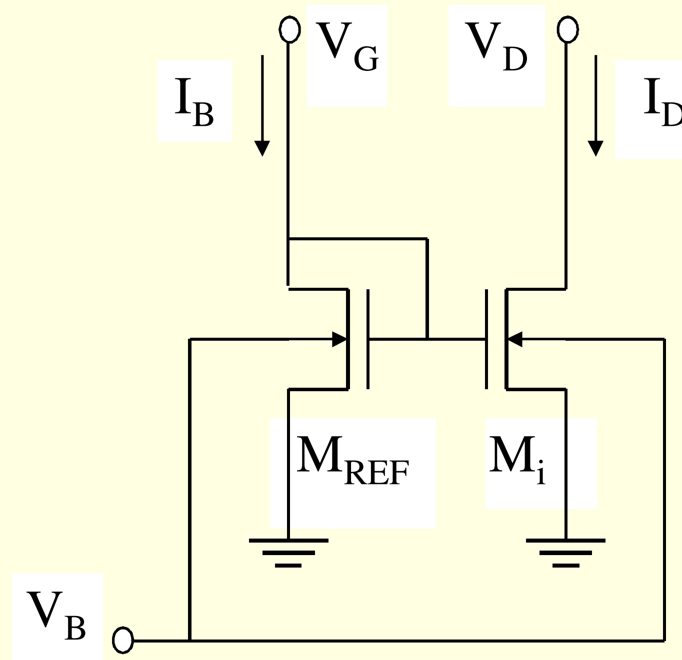


3. Evolution of matching coefficient over process generation. Squares are derived from[4], the other measurements are by the authors.

M. J. M. Pelgrom, H. P. Tuinhout, and M. Vertregt, “Transistor matching in analog CMOS applications,” in *IEDM Tech. Dig.*, 1998, pp. 915–918.

Mismatch – experimental results

Test circuit



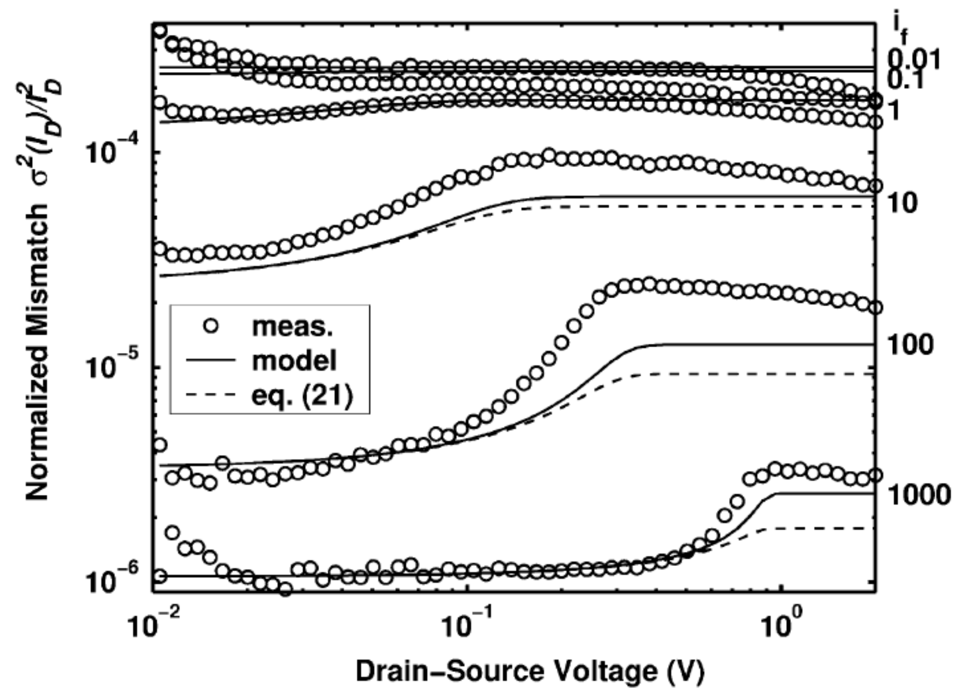


Fig. 4. Normalized current mismatch power for the *large* NMOS transistor array. Bulk-source voltage was kept at 0 V.

$12\ \mu m \times 8\ \mu m$

Test chip contains 20 samples of each group of transistors in 0.35 µm CMOS technology

Mismatch – experimental results

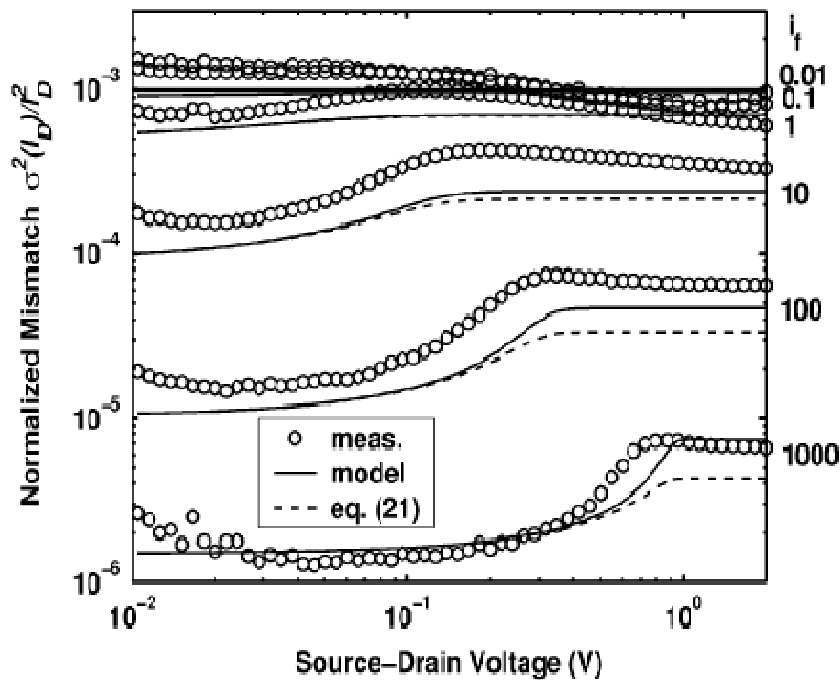


Fig. 6. Normalized current mismatch power for the *large* PMOS transistor array. Bulk-source voltage was kept at 0 V.

$12\ \mu m \times 8\ \mu m$

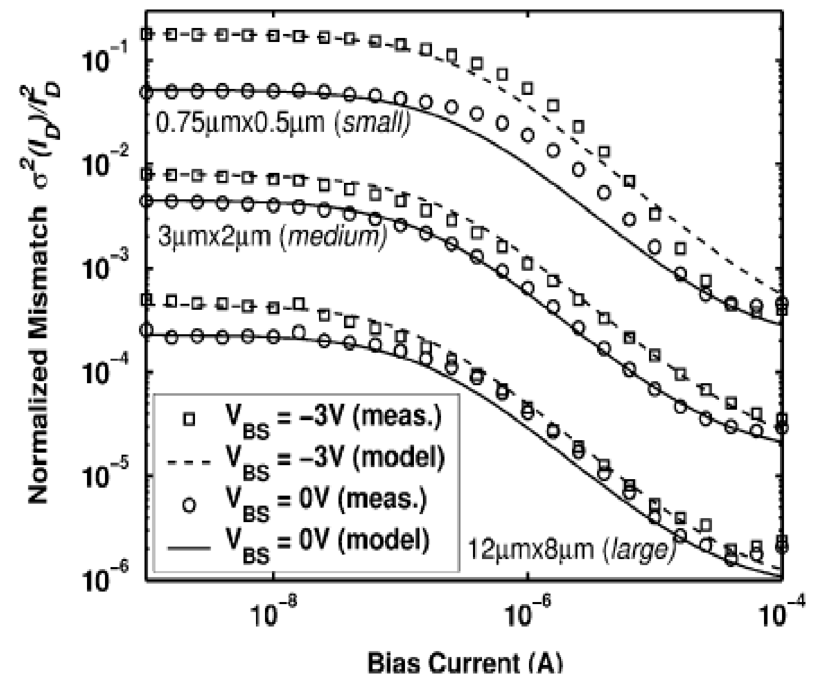
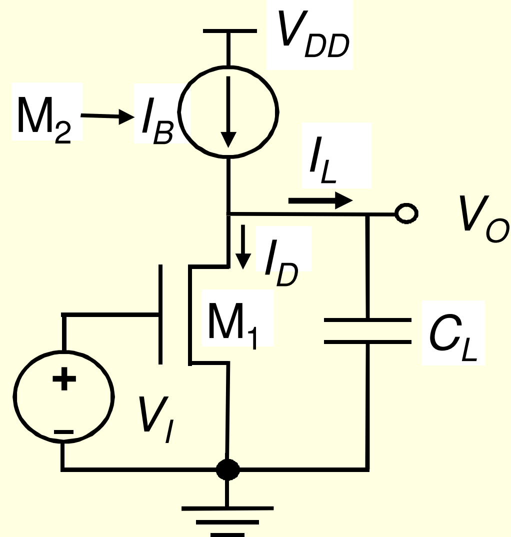


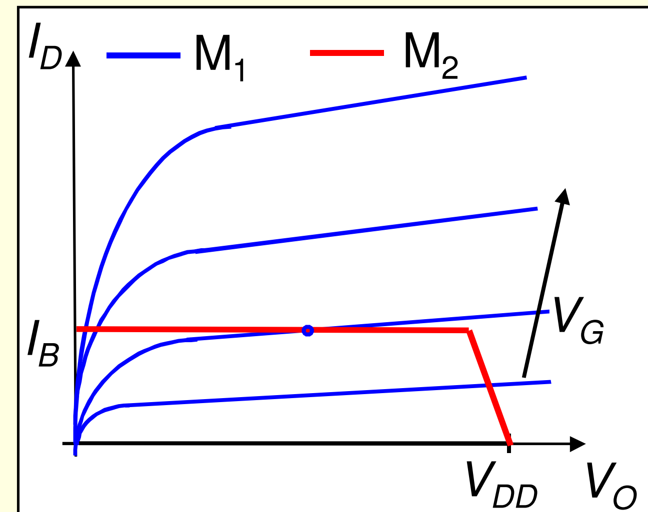
Fig. 8. Dependence of current matching on inversion level in the linear region for the *large*, *medium*, and *small* NMOS transistor arrays at two bulk bias voltages.

Contents

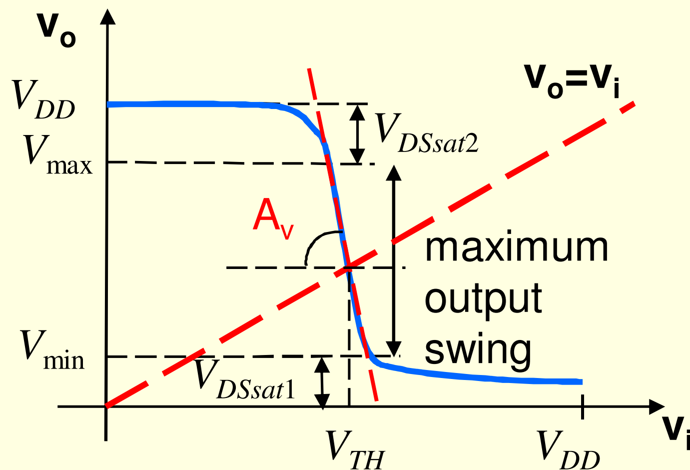
1. Why low-power & low-voltage
2. Fundamental limitations in analog integrated circuits
3. Components of the CMOS technology
4. MOSFET modeling
5. The basic gain stage
6. The current mirror
7. A self-biased current source

5. The common-source amplifier - 1





Output characteristics



Voltage transfer characteristic

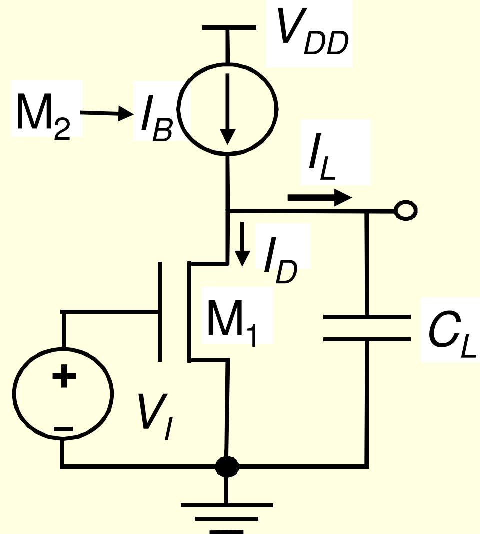
From UICM we find the dc voltage V_{TH} at the input:

$$\frac{V_{TH} - V_{T01}}{n_1 \phi_t} \cong \sqrt{1 + i_{f1}} - 2 + \ln\left(\sqrt{1 + i_{f1}} - 1\right)$$

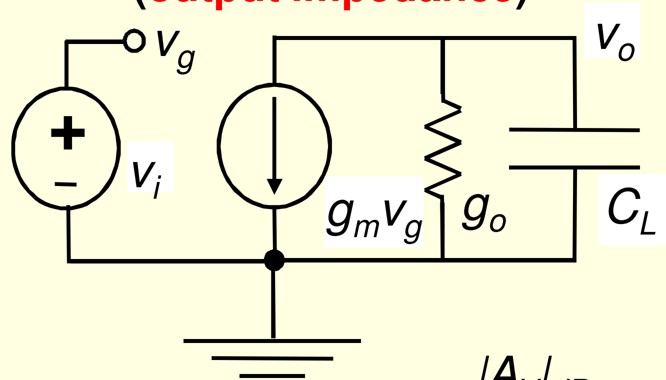
$$I_D = I_B \cong I_F{}_1 - I_{R1}; \quad i_{f1} \cong \frac{I_B}{I_{S1}}$$

0

5. The common-source amplifier - 2



V-I converter (transconductor) followed by an I-V converter (output impedance)



$$A_V = \frac{v_o}{v_i} = -g_m \left(\frac{1}{g_o + sC_L} \right) = A_{V0} \frac{1}{1 + s/\omega_b}$$

$$A_{V0} = \frac{-g_{m1}}{g_o} = \frac{-g_{m1}}{g_{ds1}}$$

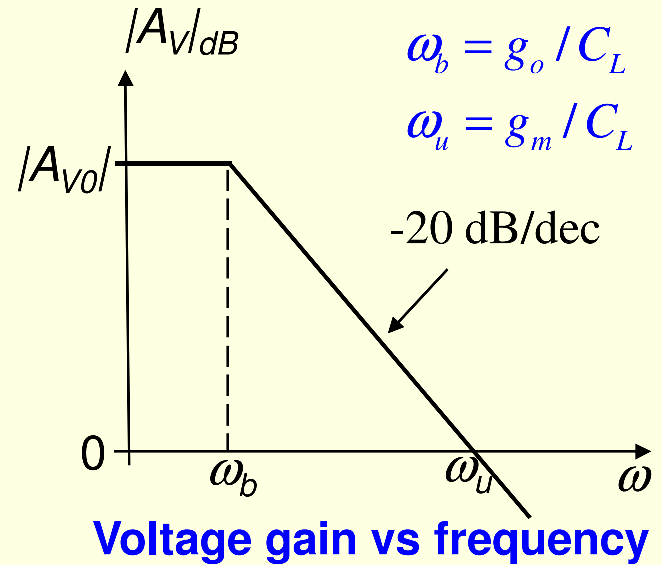
$$A_{V0} = -\frac{V_{A1}}{n_1 \phi_t} \frac{2}{1+\sqrt{1+i_{f1}}}$$

$$g_{ds1} = \frac{I_B}{V_{A1}}$$

$$V_{A1} = V_E L_1$$

$$\omega_b = g_o / C_L$$

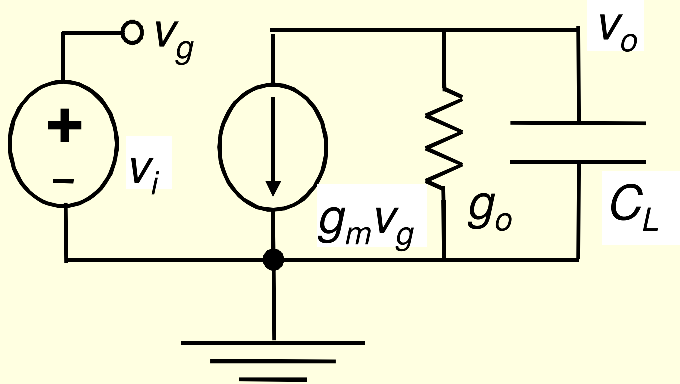
$$\omega_u = g_m / C_L$$



Voltage gain vs frequency

5. The common-source amplifier - 3

Design example



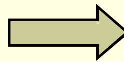
Sizing and biasing: *W, L,* I_B

$$I_{D\min} = I_{WI} = g_m n\phi_t$$

$$ECF = (I_D - I_{WI})/I_{WI} = \left(\sqrt{1+i_f} - 1\right)/2$$

$$\frac{W}{L} = \frac{g_m}{2\mu C'_{ox}\phi_t}\frac{1}{ECF}$$

Power-area tradeoff



$$A_{V0} = -\frac{V_E L}{n\phi_t}\frac{1}{ECF+1}$$

How long can L be

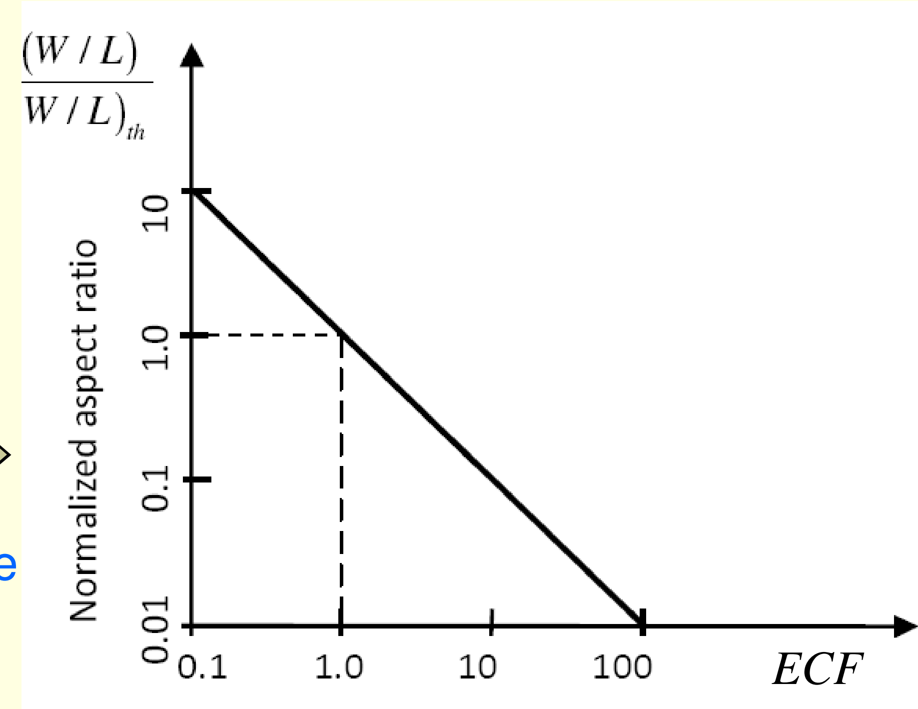
C_{IN} and transit time are both proportional to L^2 (for constant W/L)!

Specifications: ω_u, C_L, A_{V0}

$$g_m = \omega_u \cdot C_L$$

$$I_D = n\phi_t g_m \frac{\sqrt{1+i_f}+1}{2}$$

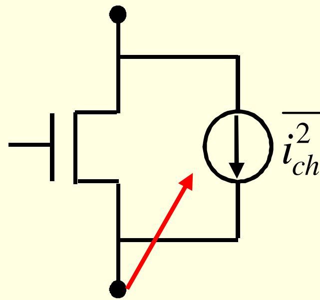
How do we choose i_f?



$$ECF = (I_D - I_{D\min})/I_{D\min}$$

5. The common-source amplifier - 4

MOST noise model



Noise current generator

Thermal **1/f**

$$\frac{\overline{i_{ch}^2}}{\Delta f} = 4\gamma kTg_{ms} + \frac{K_F g_m^2}{WLC'_{ox}}\frac{1}{f} \cong 4\gamma kTg_{ms}\left(1 + \frac{f_c}{f}\right)$$

Bias-dependent factor

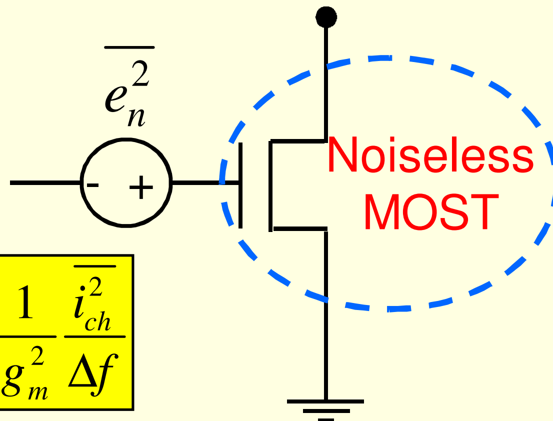
Corner frequency

$$\gamma = \frac{2}{3}\left(1 - \frac{1/2}{\sqrt{1+i_f}+1}\right)$$

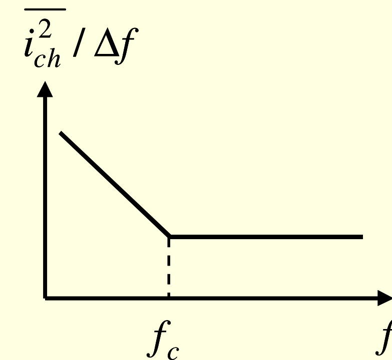
1/2 (WI) **2/3 (SI)**

$$f_c \cong \frac{\pi}{2}\frac{K_F}{nq\phi_t}f_T$$

Input-referred noise model



$$\frac{\overline{e_n^2}}{\Delta f} = \frac{1}{g_m^2}\frac{\overline{i_{ch}^2}}{\Delta f}$$



$$f_c \cong \frac{f_T}{2000}$$ ⇒ 0.35 um CMOS technology

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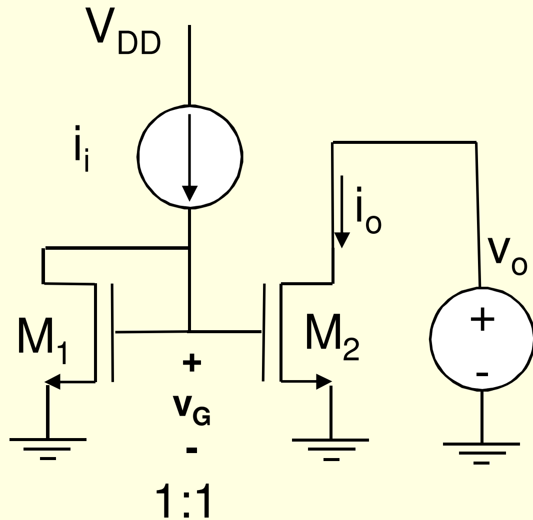
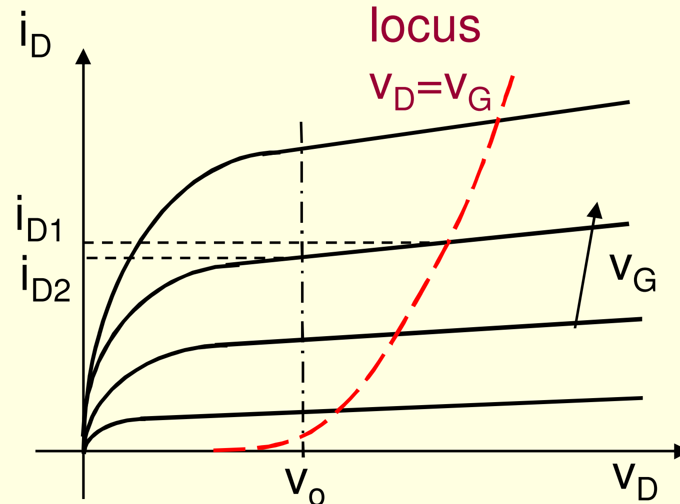
6. The current mirror
7. A self-biased current source

6. The two-transistor current mirror - 1





M_1: i→v converter
M_2: v→i converter

Error due to difference in V_D values

$$I_D \cong I_S i_f \left(V_G - V_{T0}, V_S\right)\left(1 + V_D / V_A\right) \quad V_D > V_{Dsat}$$

$$\frac{\Delta i}{i_i} = \frac{i_o - i_i}{i_i} \cong \frac{v_o - v_i}{V_A} \cong \frac{v_o - v_i}{V_E L}$$

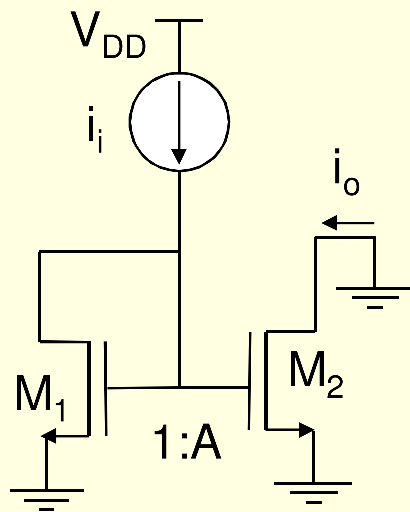
Error due to mismatch

$$\frac{\Delta I_D}{I_D} \cong \frac{1}{I_D}\left(\frac{\partial I_D}{\partial I_S}\Delta I_S + \frac{\partial I_D}{\partial V_{T0}}\Delta V_{T0}\right)$$

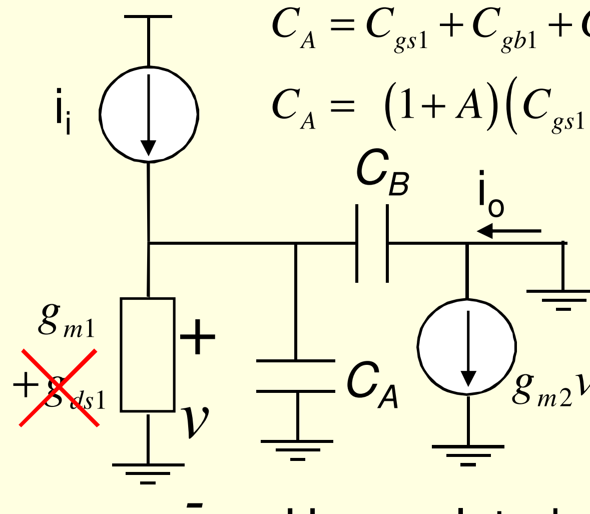
$$\cong \frac{\Delta I_S}{I_S} - \frac{g_m}{I_D}\Delta V_{T0}$$

$$\frac{\sigma^2\left(\Delta I_D\right)}{I_D^2} = \left(\frac{g_m}{I_D}\right)^2 \sigma^2\left(\Delta V_T\right) + \frac{\sigma^2\left(\Delta I_S\right)}{I_S^2} = \frac{1}{WL}\left[\left(\frac{g_m}{I_D}\right)^2 A_{VT}^2 + A_{IS}^2\right]$$

6. The two-transistor current mirror - 2



ac analysis

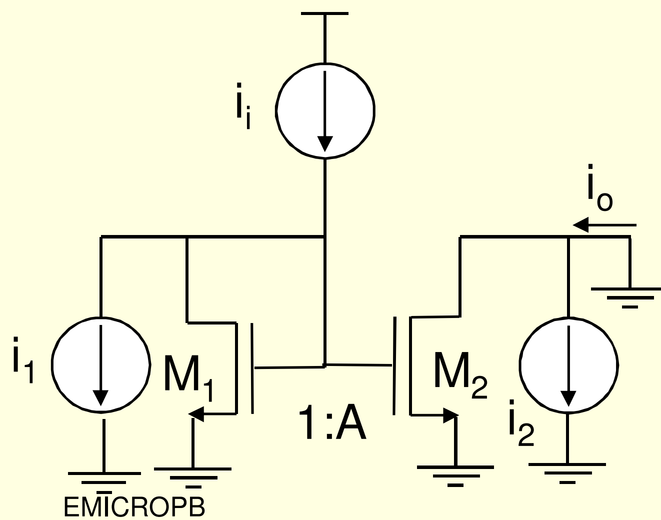


$$C_A = C_{gs1} + C_{gb1} + C_{gs2} + C_{gb2} + C_{db1} + C_B$$

$$C_A = (1+A)(C_{gs1} + C_{gb1}) + C_{db1} + C_{ovd2}$$

$$\frac{I_o}{I_i}(s) \cong \frac{A}{1+\tau s} \qquad \tau = \frac{C_A + C_B}{g_{m1}} \approx \frac{1+A}{2\pi f_T}$$

Noise analysis



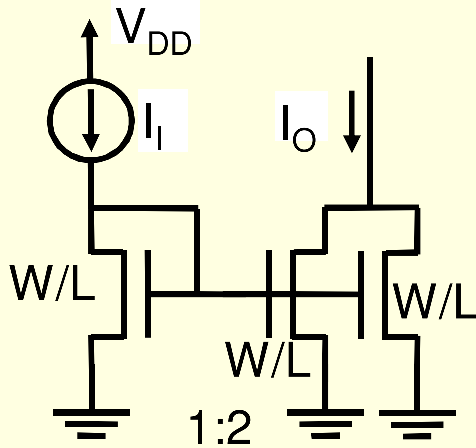
Uncorrelated noise sources

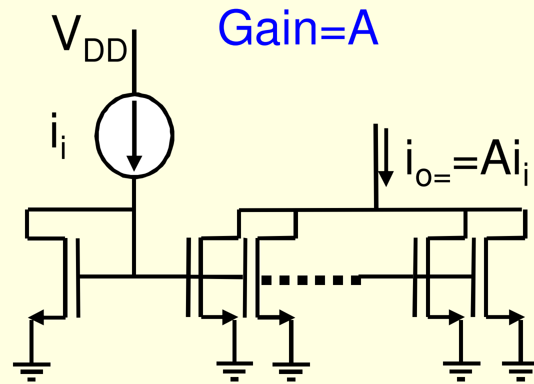
$$\overline{i_o^2} = \left(\overline{i_i^2} + \overline{i_1^2}\right)\left(\frac{g_{m2}}{g_{m1}}\right)^2 + \overline{i_2^2} \qquad \frac{g_{m2}}{g_{m1}} = A$$

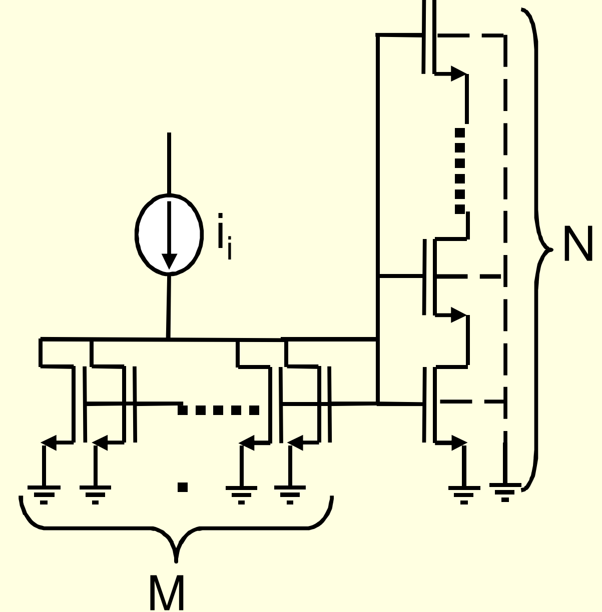
$$\overline{i_o^2} = A^2\left(\overline{i_i^2} + \overline{i_1^2}\right) + A\overline{i_1^2}$$

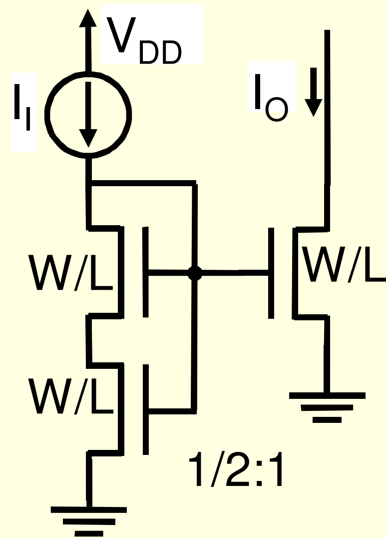
The effect of M_1 on noise is A times greater than that of M_2

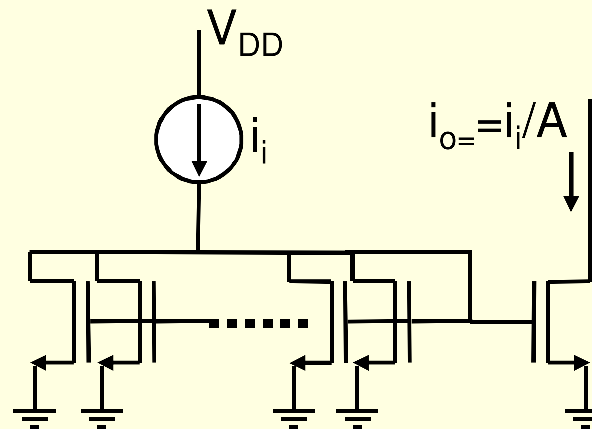
6. Current mirror: gain schemes











Gain= 1/A

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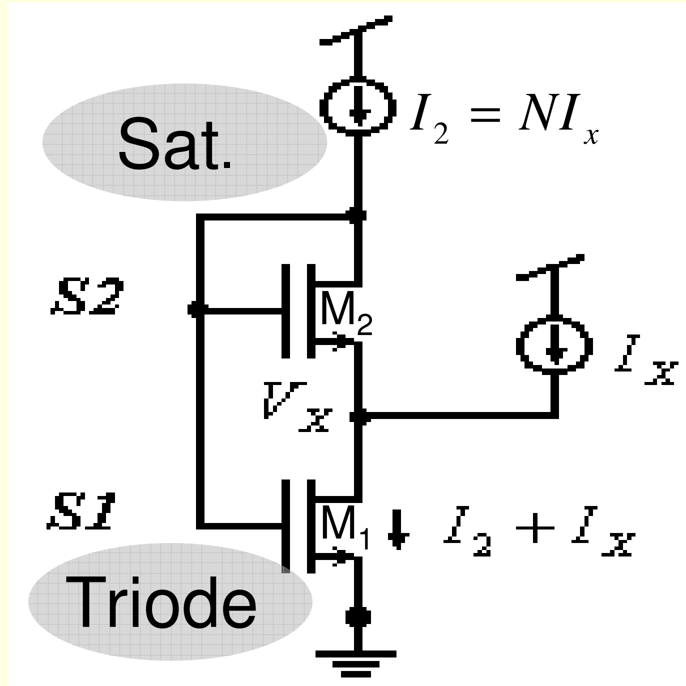
7. A self-biased current source - 1

SELF-CASCODE MOSFET (SCM)



$$I_{S2}\left(i_{f2} - i_{r2}\right) = NI_x \quad (i_{r2} \to 0) \qquad i_{f2} = i_{r1}$$

$$I_{S1}(i_{f1} - i_{f2}) = (N+1)I_x$$

$$\Downarrow$$

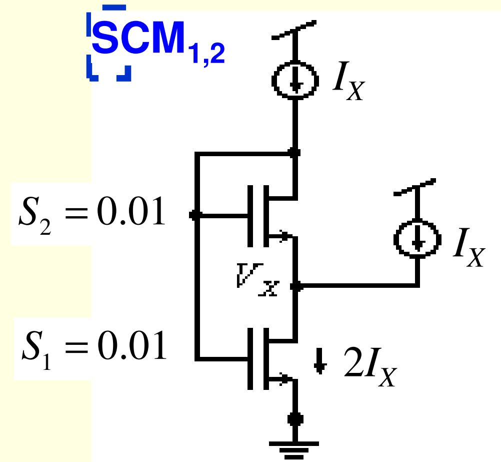
$$i_{f1} = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right] i_{f2} = \alpha i_{f2}$$

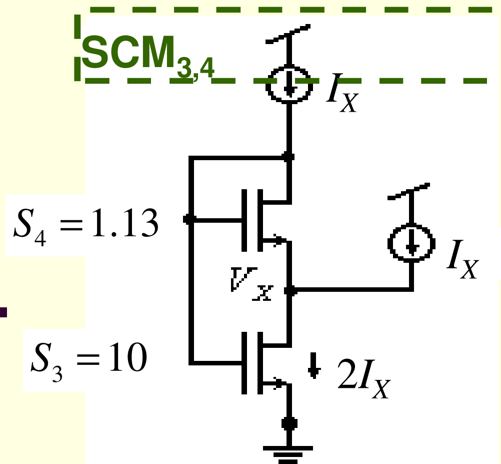
Applying UICM to both M_1 & M_2

$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2}} - 1}{\sqrt{1+i_{f2}} - 1}\right)$$

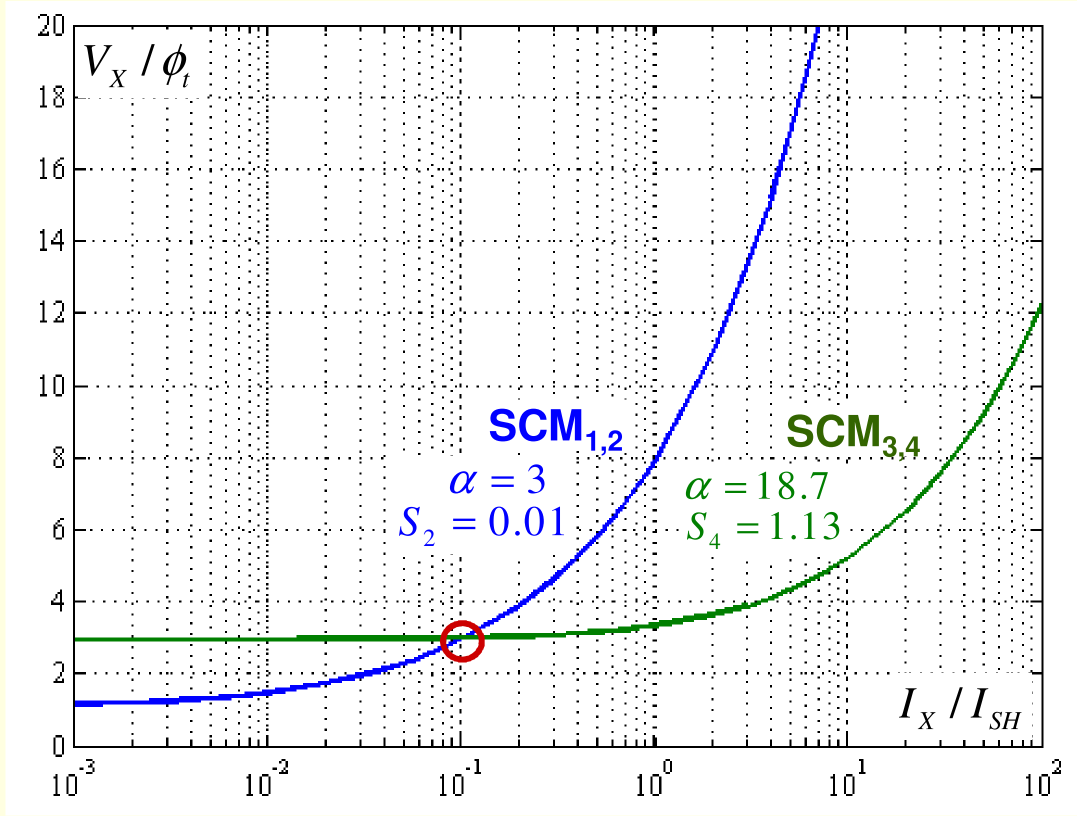
where $i_{f2} = \dfrac{NI_X}{I_{S2}} = \dfrac{NI_X}{S_2 I_{SH}}$

7. A self-biased current source - 2





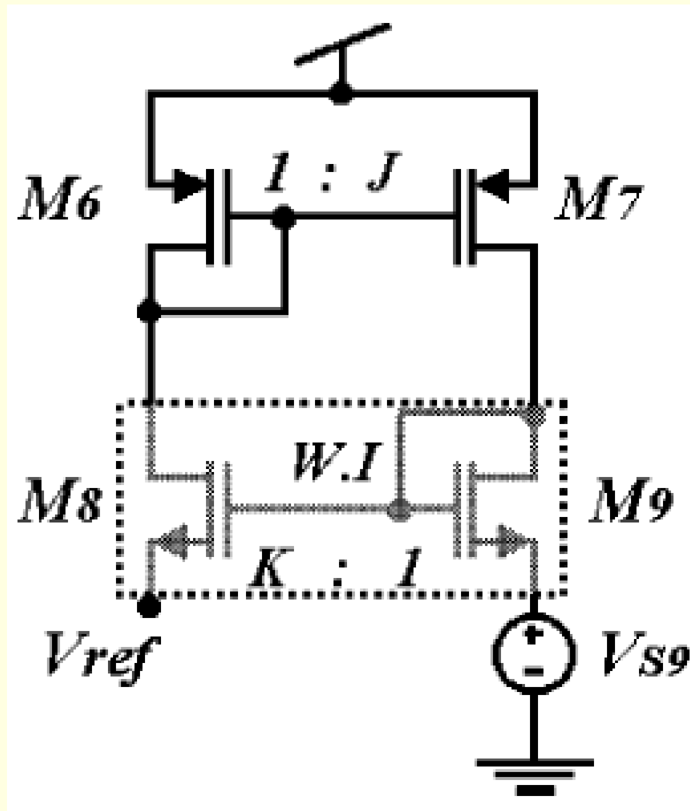
$$\alpha = 1 + \frac{S_{even}}{S_{odd}}\left(1 + \frac{1}{N}\right)$$



$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha \frac{I_X}{S_{even} I_{SH}}} - \sqrt{1 + \frac{I_X}{S_{even} I_{SH}}} + \ln\left(\frac{\sqrt{1 + \alpha \frac{I_X}{S_{even} I_{SH}}} - 1}{\sqrt{1 + \frac{I_X}{S_{even} I_{SH}}} - 1}\right)$$

7. A self-biased current source - 3

VOLTAGE FOLLOWING (NMOS) CURRENT MIRROR (PMOS)[1]



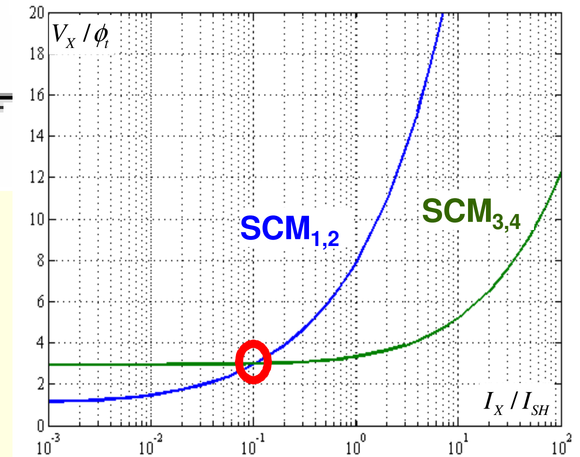
$$\frac{V_{ref} - V_{S9}}{\phi_t} = \sqrt{1 + JKi_{f8}} - \sqrt{1 + i_{f8}} + \ln\left(\frac{\sqrt{1 + JKi_{f8}} - 1}{\sqrt{1 + i_{f8}} - 1}\right)$$

When both M_8 & M_9 operate in WI:

$$V_{ref} = V_{S9} + \phi_t \ln(JK)$$

[1] B. Gilbert, AICSP vol. 38, pp. 83-101, Feb. 2004

7. A self-biased current source - 4



VFCM is a positive feedback circuit → return ratio must be < 1 for stability

7. A SBCS: Design - 5

Output current: I_{ref}=10 nA

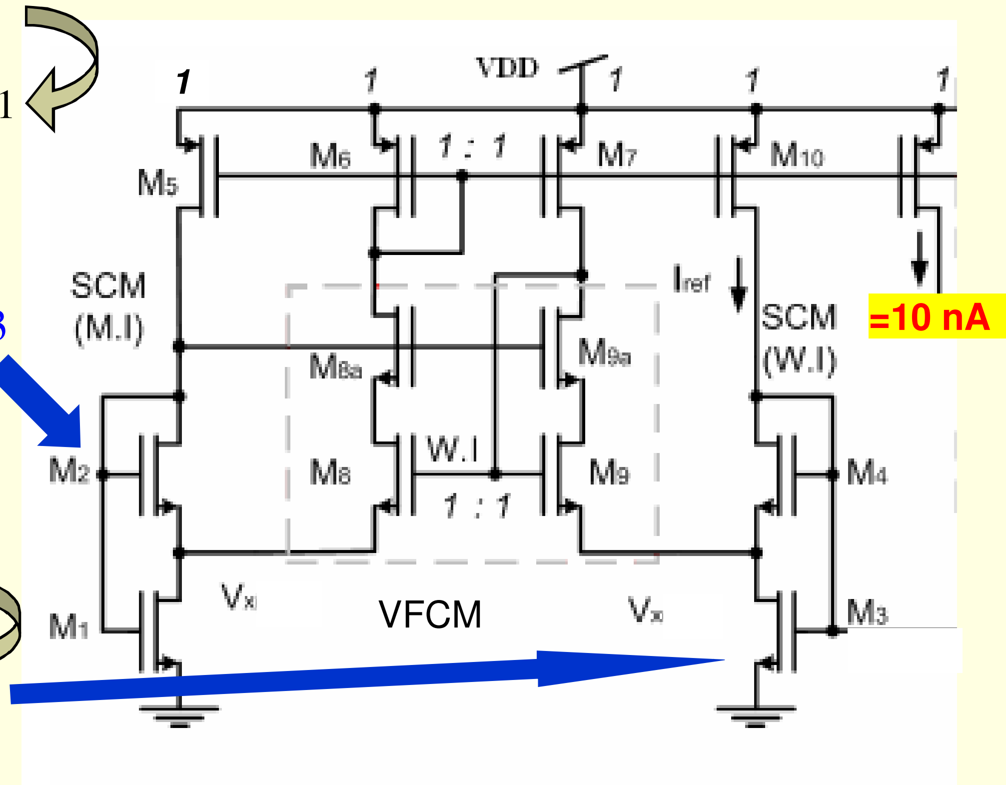
$I_{SHn\text{-}channel} \cong 100$ nA, $I_{SHp\text{-}channel} \cong 40$ nA

Let us choose $i_{f2} = 10,\ S_2 = S_1$

$$I_{S2} i_{f2} = 10 \text{ nA} \rightarrow I_{S2} = 1 \text{ nA} \rightarrow S_2 = S_1 = 0.01$$

$$\alpha_{1-2} = 1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right) = 3$$

$$\frac{V_X}{\phi_t} = \sqrt{1+30} - \sqrt{1+10} + \ln\left(\frac{\sqrt{1+30}-1}{\sqrt{1+10}-1}\right) = 2.93$$



Let us choose $i_{f3(4)} << 1$ (WI)

$$\frac{V_X}{\phi_t} \cong \ln \alpha_{3-4} \Rightarrow \alpha_{3-4} = e^{2.93} \cong 18.7$$

$$\alpha_{3-4} = 1 + \frac{S_4}{S_3}\left(1 + \frac{1}{1}\right) \Rightarrow \frac{S_4}{S_3} = 8.85$$

Let us choose i_{f3}=0.187 $\rightarrow i_{f4} = i_{f3} / \alpha_{3-4} = 0.01$

$$I_{S4} i_{f4} = 10 \text{ nA} \rightarrow I_{S4} = 1\ \mu\text{A} \rightarrow S_4 = 10$$

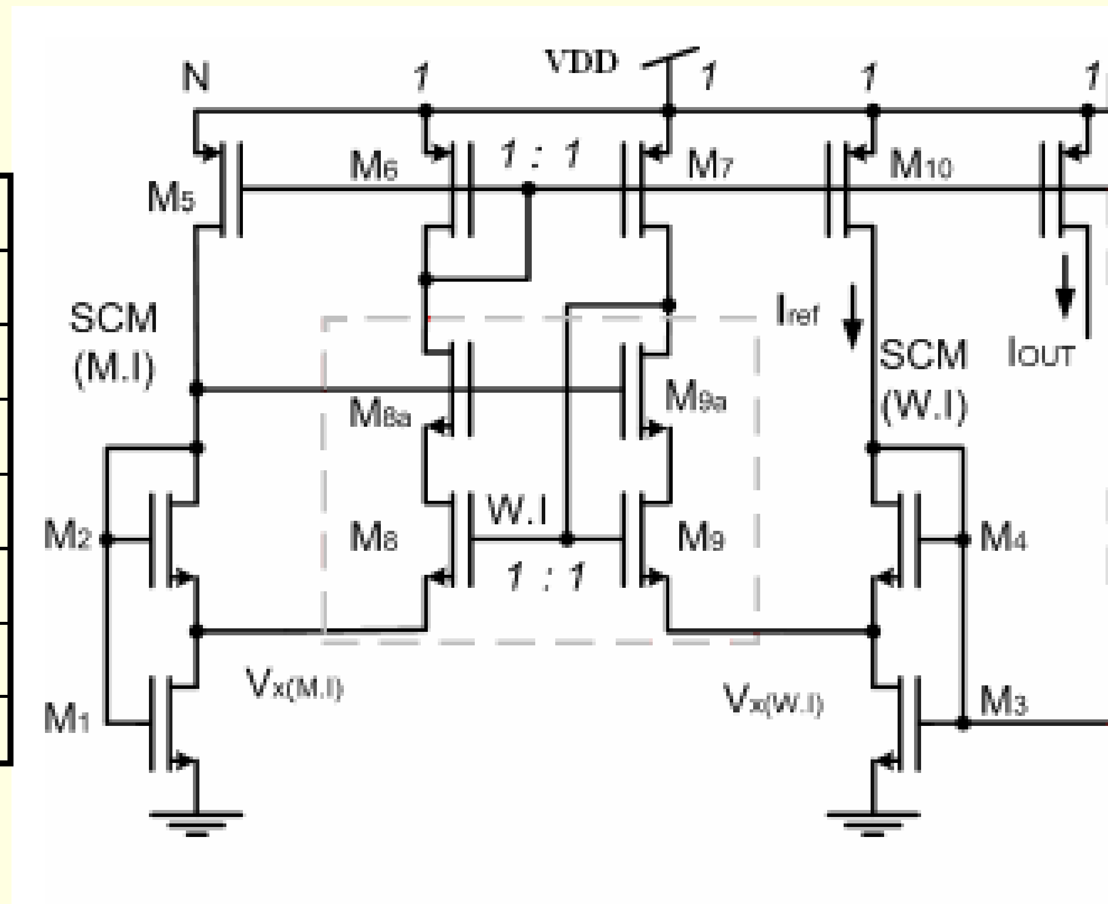
$$S_3 = \frac{S_4}{8.85} = 1.13$$

$$\frac{V_X}{\phi_t} = \sqrt{1+\alpha i_{f2(4)}} - \sqrt{1+i_{f2(4)}} + \ln\left(\frac{\sqrt{1+\alpha i_{f2(4)}}-1}{\sqrt{1+i_{f2(4)}}-1}\right)$$

7. A SBCS: Design - 6

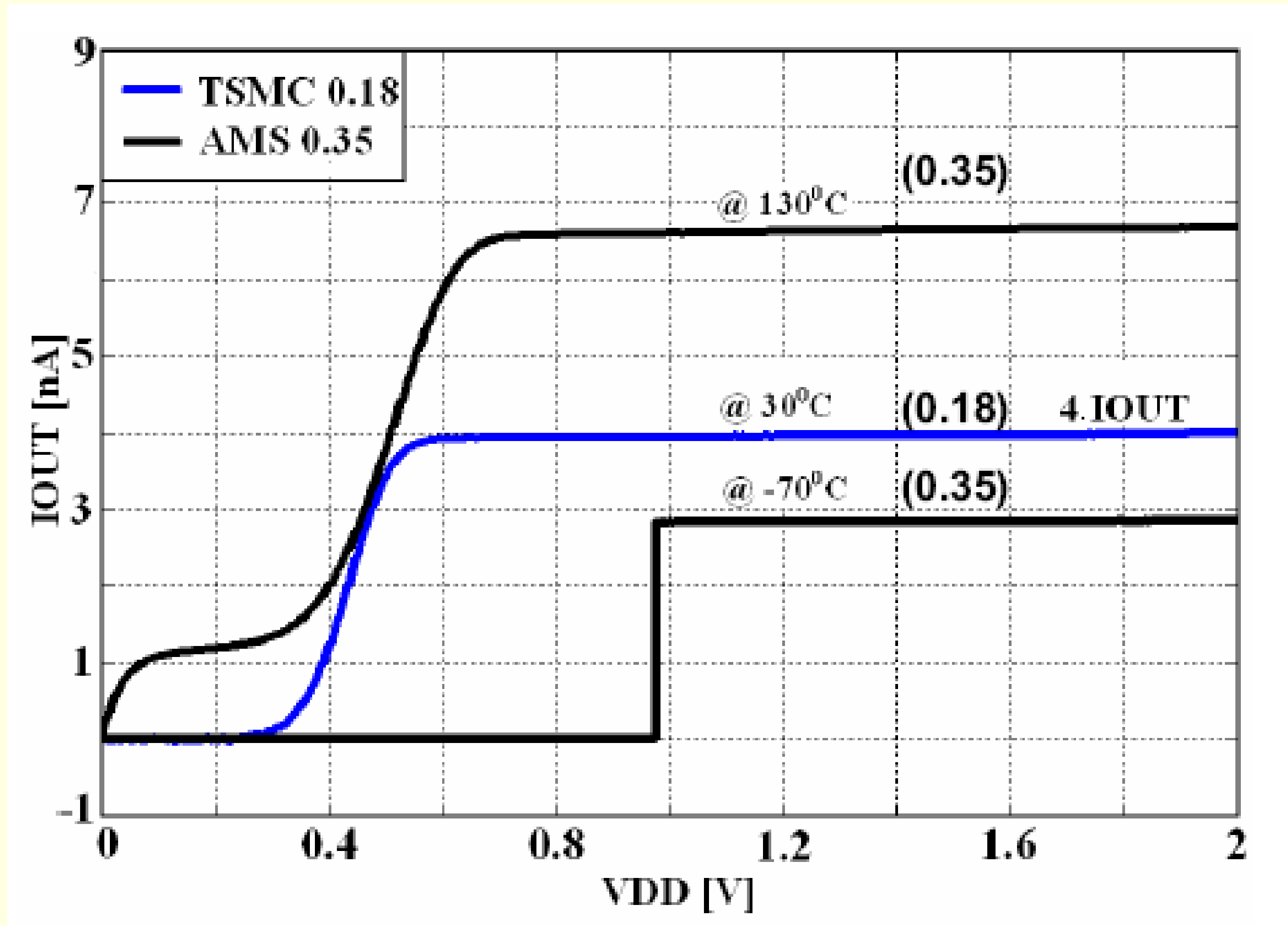
Summary

	S	i_f	i_r
M_1	0.01	30	10
M_2	0.01	10	0
M_3	1.13	0.187	0.01
M_4	10	0.01	0
M_8, $M_{8(a)}$	1	0. 1	0
M_9, $M_{9(a)}$	1	0. 1	0
M_P (all)	2.5	0.1	0



Core area in 0.35µm CMOS ≈ 0.02 mm²

7. A SBCS – 7 I_{OUT} vs. V_{DD} at constant T



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Some references for interesting work on LP-LV design

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http://www.eecs.berkeley.edu/Research/Projects/Faculty/rabaey.html

http://bwrc.eecs.berkeley.edu/Research/energy_efficient_systems.htm

http://www.csem.ch/site/

http://www.mead.ch/ (courses on Low-power & Low-voltage)

Covering the essentials of analog circuit design, this book takes a unique design approach, based on a MOSFET model valid for all operating regions, rather than on the standard square-law model. Opening chapters focus on device modeling, integrated circuit technology, and layout, whilst later chapters go on to cover noise and mismatch, and analysis and design of the basic building blocks of analog circuits, such as current mirrors, voltage references, voltage amplifiers, and operational amplifiers. An introduction to continuous-time filters is also provided, as are the basic principles of sampled-data circuits, especially switched-capacitor circuits. The final chapter then reviews MOSFET models and describes techniques to extract design parameters. With numerous design examples and exercises also included, this is ideal for students taking analog CMOS design courses and also for circuit designers who need to shorten the design cycle.

- Lecture slides
- Solutions to problems

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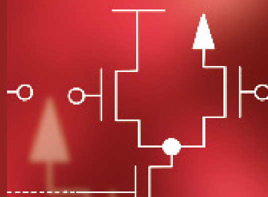

Schneider and Galup-Montoro

CMOS Analog Design Using All-Region MOSFET Modeling

CMOS Analog Design Using All-Region MOSFET Modeling

Márcio Cherem Schneider and
Carlos Galup-Montoro

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