On the Minimum Supply Voltage for MOSFET Oscillators

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***Abstract*—In order to investigate the minimum supply voltage for MOSFET oscillators, three topologies were studied. Two of them, namely the enhanced swing inductive-load ring and the enhanced swing Colpitts oscillators, can operate with supply voltages below the thermal voltage. Simplified theoretical expressions for the minimum supply voltage of the oscillators were derived. Measurement results obtained using prototypes built with zero-VT transistors and high-quality-factor inductors confirmed the operation of one of the oscillators down to a supply voltage below 5 mV.**

***Index Terms*—Fundamental limitations in MOS technology, minimum supply voltage, MOSFET ultra-low voltage analog circuits, ultra-low-voltage circuits, ultra-low-voltage Colpitts oscillator, ultra-low-voltage ring oscillators, zero-VT transistors.**

I. Introduction

EARLY in the development of the MOS technology it became clear that the reduction of the supply voltage was a prerequisite for circuit miniaturization [1]. The first study of the CMOS inverter operating in weak inversion [2] stated that CMOS logic circuits can operate with supply voltages as low as 200 mV at room temperature. The motivation for the continuous reduction of the supply voltage is as intense as ever because of the uninterrupted development of VLSI technologies, as can be seen in recent studies [3], [4].

In [5], Prof. Meindl, based on the weak inversion model of the CMOS inverter of [2], concluded that the lower bound for the supply voltage of the CMOS inverter is

$$V_{dd}(\min) > 2\phi_t \ln(1+n) \tag{1}$$

where $\phi_t = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge and n is the slope factor. For an ideal MOSFET ($n = 1$) at room temperature, (1) gives $V_{dd}(\min) = 36$ mV.

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This minimum value for the supply voltage results from the analysis of the static transfer curve of the CMOS inverter with matched n- and p-channel MOSFETs. The maximum voltage gain, which occurs at the midpoint of the voltage transfer curve, must be higher than unity and the supply voltage required to achieve this gain is given by (1). CMOS digital circuits are getting closer to the lower boundary for V_{dd} given by (1). The use of feedback to match the subthreshold n- and p-channel MOSFET currents allows digital CMOS circuits in a standard 180 nm CMOS technology to operate at $V_{dd} = 4kT/q$ [6]. More recently, operation at room temperature with $V_{dd} = 62$ mV was achieved using logic gates built around Schmitt triggers [7].

Concerning analog circuits it has been generally considered that they require higher supply voltages than digital ones [8], but blocking oscillators [9] using JFETs [10] or native MOSFETs [11], [12] are important exceptions to this rule. The oscillators of [10], [11] act as start up circuits in off-the-shelf energy harvesting devices capable of operating from supply voltages as low as 20 mV provided by thermoelectric generators. Since transistors are not able to provide the necessary voltage gain at such low supply voltages, the supplementary gain necessary to start up oscillations is obtained from feedback transformers with primary-secondary turns ratios of around 1:100. Reference [13] reports a blocking oscillator prototype circuit that starts to oscillate at a supply voltage of 5.5 mV at the expense of bulky transformers. Recently, Colpitts oscillators operating from supply voltages of the order of 20 mV [14], [15] were also reported. All of the above mentioned circuits oscillate at frequencies in the kHz range.

Considering the continuous trend toward supply voltage reduction and the ultra-low-voltage oscillators recently reported [10]–[15], it is timely to discuss the minimum supply voltage for MOSFET oscillators in order to provide a clearer perspective regarding the ultimate voltage scaling [4].

For circuits with supply voltages of 100 mV or less, transistors usually operate in weak inversion (WI). Additionally, there is not enough voltage headroom to operate MOS transistors in saturation. For these reasons, in this study we used the model of the transistor operating in the triode region in WI, which is summarized in Appendix A.

In this paper we analyze some oscillator topologies built with native (zero-V_T) MOSFETs, which are devices well suited to low voltage operation. We derived the condition for oscillation startup and the corresponding minimum supply voltage. Since the oscillation condition requires a loop gain of unity, the minimum supply voltage expressions for oscillation are similar to the Meindl formula (1) for $V_{dd}(\min)$. We have carefully ana-

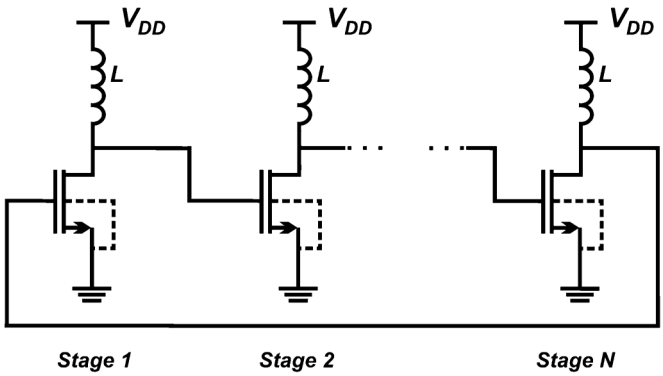

Fig. 1. Schematic diagram of an N-stage inductive-load ring oscillator.

lyzed the cases in which the supply voltage is below the Meindl limit and included experimental results to support the theoretical formulas.

The paper is organized as follows. Section II presents an inductive load ring oscillator and Section III an enhanced swing version of it. An enhanced swing Colpitts oscillator is analyzed in Section IV. Sections V and VI describe experimental and simulation results with the ring and Colpitts oscillators, respectively. Section VII describes the applications envisaged in this study, while the conclusions are summarized in Section VIII.

II. The Inductive-Load Ring Oscillator

Starting up a conventional ring oscillator with a power supply below 100 mV is extremely difficult [16]. The magnitude of the minimum supply voltage $V_{dd}(\min)$ is usually limited by the imbalance of the threshold voltages of the n- and p-channel transistors of the logic inverter [16]. In order to reduce the $V_{dd}(\min)$ of the conventional ring oscillator, one can use the inductive-load ring oscillator topology [17] shown in Fig. 1. This topology, which replaces the active load PMOS of the logic inverter with an inductor, not only reduces $V_{dd}(\min)$ but also boosts the oscillation amplitude beyond the supply rail. It should be noted that for a number of stages $N = 2$ this structure reduces to the widely used cross-coupled LC oscillator [18].

Using the MOSFET model described in Appendix A, the simplified small-signal equivalent circuit of a single stage of the inductive-load ring oscillator is shown in Fig. 2, where g_m and g_{md} represent the gate and drain transconductances respectively, C is the sum of all capacitances between the drain node and the ac ground, and G_P models the inductor loss. The effect of C_{gd}, which is relevant due to both the overlap capacitance and operation of transistors in the triode region, has not been taken into account for the sake of simplicity. For a more accurate analysis, which includes C_{gd}, the reader is referred to [23].

The transfer function of the single stage in Fig. 2 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi} \tag{2}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L(g_{md}+G_p)} \tag{3}$$

where ϕ is the phase shift between output and input.

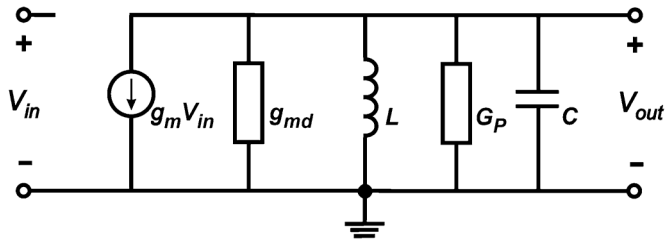

Fig. 2. Simplified small-signal model of a single stage of the inductive-load ring oscillator.

The requirement of gain greater than unity for the starting up of oscillations is satisfied for

$$\frac{g_m}{g_{md}+G_P}\frac{1}{\sqrt{1+(\tan\phi)^2}} > 1. \tag{4}$$

For the sake of simplicity let us consider the case of an even number of stages. In this case, the ring oscillates with $\phi = \pi$ (see Appendix B). Thus, since $g_m = (g_{ms} - g_{md})/n$ (see Appendix A), (4) can be rewritten as

$$\frac{g_{ms}}{g_{md}} > 1 + n\left(1+\frac{G_p}{g_{md}}\right). \tag{5}$$

In WI and in the triode region we have (see Appendix A)

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}. \tag{6}$$

From (5) and (6), the minimum supply voltage required to start up the oscillator is

$$V_{dd}(\min) = V_{ds}(\min) = \phi_t \ln\left[1+n\left(1+\frac{G_p}{g_{md}}\right)\right]. \tag{7}$$

If the inductor losses are negligible, (7) reduces to

$$V_{dd}(\min) > \phi_t \ln(1+n). \tag{8}$$

Thus, the minimum supply voltage for oscillation is one-half of the minimum supply voltage required for proper operation of the logic inverter ((1)). This result was to be expected, since if the inductor is lossless, oscillation is achieved for an intrinsic gain of the transistor higher than unity, as required for one of the transistors of the CMOS inverter.

We can readily note from (8) that for the case of $G_p \ll g_{md}$, the minimum supply voltage is proportional to the absolute temperature and independent of the process. When G_p is of the order of or greater than g_{md}, however, the value of $V_{dd}(\min)$ can be severely affected by the process and the temperature-dependent threshold voltage V_T, since in weak inversion g_{md} is an exponential function of V_T, which implies a quasi-linear dependence of $V_{dd}(\min)$ on the threshold voltage. Finally, the value of the oscillation frequency is expected to vary by $\pm 20\%$ to 30% with process parameters in a well established technology.

If we recalculate the $V_{dd}(\min)$ value required for a generic voltage gain A_v, in lieu of unity gain, we obtain

$$V_{dd}(\min) > \phi_t \ln(1+nA_v). \tag{9}$$

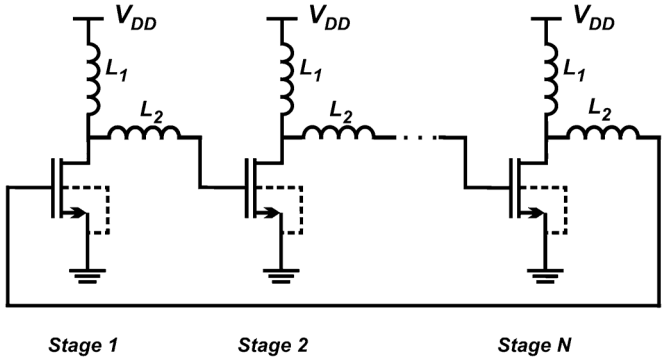

Fig. 3. Schematic diagram of an N-stage enhanced swing (ES) inductive-load ring oscillator.

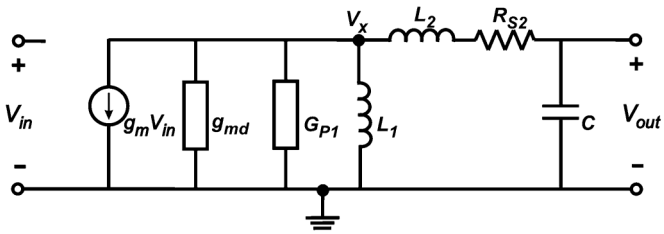

Fig. 4. Simplified small-signal model of a single stage of the ES inductive-load ring oscillator.

Equation (9) can be used to better understand the results reported in the next section.

III. The Enhanced Swing Inductive-Load Ring Oscillator

The enhanced swing (ES) inductive-load ring oscillator [19] shown in Fig. 3 boosts the voltage gain due to the coupling inductors (L_2) between stages.

The simplified small-signal equivalent circuit of a single stage of the ES inductive-load ring oscillator is shown in Fig. 4, where R_{S2} represents the series resistance of inductor L_2, G_{p1} is the parallel conductance of L_1, and all other symbols have the same meaning as in Fig. 2.

A detailed analysis of the circuit in Fig. 4 is carried out in Appendix C, but we can obtain very directly the main results by making some approximations.

Neglecting the losses in the inductors, the oscillation frequency ω is given by

$$(L_1 + L_2)C\omega^2 = 1. \tag{10}$$

The voltage gain between v_x and v_{out} at the resonant frequency ω is

$$\frac{v_{out}}{v_x} = \frac{(L_1 + L_2)}{L_1}. \tag{11}$$

In view of the above voltage gain, the circuit can start up oscillations with a transistor gain v_x/v_{in} lower than unity provided that it is higher than $L_1/(L_1 + L_2)$. Thus, the minimum transistor gain necessary to start up oscillations is

$$A_v = \frac{v_x}{v_{in}} = \frac{L_1}{L_1 + L_2}. \tag{12}$$

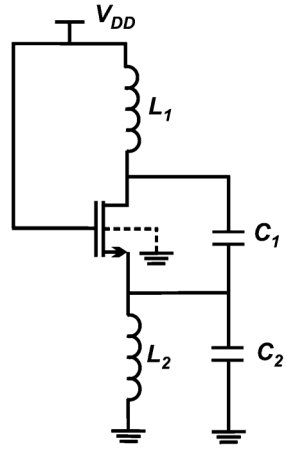

Fig. 5. Enhanced swing Colpitts oscillator (ESCO).

The supply voltage required to start up oscillations, calculated from (9) and (12), is

$$V_{dd}(\min) > \phi_t \ln\left(1 + n\frac{L_1}{L_1 + L_2}\right). \tag{13}$$

If $L_2 \gg L_1$, the voltage gain of the transistor can be (much) lower than unity. Thus, the ES inductive-load ring oscillator is capable of oscillating at supply voltages well below the thermal voltage, as we will show in the results of Section V.

IV. The Enhanced Swing Colpitts Oscillator (ESCO)

From the study on the previous ring oscillators we can conclude that a good practice for ultra-low-voltage oscillators is the choice of a topology that allows both the application of all the available voltage bias to the transistors and the boosting of the oscillation amplitude beyond the supply rails. A Colpitts oscillator appropriate for ultra low voltage is simply obtained through substitution of the DC current source of the conventional Colpitts oscillator by an inductor, as shown in Fig. 5. This topology is known as the enhanced swing Colpitts oscillator (ESCO) [20] and its small-signal model is shown in Fig. 6. Note that the transistor capacitance C_{gs} is absorbed by C_2. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

To calculate the common-gate voltage gain we can proceed as follows. Following an inspection of the small-signal equivalent circuit of Fig. 6 we obtain

$$-V_d(s)\left(G_1 + \frac{1}{sL_1}\right)\Big|_{s=j\omega} = V_s(s)\left(G_2 + \frac{1}{sL_2} + sC_2\right)\Big|_{s=j\omega} \tag{14}$$

where V_d and V_s are the small-signal voltages at the drain and source, respectively. Assuming that the Q values of the LC tanks are high at the resonant frequency ω, the relationship between the source and drain voltages calculated from (14) is

$$\frac{V_d}{V_s} = a \cong -\frac{L_1}{L_2}(1 - \omega^2 L_2 C_2) = \frac{C_2}{C_{eq}} - \frac{L_1}{L_2} \tag{15}$$

where C_{eq} is calculated in Appendix D. The value of a, calculated from (D4) and (15), is given by

$$a = u + \sqrt{u^2 + \frac{L_1}{L_2}} \tag{16}$$

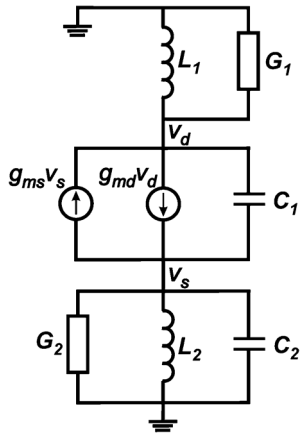

Fig. 6. Schematic diagram of the ESCO small-signal model.

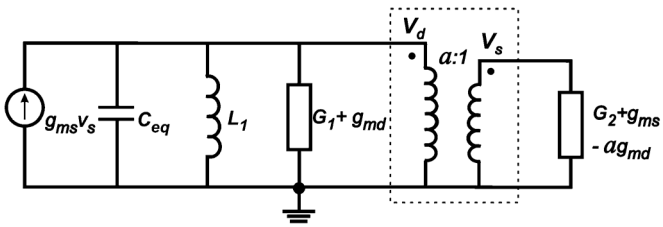

Fig. 7. ESCO with capacitive divider modeled as a transformer.

where

$$u = \frac{1}{2}\left(1 + \frac{C_2}{C_1} - \frac{L_1}{L_2}\right). \tag{17}$$

The value of a in (16) is always greater than unity. Note that for $L_2 \to \infty$ the value of a is

$$a_{L_2 \to \infty} = 1 + C_2/C_1 \tag{18}$$

which is the result for the conventional Colpitts oscillator.

To achieve high swing with low supply voltages, the value of a must be relatively close to unity, i.e. $C_2/C_1 \ll 1$. In this case (16) can be approximated as

$$a_{C_2 \ll C_1} = 1 + \frac{\frac{C_2}{C_1}}{1 + L_1/L_2} \tag{19}$$

Another interesting case is $L_1 = L_2$. In this case (16) reduces to

$$a_{L_1=L_2} \cong \frac{C_2}{2C_1} + \sqrt{1 + \left(\frac{C_2}{2C_1}\right)^2} \tag{20}$$

where, for small capacitive ratios, C_2/C_1, becomes

$$a_{L_1=L_2} \cong 1 + \frac{C_2}{2C_1}. \tag{21}$$

After having calculated the value of a, we now model the oscillator circuit, as shown in Fig. 7[21].

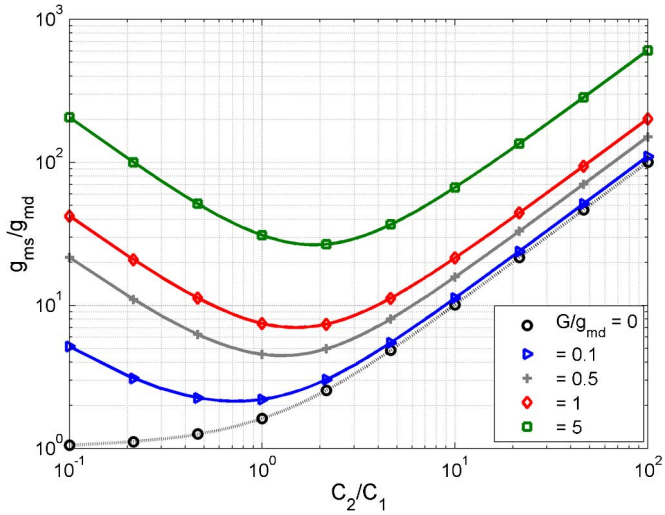

Fig. 8. Minimum transistor intrinsic gain (to start up oscillations) versus C_2/C_1 ratio for $L_1 = L_2$, with G/g_{md} as a parameter.

A. Minimum Transistor Gain and Supply Voltage Required for Oscillation Startup

For the occurrence of oscillation, the transistor must be able to compensate the losses of the passive components. In other words, reflecting to the primary winding the conductance connected to the secondary winding, the requirement for oscillation is written as

$$g_{ms}V_s = g_{ms}\frac{V_d}{a} > \left[G_1 + g_{md} + \frac{1}{a^2}(G_2 - ag_{md} + g_{ms})\right] V_d \tag{22}$$

or equivalently

$$g_{ms} > ag_{md} + \frac{a^2 G_1}{(a-1)} + \frac{G_2}{(a-1)}. \tag{23}$$

The curves in Fig. 8 represent the minimum gain g_{ms}/g_{md} calculated from (23) for the case in which $G_1 = G_2 = G$.

As is clear from Fig. 8, there is an optimum value of the voltage gain a that minimizes the transconductance required for oscillation. The value a_{opt} that minimizes the right-hand side of (23) is

$$a_{opt} = 1 + \sqrt{\frac{G_1 + G_2}{G_1 + g_{md}}}. \tag{24}$$

Let us now consider some particular cases of interest. For the classical Colpitts oscillator, in which the transistor operates in saturation, G_2 and g_{md} can be neglected. Thus, (23) reduces to

$$g_{ms} > \frac{a^2 G_1}{(a-1)} \tag{25}$$

while (24) gives $a_{opt} = 2$. Consequently, the source transconductance necessary for oscillation is, at least, $4G_1$. Thus, the voltage gain g_{ms}/G_1 must be greater than 4 and, from (18), $C_1 = C_2$, which is the well-known result for the classical Colpitts oscillator [22].

In the hypothetical case of ideal inductors ($G_1 = G_2 = 0$) it follows from (23) that

$$\frac{g_{ms}}{g_{md}} > a. \tag{26}$$

Thus, the open-loop gain (g_{ms}/g_{md} times $1/a$) must be greater than unity. It is important to note that g_{ms}/g_{md}, which is the intrinsic gain of the transistor operating in the common gate topology, is always greater than unity, as is clear from (6).

This remarkable property of the common-gate amplifier is essential for lowering the supply voltage limit for the operation of oscillators as we will see in the following.

For $C_2/C_1 \ll 1$, it follows from (19) and (26) that

$$\frac{g_{ms}}{g_{md}} > a = 1 + \frac{\frac{C_2}{C_1}}{1 + L_1/L_2}. \tag{27}$$

Assuming, as in the previous section, that the MOSFET operates in the subthreshold region, we can combine (6) and (26) to obtain

$$\frac{V_{DS}}{\phi_t} = \ln\left(\frac{g_{ms}}{g_{md}}\right) > \ln a. \tag{28}$$

Now, substituting (27) into (28), we obtain

$$\frac{V_{dd}(\min)}{\phi_t} > \ln\left(1 + \frac{\frac{C_2}{C_1}}{1 + L_1/L_2}\right) \cong \frac{\frac{C_2}{C_1}}{1 + L_1/L_2}. \tag{29}$$

Theoretically, as (29) shows, the ESCO can oscillate at very low supply voltages. In practice, however, the unavoidable losses, the parasitic capacitance of the drain node, and operation of the transistor in moderate or strong inversion will contribute to increasing the value of V_{DD} given by (29).

Some simulated and experimental results for the minimum supply voltage, including losses and considering the transistor operation in moderate inversion, will be given in Section VI.

V. Experiments With the Ring Oscillator

Meindl's formula for $V_{dd}(\min)$ as well as the theoretical analysis of the previous sections does not include the threshold voltage V_T of MOS transistors. In effect, the minimum supply voltage is related to the fundamental (exponential) nonlinearity of the transistors and the threshold voltage is not involved at all. However, clearly, the threshold voltage of the transistors has enormous importance in the design of all kinds of circuits, since the current drive capability of transistors is dependent on it. In our prototypes we used native (zero-V_T MOSFETs) because they are usually available in modern technologies and they have high drive capability and sufficient voltage gain at very low supply voltages, since they operate in weak inversion. Concerning the inductors in this study, we used off-the shelf inductors with high quality factors since our goal here is to arrive at the minimum supply voltage. Due to the reduced quality factor of the integrated inductors available, the minimum supply voltage for the integrated prototypes we worked on is above the thermal voltage [23].

We built a prototype of a two-stage ES inductive-load ring oscillator with off-the-shelf inductors and zero-V_T transistors

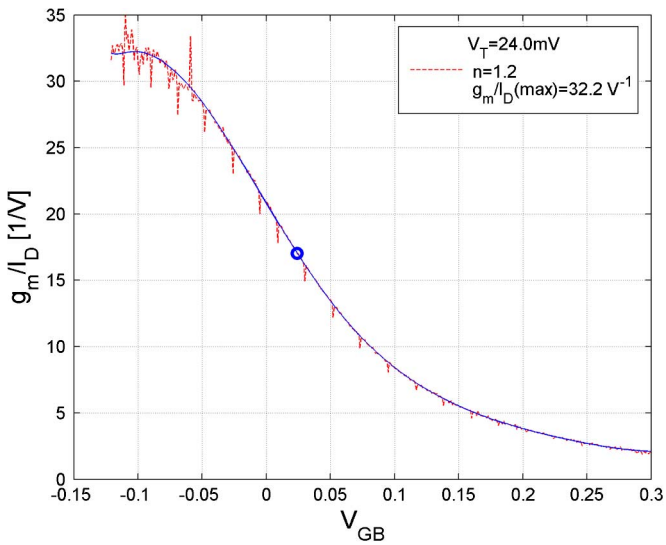

Fig. 9. g_m/I_D curve used to extract the main static MOSFET parameters.

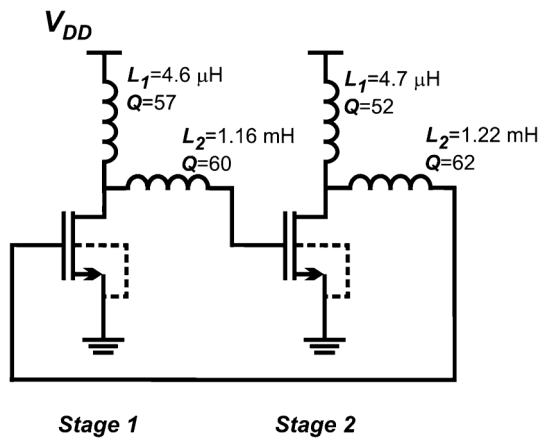

Fig. 10. The ES inductive-load ring oscillator with values for the passive components characterized at 1 MHz.

with aspect ratio $\mathrm{W/L} = 1500\ \mu\mathrm{m}/0.42\ \mu\mathrm{m}$ integrated in a 0.13 μm CMOS process. Using a semiconductor parameter analyzer (Agilent 4156C), the main transistor parameters were measured from the transconductance-to-current ratio curve [24] shown in Fig. 9. The oscillator circuit, along with the values for the inductor parameters, is shown in Fig. 10.

The prototype oscillates at approximately 1.1 MHz for a supply voltage of 3.7 mV, as shown in Fig. 11. Note the extremely high swing voltages at the outputs. The different magnitudes of the outputs are a consequence of the mismatch between inductors.

Fig. 12 illustrates the variation in the amplitude of the gate voltage in terms of the supply voltage. The curves that represent the measured values are very close to those obtained for the simulated values. Simulation results in this paper were run in Spectre, the circuit simulator of Cadence.

Fig. 13 shows a picture of the discrete prototype of the enhanced-swing inductive-load ring oscillator. In this experiment, the startup supply voltage is slightly less than 3.5 mV.

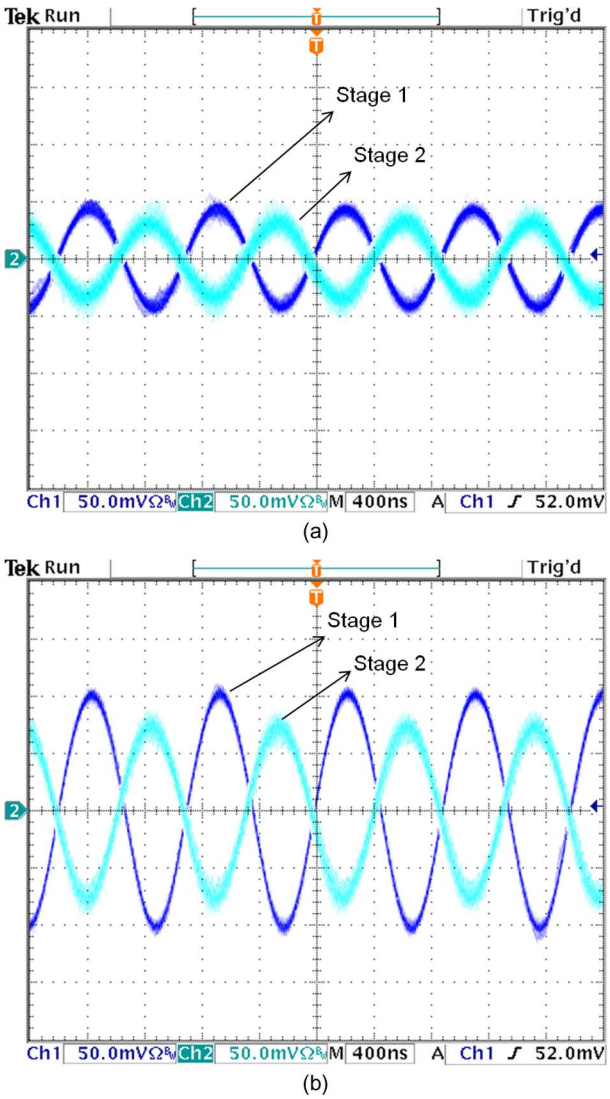

Fig. 11. Experimental gate voltages of the two-stage ES inductive-load ring oscillator built with the transistors characterized in Fig. 9 and inductors with the parameters given in Fig. 10. (a) $V_{dd} = 3.7$ mV, (b) $V_{dd} = 4.7$ mV.

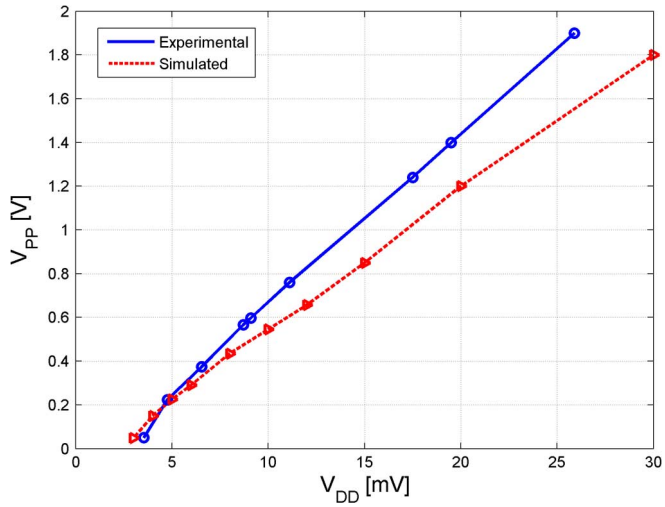

Fig. 12. Simulated (dotted line) and experimental (solid line) peak-to-peak gate voltage versus supply voltage of the ES inductive-load ring oscillator.

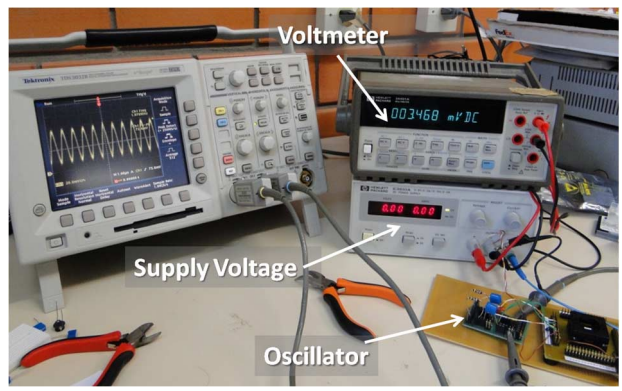

Fig. 13. Picture showing the discrete prototype of the enhanced swing inductive-load oscillator and test equipment.

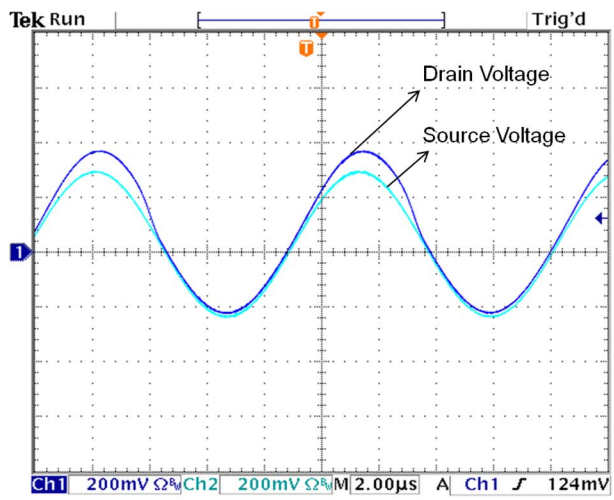

Fig. 14. Experimental drain and source voltages of the ESCO of Fig. 5 for $V_{dd} = 25$ mV, $L_1 = L_2 = 9.8$ nH, $C_1 = 1.54$ nF, $C_2 = 0.44$ nF and temperature around 23°C.

VI. Experiments With the Colpitts Oscillator

We built a prototype of the ESCO with off-the-shelf passive components and a zero-V_T transistor in 0.13 μm CMOS technology (but not from the same run as the transistors used for the ring oscillator) with aspect ratio $W/L = 2500\ \mu m/0.42\ \mu m$. The main transistor parameters are $V_T = -10$ mV, and $n \cong 1.17$. The oscillator circuit is shown in Fig. 5. The values measured for the inductances at 100 kHz were both equal to 9.8 mH with quality factors of around 90. With $C_2 = 440$ pF and $C_1 = 1.54$ nF, the prototype of Fig. 5 oscillates at around 108 kHz, which is very close to the theoretical frequency of oscillation of 112 kHz calculated from (D3) and (D4). The experimental waveforms of both drain and source voltages for $V_{dd} = 25$ mV are shown in Fig. 14.

Note that the drain and source voltages are almost in-phase signals, the drain voltage being slightly distorted.

Circuit simulations were run for the ESCO in Fig. 5 in order to find the minimum supply voltage required for sustained oscillations. The values of the components are those given in this section, except for C_1 and C_2, whose values were chosen to ensure an oscillation frequency of the order of 110 kHz for a given C_2/C_1 ratio. The quality factor of the capacitors is around

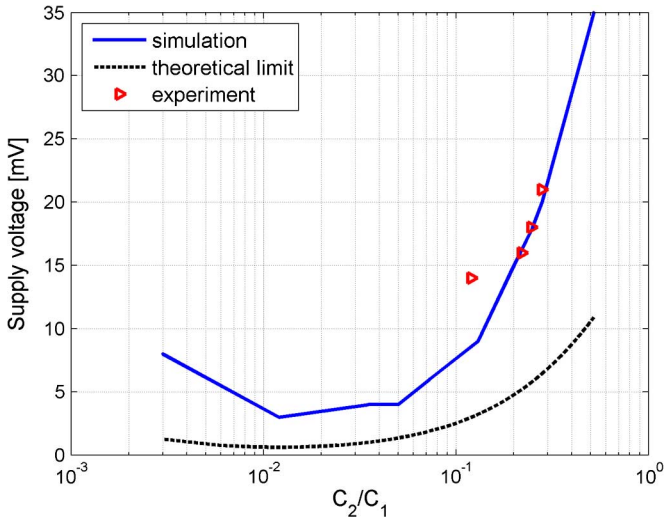

Fig. 15. Minimum supply voltage for sustained oscillations versus C_2/C_1 of the ESCO in Fig. 5. Values of components are given in the text. The theoretical limit derived from (23), with a as given by expression (16), is $V_{dd}(\min)/\phi_t = \ln[a + ((a^2G_1 + G_2)/g_{md}(a-1))]$.

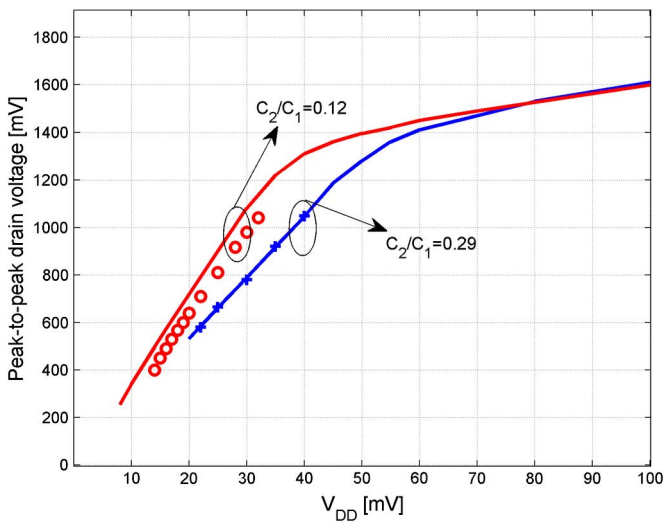

Fig. 16. Simulated (solid lines) and experimental (symbols) peak-to-peak drain voltage versus supply voltage for $C_2/C_1 = 0.29$ and 0.12.

2,000. The MOS transistor, previously described in this text, was the same for all simulations.

Fig. 15 shows the simulation results for the minimum supply voltage of the ESCO which ensures sustained oscillations. Note that, in this particular case, losses of the passive components do not play an important role, except for very low C_2/C_1 ($a \to 1$) ratios, below approximately 10^{-2}. This can be explained with the help of expression (23), which indicates that for G_1 and $G_2 \ll g_{md}$ the ratio g_{ms}/g_{md} is almost independent of G_1 and G_2, except for $a \to 1$.

Four experimental values, $C_2/C_1 = 0.12$, 0.22, 0.25, and 0.29, represented by triangular symbols, show acceptable agreement with the simulation results.

Note that for the $C_2/C_1 = 0.12$ circuit oscillations in the circuit prototype were sustained at a supply voltage of only 15 mV, with the simulation indicating a supply voltage of 8 mV.

TABLE I
EXPERIMENTAL RESULTS FOR THE OSCILLATION FREQUENCY AND MINIMUM SUPPLY VOLTAGE OF THE OSCILLATOR TOPOLOGIES

Topology	Theoretical V_{dd} (min) *	IC prototype 130nm CMOS		Discrete prototype	
		V_{dd} (min)	f_{osc}	V_{dd} (min)	f_{osc}
ILRO	$\phi_t \ln(1+n)$	53 mV	550 MHz	50 mV	11 MHz
ESILRO	$\phi_t \ln\left(1+n\frac{L_1}{L_1+L_2}\right)$	30 mV+	400 MHz	3.5 mV	1.1 MHz
ESCO	$\phi_t \ln\left(1+\frac{C_2/C_1}{1+L_1/L_2}\right)$	86 mV	700 MHz	15 mV	108 kHz

* For lossless passive devices and operation of MOSFETs in weak inversion
+ Post-layout simulation
ILRO, ESILRO, and ESCO refer to inductive-load ring, enhanced swing inductive-load ring, and enhanced swing Colpitts oscillators, respectively.
Values of components:
ILRO – IC prototype – L = 100 nH, Q = 8.
ILRO – discrete prototype – L = 4.6 uH, Q = 50.
ESILRO – IC prototype – L_1 = 20 nH, Q_1 = 9; L_1 = 80 nH, Q_2 = 8.
ESILRO – discrete prototype – L_1 = 4.6 uH, Q_1 = 55, L_2 = 1.2 mH, Q_2 = 60.
ESCO – IC prototype – L_1 = 13.6 nH, Q_1 = 13.9, L_2 = 24.2 nH, Q_2 = 13.3, C_1 = 6 pF, C_2 = 3.5 pF.
ESCO – discrete prototype – $L_1 = L_2$ = 9.8 mH, $Q_1 = Q_2$ = 80, C_1 = 1.54 nF, C_2 = 0.44 nF.

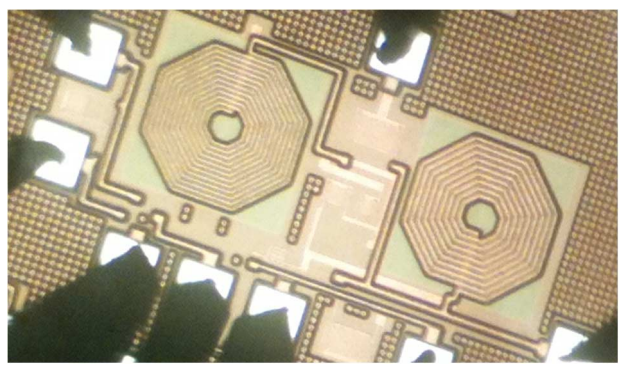

Fig. 17. Micrograph of the ESCO integrated in 130 nm technology.

The dotted line indicates the theoretical limit for transistor operation in weak inversion, with $n = 1$.

Fig. 16 illustrates the variation in the amplitude of the drain voltage in terms of the supply voltage. Once again the curves which represent the measured values are close to those obtained for the simulated values. For supply voltages higher than 40 mV, the source and drain voltages become significantly distorted.

Table I summarizes the main results of this work. The second column gives the theoretical values of $V_{dd}(\min)$ for the three oscillator topologies for the case of lossless passives and MOSFET operation in weak inversion. The layout of the integrated ESCO is shown in Fig. 17.

It is interesting to note that, for both the ESILRO and the ESCO, low ratios between the values for the energy storage devices, either capacitors or inductors, can lead to very low $V_{dd}(\min)$, which is feasible with discrete components, but can be hard to achieve in integrated implementations. The minimum $V_{dd}(\min)$ of both the discrete and integrated (post-layout simulation) oscillators were achieved in the ESILRO. The latter

result suggests that an integrated ESILRO can be used for the starting up of circuits where the primary source of energy is, for example, a thermoelectric generator attached to the human body [27].

Due to the high-drive current of zero-V_t transistors even at low supply voltages, the oscillation frequency of the integrated oscillators can be quite high, as shown in Table I. The maximum oscillation frequency is limited by the transistor f_{max}, which is the frequency at which the maximum available power gain equals unity. It has been shown in [15] that the intrinsic cutoff frequency f_t of a minimum length ($L = 0.42$ um) zero-V_t transistor in a 0.13 um technology is in the range of 100 MHz–1 GHz for a gate-source voltage between 10 and 100 mV. Roughly, $\boldsymbol{f_{\max}/f_t \approx 1/2\sqrt{2\pi f_t R_g C_{gd}}}$, where the product of R_g, the gate resistance, and C_{gd}, the gate-to-drain capacitance, is relatively insensitive to bias. Since in a transistor with an optimized number of fingers at low currents we have $\boldsymbol{2\pi f_t R_g C_{gd} \ll 1}$, we expect the f_{max} of a zero-V_t transistor of a 130 nm process to be of the order of 10 times higher than f_t, i.e. some GHz for the supply voltage range of 10 to 100 mV.

VII. Applications

DC voltages supplied by energy harvesters such as body-worn thermoelectric generators or photovoltaic cells in dark rooms are typically of the order of some tens of mV. Therefore, a DC-DC boost converter is necessary to provide an output voltage of around 1 V to supply the electronic circuitry of currently used technologies. A major design challenge in boost converters of very low-voltage input is the generation of oscillations to turn on and off a MOS switch. Some startup solutions have recently been proposed for harvested inputs in the tens of mV range. Such solutions use transformers [12], previously charged capacitors or batteries [26], mechanical switches [27], or an oscillator tuned after fabrication [28]. The startup solutions devised in [26]–[28] require an external energy storage component, a MEMS switch, or an additional process for the tuning of the threshold voltage. More recently, a fully electrical startup for a 50-mV batteryless boost converter was presented [29]. The startup oscillator circuit employs cross-coupled native NMOS transistors and surface-mount inductors. Table II gives a comparison of the values for minimum startup supply voltages in some representative papers available in the technical literature.

The aim of the analysis of the ULV oscillators reported herein is to provide solutions for startup circuits in energy harvesters whose DC input is of the order of some tens of mV. In addition, we propose that the ULV oscillators could also be used in combination with a voltage multiplier to directly supply electronic circuitries.

VIII. Conclusions

Electronic circuits are dependent on voltage gain to operate properly. Voltage gain, a consequence of the nonlinearity of transistors, requires a minimum supply voltage to emerge with the necessary strength. For ideal MOS transistors ($n = 1$) operating in weak inversion in the common-source configuration, the intrinsic gain equals unity for $V_{ds} = (\ln 2)kT/q$, but the intrinsic gain of the common-gate configuration is always greater than unity. MOSFET oscillators, when appropriately designed, can operate with supply voltages well below $(\ln 2)kT/q$. One option to this end is to use the MOSFET in the common-gate configuration, as is the case of the ES Colpitts oscillator. A second option is to use the transistor in the common-source topology and boost the voltage gain with the appropriate inductive load, as is the case of the enhanced swing inductive-load ring oscillator. Concerning the implementation of ultra-low-voltage oscillators, we propose the use of native (zero-V_T) MOSFETs and high-quality-factor inductors for operation with supply voltages below the thermal voltage.

TABLE II
Comparison of Recently Reported Minimum Startup Supply Voltages for Oscillators

Ref.	Start up solution	Process	Minimum start up voltage
[12]	External transformer	0.13 µm	40 mV
[26]	Capacitor or previously charged battery	0.13 µm	600 mV
[27]	Mechanical switch	0.35 µm	35 mV
[28]	Post-layout hot carrier injection to adjust threshold voltage	65 nm	80 mV
[29]	External SMD inductor	65 nm	50 mV
This study	ESCO (integrated transistors + off-the-shelf components)	0.13 µm	15 mV
	ESILRO (integrated transistors + off-the-shelf components)	0.13 µm	3.5 mV

Appendix A

Fundamentals of the Model of the Mosfet Operating in the Triode Region in Weak Inversion [24], [25]

In the triode region, in weak inversion, the drift current is negligible, and the diffusion current is proportional to the carrier density gradient $(Q'_{IS} - Q'_{ID})/L$, where Q'_{IS} is the inversion charge density at the source, Q'_{ID} is the inversion charge density at the drain, and L is the channel length.

For an NMOS transistor the drain current is given by

$$I_D = -W\mu\phi_t \frac{Q'_{IS} - Q'_{ID}}{L}. \tag{A1}$$

where W is the channel width, μ is the carrier mobility, ϕ_t is the thermal voltage and, interestingly, $\mu\phi_t$ is the diffusion coefficient.

In weak inversion the inversion charge density is an exponential function of the applied voltages as shown below

$$Q'_{IS(D)} = Q'_{I0} e^{\left(\frac{V_G - V_T}{n\Phi_i} - \frac{V_{S(D)}}{\Phi_i}\right)}. \tag{A2}$$

$(V_G - V_T)/n$ can be regarded as the effective gate voltage at the channel. n is called the slope factor and represents the capacitive divider comprised of the oxide and depletion capacitances. The pre-exponential factor is independent of the applied

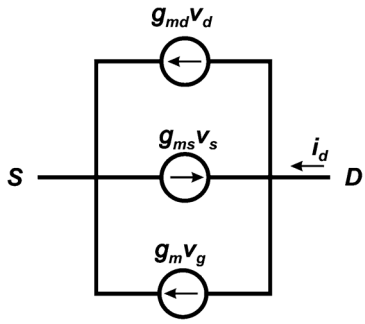

Fig. A1. Small signal model of the MOSFET. Voltages are referenced to bulk.

voltages. We can calculate the source, drain and gate transconductances from (A1) and (A2) as

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = -\mu \frac{W}{L} Q'_{IS}, \tag{A3}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = -\mu \frac{W}{L} Q'_{ID}, \tag{A4}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = -\mu \frac{W}{L} \frac{Q'_{IS} - Q'_{ID}}{n} = \frac{g_{ms} - g_{md}}{n}. \tag{A5}$$

From (A2), (A3), and (A4) it follows that

$$\frac{g_{ms}}{g_{md}} = e^{\frac{V_{DS}}{\phi_t}}. \tag{A6}$$

The small signal model of the MOSFET is shown in Fig. A1.

Appendix B

Oscillation Frequency of the Inductive-Load Ring Oscillator

We can rewrite (3) as

$$\frac{\omega}{\omega_o} = \sqrt{1 + \frac{(\tan\phi)^2}{4Q^2}} - \frac{\tan\phi}{2Q} \tag{B1}$$

where $\omega_o = 1/\sqrt{LC}$ is the equivalent LC resonant frequency of a single stage, and, $Q = 1/(g_{md} + G_P)\omega_o L$ is the quality factor. Note that when the condition $\phi = \pi$ holds, which is the case for an even number of stages, ω equals ω_o.

The dispersion relation of a stage, which shows the dependence of ω/ω_o for any ϕ, is shown in [23].

The condition of loop gain equal to unity for oscillation requires the phase shift ϕ between two adjacent stages to be $\phi = 2k\pi/N$, where N is the number of stages and k is an integer number. Except for $N = 2$ and 4, more than a single value for the phase shift satisfies the phase condition required for oscillation, as shown in Fig. B1. However, as explained in [18], the circuit will oscillate at the frequency for which the gain is higher. For an even number of stages we have $\phi = \pi$, while for the case of an odd number of stages $\phi = (N-1)\pi/N$.

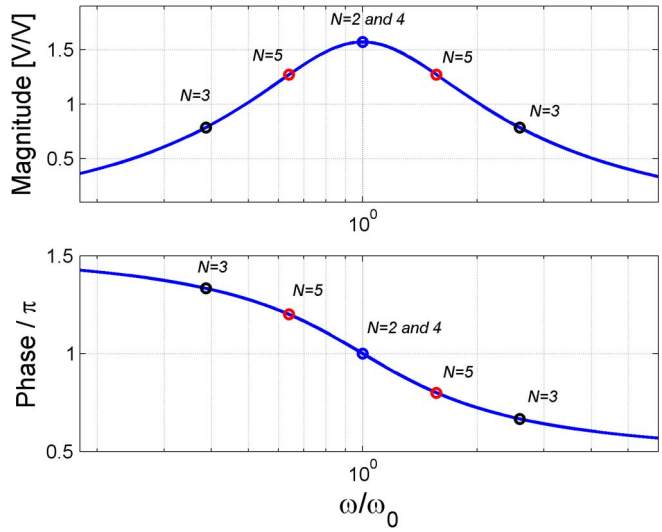

Fig. B1. Magnitude and phase, (2) and (3), of the transfer function of a single stage of the inductive-load ring oscillator.

Appendix C

Oscillation Frequency of the ES Inductive-Load Ring Oscillator

The transfer function of the single stage circuit in Fig. 4 is

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{sC + \left(g_{md} + G_{p1} + \frac{1}{sL_1}\right)(L_2 C s^2 + R_{S2} C s + 1)} \tag{C1}$$

or

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{(g_{md} + G_{p1})(1 - L_2 C\omega^2) + \frac{R_{S2}C}{L_1}} \frac{1}{1 - j\tan\phi} \tag{C2}$$

The phase shift ϕ between V_{out} and V_{in} calculated from (C1) is

$$\phi = \pi - \tan^{-1}\left(\frac{[L_1 + L_2 + L_1 R_{S2}(g_{md} + G_{P1})]\, C\omega^2 - 1}{(g_{md} + G_{P1})\omega L_1 (1 - L_2 C\omega^2) + R_{S2} C\omega}\right). \tag{C3}$$

Considering, for the sake of simplicity, the case of a ring oscillator with an even number of stages ($\phi = \pi$), we can calculate the oscillation frequency from (C3) as

$$\omega = \frac{1}{\sqrt{[L_1 + L_2 + L_1 R_{S2}(g_{md} + G_{P1})]\, C}} \tag{C4}$$

Finally, for lossless inductors, (C4) reduces to

$$\omega = \frac{1}{\sqrt{(L_1 + L_2)C}}. \tag{C5}$$

The greater-than-unity gain required to start up oscillations is achieved for

$$g_m > \left[(g_{md} + G_{P1})(1 - L_2 C\omega^2) + \frac{R_{S2}C}{L_1}\right] \sqrt{1 + (\tan\phi)^2}. \tag{C6}$$

As for the first ring oscillator, let us consider, for the sake of simplicity, the case of an even number of stages ($\phi = \pi$). Writing g_m in terms of g_{ms} and g_{md} we obtain

$$\frac{g_{ms}}{g_{md}} > \left[1+n(1-L_2C\omega^2)\right] + \frac{n}{g_{md}}\left[G_{p1}(1-L_2C\omega^2)+\frac{R_{S2}C}{L_1}\right] \tag{C7}$$

Neglecting the losses in the inductors and considering the resonant frequency approximated by (C5)

$$\frac{g_{ms}}{g_{md}} > 1 + n\frac{L_1}{L_1+L_2} \tag{C8}$$

Finally, combining (6) and (C8) gives

$$V_{dd}(\min) > \phi_t \ln\left(1 + n\frac{L_1}{L_1+L_2}\right) \tag{C9}$$

Appendix D

Oscillation Frequency of the ES Colpitts Oscillator

For the sake of simplicity, let us assume that the ESCO oscillation frequency is independent of both losses and transistor parameters. The oscillation frequency can be calculated (see Fig. 6) as the resonance frequency of the equivalent LC tank composed of inductor L_1 and an equivalent capacitance C_{eq} given by

$$C_{eq} = \frac{C_1 C_2'}{C_1 + C_2'} \tag{D1}$$

where

$$C_2' = C_2 - \frac{1}{\omega^2 L_2} \tag{D2}$$

is the capacitance equivalent to the L_2C_2-tank at the oscillation frequency ω, which is such that

$$\omega^2 L_1 C_{eq} = 1. \tag{D3}$$

The value of the equivalent capacitance is found from (D1), (D2) and (D3). After some algebra we have

$$C_{eq} = \frac{(C_1+C_2)\frac{L_2}{L_1} + C_1 - \sqrt{\left[(C_1+C_2)\frac{L_2}{L_1} - C_1\right]^2 + 4\frac{L_2}{L_1}C_1^2}}{2}. \tag{D4}$$

In fact, two solutions can be found for the equivalent capacitance; however, only the lower capacitance, which is associated with the higher frequency of oscillation, is possible. The reason for this is that the loop gain will be negative for the lower frequency; thus, the circuit cannot oscillate at the lower frequency.

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