A DIGITALLY PROGRAMMABLE CURRENT SCHMITT-TRIGGER

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Abstract

This work presents a new compact structure for a digitally programmable current Schmitt-trigger comparator, which is compatible with VLSI processes and allows low-voltage operation. The digital programmability is achieved by means of MOSFET-only current dividers. The effects of offset voltages and limited frequency response of opamps's on the accuracy of the comparator are shown.

1.Introduction

The development of basic circuit cells is very important to decrease the development time of more complex systems. Comparators can be seen as a class of these cells.

Schmitt-triggers are often used because of its property of eliminating the comparator chatter. Current Schmitt-triggers are particularly useful in photo detectors, optic remote control and medical instruments [1].

This work presents a new compact structure for a digitally programmable current Schmitt-trigger comparator, which is compatible with VLSI processes. Several different current comparators structures have already been presented [2-5]. Some of them operate at high speed [2, 3], others present high accuracy or are offset-free [2, 4, 5], but none of them have the digital programming characteristic. Combined with self-adaptive structures, this comparator can achieve high speed and high accuracy.

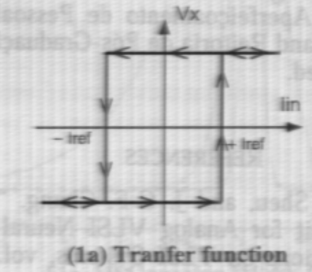
This paper is organized as follows. Section 2 presents the basic non-programmable structure of the Schmitt-trigger comparator. In section 3, we show how to program the Schmitt-trigger by means of MOSFET-only current dividers. In section 4, we analyze the effects of offset voltages and frequency response of opamp's on the accuracy of the comparator. Simulation results are shown in section 5.

2. The basic structure of the comparator

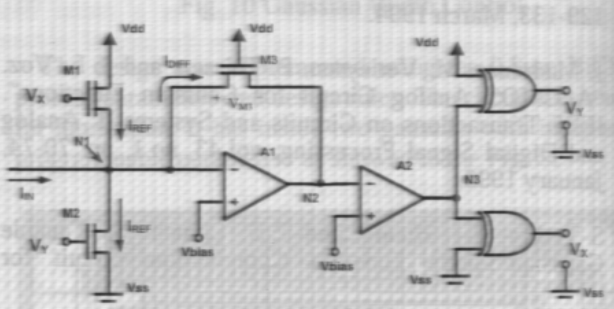
The basic non-programmable structure of the proposed Schmitt-trigger can be seen in Fig. 1.

The bias voltage V_{BIAS} is such that it allows maximum current swing through M_3. It also guarantees the drain currents I_{D_M1} and I_{D_M2}, through M1 and M2 respectively, to have the same magnitude, equal to I_{REF} [6,8]. Thus:

$$I_{D\_M1} = I_{D\_M2} = I_{REF} \qquad (1)$$



(1a) Tranfer function



(1b) Electrical scheme

Fig. 1: Non-programmable Schmitt-trigger.

The circuit that generates V_{BIAS} is a simple series association of two identical transistors as shown in Fig. 2 [8-10].

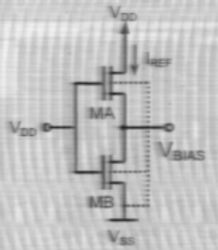


Fig. 2 – Circuit to generate the bias voltage V_{BIAS}.

Transistor M3 was designed to operate in the triode region for an input current below $1.5 \cdot I_{REF}$. Indeed, M3 acts an I-to-V converter.

Now, we can start to analyze the operation of the comparator. The comparator (A2) output changes whenever the current I_{DIFF} equals zero, as can be seen in Fig. 1. Under this condition, voltage V_{M3} is zero, too, and the voltages on the non-inverter and inverter inputs of A2 opamp are the same and equal to V_{BIAS}, driving the comparator to the threshold state.

The current I_{DIFF} is given by (2) and (3), depending on the state of V_X.

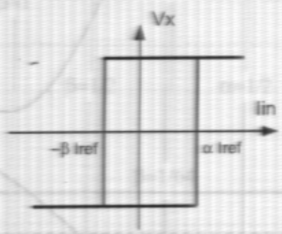
$$I_{DIFF} = I_{IN} + I_{REF}, \qquad \text{if } V_X = \text{HIGH} \qquad (2)$$

$$I_{DIFF} = I_{IN} - I_{REF}, \qquad \text{if } V_X = \text{LOW} \qquad (3)$$

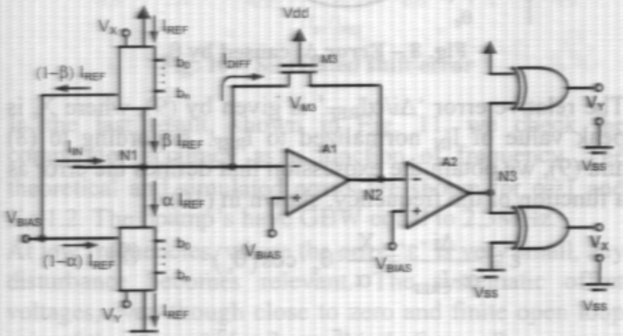
If V_X is on the "high" state, M1 is 'ON' and M2 'OFF'. According to (2), to have $I_{DIFF} = 0$, I_{IN} must be equal to '$-I_{REF}$'. In the same way, when V_X is "low" M2 is 'ON' and M1 is 'OFF'. According to (3), to have $I_{DIFF} = 0$, I_{IN} must be '$+I_{REF}$'. Hence, we obtain a hysteresis loop with the transition points at '$\pm I_{REF}$'.

3. Programmable structure

One can program the Schmitt-trigger if current dividers substitute for transistors M1 and M2 in the circuit shown in Fig. 1. These dividers present an input current equal to 'I_{REF}' and output currents equal to '$\alpha \cdot I_{REF}$' and '$(1-\alpha) \cdot I_{REF}$', where 'α' is digitally controlled by a binary word. Fig 4 illustrates the new hysteresis loop, together with the programmable circuit. Note that 'α' and 'β' are programmed by a digital word.



(4a) Tranfer function



(4b) Electrical scheme

Fig. 4 – Digitally programmable Schmitt-trigger

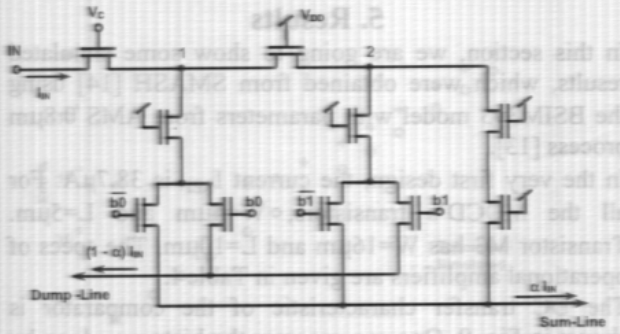


Fig. 5 – 2-bit MOCD

The current divider is a well-known and widely applied network called Mosfet-Only-Current-Divider (MOCD). This current divider was introduced in [11] and it operates similarly to the classic R-2R network. Its principle of operation is detailed in [11, 12]. Fig. 5 shows a single 2-bit network. The terminal labeled V_C can be used as an 'ON/OFF' switch. The voltage at 'sum' and 'dump' terminals must be the same. As previously mentioned, 'α' and 'β' are controlled by binary words applied to the MOS switches in the parallel branches of the MOCD. Equation (4) gives 'α' and 'β', where 'b' is the digital word in base 10 and 'n' is the number of bits.

$$\alpha, \beta = \frac{b+1}{2^n} \qquad (4)$$

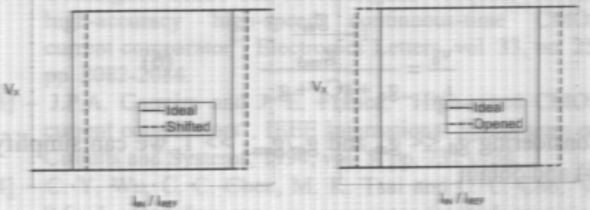
The operational amplifiers of the comparator are Class A Miller opamp's. The main characteristics of the Miller opamp's are shown in Table I. In order to improve the comparator performance, each differential amplifier should have a specific design. A1 should have a very high GBW and A2, which operates as a voltage comparator, must be as fast as possible.

DC gain	97	dB
Gain-Bandwidth Product (GBW)	2.0	MHz
Phase Margin	64	Degree
Maximum Output Current	96	μA
Supply Current	144	μA
Slew Rate	2.3	V/μs
PMOS input pair		

Table I – Characteristics of the Miller opamp

4. Error analysis

One can find two main errors in the hysteresis curve: a right or left shift from the origin and an opening of the hysteresis loop, as depicted in Fig. 6. The first one is caused by an offset current that adds a systematic error to the comparison level for any 'α' or 'β'. Its main error sources are the offset voltages of the opamp's. The second effect is caused by a switching delay between the instants that I_{IN} reaches the comparison level and the actual V_X switching. The phase delay of opamp A1 and the transient response of A2 are responsible for this switching delay, as will be shown in section 4.2.



(6a) Shifted loop **(6b) Opened loop**

Fig. 6 –Graphical representation of the main errors in the hysteresis loop

4.1 Hysteresis loop shift

The offset voltages of both A1 and A2 contribute to the shift of the hysteresis loop. First let us consider only the effect of offset voltage 'V_{OS_1}' of A1. It is easy to see this offset voltage gives rise to an offset current equal to $V_{OS\_1} \cdot g_{ms3}$ through M3, where gms_3 is given by

$$gms_3 = \mu n C'_{OX} \frac{W}{L}\left(\frac{V_{DD} - V_T}{n} - V_{BIAS}\right) \tag{5}$$

On the other hand, assuming the offset voltage of A2 to be 'V_{OS_2}', the switching of V_X occurs at an input voltage of A2 equal to $V_{BIAS}+V_{OS\_2}$. Therefore, an extra current equal to $V_{OS\_2} \cdot g_{ms3}$ through M3 is needed to compensate V_{OS_2}. The combination of the two offset voltages results in an offset current in the hysteresis loop given by $I_{OFF} = (V_{OS\_1} + V_{OS\_2}) \cdot gms_3$.

This error can be minimized with a very careful layout to minimize V_{OS}. Smaller g_{ms3} values would reduce I_{OFF}. However, A1 would saturate for smaller values of I_{IN}. Consequently, the value of g_{ms3} would have to be increased.

4.2 Opening of the hysteresis loop

As mentioned before, the opening of the loop is caused by a switching delay. The two main sources of this error are the finite gain-bandwidth product of A1 and the transient response of comparator A2. The limited frequency response of A1 needs a careful attention because its effect is more difficult to eliminate. To verify the influence of the frequency response of A1, let us consider Fig. 7, which represents a first order AC equivalent of the circuit in Fig. 4. To simplify the analysis, the conversion i_{in} to v_0 is assumed to be linear. Furthermore, the effect of the conductances of the MOCD's in the frequency range that we are interested in is very small owing to the high opamp DC gain.

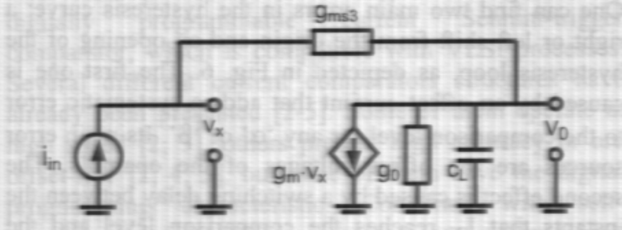


Fig. 7 – Equivalent AC circuit

The transimpedance v_o/i_{in} associated with the circuit in Fig. 7 is given by

$$\frac{v_0}{i_{in}} = \frac{1 - \frac{g_m}{g_{ms3}}}{g_0 + sC_L + g_m} \tag{6}$$

Considering $g_0 \ll g_m$ and $g_m/g_{ms3} \gg 1$, we can simplify (6) and obtain

$$\frac{v_0}{i_{in}} \cong -\frac{1}{g_{ms3}} \cdot \frac{1}{1 + s\frac{C_L}{g_m}} = -\frac{1}{g_{ms3}} \cdot \frac{1}{1 + \frac{s}{2\pi \cdot GBW}} \tag{7}$$

where $GBW = g_m/2\pi \cdot C_L$.

The phase delay (θ_c) of 'v_0' can be measured from the transimpedance phase. From (7) and for small phase values, we have

$$\theta_c = \mathrm{arctg}\left(\frac{f}{GBW}\right) \cong \frac{f}{GBW} \tag{8}$$

Now, we are going to consider the effect of this phase delay on the comparator threshold. Let 'θ_c' be the phase between v_0 and i_{in}, at a specific frequency. The ideal switching occurs when I_{IN} reaches αI_{REF} (βI_{REF}). At this point, V_0 is supposed to be equal to V_{BIAS}. However, V_0 will equal V_{BIAS} a "little bit late" due to the phase delay 'θ_c'. The delay is graphically shown in Fig. 8.

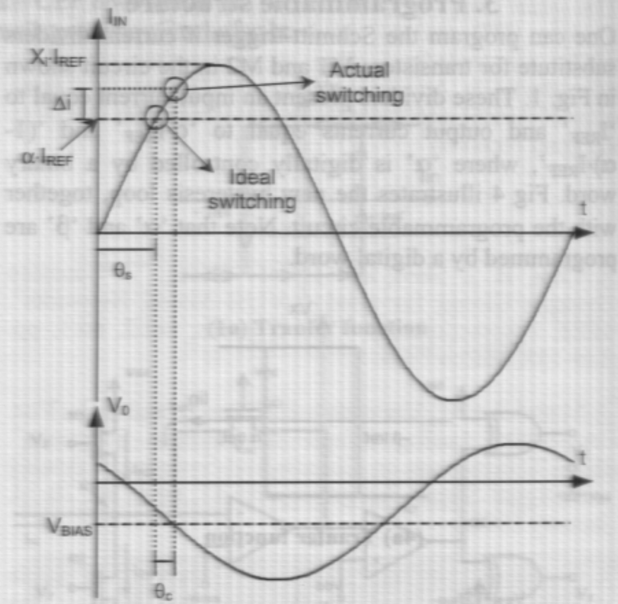


Fig. 8 – Error Δi caused by θ_c

The relative error '$\Delta i/\alpha I_{REF}$' is given by (9), where X_i is peak value of I_{IN} normalized to I_{REF}. According to (8) and (9), we obtain the expression that defines the error as a function of the frequency, shown in (10).

$$\varepsilon \equiv \frac{\Delta i}{\alpha \cdot I_{REF}} \cong \frac{X_i}{\alpha} \cdot \theta_c \cdot \cos(\theta_s) \cdot \tag{9}$$

$$\varepsilon \cong \frac{f}{GBW} \cdot \frac{X_i}{\alpha} \cdot \cos\left[\sin^{-1}\left(\frac{\alpha}{X_i}\right)\right] \tag{10}$$

5. Results

In this section, we are going to show some simulated results, which were obtained from SMASH [14] using the BSIM3v3 model with parameters from AMS 0.8µm process [13].

In the very first design, the current I_{REF} is 38.7µA. For all the MOCD's transistors, W=4µm and L=5µm. Transistor M3 has W=16µm and L=10µm. The specs of operational amplifiers are given in Table I.

The DC transfer characteristic of the comparator is shown in Fig. 9. One can program the histeresys loop by means of 'α' and 'β'.

The second result, shown in Fig. 10, was obtained when an offset of 5mV was introduced in each opamp. The expected shift is 2.8µA. The simulated result (3.3µA) is very close to the theoretical one.

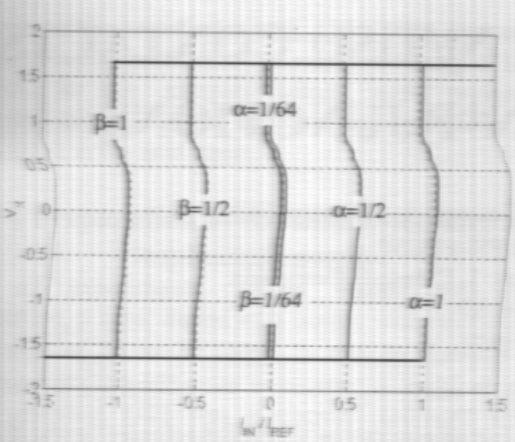


Fig. 9 – DC hysteresis loop

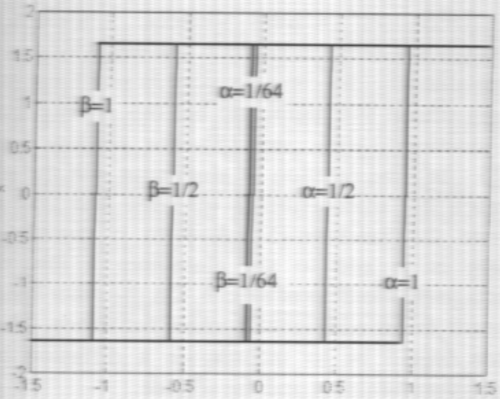


Fig. 10 – Simulated shift error

In the last result, shown in Fig. 11, we check the comparator accuracy as a function of frequency. The theoretical and simulated errors are shown for α=1 and X_i=1.2. The opamp's have GBW equal to 2.3MHz.

At low frequencies, where the error 'ε' is very small, any disturbance becomes relevant. The systematic offset voltages, even though close to zero and finite open loop gain of the opamp's produce a kind of error floor, as can be seen in Fig. 11.

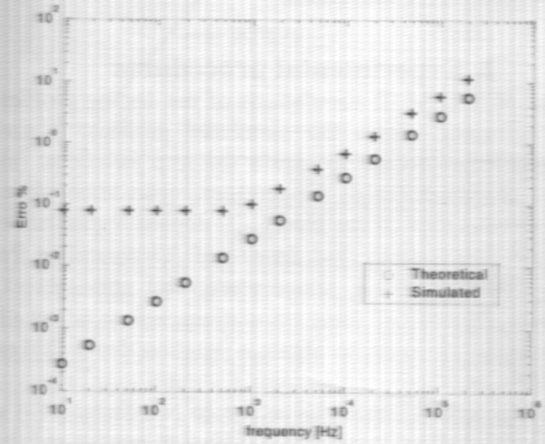


Fig. 11 – The error as a function of frequency

6. Layout

We layed out the circuit on the 0.8µm process from AMS, which is a double-metal/double-poly process. The core area is 0.71mm^2 and 2.37mm^2 with pads. The final layout is shown in Fig. 12.

The design sent to fabrication includes two comparators and a voltage divider implemented with two MOCD's instead of two single transistors.

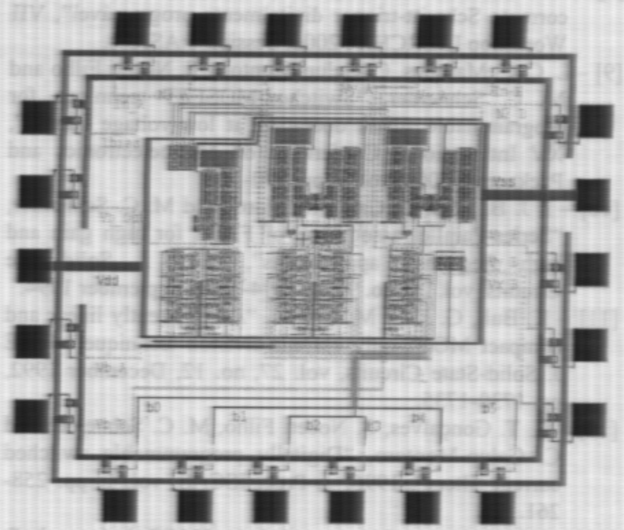


Fig. 12 – Layout of two comparators and a voltage divider

7. Conclusion

A new topology for a current Schmitt-trigger was presented. Its main advantage is the very simple digital programmability. Some simulated results were shown and the concepts were proven. The circuit was layed out and sent to a foundry.

Acknowledgment

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