A Simple Biasing Circuit for Low-Voltage MOS Cascode Current Mirrors at Any Current Level

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Abstract

In this paper we propose a very simple bias circuit that allows for maximum output voltage swing of MOSFET cascode stages. The proposal is valid for any current density being the design equations derived from the current-based MOSFET model developed in [1]. Starting from the saturation voltage and from the current density of the current mirror we determine the aspect ratio of the transistors in the bias circuit in order to optimize the output voltage swing. Experimental results validate the strategy for designing the bias network.

1. Introduction

Low-voltage current mirrors are indispensable building blocks for analog circuits. Even though simple current mirrors allow for high output voltage swing, their low transconductance-to-output conductance ratio precludes them from being used for low voltage applications where a high value of this ratio is mandatory.

Cascode current mirrors (CCM) have a much higher output resistance than simple current mirrors yet at the expense of the output voltage swing. Self-biased CCMs [2, 3] are very simple to design but have as the main drawback a very serious loss of signal swing. Cascode mirrors with fixed bias [4-6] can be optimized for high output voltage swing. The very simple circuits proposed in [6] and [7] to bias cascode mirror are valid either for weak inversion or for strong inversion, respectively, but are no longer valid if the MOS transistors operate in moderate inversion. The cascode biasing circuit proposed in [3] can operate at any current level with a minimal output saturation voltage but spends a lot of silicon area and is not suitable for high frequency applications.

In this paper we extend for moderate and strong inversion the biasing circuit shown in [7], initially proposed for operation in weak inversion. In the first part of the paper we revisit the MOSFET model from [1] and introduce a definition of the saturation voltage based on the needs of circuit designers. Additionally, the small-signal output resistance is discussed and associated with the saturation voltage of the driver transistor in the CCM.The analysis of the biasing topology is discussed next. Design equations as well as experimental results are eventually presented.

2. The Saturation Voltage

According to the MOSFET model in [1], the drain current can be decomposed into the forward (I_F) and reverse (I_R) currents:

$$I_D = I_F - I_R \qquad (01)$$

where $I_F(I_R)$ is dependent of the gate and source (drain) voltages.

In forward saturation, the drain current is almost independent of the drain voltage; therefore, $I_F >> I_R$ and $I_D \cong I_F$.

The MOSFET output characteristic [1] is modeled in normalized form as:

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \qquad (02)$$

where:

$$i_{f(r)} = \frac{I_{F(R)}}{I_S}, \quad I_S = I_{SQ}\left(\frac{W}{L}\right), \quad I_{SQ} = \mu . n . C'_{ox} . \frac{\phi_t^2}{2} \qquad (03)$$

I_S is the specific current, I_{SQ} is the specific sheet current, $i_{f(r)}$ is the normalized forward (reverse) current, ϕ_t is the thermal voltage and "n" is the slope factor. Equations (01) through (03) can be found in [1].

In order to define a saturation voltage that is meaningful for circuit designers, we first define the maximum allowable voltage gain of the common gate amplifier $A = g_{ms}/g_{md}$, where g_{ms} is the source transconductance while g_{md} is the MOSFET output conductance. Indeed, "A" is equal to the ratio of the slope of the transistor output characteristic at the origin ($V_D = V_S$) to the slope of the characteristic for any value of the drain voltage. Clearly, the so-called saturation voltage should be associated with a large value of "A".

From (02) one can easily derive the value of the saturation voltage V_{DSSAT} [1] as:

$$\frac{V_{DSSAT}}{\phi_t} = \ln(A) + \left(1 - \frac{1}{A}\right)\left(\sqrt{1 + i_f} - 1\right) \qquad (04)$$

Note that for large values of "A", $i_f >> i_r$ and, consequently, $i_d \cong i_f$. Therefore, one can substitute i_ϕ, the normalized drain current, for i_f in (04).

This definition of the saturation voltage is very appropriate for building blocks such as current mirrors where swing and voltage gain are essential specifications. Figure 1 illustrates the dependence of the saturation voltage on the inversion level. For strong-inversion $V_{DSSAT} = \phi_t \sqrt{i_f}$, while for weak-inversion $V_{DSSAT} = \phi_t . \ln(A)$.

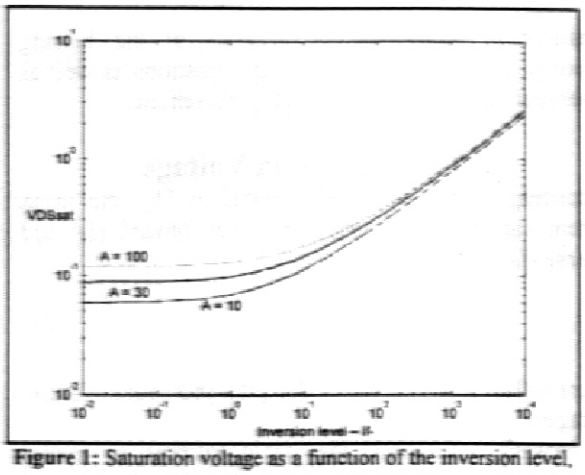

Figure 1: Saturation voltage as a function of the inversion level, gain A as parameter and ϕ_t=26mV.

3. The Output Resistance

Cascode stages are capable of exhibiting very high output resistance and a gain-bandwidth product almost equal to that of a simple stage [8]. With the aid of Figure 2.(a), one can readily determine the output impedance at the drain of M4:

$$\frac{v_{out}}{i_{out}} \cong \frac{g_{ms4}/g_{md4}}{g_{md2}} \qquad (05.a)$$

The result in (05) can be readily interpreted by noting that the drain voltage of M2 is equal to the output voltage divided by the voltage gain of the common-gate configuration. Typically, the output impedance of a cascode stage can be from 10 to 100 times higher than that of a simple stage. Assuming that M2 and M4 to be operating in saturation and to have the same aspect ratios, then $g_{ms4}=g_{ms2}$. Therefore, (05.a) can be written as:

$$\frac{v_{out}}{i_{out}} \cong \frac{g_{ms2}/g_{md2}}{g_{md4}} = \frac{A}{g_{md4}} \qquad (05.b)$$

where "A", the voltage gain of M2 depends on the drain-source voltage, and thus on the bias voltage V_B. Therefore, V_B should be sufficiently high to allow for a high "A" but not too much high to avoid a reduction in the output voltage swing. The following section shows how to optimize the bias network.

4. Bias network

In the topology of the CCM shown in Fig 2(a) all transistors share a common substrate . If V_B is adequately chosen, the output voltage of this circuit can be as low as $2V_{DSSAT}$. Biasing the transistors deep in weak inversion allows for low voltage operation and low power consumption but the frequency response is very poor. A balance between frequency response and voltage swing is achieved in moderate inversion

Two structures proposed to generate appropriate bias voltage for current mirrors, Fig. 2(b) [6] and Fig 2(c) [7], are quite simple but were introduced for operation of transistors in either strong or weak inversion, respectively.

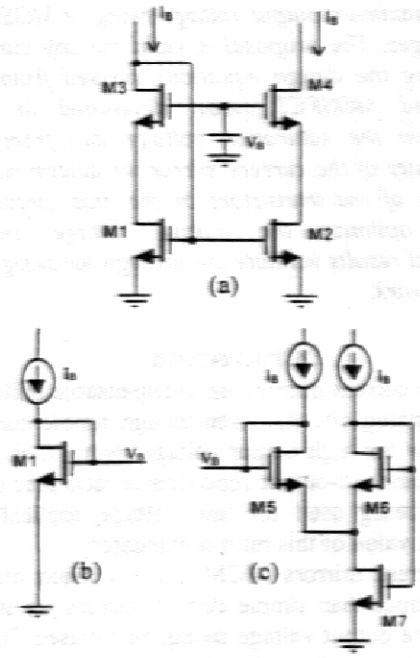

Figure 2: (a) Low-voltage CCM, (b)Biasing circuit [6], (c) Biasing circuit [7]

Our purpose in this work is to extend the application of the circuit in Fig 2(c) to any current level. To better understand the bias network of Figure 2.(c), we have split transistors M5 and M7 into a series association of transistors (MA5 and MB5) and a parallel association of identical transistors (MA7 and MB7), respectively, as shown in Figure 3. The aspect ratios of the transistors in the current mirror are assumed to be equal and are taken as the reference value. We have chosen the aspect ratios of MA5 and M6 to be equal to the reference value and the bias current to be equal to the input current. Therefore, the gate-source voltage of MA5 is equal to the gate-source voltage of M4. Consequently, the sum of the drain-source voltages across MB5 and MB7 equals the drain-source voltage across M2. From now on, to simplify matters, we will

assume that the normalized sheet current I_{SQ} is equal for all transistors, even though it is slightly dependent of the gate voltage. Consequently, we consider the normalized forward currents of M4, MA5 and M6 identical because the three transistors have the same geometry and they are biased at the same current in saturation. Making the aspect ratios $\tau_1=\tau_2=\tau$ and calling $\alpha=(\tau+1)/\tau$, one can readily conclude that $i_{MB5}=i_{MB7}=i_f$, and $i_{MA5}=i_{MB7}=\alpha.i_f$. Here, i_f refers to the inversion level of the CCM transistors, which is almost equal for both M2 and M4 as long as M2 and M4 are operating in the saturation region. From the previous considerations we can derive the following equation:

$$\frac{V_{DSMB5}+V_{DSMB7}}{2\phi_t}=\sqrt{1+\alpha.i_f}-\sqrt{1+i_f}+\ln\left(\frac{\sqrt{1+\alpha.i_f}-1}{\sqrt{1+i_f}-1}\right) \quad (06)$$

In weak inversion ($i_f \to 0$) the second member of (06) can be written as $\ln\alpha$ whereas deep in strong inversion ($i_f \to \infty$) it can be approximated by $\left(\sqrt{\alpha}-1\right)\sqrt{i_f}$.

In order to bias M2 on the verge of saturation, the sum of the drain-source voltages in (06) should be equal to the saturation voltage (V_{DSSAT}) of M2. Equating (04) to (06) allows one to determine the curves shown in figure 4 for different gains. Note from (06) that the choice of "α", which defines the aspect ratio "τ", depends on the inversion level but is independent of the technological parameters. Note also that "τ" is within a range from 0.1 to 0.8 approximately. In strong inversion the optimum value of τ is 0.8 $\left(\sqrt{\alpha}=1.5\right)$. On the other hand, in weak inversion "τ" varies from 0.1 to 0.5, depending on the value of the voltage gain.

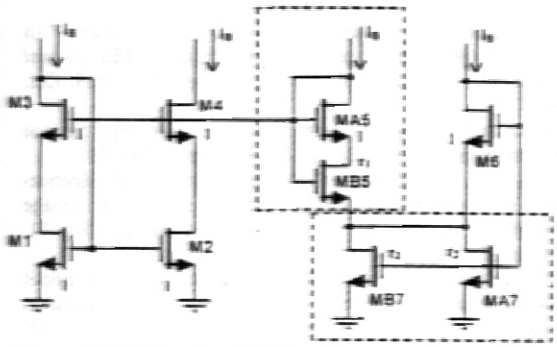

Figure 3: High-swing CCM with composite transistors.

Even though the present analysis has been performed for long-channel devices, we can apply it to short-channel devices as long as A is not higher than the maximum achievable gain of the short-channel device. Our analysis has not taken into account transistor or current mismatching. In a practical circuit the aspect ratio τ could be slightly decreased in order to add a small safety margin to the drain-source voltage of M2 that would compensate for transistor mismatching. The price to be paid would be a slightly smaller output voltage swing of the CCM.

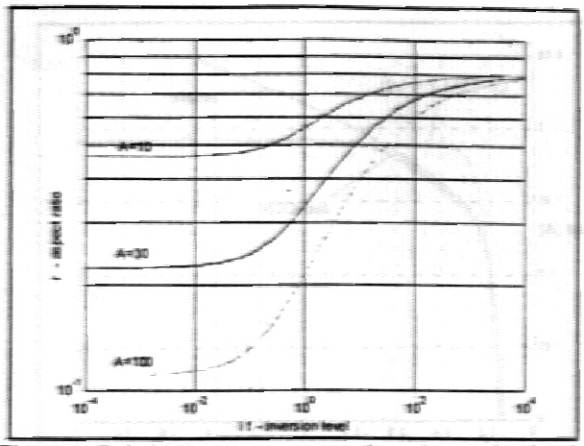

Figure 4: Relation between aspect ratio and inversion level.

5. Experimental results

To validate the design methodology, simple, self-biasing cascode (self-CCM) and low-voltage cascode (LV-CCM) current mirrors have been implemented and measured. N-channel transistors ($V_T \approx 0.6V$) from a 2μm CMOS technology have been used in the current mirrors. All transistors in the simple mirrors and CCM's have the same aspect ratios.

Figures 5 through 9 present details of the output characteristics of the current mirrors. Values of τ=1/3, 1/2 and 2/3, respectively, have been chosen according to Figure 4, for i_f=1, 10 and 100 and A=30.

Figures 5 through 7 shows that the LV-CCM's reach saturation at a drain-source voltage roughly twice the saturation voltage of the simple current mirror. The self-biased CCM saturates at a much larger voltage than the "optimally" biased CCM.

An alternative approach to choosing the aspect ratio "τ" in the bias network according to the current level would be to choose a constant "τ", say, τ=0.5.

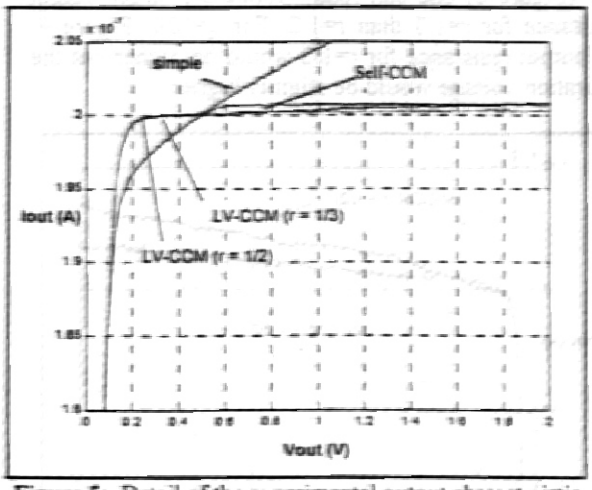

Figure 5:. Detail of the experimental output characteristic of the current mirrors in weak inversion (i_f=1).

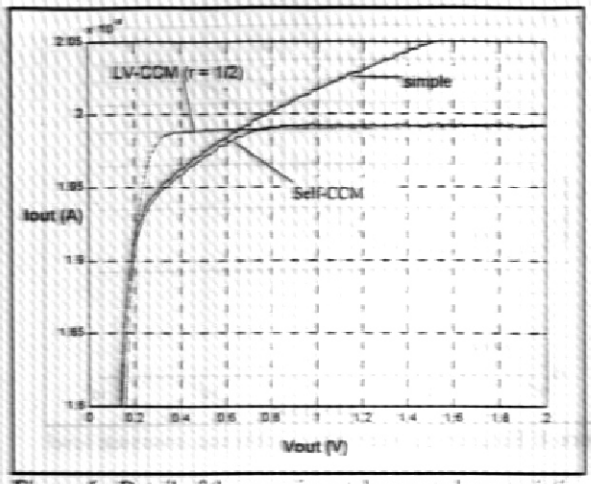

Figure 6:. Detail of the experimental output characteristics of the current mirrors in moderate inversion (i_f=10).

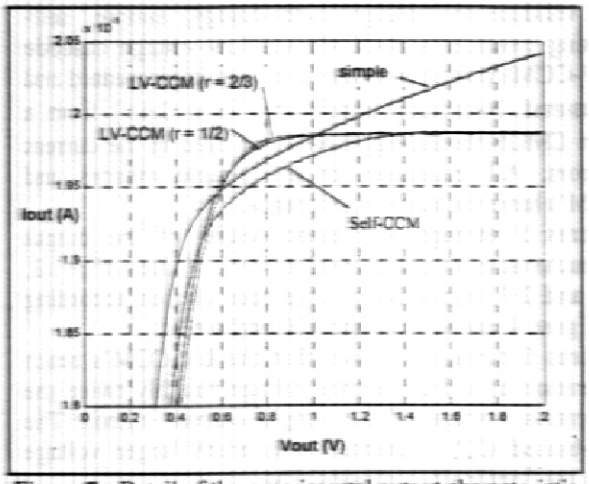

Figure 7:. Detail of the experimental output characteristic of the current mirrors in strong inversion (i_f=100).

For comparison purposes Figures 8 and 9 show expanded details of the output characteristics of the LV-CCM with r=0.5 and "r" chosen from Figure 4. For i_f=1 (Figure 8) one can ready notice the larger output resistance for r=1/3 than r=1/2. For i_f=100 (Figure 9) the output resistance for r=1/2 would be higher but the saturation voltage would be slightly higher.

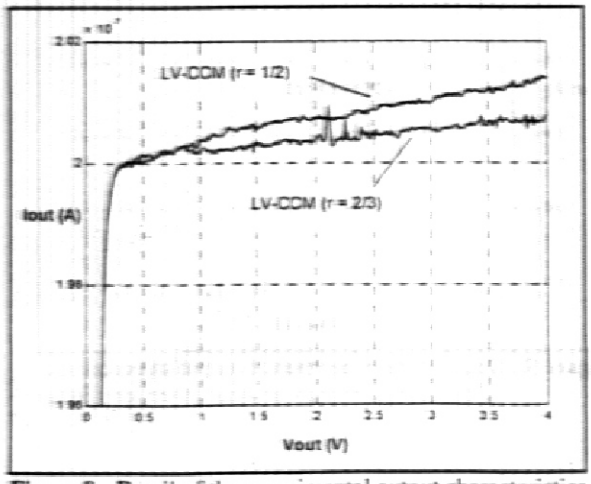

Figure 8:. Detail of the experimental output characteristics of the current mirrors in weak inversion (i_f=1).

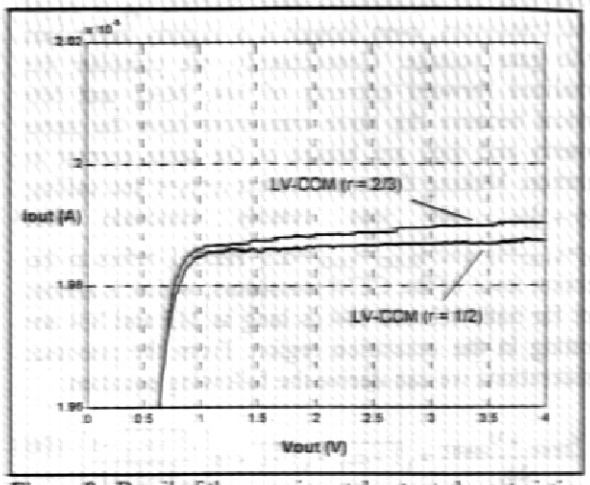

Figure 9:. Detail of the experimental output characteristics of the current mirrors in strong inversion (i_f=100).

6. Conclusions

A very simple bias circuit, valid for any current density, which allows for maximum output voltage swing of cascode stages has been presented and analyzed. Starting from the multiplication factor of the output impedance required for the cascode stage relative to the simple stage and from the output swing it is possible to determine the "optimal" biased network. Experimental results have corroborated the design methodology of the bias network.

Acknowledgment

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