THE ACM MOSFET MODEL: A CHARGE BASED COMPACT MODEL FOR CIRCUIT SIMULATION

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Abstract - This paper reviews the ACM MOSFET model, a physically based model for the MOS transistor, suitable for circuit simulation. This model is useful not only for the simulation of high current circuits but also for low-voltage operated circuits because it accurately represents moderate and weak inversion regions. All the static and dynamic characteristics of the MOSFET are described by single-piece functions with infinite order of continuity for all regions of operation. The proposed model preserves the structural source-drain symmetry of the transistor and uses a reduced number of physical parameters. It is also charge-conserving and has explicit equations for the MOSFET capacitances. The short channel effects are implemented using a compact and physical approach. The appropriateness of the model for circuit simulation has been evaluated through several simulation examples.

1.INTRODUCTION

MOSFET models included in circuit simulators can be classified into the following three categories: analytical models, table lookup models and empirical models. Practically all the models in current use are analytical.

MOSFET analytical models are based on either the regional approach or surface potential formulations, or semi-empirical equations [1-8]. Models based on the regional approach use different set of equations to describe the device behavior in different regions. In the regional approach, the weak and strong inversion regions are generally bridged by using a non-physical curve fitting. Models based on surface potential formulation are inherently continuous; however, they demand the solution of an implicit equation for the surface potential. Semi-empirical models take the risk of becoming neither scalable nor suited for statistical analysis.

ACM model is a charge-based physical model [1-3, 7,18]. All the large signal characteristics (currents and charges) and the small signal parameters ((trans)conductances and (trans)capacitances) are given by single-piece expressions with infinite order of continuity (C_∞ functions) for all regions of operation. ACM model preserves the structural source-drain symmetry of the transistor and uses a reduced number of physical parameters. It is also charge-conserving and has explicit equations for the 16 MOSFET (trans)capacitances.

2. FUNDAMENTALS

The fundamental assumption of our model is the linear dependence of the inversion charge density Q'_I on the surface potential ϕ_S [1, 5].

This assumption has allowed the model in [1] to be fully formulated in terms of the inversion charge densities at the source (Q'_{IS}) and drain (Q'_{ID}) channel ends. The relationship between the inversion charge density and the terminal voltages is [3]

$$V_P - V_C = \phi_t\left[\frac{Q'_{IP} - Q'_I}{nC'_{ox}\phi_t} + \ln\left(\frac{Q'_I}{Q'_{IP}}\right)\right] \quad (1)$$

where V_C is the channel voltage, V_P is the pinch-off voltage, Q'_{IP} is the inversion charge density at pinch-off, n is the slope factor and ϕ_t is the thermal voltage. All the voltages are referred to the local substrate, as in [3-5]. This relationship, also known as "Unified Charge Control Model (UCCM)"[6, 19] can be deduced from Boltzmann

statistics, the charge sheet approximation and the linear relationship between inversion charge density and surface potential, as shown in [3].

Equation (1) is not explicit for Q'_I, and ACM model uses the analytical approximation for Q'_I shown in [7].

3.SHORT CHANNEL EFFECTS

The common approach to model second order effects in MOSFETs, also employed in ACM, is to decorate the long-channel model with a list of corrections related to these effects. All the expressions are derived from the charge-based physical model of the long-channel MOSFET reported in [1 - 3] and are valid for any inversion level.

3.1. Charge sharing and drain induced barrier lowering

If velocity saturation effects are negligible, the drain current of a MOS transistor can be written as

$$I_D = f(V_P, V_S) - f(V_P, V_D) \tag{2}$$

For a long and wide transistor, the pinch-off voltage is a function of V_G only, but for short and narrow channel devices V_P is a function of V_G, V_S and V_D. To keep the symmetry of equation (2), V_P is modeled as

$$V_P(V_G, V_S, V_D) = V_{P0}(V_G) + \frac{\sigma}{n}(V_D + V_S) \tag{3}$$

$V_{P0}(V_G)$ is the pinch-off voltage at equilibrium (V_D=V_S=0) and is given by

$$V_{P0} = \left(\sqrt{V_G - V_{T0} + \phi_o + \gamma\sqrt{\phi_o} + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2}\right)^2 - \phi_o \tag{3a}$$

$$\gamma' = \gamma - \frac{\varepsilon_o \varepsilon_{Si}}{C_{ox}}\left[\frac{2.\eta_L}{L_{eff}} - \frac{3.NP.\eta_W}{W_{eff}}\right]\sqrt{\phi_o} \tag{3b}$$

where ϕ_o is a fitting parameter whose value is about twice the Fermi potential ($2\phi_F$) and V_{T0} is the threshold voltage at equilibrium. γ is the body effect coefficient of a wide, long-channel device. γ' is the body effect coefficient modified to include short and narrow channel effects. η_L and η_W are parameters to be adjusted; L_{eff} and W_{eff} are the effective length and width, respectively. The parameter σ accounts for the drain induced barrier lowering (DIBL) [6] and is proportional to $1/L^2_{eff}$.

3.2 Mobility reduction

The electron mobility in the inversion layer depends on the transverse electric field [8]. The effective mobility is dependent on all terminal voltages but is modeled here by

$$\mu = \frac{\mu_o}{1 + \theta.\gamma\sqrt{V_{P0} + \phi_o}} \tag{4}$$

where μ_o is the zero bias mobility, and θ is a fitting parameter. (4) has been derived assuming that the transverse field is mainly determined by the average depletion charge, a quite reasonable assumption for low and moderate inversion levels.

3.3 Velocity saturation

The velocity saturation is modeled as a function of the longitudinal electric field as in [5]. Applying this model together with the basic assumption of our model to the differential equation of the drain current leads, after integration along the channel [7], to:

$$I_D = \frac{\mu W_{eff}}{C'_{ox} L_{eq}} \frac{1}{1 + \frac{|Q'_S - Q'_D|}{Q'_A}} \frac{[(Q'^2_S - Q'^2_D) - 2nC'_{ox}\phi_t(Q'_S - Q'_D)]}{2n} \tag{5}$$

$$Q'_A = n.C'_{OX}.L_{eq}\frac{v_{lim}}{\mu} = n.C'_{OX}.L_{eq}.UCRIT \tag{6}$$

v_{lim} is the saturation velocity and $L_{eq} = L_{eff} - \Delta L$, where ΔL is the channel shrinkage due to CLM (section 3.4).

The maximum current that can flow in the channel occurs when saturation velocity is reached:

$$I_D = -Wv_{lim}Q'_{ID} \tag{7}$$

Equating (7) to (5) allows one to calculate the value of Q'_{ID} which corresponds to the onset of saturation, for any regime of operation [7]:

$$Q'_{IDSAT} = Q'_{IS} - nC'_{OX}\phi_t - Q'_A\left[1-\sqrt{1-\frac{2(Q'_{IS}-nC'_{OX}\phi_t)}{Q'_A}+\frac{(nC'_{OX}\phi_t)^2}{Q'^2_A}}\right] \tag{8}$$

The inversion charge density at the onset of saturation (Q'_{IDSAT}) is a function of the source and gate voltages, through Q'_{IS}, and of the channel length, through Q'_A.

From the charge-voltage relationship given by (1) one can readily calculate V_{DSSAT}, the drain-to-source voltage for which the charge density at the drain end corresponds to the onset of saturation:

$$V_{DSSAT} = \phi_t\left[\frac{Q'_{IDSAT}-Q'_{IS}}{nC'_{OX}\phi_t}+\ln\left(\frac{Q'_{IS}}{Q'_{IDSAT}}\right)\right] \tag{9}$$

3.4. Channel-length modulation (CLM)

For a MOSFET operating in the saturation regime, the gradual channel approximation becomes less valid, specially in the vicinity of the drain junction, where the two-dimensional nature of the space-charge region must be considered [8]. Therefore, an analytical formulation of the saturated part of conducting channel is not an easy task; as a consequence, many semi-empirical models have been tried to describe CLM. The approach employed here divides the region between drain and source into two parts, the non-saturated part of the channel, closer to the source, and the saturated part, closer to the drain. In the saturated part of the channel, the carrier velocity is assumed to be constant and equal to the saturation velocity. The channel length L_{eq}, i. e., the non-saturated part of the channel, is generally written as $L_{eq} = L - \Delta L$, where ΔL is the channel shrinkage due to CLM. Here we model the CLM as in [4].

4. SMALL-SIGNAL PARAMETERS

4.1. Transconductances

At low frequencies, the variation of the drain current due to small variations of the gate, source and drain voltages is

$$\Delta I_D = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_S,V_D,V_B}\Delta V_G + \left.\frac{\partial I_D}{\partial V_S}\right|_{V_G,V_D,V_B}\Delta V_S + \left.\frac{\partial I_D}{\partial V_D}\right|_{V_S,V_G,V_B}\Delta V_D + \left.\frac{\partial I_D}{\partial V_B}\right|_{V_S,V_D,V_G}\Delta V_B \tag{10a}$$

and

$$g_{mg} = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_S,V_D,V_B},\ -g_{ms} = \left.\frac{\partial I_D}{\partial V_S}\right|_{V_G,V_D,V_B},\ g_{md} = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_S,V_G,V_B},\ g_{mb} = \left.\frac{\partial I_D}{\partial V_B}\right|_{V_S,V_D,V_G}. \tag{10b}$$

are the gate, source, drain and bulk transconductances, respectively [4].

If the variation of the gate, source, drain and bulk voltages is the same, $\Delta I_D = 0$. Therefore, we can conclude that

$$g_{mg} + g_{md} + g_{mb} = g_{ms} \tag{10c}$$

Thus, 3 transconductances are enough to characterize the low-frequency small-signal behavior of the MOSFET.

Applying the definition (10b) of source and drain transconductances to the equation of the drain current together with equation (1) allows one to deduce simple expressions for the transconductances [3].

$$Q'_A = n.C'_{OX}.L_{eq}\frac{v_{lim}}{\mu} = n.C'_{OX}.L_{eq}.UCRIT \tag{6}$$

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almost independent of the current level in weak inversion and increases in moderate and strong inversion, as predicted by (12).

Fig. 4 shows that the Early voltage is almost independent of V_D in weak inversion but increases slightly with the drain voltage in strong inversion. This difference can be explained with the help of expression (12), where one can note that the influence of DIBL on the Early voltage is more important at low current densities.

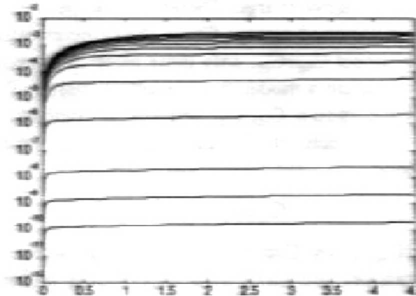


Fig. 2. Output characteristics of an NMOS transistor (L = 1.25µm) for V_G = 0.5, 0.6, 0.7, 0.9, 1.2, 1.6, 2.0, 2.4, 2.8, 3.2, 3.6, 4.0, 4.4 V

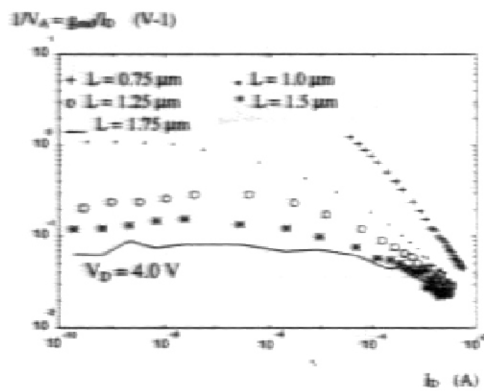


Fig.3. The output conductance-to-current ratio of NMOS transistors vs drain current for MOSFETs whose channel lengths range from 0.75µm to 1.75µm.

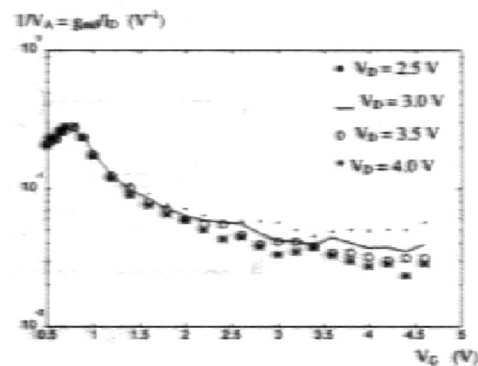


Fig.4. The output conductance-to-current ratio vs gate voltage of an NMOS transistor (L=1.25µm), with V_D varying from 2.5V to 4.0V.

4.3. Intrinsic Capacitances

The MOSFET intrinsic capacitances are defined by the general expressions:

$$C_{XY} = -\left.\frac{\partial Q_X}{\partial V_Y}\right|_0 , X \neq Y \tag{14}$$

$$C_{XX} = \left.\frac{\partial Q_X}{\partial V_X}\right|_0 \tag{15}$$

where Q_x can be any of the charges Q_S, Q_D, Q_B or Q_G and V_X and V_Y can be any of the voltages V_G, V_S, V_D or V_B. The notation "0" indicates that the derivatives are evaluated at the bias point. Because the MOSFET is an

active device, the capacitances C_{xy} are non-reciprocal, that is, in general, $C_{xy} \neq C_{yx}$. Taking into account charge conservation, $Q_S+Q_D+Q_B+Q_G=0$, and that only three voltage differences out of four can be chosen independently, it follows that the MOSFET is characterized by nine independent capacitances [8]. From the definitions of capacitance in (14) and (15) and the expressions of the MOSFET charges [18] we can derive formulas for the small-signal capacitances. Capacitances C_{gs}, C_{gd}, C_{gb}, C_{bs} and C_{bd} are widely used in AC modeling because they together describe accurately charge storage in MOSFETs up to moderate frequencies and can be calculated directly from the gate and bulk charges [4, 8]. It should be recalled, however, that a MOSFET model containing only these five capacitances does not conserve charge. Therefore, for the electrical simulation of charge sensitive circuits such as switched-capacitor or switched-current filters, the complete quasi-static model must be taken into account [8]. Considering that in our model $C_{bg}=C_{gb}$, only three more independent capacitances must be added to the basic MOSFET model in order to attain a model that conserves charge. To keep the symmetry of the device in the small-signal schematic we have chosen C_{sd}, C_{ds} and C_{dg} to complete the quasi-static MOSFET model. Small-signal analysis shows that the effects of C_{dg} and C_{gd} can be combined and replaced with C_{gd} and transcapacitance C_m (see Fig. 5) where:

$$C_m=C_{dg}-C_{gd}=-(C_{sg}-C_{gs}) \quad (16)$$

It can be readily verified that $C_m=(C_{sd}-C_{ds})/n$. Consequently, the small-signal schematic of Fig. 5, constituted of five capacitances, three transcapacitances and three transconductances preserves the inherent symmetry of the MOSFET.

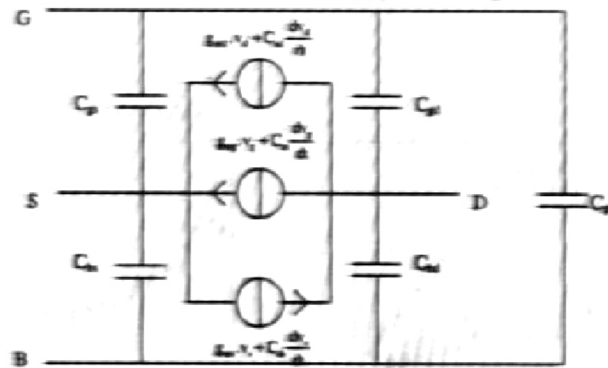


Fig. 5. Small-signal MOSFET model.

5.NOISE MODEL

The MOSFET noise can be considered as composed of thermal (white) noise and flicker (low-frequency) noise [8, 10]. It is usually modeled by including a current source between source and drain.

The expression of the total current, including both diffusion and drift components, together with Nyquist relationship [8, 11] allow calculating the PSD of the thermal noise:

$$S_{thermal}=-4kT\mu Q_I/L^2 \quad (17)$$

where k is the Boltzmann constant, T the absolute temperature and Q_I the total inversion charge. Equation (17) is valid from weak to strong inversion and, as quoted in [8, 11], includes the contribution of shot noise in weak inversion.

From equation (17), it follows that the MOSFET thermal noise is the same as the one produced by a conductance G_{Nth} whose value is

$$G_{Nth} = \mu|Q_I|/L^2 = g_{ms}\frac{Q_I}{Q_{IS}WL} \quad (18)$$

In the linear region, the inversion charge density is almost uniform, $Q'_I \cong Q_I/WL$, and the conductance G_{N0} equals the source transconductance. In saturation, the relation between G_{N0} and g_{ms} becomes 1/2 in weak inversion and 2/3 in strong inversion.

For both the calculation of the thermal noise in the linear region or its estimation in saturation, one can use

$$S_{thermal} \cong 4kTg_{ms} \tag{19}$$

Some models use an interpolation function to calculate the PSD of thermal noise from weak to strong inversion [4]. But for the accurate calculation of the thermal noise, the expression of the total charge Q_I must be used.

Flicker noise in MOS transistors is generally associated with charge fluctuation arising from dynamic trapping of electrons by interface states. As shown in [10] the PSD of the drain current is given by

$$S_{flicker} = \frac{KF.g_{mg}^2}{WLC_{ox}'^2.f} \tag{20}$$

where KF is a technology dependent flicker noise constant.

6. SIMULATION EXAMPLES

As long as CMOS technology is widely used in semiconductor industry, MOSFET models for circuit simulation are very important, specially for analog and mixed-mode circuit simulation. Nowadays there are strong efforts to evaluate the MOSFET models currently in use and several works were recently published presenting model benchmarks [12 - 15]. This section shows several examples of simulation which demonstrate the suitability of the ACM model to some of the tests proposed in [12 - 14].

The continuity of the static and dynamic characteristics in the transition from linear to saturation region and from weak to strong inversion [12] have already been shown in [7].

The circuit shown in Figure 6a [14] has been proposed to verify the symmetry of the capacitances C_{gd} and C_{gs}. The drain terminal is precharged to 5V and then a pulse is applied in the gate. If C_{gd} and C_{gs} are symmetric the drain and source will be at the same potential, after switch turns off the pulse. Fig. 6b presents the results for our model.

The circuit in Fig. 7, for the Gummel symmetry test [13, 15], is used to show the symmetry of forward and reverse modes of operation and the continuity, around the origin, of the drain current and charges as well as their derivatives. Fig. 8 shows the first and second order derivatives of the drain current. Both are continuous and symmetric around $V_{DS}=0$. It can be remarked that the BSIM 3v3 MOSFET model [16] does not pass in this test [15].

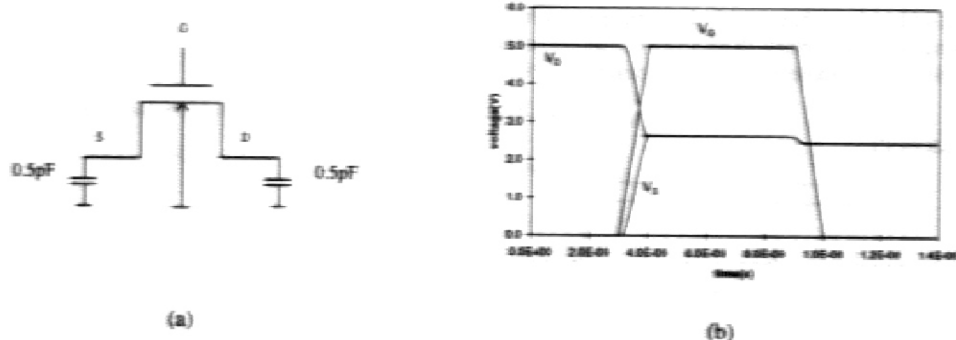


Fig.6 - The circuit used to test the symmetry of C_{gd} and C_{gs} (a) and the simulation results for our model (b).

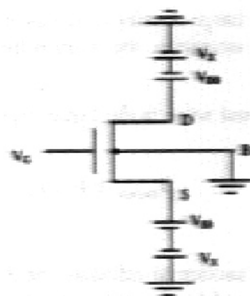
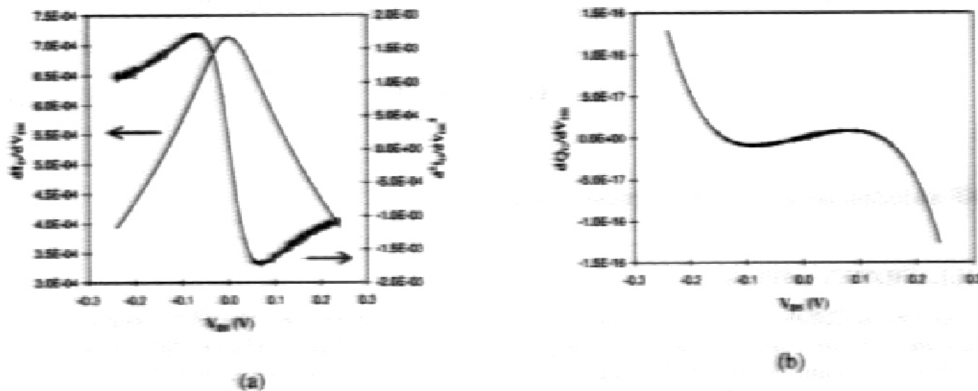


Fig.7 - Circuit for the Gummel symmetry test.



(a)

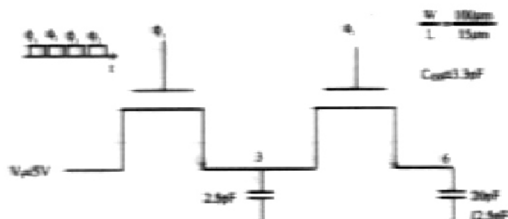
(b)

Fig. 8. - Symmetric and continuous first and second order derivatives of the drain current (a) and the derivative of the gate charge (b).

Charge conservation is a very important property when simulating charge sensitive circuits such as switched capacitor, switched current and dynamic memory circuits. Although charge conservation has been widely discussed in the literature there are some MOSFET models that do not conserve charge, e.g., the widely used SPICE 3 model.

To demonstrate that the ACM model is charge conserving, a basic switched capacitor circuit (fig. 9a) has been simulated. The simulations have been run for two different values of the load capacitor. The internal time step has also been modified for each value of the load capacitor.

Figures 9b and c show the simulation results obtained for the ACM model for $C_L = 20pf$. The results are independent of the internal time step. The voltage at nodes 3 and 6 are consistent and the output rises with the correct time constant. Simulations using SPICE 3 models at the same conditions were done. The results in figures 9 d and e show that SPICE 3 model gives different results for different internal time steps and that the time constant is not correct. With a small load capacitance the ACM model also present correct results but SPICE 3 model gives completely erroneous results (fig. 9f).



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(b)

Fig. 9- a) Schematic of a switched capacitor circuit, b) the simulation results with ACM MOSFET model for C_L=20pF and an internal time step of 1μs; c) the simulation results with ACM MOSFET model for C_L=20pF and an internal time step of 10ns, d) output voltage for SPICE 3 model with C_L=20pF and for internal time steps equal to 1μs and 10ns, e) ACM Mosfet model results for C_L=2.5pF and f) output voltage for SPICE 3 for C_L=2.5pF.

Finally, it is important to notice that in circuit simulation the gate capacitance must be well represented. The simulation of a transistor with the drain, source and bulk tied together, shows that ACM model represents well the gate capacitance (fig. 10) even in the accumulation region.

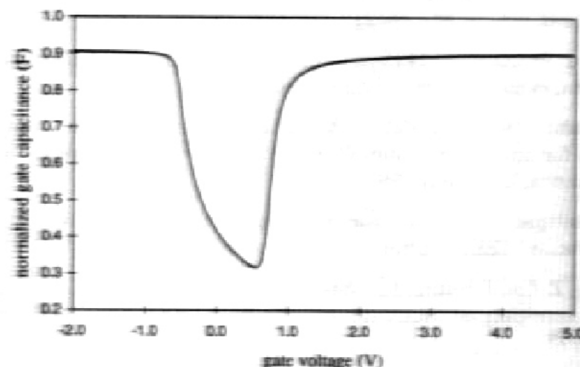

Fig.10 - Normalized gate capacitance (C_g/C_{ox}) versus gate voltage.

7. CONCLUSIONS

The ACM MOSFET model has been reviewed and discussed. It has been shown that the model is very suitable to represent both static and dynamic characteristics. Several tests applied to the model demonstrate that it conserves charge and is symmetric and continuous, particularly around V_{DS}=0.

The model is available in the last release of the SMASH circuit simulator[20] and the complete set of equations that describe the model can be found in [18].

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