A COMPACT MOSFET MODEL FOR CIRCUIT SIMULATION

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Abstract - **This paper presents a physically based model for the MOS transistor suitable for design and simulation of integrated circuits. The static and dynamic characteristics of the MOSFET are accurately described by single-piece functions of the inversion charge densities at source and drain. A new compact approach for saturation is presented. Several examples of electrical simulations compare the performances of our model and widely used MOSFET models.**

I.INTRODUCTION

MOSFET models included in circuit simulators can be classified into the following three categories [1]: analytical models, table lookup models and empirical models. Practically all the models in current use are analytical models.

MOSFET analytical models are based on either the regional approach or surface potential formulations, or semi-empirical equations [2]. Models based on the regional approach use different set of equations to describe the device behavior in different regions. In the regional approach, the weak and strong inversion regions are generally bridged by using a non-physical curve fitting. Models based on surface potential formulation are inherently continuous; however they demand the solution of an implicit equation for the surface potential. Semi-empirical models take the risk of becoming neither scalable nor suited for statistical analysis.

This paper presents a charge-based physical model [2 - 4]. All the large signal characteristics (currents and charges) and the small signal parameters ((trans)conductances and (trans)capacitances) are given by single-piece expressions with infinite order of continuity (C∞ functions) for all regions of operation. Our model

preserves the structural source-drain symmetry of the transistor and uses a reduced number of physical parameters. It is also charge-conserving and has explicit equations for its 16 transcapacitances.

In Section 2 the fundamentals of our model are presented and the implementation in a circuit simulator is described in Sections 3 and 4. In Section 5 we present some examples of simulation to compare the relative performances of our model, SPICE3, EKV and BSIM3v3 models.

2. FUNDAMENTALS

The fundamental assumption of our model is the linear dependence of the inversion charge density Q'_i on the surface potential ϕ_s [2, 6], for a given gate-to-bulk voltage (V_G):

$$dQ'_i = nC'_{ox}d\phi_s \tag{1}$$

where C'_{ox} is the oxide capacitance per unit area and n is the slope factor, slightly dependent on the gate voltage.

Equation (1) has allowed the model in [2] to be fully formulated in terms of the inversion charge densities at the source (Q'_{IS}) and drain (Q'_{ID}) channel ends.

The relationship between the inversion charge density and the terminal voltage is [4]

$$V_P - V_{Cb} = \phi_t\left[\frac{Q'_P - Q'_i}{nC'_{ox}\phi_t} + \ln\left(\frac{Q'_i}{Q'_P}\right)\right] \tag{2}$$

where V_{Cb} is the channel voltage, V_P is the pinch-off voltage, Q'_P is the inversion charge density at pinch-off and ϕ_t is the thermal voltage.

Equation (2) cannot be solved analytically for Q'_i but it can be approximated by an analytical expression [4].

$$q = \ln\left[1 + \frac{e^{u-1}}{1 + k(u)\ln(1+e^{u-1})}\right] \tag{3}$$

with
$$k(u) = 1 - \frac{84.4839}{u^2 + 150.8640} \tag{4}$$

where
$$u = \frac{V_P - V_{S(D)}}{\phi_t} \quad \text{and} \quad q = \frac{Q'_{i(S,D)}}{nC'_{ox}\phi_t} \tag{5}$$

3. I-V MODEL

3.1. Short and narrow channel effects

The drain current of a MOS transistor, if velocity saturation is not considered, can be written as

$$I_D = f(V_P, V_S) - f(V_P, V_D) \tag{6}$$

where all potentials are refered to the bulk [2]

For a long and wide transistor the pinch-off voltage is only a function of V_G, but for short and narrow channel devices V_P becomes a function of V_G, V_S and V_D. To maintain the symmetry of equation (6), V_P is modeled as

$$V_P(V_G, V_X, V_Y) = V_P(V_G, V_X) + \frac{\sigma}{n} V_Y \tag{7}$$

This formulation is very useful to include the second order electrostatic effects of the terminal voltages when calculating the charge densities at the source and drain ends. To calculate Q'_{IS} $V_X = V_S$ and $V_Y = V_D$ and for Q'_{ID} calculation $V_X = V_D$ and $V_Y = V_S$.

$V_P(V_G, V_X)$ is given by

$$V_P = \left(\sqrt{V_{GB} - V_{TO} + \phi_o + \gamma \sqrt{\phi_o + \left(\frac{\gamma'}{2}\right)^2}} - \frac{\gamma'}{2} \right)^2 - \phi_o \tag{8}$$

where ϕ_o is a fitting parameter and its value is about twice the Fermi potential ($2\phi_F$), V_{TO} is the threshold voltage at equilibrium, and γ' is the body factor. γ is the body factor of a wide, long-channel device. The short and narrow channel effects due to charge sharing are included in γ' in a similar way as in [5]. The parameter σ accounts for the drain induced barrier lowering (DIBL) [7] and is proportional to $1/L^2_{eff}$.

3.2 Mobility reduction [4]

The mobility reduction due to the vertical field is modeled by

$$\mu = \frac{\mu_o}{1 + \theta(\gamma \sqrt{V_{PO} + PHI} - \frac{Q'_{IS} + Q'_{ID}}{2 C'_{ox}})} \tag{9}$$

where μ_o is the zero bias mobility, V_{PO} is the pinch-off voltage of a wide, long-channel device and θ is a parameter of adjust.

3.3 Velocity saturation

The effect of velocity saturation in our model is based on the expression [6] below:

$$\mu_s = \frac{\mu}{1 + \frac{\mu}{v_{sm}} \frac{d\phi_s}{dx}} \tag{10}$$

The substitution of both the approximation (1) and (10) into the differential equation of the drain current leads, after integration along the channel, to [4]

$$I_D = \frac{\mu W_{eff}}{C'_{OX} L_{eq}} \frac{1}{1 + \frac{|Q'_I - Q'_\tau|}{Q'_A}} \left(\frac{Q'^2_I - Q'^2_\tau}{2n} \right) \tag{11}$$

where

$$Q'_{I(\tau)} = Q'_{IS(ID)} - n.C'_{OX}\phi_\tau \,, \tag{12}$$

$$Q'_A = n.C'_{OX}.L_{eq}\frac{v_{sm}}{\mu} \tag{13}$$

v_{sm} is the saturation velocity.

3.4 Saturation voltage

The maximum current that can flow in the channel occurs when velocity is saturated:

$$I_D = -W v_{sm} Q'_{ID} \tag{14}$$

Equating equations (11) and (14) allows to calculate the value of Q'_{ID} which corresponds to saturation

$$Q'_{IDSAT} = Q'_{IS} - nC'_{OX}\phi_\tau - Q'_A \left[1 - \sqrt{1 - \frac{2(Q'_{IS} - nC'_{OX}\phi_\tau)}{Q'_A} + \frac{(Q'_{IS} - nC'_{OX}\phi_\tau)^2}{Q'^2_A}} \right] \tag{15}$$

Q'_{IDSAT} can be approximated by

$$Q'_{IDSAT} = \frac{\phi_\tau}{L_{eq} UCRIT} \frac{\left(1 - \frac{Q'_{IS}}{2nC'_{OX}\phi_\tau}\right)}{1 + \frac{\phi_\tau}{L_{eq} UCRIT}\left(1 - \frac{Q'_{IS}}{nC'_{OX}\phi_\tau}\right)} Q'_{IS} \tag{16}$$

V_{DSSAT} is calculated from (2).

For the current to saturate properly the drain to source voltage should be smoothly clamped at V_{DSSAT} by means of equation (17) [8].

$$V'_{DS} = f_D - \sqrt{f_D^2 - V_{DS} V_{DSSAT}} \tag{17}$$

where

$$f_D = \frac{1}{2}\left[V_{DS} + (1+s)V_{DSSAT}\right] \tag{18}$$

s is a fitting parameter equal to 0.01.

In the calculation of Q', the voltage V_D is replaced by

$$V'_D = V'_{DS} + V_S \tag{19}$$

3.5 Channel length modulation [5, 7]

The channel length modulation is modeled by

$$\Delta L = \lambda . L_C . \ln\left[1 + \frac{(V_{DS} - V'_{DS})}{L_C . UCRIT}\right] \tag{20}$$

with

$$L_C = \sqrt{\frac{\varepsilon_o . \varepsilon_{Si} . X_j}{C'ox}} \tag{21}$$

λ is an adjusting parameter, $\varepsilon_o\varepsilon_{Si}$ is the permittivity of silicon, and x_j is the junction depth.

The equivalent channel length is given by

$$L_{eq} = L_{eff} - \Delta L \tag{22}$$

4. CHARGE EQUATIONS AND CAPACITANCES

Models that do not conserve charge generate critical errors for the analysis and design of some important MOS circuits, such as switched capacitors, switched current and dynamic memories. Charge nonconservation is due to the use of capacitance models instead of charge models [9]. Our model is a charge based model, i.e., it has explicit equations for the source, drain, bulk, and gate charges. The charge equations below are continuous and have continuous derivatives in all regions of operation, allowing the calculation of the 16 MOSFET (trans)capacitances.[2]

$$Q_B = -W_{eff} L_{eff} C'ox\left[(n-1)\phi_t + \frac{\gamma'^2}{2.(n-1)}\right] - \frac{n-1}{n} Q_I \tag{23}$$

$$Q_G = Q_B - Q_I \tag{24}$$

$$Q_S = W_{eff} L_{eff}\left[\frac{6.Q'^2_I + 12.Q'_I.Q'^2_I + 8.Q'^2_I.Q'_I + 4.Q'^3_I}{15.(Q'_I + Q'_I)^2} + \frac{n.C'ox.\phi_t}{2}\right] \tag{25}$$

$$Q_b = Q_i - Q_s \tag{26}$$

where the inversion charge is

$$Q_i = W_{eff} L_{eff} \left(\frac{2}{3} \frac{Q'^2_r + Q'_r . Q'_s + Q'^2_s}{Q'_r + Q'_s} + n.C'ox.\phi_t \right) \tag{27}$$

The derivatives of the charge densities are given by

$$\frac{dQ'_{s(d)}}{dV_{s(d)}} = n.C'ox.\frac{Q'_{s(d)}}{Q'_{f(r)}} \tag{28}$$

5. RESULTS

The results shown in figures 1 to 3 correspond to the tests 1 to 3 suggested in [10] to evaluate the quality of a model. They show that our model is continuous from weak to strong inversion and represents well the moderate inversion region; the plot of the ratio g_m/I_D versus V_G presents the expected shape. No discontinuities are observed in g_m (figure 3).

Figure 4 shows the 9 independent (trans)capacitances. All the curves are continuous and vary smoothly.

Tests to verify charge conservation were done using our model, EKV, and SPICE3 from SMASH [11], and BSIM3v3 from T-Spice[12]. The first test is performed in the charge pumping circuit shown in figure 5, where a 5V pulse train is applied to the gate and the voltages at drain and source are measured. If the model conserves charge the voltage at the drain (source) should rise and return to zero for each input pulse. Figure 6 shows the simulation results. Our model and BSIM3v3 give correct results while EKV and SPICE3 provide incorrect results. The second test has been performed in the sample-hold circuit shown in figure 7. Here, again, the results given by SPICE3 and EKV are not consistent, as can be seen in figure 8.

6. CONCLUSIONS

A compact MOSFET model for circuit simulation was presented. Simulations with an NMOS transistor showed that the proposed model attains the criteria of continuity and agree well with the EKV model regarding the DC characteristics. The simulation of both a charge pumping and a sample-hold circuit showed that our model, as well asBSIM3v3,conserves charge, while the SPICE3 and EKV models do not. Some advantages of our model over BSIM3v3 are the use of compact expressions to describe all regions of operation as well as the smaller number of device parameters.

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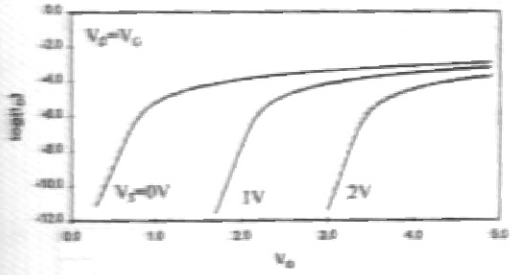

Fig.1 $\log(I_D)$ x V_G - our model ——
EKV model ——

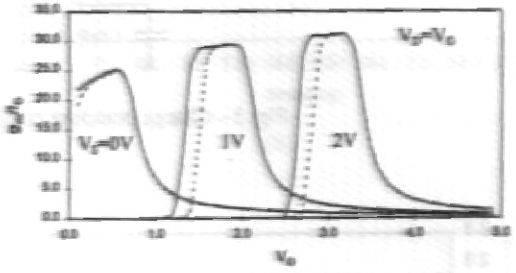

Fig.2 - g_m/I_D x V_G - our model ——
EKV model ——

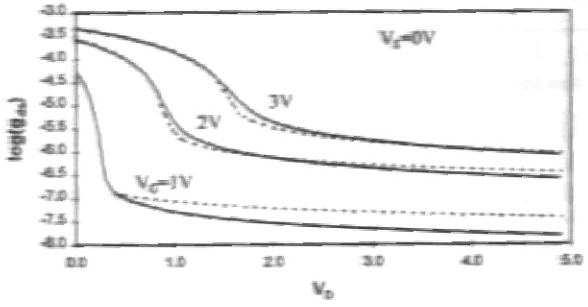

Fig. 3 - $\log(g_{ds})$ x V_D - our model ——
EKV model ——

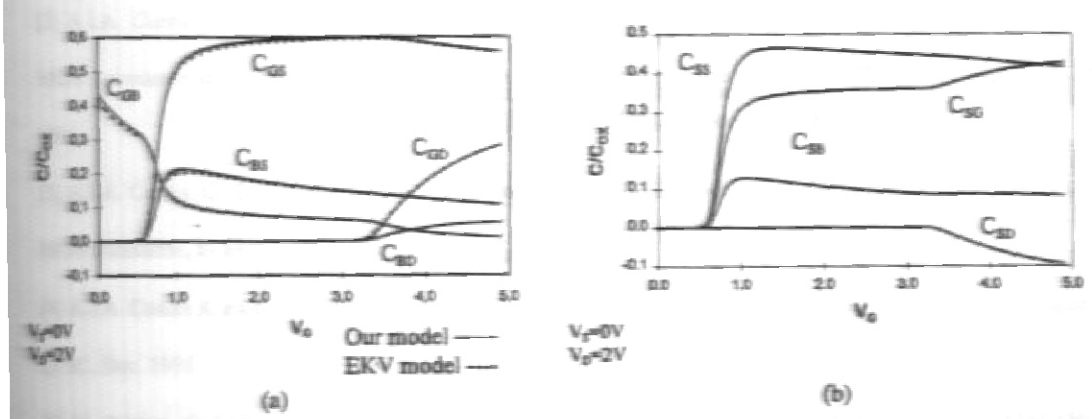

Fig. 4 - (a) Comparisons between the 5 capacitances available in EKV and those of our model (b) 4 capacitances in our model that are not modeled in EKV. The simulations were done in SMASH

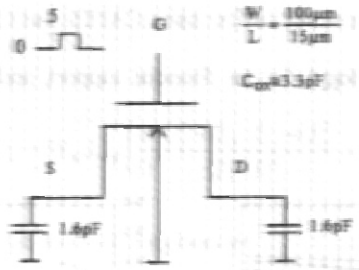

Fig. 5 - Charge pumping circuit for charge conservation test

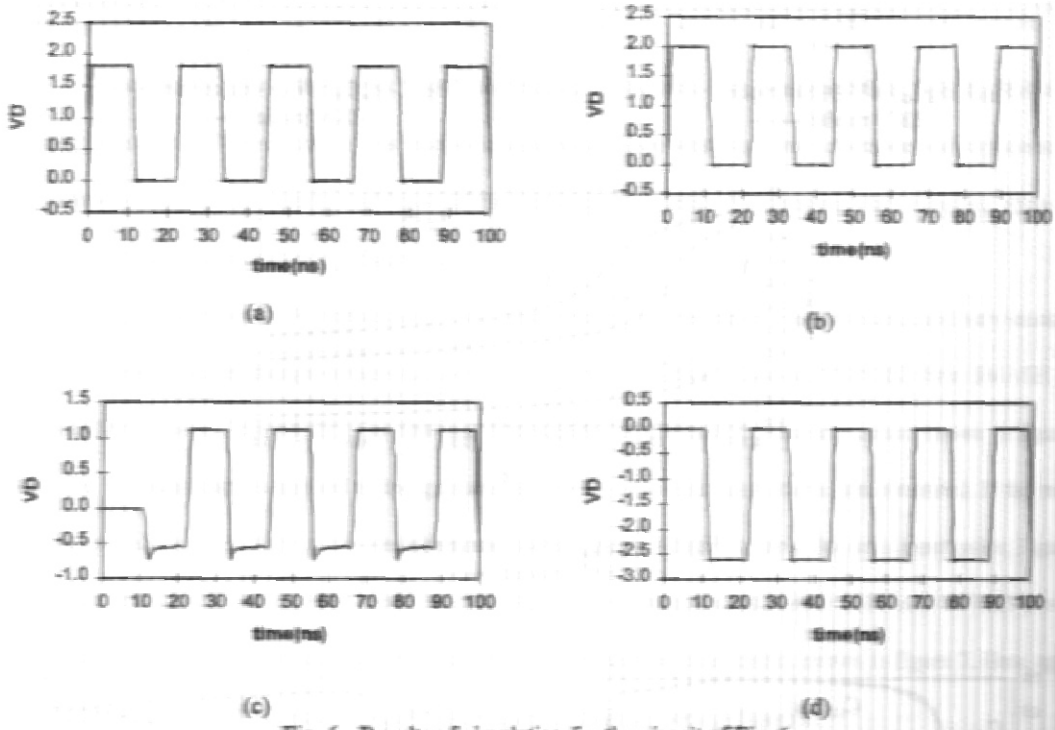

Fig. 6 - Results of simulation for the circuit of Fig. 6
(a) our model (b) BSIM3v3, (c) EKV, (d) SPICE3

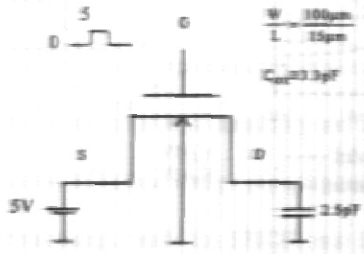

Fig. 7 - Sample and hold circuit for charge conservation test

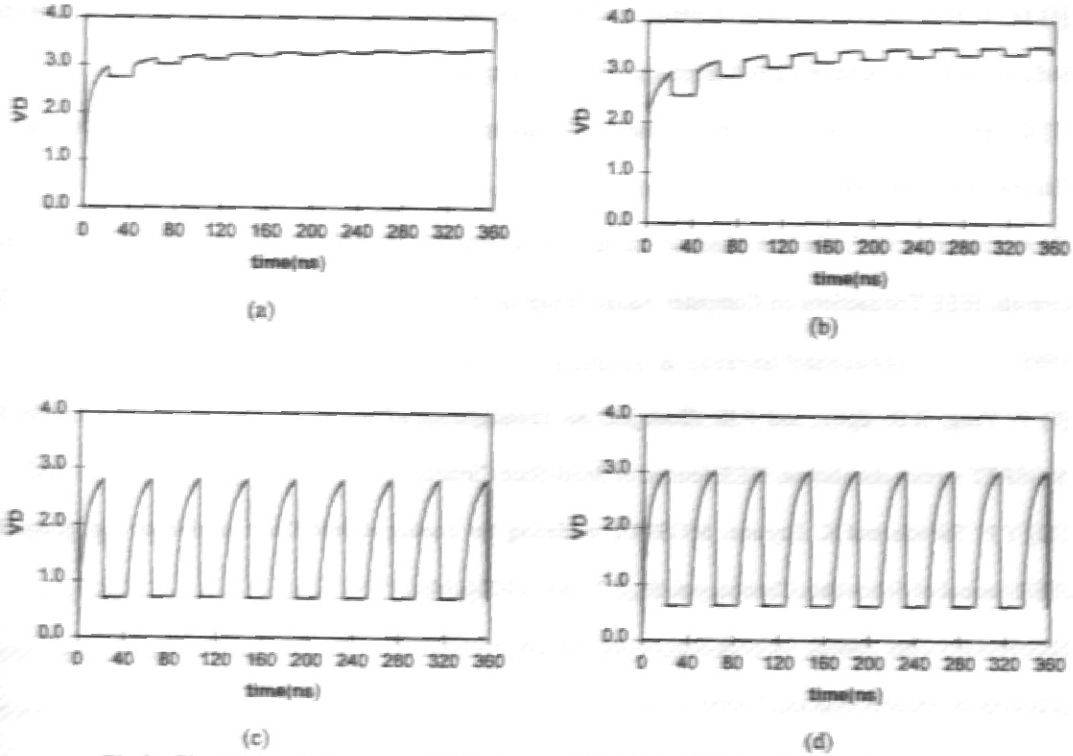

Fig.8 - Simulation of the sample-hold (a) our model, (b) BSIM3v3, (c) EKV, (d) SPICE3

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