A Design Methodology for MOS Amplifiers

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Abstract

This paper presents a design methodology for MOS amplifiers. The methodology is based on a universal model of the MOSFET, being valid from weak to strong inversion. A set of very simple expressions allows quick design by hand as well as an evaluation of the best solution in terms of power consumption or silicon real state. A design of both a common-source and a differential amplifier illustrate the applicability of the proposed methodology.

1. Introduction

The design of CMOS amplifiers is either based on MOSFET models developed for weak inversion or strong inversion [1,2]. The current trend towards low-power or small area circuits many times require the transistor to be biased in the moderate inversion region. Therefore, a MOSFET model capable of providing the designer with a set of equations valid for any inversion level is a very powerful tool. Moreover, the availability of a good model for all regions of operation can save many hours of simulation since it allows the designer to start with a solution which is very close to the desired one. Here, we use the universal MOSFET model developed in [3-4], which employs the bias current as the key variable, as our basic reference for design. The proposed design methodology for amplifiers accounts for specifications such as gain-bandwidth product, phase margin, biasing, gain and voltage swing. Figures of merit associated to power and silicon real estate consumption are presented. Two design examples illustrate the methodology proposed.

2. MOSFET model

The MOSFET model employed in our methodology has been developed in [3]. The set of equations that has been used for design are:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_f}} \quad (1.a) \qquad i_f = \frac{I_D}{I_S} \quad (1.b)$$

$$I_S = I_{SQ}\left(\frac{W}{L}\right) \quad (1.c) \qquad I_{SQ} = \mu n C'_{ox}\frac{\phi_t^2}{2} \quad (1.d)$$

$$f_T \cong \frac{\mu\phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right) \quad (2)$$

$$\frac{V_{DS,sat}}{\phi_t} \cong (1-\varepsilon)\left(\sqrt{1+i_f}-1\right)+\ln\left(\frac{1}{\varepsilon}\right) \quad (3)$$

$$\frac{V_P - V_S}{\phi_t} = \sqrt{1+i_f}-\sqrt{1+i_p}+\ln\left[\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_p}-1}\right] \quad (4.a) \qquad V_P = \frac{V_G - V_{TO}}{n} \quad (4.b)$$

I_{SQ}, (1.d), is the saturation current for a square transistor. I_{SQ} depends on the slope factor n, which is almost constant, and on technological parameters: mobility μ, oxide capacitance per unit area C'_{ox} and the thermal voltage ϕ_t. The transistor dimensions, width W and length L, are included in the saturation or normalization current I_S, (1.c). i_f is the normalized current or inversion level [3]. (1.a) shows that the ratio of transconductance-to-currents in MOSFETs is quite different from bipolar transistors, where $\phi_t g_m/I_C=1$. If g_m is defined in a bipolar design, so is I_C. However, in a MOSFET design, the specification of g_m allows the designer to choose from a range of currents, according to (1.a). Equation (2) gives us the intrinsic cut-off frequency f_T in terms of the inversion level. Note that f_T depends only on technology and on current density (i_f). An approximate formula for the source-to-drain saturation voltage as a function of the inversion level is shown in (3), where $(1-\varepsilon)$ is the degree of saturation(see appendix A). ε can be chosen as, say, 5%. The relation between gate and source voltage is given by (4.a) and (4.b), also in terms of the inversion level. V_P is the "pinch-off" voltage and i_p is its correspondent normalized current where can be adopted i_p=8.

3. Single Stage Amplifier

The common source amplifier has already been studied in [4],[5] and it is only included here to provide a new insight into the design methodology. In the ideal CMOS amplifier, the transconductance required for a load

capacitance equal to CL and gain bandwidth GBW is $g_m = 2\pi \cdot GBW \cdot CL$. By using this equation and (1) the drain current and the aspect ratio can be written as:

$$I_D = 2\pi \cdot GBW \cdot CL \cdot n \cdot \phi_t \frac{1+\sqrt{1+i_f}}{2} \quad (5) \qquad \frac{W}{L} = \frac{2\pi \cdot GBW \cdot CL}{\mu C'_{ox} \phi_t} \left(\frac{1}{\sqrt{1+i_f}-1} \right) \quad (6)$$

(5) and (6) show that there is a degree of freedom for the design. The DC current and the aspect ratio are determined as long as the inversion level is chosen. The compromise between area and consumption can be reached by an appropriate choice of i_f. It is remarkable to note that a low inversion level is translated into a low power consumption but a high aspect ratio. Moreover, the lowest current to meet the specification of GBW is in weak inversion, when $i_f \ll 1$. However, this solution leads to a prohibitively high aspect ratio.

The evaluation of the resulting designs is an important task. In this work, we define two figures of merit of an amplifier, one for the power consumption and the other for the area. In [6], the current excess factor CEF has been defined as the ratio of the total current of an amplifier to that of an ideal CMOS inverter operating in weak inversion. Here we apply this concept to equation (5) , but we use an inversion level corresponding to moderate inversion, $i_f=8$, as reference. Moreover, we extend this concept to the aspect ratio of a single transistor operating with $i_f=8$ too:

$$CEF = \frac{Itot}{2\pi \cdot GBW \cdot CL \cdot n \cdot \phi_t \cdot 2} \quad (7) \qquad AEF = \frac{\sum W/L}{2\pi \cdot GBW \cdot CL/\mu \cdot C'_{ox} \cdot \phi_t \cdot 2} \quad (8)$$

AEF is the area excess factor, which is the ratio of the sum of all aspect ratios to the reference aspect ratio.

	weak inversion ($i_f \ll 1$)	moderate inversion* ($i_f=8$)	strong inversion ($i_f \gg 1$)
CEF	1/2	1	∞
AEF	∞	1	0

Table 1: Limit values of the current and area excess factors (*: 1 transistor)

4. The Differential Stage Amplifier

One of the most important building blocks for analog design is the differential pair. Figure 1 shows the conventional configuration of the simple differential stage for P-channel input transistors.

4.1 AC modeling

The AC analysis of the differential amplifier [1] shows that the unity gain frequency is given by $GBW = g_{m1}/2\pi CL$. The equation for the nondominant pole due to C_{p4}, the total parasitic capacitance at node 4, is

$$f_{nd} = \frac{g_{m3}}{2\pi C_{p4}} \tag{8}$$

As shown in [1], the nondominant pole acts on only half the signal. Therefore, the phase margin (PM) is written as

$$PM = 90^{\circ} - \mathrm{Arctg}\left(\frac{GBW}{f_{nd}}\right) + \mathrm{Arctg}\left(\frac{GBW}{2f_{nd}}\right) \tag{9}$$

The nondominant pole can be chosen approximately equal to the intrinsic cutoff frequency (2). Even though the phase shift introduced by the nondominant pole is not of a major concern in the design of a single differential pair, it can lead to a severe degradation in the frequency response of an operational amplifier.

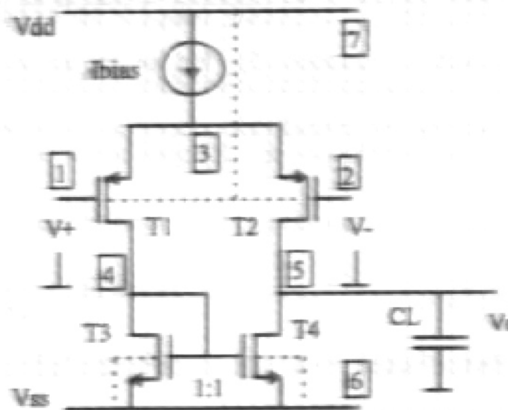

Figure 1 - P-channel input OTA

4.2 The Total Current and Area

The normalized total current (CEF) and area (AEF) excess factors of the OTA shown in figure 2 are:

$$CEF = \frac{Itot}{2\pi \cdot GBW \cdot CL \cdot n \cdot \phi_t \cdot 2} = \frac{1+\sqrt{1+i_{f1}}}{2} \tag{11}$$

$$AEF = \frac{\sum W/L}{2\pi \cdot GBW \cdot CL/\mu_n \cdot C'_{ox} \cdot \phi_t \cdot 2} = \left(\frac{4\mu_n}{\mu_p}\right)\left(\frac{1}{\sqrt{1+i_{f1}}-1} + \frac{\mu_p}{\mu_n i_{f3}}\left(1+\sqrt{1+i_{f1}}\right)\right) \tag{12}$$

According to (11), the designer has to minimize i_{f1} for minimum power consumption. The minimum value of CEF, CEF_{min}, can be approximated as in a single stage amplifier, setting $i_{f1} \ll 1$, which means $CEF_{min}=1$.

It can be shown from (12) that the total area as function of i_{f1}, at constant i_D, has a minimum at i_{f1Amin} given by

$$i_{f1Amin} = \frac{i_D \mu_N}{\mu_P} + 2\sqrt{\frac{i_D \mu_N}{\mu_P}} \tag{13}$$

where i_{f1Amin} is the value of i_{f1} corresponding to the circles in Figure 2, which shows the CEF and AEF as functions of i_{f1}.

4.3 DC Gain

The DC gain in the differential amplifier is given by

$$Avo = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{14}$$

Where $g_{ds}=I_D/VA$ is the output conductance and VA is the Early voltage, and the substitution of the expressions for g_{ds} into (14), assuming $VA_2=VA_4=VA$ leads to the expression next for the normalized voltage gain:

$$Avo\frac{2\phi_t n}{VA} = \frac{\phi_t n g_{m1}}{I_{D1}} = \frac{2}{1+\sqrt{1+i_{f1}}} \tag{15}$$

Figure 3 shows the normalized gain in terms of the inversion level.

4.4 Voltage Swing

A simple circuit analysis associated to equations (3) and (4) results in expressions to the voltage swing as functions of the envolved inversions levels.

5. Design methodology

After having presented several aspects of circuit design we are now in a position to describe a design methodology. Assuming that load capacitance, gain-bandwidth product and DC gain are the specifications to be met, the design of a differential amplifier can be suggested as follows:

1. Using expressions (4) and (5), plot curves of I_D and W/L as functions of the inversion level. Choose a value for i_f and, consequently, a pair (I_D, W/L), which meets the GBW specified.

3. Specify W and L of the current mirror transistors such that an acceptable phase margin is achieved. If the phase shift introduced by the current mirror at the frequency equal to the gain-bandwidth is very small, another criterion, such as the saturation voltage can be used to dimension T3 and T4.
4. Verify if the gain specification is satisfied. If not, an increase in channel lengths or/and reduction in inversion levels can be employed to increase the gain.
5. Design the current source. For a low voltage design, the saturation voltage of the current source should be as small as possible. Therefore, inversion coefficients close to 1 can be used in order to achieve a good compromise between area and saturation voltage.

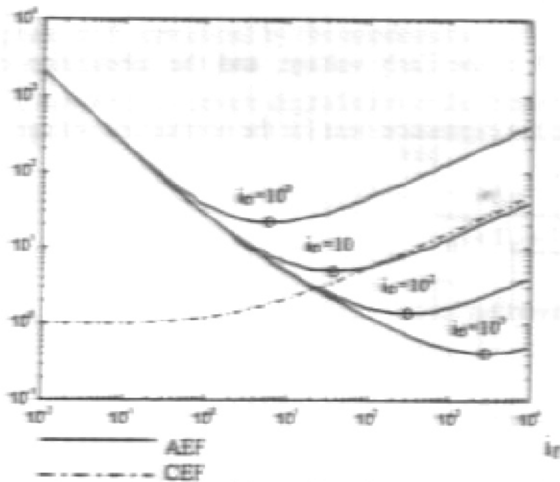

Figure 2 -AEF and CEF as functions of i_{fi} and i_{fD}, with indication of the minimum areas (o). μ_N=0.0465 $m^2/(Vs)$ and μ_P=0.0168 $m^2/(Vs)$.

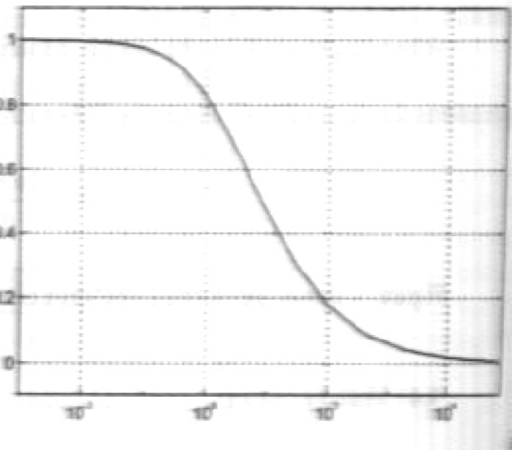

Figure 3 -Normalized DC voltage gain as function of the inversion level of T1.

6. Examples

In this section we have developed examples for GBW=10MHz and GBW=100MHz, both with CL=10pF as specifications (respectively g_{mi1}=0.628mA/V and g_{mi1}=6.28mA/V).

6.1 Analyses of Various Pairs i_{f1} and i_{f3}

The next tables illustrate the behavior of the all involved variables with differents pairs of i_{f1} and i_{f3} for the given specifications.

(GBW; CL)	(10MHz; 10pF)					
(i_{f1}; i_{f3})	(1; 8)	(4; 8)	(8; 8)	(8; 40)	(8; 100)	(40; 8)
Itot (A)	51μ	68μ	84μ	84μ	84μ	157μ
CEF	1.21	1.62	2.00	2.00	2.00	3.70
$(W/L)_1$	1508	505	312	312	312	116
$(W/L)_3$	68	91	113	22	9	209
$\sum W/L$	3152	1192	850	668	642	650
AEF*	27.90	10.56	7.53	5.93	5.68	5.74
$V_{ICM\,MAX}$ (V)*	2.07	2.01	1.97	1.97	1.97	1.82
$V_{ICM\,MIN}$ (V)*	-3.67	-3.71	-3.73	-3.53	-3.35	-3.76
$V_{O\,MAX}$ (V)*	0.81	0.84	0.86	0.86	0.86	0.89
$V_{O\,MIN}$ (V)*	-2.37	-2.37	-2.37	-2.28	-2.19	-2.37
Avo (dB)*	35	33	31	31	31	26
f_{T3}/GBW	157	157	157	424	710	157
PM	89.81°	89.81°	89.81°	89.93°	89.95°	89.81°

Table 2

(GBW; CL)	(100MHz; 10pF)					
(i_{f1}; i_{f3})	(8; 8)	(8; 100)	(8; 1000)	(40; 100)	(100; 1000)	(100; 8)
Itot (A)	850μ	850μ	850μ	1.57m	2.34m	2.34m
CEF	2.00	2.00	2.00	3.70	5.52	5.52
$(W/L)_1$	3123	3123	3123	1156	690	690
$(W/L)_3$	1130	90	9	167	25	3121
$\sum W/L$	8506	6426	6264	2646	1430	7622
AEF*	7.53	5.69	5.54	2.34	1.26	6.75
$V_{ICM\,MAX}$ (V)*	1.97	1.97	1.97	1.82	1.68	1.68
$V_{ICM\,MIN}$ (V)*	-3.73	-3.35	-2.34	-3.38	-2.41	-3.79
$V_{O\,MAX}$ (V)*	0.86	0.86	0.86	0.88	0.90	0.90
$V_{O\,MIN}$ (V)*	-2.37	-2.2	-1.66	-2.19	-1.66	-2.37
Avo (dB)*	31	31	31	26	22	22
f_{T3}/GBW	16	71	240	71	240	16
PM	88.18°	89.60°	89.88°	89.60°	89.88°	88.18°

Table 3

*ϕ_t=26mV, ε=5%, i_f=8, n=1.3, V_{TON}=0.53V, V_{TOP}=0.75V, Vdd=2.5V, Vss=-2.5V, VA=5V, C'ox=0.023F/m², L=0.7μm, μ_N=0.0465m²/(Vs) and μ_P=0.0168m²/(Vs).

It makes clear that the designer has many design alternatives. The GBW=10MHz requirement allows a design near the weak inversion. In otherwise the GBW=100MHz heve to operate near the strong inversion to avoid enormous areas. The last column of each table represents an incorrect design: high area and high power consumption. It becomes clear that i_D should be grater then i_B. From the Tables 2 and 3 we also can verify that the sensibility of the voltage swing with respect to the inversion level is much lower than that of the area and power.

6.2 Simulated Cases

From Table 2 it was simulated the case (i_D; i_B)=(4; 8) and from Table 3 the one (i_D; i_B)=(40; 100). In Tables 4 and 5, and Figures 6 and 7 are shown the simulation results using the SMASH simulator release 2.2 with EKV [7] model and ES2 parameters technology with L=0.7μm for all transistors.

Parameter	Theoretical	Simulated
g_{m1} (mA/V)	0.628	0.79
GBW (MHz)	10	11.6
Avo (dB)	33	27
PM	89.81°	88°

Table 4

Parameter	Theoretical	Simulated
g_{m1} (mA/V)	6.28	8.48
GBW (MHz)	100	114
Avo (dB)	26	25
PM	89.60°	85.3°

Table 5

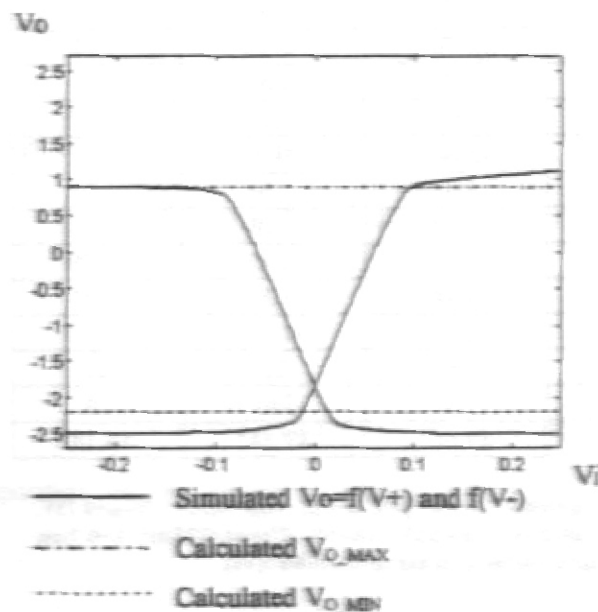

Figure 6 -Simulated Vo as function of Vi=V- and Vi=V+. And the indication of the calculated V_{O_MAX} and V_{O_MIN} for GBW=10MHz.

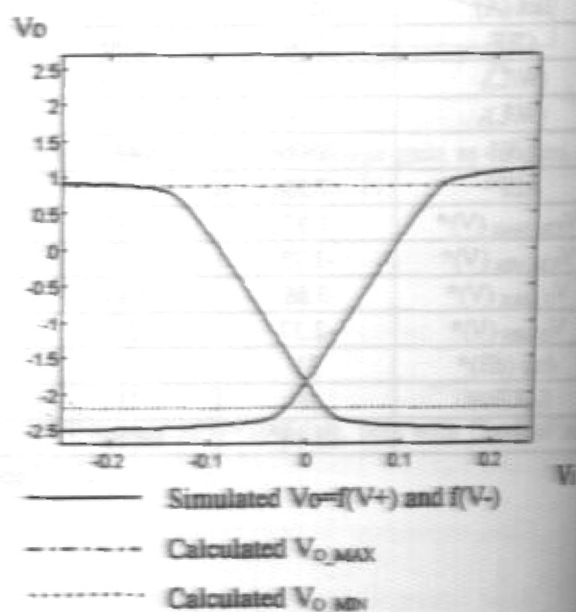

Figure 7 -Simulated Vo as function of Vi=V- and Vi=V+. And the indication of the calculated V_{O_MAX} and V_{O_MIN} for GBW=100MHz.

7. Conclusions

In this work a methodology to design MOS amplifiers has been developed. The methodology is based on a current-based MOSFET model which has accurate and continuous equations from weak inversion to strong inversion. Therefore, the proposed method is suitable for low power design. The design methodology employs the inversion level to adjust to AC parameters of the OTA. We presented two figures of merit for amplifiers, the current excess factor and the area excess factor, which can help the designer choose an optimized circuit according to his or her needs. Designs examples were presented to illustrate the design methodology. And simulations of some of this examples were done to verify the applicability of the method.

8. References

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Appendix A

The MOSFET saturation degree, $1-\varepsilon$, is a measurement of how close to the saturation region the MOSFET is operating. ε is defined as

$$\varepsilon = Q'_{ID}/Q'_{IS} \tag{A1}$$

where $Q'_{IS(D)}$ is the inversion charge per unit area at source (drain). It is related to the applied voltages by[3]

$$Q'_{IP} - Q'_{IS(D)} = nC'_{ox}\left[V_P - V_{S(D_sat)} - \phi_t \ln\left(Q'_{IS(D)}/Q'_{IP}\right)\right] \tag{A2}$$

In (A2) V_P and Q'_{IP} are the channel voltage and charge per unit area at pinch-off [3]. Applying (A2) to both Q'_{ID} and Q'_{IS} and using (A1) to define saturation, the drain-to-source saturation voltage is given by

$$\frac{V_{DS_sat}}{\phi_t} = (1-\varepsilon)\frac{|Q'_{IS}|}{nC'_{ox}\phi_t} + \ln\left(\frac{1}{\varepsilon}\right) \tag{A3}$$

Substituting $|Q'_{IS}|/nC'_{ox}\phi_t = \sqrt{1+i_f} - 1$ [3], allows (A3) to be written as in (3).