LOW OUTPUT CONDUCTANCE, HIGH CUTOFF FREQUENCY TRANSISTORS FOR GATE ARRAY IMPLEMENTATION OF ANALOG CIRCUITS

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ABSTRACT

This paper presents a simple approach to design low output conductance composite transistors, wider at the drain end than at source end. These transistors have two main advantages over "DC equivalent" transistors of uniform width: significant silicon area savings and an increase in the cutoff frequency. The main envisaged application is the integration of analog circuits in digital gate arrays.

I. INTRODUCTION

The MOS technology has proven to be well suited for the implementation of mixed analog-digital systems. To increase design speed the gate array approach has been extensively used for digital circuits. However, only very few gate array implementations of combined analog and digital circuits have been reported [1-3]. Gate array transistors usually have minimum channel lengths. Although this feature is desirable in digital applications, several transistor channel widths and lengths are needed for precision analog circuits. It has been pointed out [1] that parallel connection of unit transistors yields wide-channel transistors while serial connection produces long-channel transistors. However, the transit time of the series connected transistors is proportional to the square of the number of series transistors.

This paper presents a simple method to design composite MOS devices consisting of associations of unit transistors. It is shown that the T-transistor of Fig. 1 (a), with the drain end wider than the source end, has almost the same DC characteristics as the R-transistor of Fig. 1 (b). Two advantages are obtained from using a T-transistor in lieu of an R-transistor: area savings and an increase in the cutoff frequency.

II. DC CHARACTERISTICS

In the triode region, using the gradual channel approximation. the drain current I_d of an MOS transistor can be written [4] as

$$I_d = K\left[g(v_g, v_d) - g(v_g, v_s)\right] \quad (1)$$

where all voltages are referred to the substrate voltage, emphasizing the symmetry between drain and source.

From eqn. (1), the following expression holds for the composite transistor shown in Fig. 2

$$g(v_g, v_x) = \frac{K1}{K1+K2} g(v_g, v_d) + \frac{K2}{K1+K2} g(v_g, v_s) \quad (2)$$

Hence, the drain current in the composite transistor is:

$$I_d = \frac{K1.K2}{K1+K2}\left[g(v_g, v_d) - g(v_g, v_s)\right] \quad (3)$$

Therefore, in the triode region, the composite transistor has a DC behavior equal to that of a single transistor whose aspect ratio is K1 K2/(K1+K2). Moreover, two transistors are also equivalent in the saturation region if they have:

(i) the same aspect ratio K
(ii) the same channel width at the drain end.

Satisfied these conditions, it can be verified that the current density and the electrical field at the channel end near the drain are almost the same. Therefore, the composite transistors in Fig. 1 are equivalent at DC. Notice that the transistors connected between nodes X and S in Fig. 1 are always in the triode region provided the transistors connected to the drain end are not in punch-through.

Fig. 3 shows the DC output characteristics of a unit transistor and of a square (3x3) composite transistor. Their equivalence in the triode region and the smaller output conductance of the composite transistor in saturation are readily verified.

The DC equivalence of the composite transistors of Fig. 1 is illustrated in Figs. 4 and 5. In Fig. 4, the two plots of the internal potential V_X are almost coincident, in particular for high values of the gate voltage. Fig. 5 shows the DC output characteristics of the two transistors. These characteristics are also almost coincident, particularly the output conductance in the saturation region.

III. TRANSIT TIME

The transit time in an MOS transistor is given by [4]:

$$\tau = \frac{Q_I}{I_d} \tag{4}$$

where Q_I is the total inversion charge.

The transit time of the saturated trapezoidal transistor (Fig. 1), calculated in strong inversion using the approximations for the inversion charge and the drain current presented in reference [5], is given by

$$\tau = \tau_u \left[\sqrt{1+m} \left(1 - \frac{1}{m^2} \right) + \left(1 + \frac{1}{m} \right)^2 \right] \tag{5}$$

where $\tau = \tau_u$ is the transit time of the unit transistor in saturation and m is the number of parallel-connected unit transistors at the drain side.

In order to evaluate experimentally expression (5), the normalized transit time can be written as:

$$\frac{\tau}{\tau_u} = \frac{C_{gs}}{C_{gsu}} \frac{g_{mu}}{g_m} \tag{6}$$

where C_{gs} is the gate-to-source capacitance and g_m is the small-signal gate transconductance [4].

g_m and g_{mu} have been measured in an HP 4145B semiconductor parameter analyzer while C_{gs} and C_{gsu} have been measured according to the electrical scheme shown in Fig. 6.

Fig. 7 shows the experimental results obtained from the circuit in Fig. 6 for both the T-transistor and the R-transistor from Fig. 1. The capacitive coupling in the R-transistor is about 6 times larger than in the T-transistor. Clearly, the transit time of the T-transistor is smaller than the transit time of the R-transistor due to a shorter distance between points S and X. Moreover, the gate area of the T-transistor is reduced, relative to the R-transistor.

Fig. 8 exhibits the normalized transit time of the composite transistor in terms of the number of transistors connected to the drain side. The transit time increases very slowly with the increasing number of parallel-connected transistors at the drain side.

IV. DISCUSSION AND CONCLUSIONS

All the experimental results presented in this paper were obtained from samples of the C4007 integrated circuit. However, we have also measured DC characteristics of MOS composite transistors, made up of minimum channel-length (1.2um) unit transistors, integrated in the 7th CMOS Brazilian multiproject chip. The DC measurements in the integrated composite transistor have also corroborated the theoretical prediction stated in section II.

We have proposed in this paper a method to design composite transistors wider at the drain end than at the source end. These transistors can be designed to have a g_m/g_{ds} ratio substantially larger than that of a single transistor without the corresponding reduction in the cutoff frequency which would occur in a rectangular transistor. Hence, composite transistors are very useful for the design of simple scheme analog sections for high speed and low voltage applications.

The use of composite transistors is not limited to applications in gate arrays. They can also be employed in full custom circuits providing easy-to-implement equivalents to nonrectangular transistors [6]. Moreover, the IC designer can benefit from better matching properties if unit transistors in composite devices are placed so that the effect of parameter gradients is minimized.

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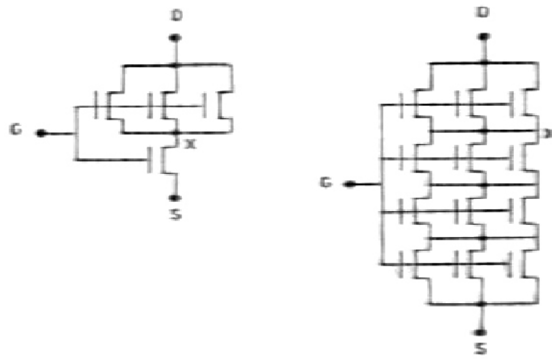


Fig. 1 - Composite transistors
(a) Trapezoidal transistor (T-transistor)
(b) Rectangular transistor (R-transistor)

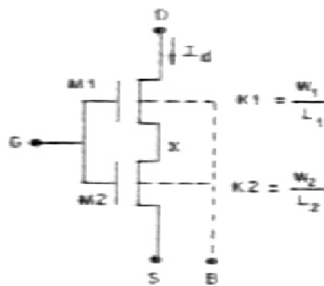


Fig. 2 - Series connected transistors

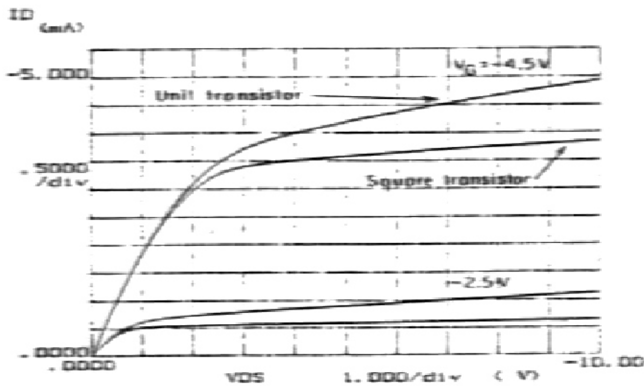


Fig. 3 - DC characteristics of a unit transistor and a square (3 x 3) composite transistor.

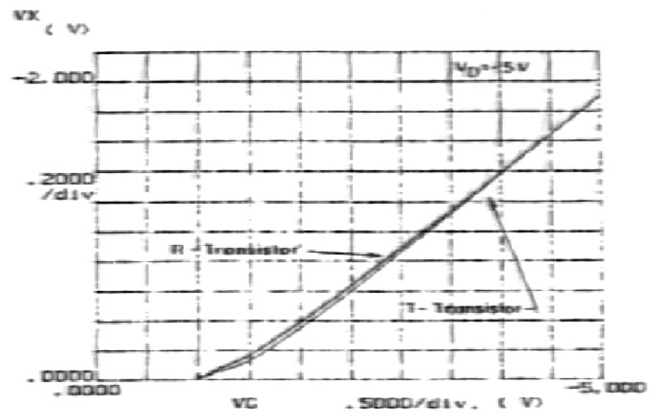
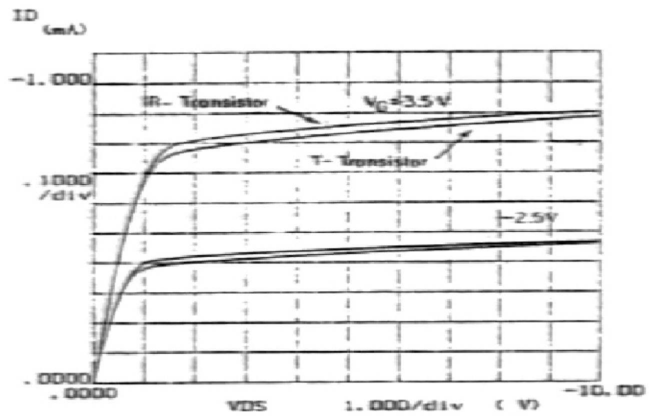
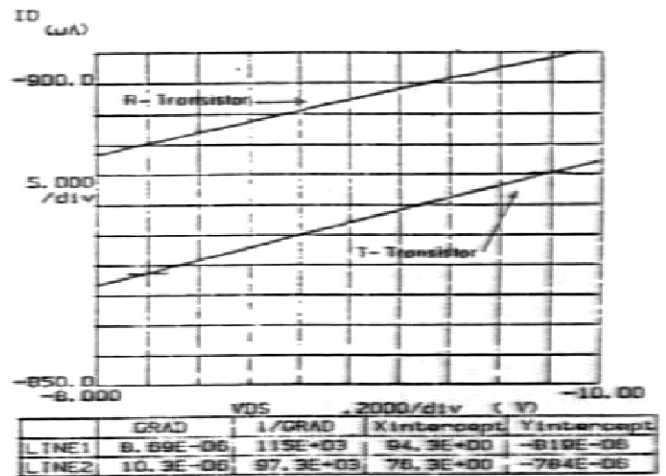


Fig. 4 - Voltages at internal node X of the composite transistors of Fig. 1.





	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	8.69E-06	115E+03	94.3E+00	-819E-06
LINE2	10.3E-06	97.3E+03	76.3E+00	-784E-06

(b)

Fig. 5 - (a) DC characteristics of the composite transistors of Fig. 1. (b) Detail of the saturation region.

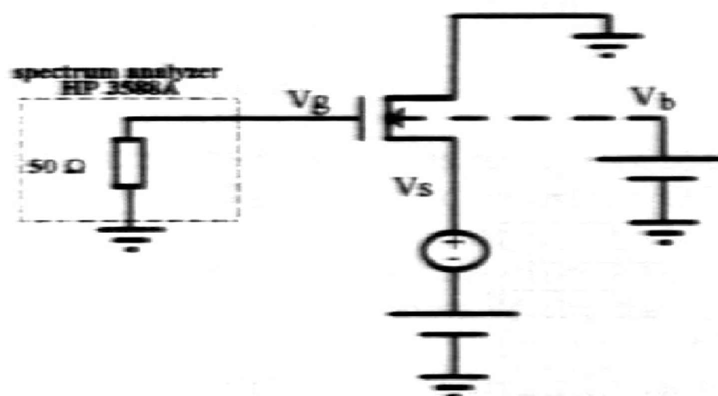


Fig. 6 - Circuit for the measurement of gate-to-source capacitance.

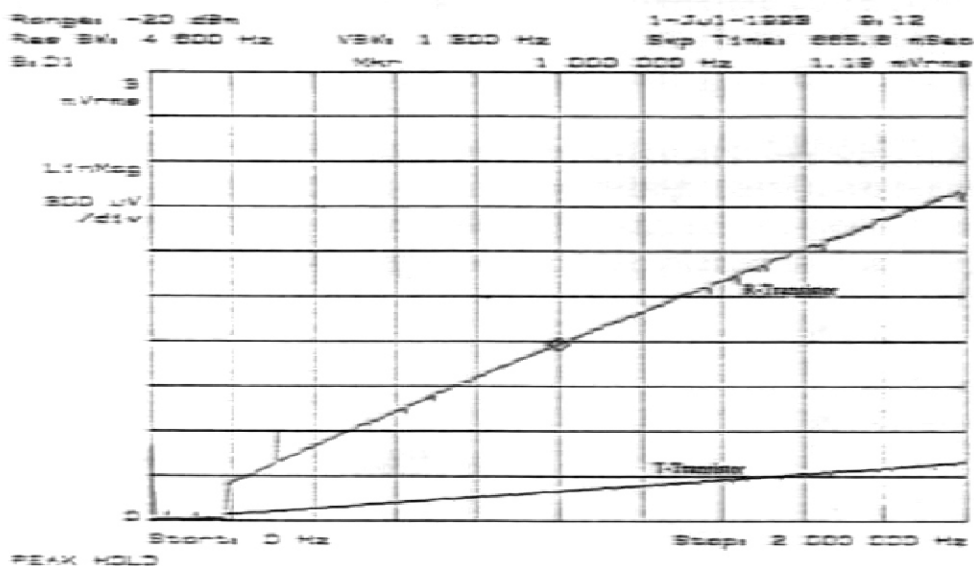


Fig. 7. Experimental results for the gate-to-source coupling in the R and T-transistors (Vdb=Vgb= -3V, Vsb= 0V)

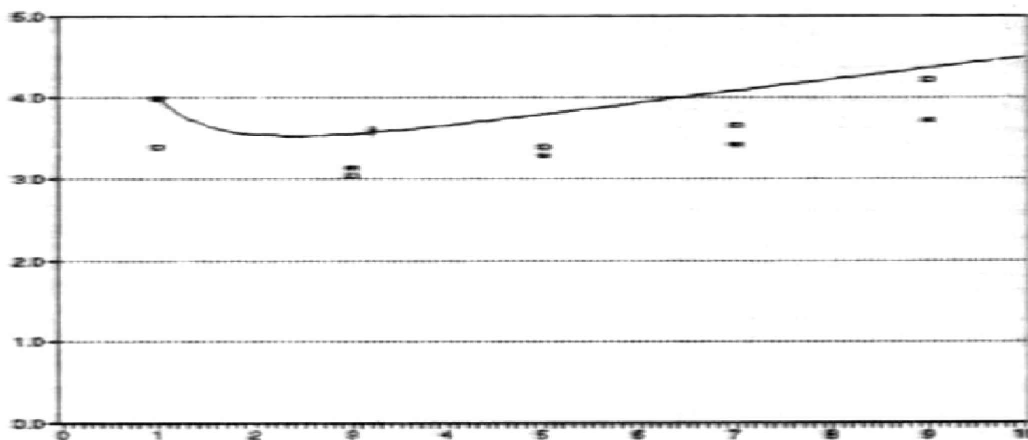


Fig. 8. Normalized transit time of the T-transistor (m is the number of parallel-connected transistors at the drain side)

- theoretical; □ measured at Vgs= -2V; * measured at Vgs= -3V;