Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors

Alfredo Arnaud, *Member, IEEE*, Rafaella Fiorelli, *Student Member, IEEE*, and Carlos Galup-Montoro, *Member, IEEE*

***Abstract*—In this paper, series-parallel (SP) current-division will be employed for the design of very low transconductance OTAs. From the theory and measurements, it will be shown that SP mirrors allow the division of currents with division factors of thousands, without reducing matching or noise performance. SP mirrors will be applied to the design of OTAs ranging from 33 pS to a few nS, with up to 1 V linear range, consuming in the order of 100 nW, and with a reduced area. An integrated 3.3-s time-constant integrator will also be presented. Several design concerns will be studied: linearity, offset, noise, and leakages, as well as layout techniques. A final comparative analysis concludes that SP association of transistors allows the design of very efficient transconductors, for demanding applications in the field of implantable electronics, among others.**

***Index Terms*—Low offset transconductors, MOS analog design, MOS matching, series-parallel transistors.**

I. Introduction

In recent years, there has been considerable research effort in the development of integrated transconductance amplifiers (OTAs), with very small transconductance and improved linear range due mainly to their application in biomedical circuits and in neural networks. Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with a linear range up to 1 V or more [1]–[10]. However, the use of complex OTA architectures also increases noise, mismatch offset, and transistor area, and results in design trade-offs [1].

In a classical symmetrical OTA, voltage to current conversion is carried out in the input differential pair while the other transistors just copy the current to the output. Although bias current can be extremely low [11], leading to an extremely low transconductance, a drawback in this case is the poor linearity as the input transistors operate in weak inversion. In weak inversion, the range of operation of the OTA is limited to 60–70 mV at the input; for greater input voltages there is a considerable distortion in the circuit. Despite the existence of alternative continuous time approaches [11] to sub-Hertz filters we will focus on the classical OTA-C structure. It is possible to summarize the challenge presented by the design of very low transconductance OTAs for modern G_m-C filters as follows: to increase linear range while preserving low noise, low offset, and reduced area and power consumption. In [12], a tutorial focused on classic linearization techniques for OTAs is presented, while in [1], an interesting comparative study of different linearized OTAs in the nanosiemens range was shown. Although many working principles and circuit topologies have been reported for very low transconductance OTAs, a rough classification may include the following.

- — Those circuits that modify the differential pair performing the voltage-to-current conversion in such a way as to reduce the transconductance and increase its linear range. Techniques include classic or active source degeneration [12], [13], bump transistors [4], and bulk or floating gate driven MOS [1], among others.
- — Those circuits that use current cancellation [5] or current division [3], [14] to divide the OTA transconductance by a desired factor, but do not increase the input linear range.
- — Circuits using voltage division techniques for the extension of the linear range [2], [7].

Of course, techniques can be combined. Regarding their limitations, modified-differential pairs increase offset and noise, and are limited to a few nanosiemens in their transconductance; further transconductance reduction requires the use of some kind of division scheme. Current cancellation and voltage division also show, in general, significant input offset and noise. Simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area. But the use of series-parallel division of current [3], [14] in an OTA as in Fig. 1, allows the implementation of an area-efficient current divider. In this paper, we will examine this circuit in detail, particularly with reference to offset.

In the rest of this section, series-parallel (SP) OTAs are introduced, as well as the current-based ACM MOSFET model, essential for the analysis of SP association of transistors. In Section II, it is shown, from both circuit analysis and measurements, that SP association of transistors helps in the design of current mirrors, even with copy factor of thousands, and a low current mismatch. Section III contains several SP OTA design issues which will be examined: linearity, noise, offset, frequency response, and leakage current effects. Section IV shows the design and measurement results for several OTAs, and a 3.3-s time-constant G_m-C integrator. At the end, a comparative study of this work and others in the field of very large time constant integrated G_m-C filters is presented.

Manuscript received September 23, 2005; revised April 4, 2006. This work was supported in part by the PROSUL project from CNPq, Brazilian agency for scientific development, and by FCE-CONICYT and CSIC, Uruguay.

A. Arnaud was with Universidad de la República, Uruguay. He is now with the Electrical Engineering Department, Catholic University, Montevideo CP11600, Uruguay, (e-mail: aarnaud@ucu.edu.uy).

R. Fiorelli is with the Universidad de la República, Montevideo, CP11300, Uruguay (e-mail: fiorelli@ fing.edu.uy).

C. Galup-Montoro is with the Electrical Engineering Department, Federal University of Santa Catarina, Florianopolis, SC 88040-900, Brazil (e-mail:carlos@eel.ufsc.br).

Digital Object Identifier 10.1109/JSSC.2006.880606

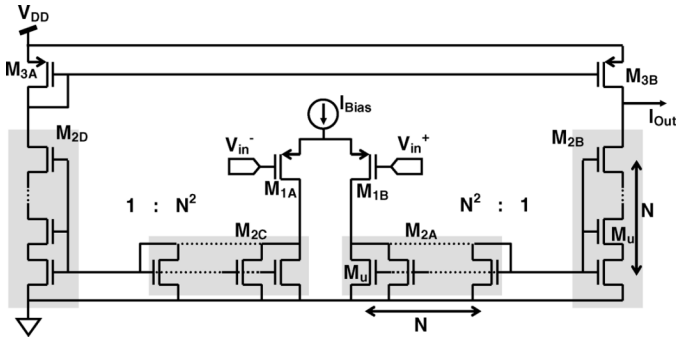

Fig. 1. PMOS-input symmetrical OTA with series-parallel current division to reduce transconductance without loss in linear range.

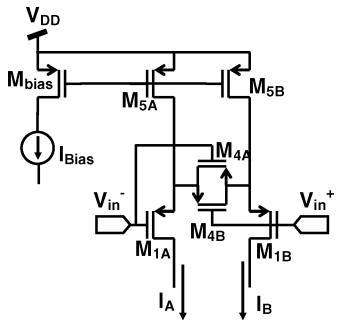

Fig. 2. Active linearization of a differential pair to enhance linearity: $I_A - I_B = g_{m\_\text{eff}}\left(V_{\text{in}}^{+} - V_{\text{in}}^{-}\right)$.

A. Series-Parallel OTA

For the nMOS current mirrors in Fig. 1, N unit transistors M_u are placed in series and in parallel to achieve an effective output transconductance G_m

$$G_m = \frac{g_{m1}}{N^2} \tag{1}$$

where g_{m1} is the gate transconductance of the transistors M_1. Using this technique, a 33 pS transconductor with a $\pm$150 mV linear range has been previously demonstrated [14]. To enhance linearity, a modified differential input pair as shown in Fig. 2 [13] can substitute M_1 in Fig. 1. The effective transconductance g_{m_eff} of the pair in Fig. 2 to substitute g_{m1} in (1) is calculated by small-signal analysis, assuming that transistors M_4 operate in the linear region, each behaving as a resistor of value $2R$. Therefore,

$$g_{m\_\text{eff}} = \frac{g_{m1}}{1 + n g_{m1} R} \tag{2}$$

where n is the slope factor [15], [16], slightly greater than unity and weakly dependent on the gate voltage.

The current mirrors of Fig. 1 are not only area-efficient because their area is proportional to the square root of the copy factor, but are also mismatch-efficient because they benefit from the improved matching of a large number of equal unit transistors. With the appropriate placement, the designer can apply the most usual matching rules to M_{2A}–M_{2B} and M_{2C}–M_{2D}: common centroid geometry, and same surroundings; even while using copy factors as large as thousands if for example $N = 50$ or $N = 100$ are selected. To preserve mismatch benefits while using moderate copy factors, the current mirror in Fig. 3 can be used.

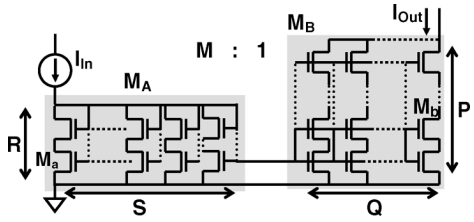

Fig. 3. Generic SP current mirror. $P \times Q$ unit transistors M_b, and $R \times S$ unit transistors M_a, are series-parallel connected at the output and input branch respectively. Unit transistors are identical $M_a \equiv M_b = M_u$ to achieve an effective copy factor $M = S \cdot P/Q \cdot R$. Each M_a, M_b in a generic position i, j in the array show a fluctuation $\Delta\beta_{a(b)ij}$, $\Delta V_{Ta(b)ij}$ resulting in a current mismatch ΔI_{out}.

B. The ACM Model

For the theoretical deductions and simulations, the one-equation-all-region MOSFET model of [15] and [16] is employed because it allows an accurate representation of the series-parallel association. In the ACM model, the drain current I_D is expressed as the difference between the forward (I_F) and reverse (I_R) components

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) = I_S(i_f - i_r) \tag{3}$$

$$I_S = \frac{1}{2}\mu C'_{\text{ox}} n \phi_t^2 (W/L). \tag{4}$$

I_S is the specific current, which is proportional to the aspect ratio W/L of the transistor. V_G, V_S, and V_D are the gate, source, and drain voltages, with reference to the substrate. Here, μ is the effective mobility, ϕ_t is the thermal voltage, and C'_{ox} is the gate oxide capacitance per unit area. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. Note that, in the saturation region, the drain current is almost independent of V_D; therefore, $i_f \gg i_r$ and $I_D \cong I_F$. On the other hand, if V_{DS} is low (linear region), then $i_f \cong i_r$. The inversion level $i_f(i_r)$ represents the normalized carrier charge density at the MOSFET source (drain) Q'_{IS} (Q'_{ID}).

The small-signal transconductances g_m, g_{ms}, g_{md} (gate, source, and drain transconductances) are given by [15], [16]

$$g_{ms} = -\mu \frac{W}{L} Q'_{IS} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_f} - 1\right) \tag{5}$$

$$g_{md} = -\mu \frac{W}{L} Q'_{ID} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_r} - 1\right) \tag{6}$$

$$g_m = \frac{(g_{ms} - g_{md})}{n}. \tag{7}$$

The other small-signal parameters can also be given in terms of the inversion levels. See, for example, [15] for intrinsic capacitances, and [14] for linearity. Recently, noise [17] and mismatch [18] models have also been introduced in terms of the inversion levels.

From now on, for a given transistor M_X (either composite or not), its gate, source, drain transconductances, drain current, inversion level, threshold voltage standard deviation (SD), current factor SD, aspect ratio, and gate area will be noted by g_{mX},

g_{msX}, g_{mdX}, I_{DX}, i_{fX}, $\sigma^2_{V_TX}$, $\sigma^2_{\beta X}$, $(W/L)_X$, and $(WL)_X$, respectively.

II. Series Parallel Current Division/Multiplication and Mismatch

It is widely recognized that the performance of most analog or even digital MOS circuits is limited by random mismatch between transistors. Matching can be modeled by the random variations in geometric, process, and/or device parameters. The approach most employed by designers is to consider only variations in the threshold voltage V_T, and the current factor $\beta = \mu C'_{\rm ox} W/L$. Thus, the threshold voltage and current factor of each one in a small (maybe only two) or large group of matched transistors will not be exactly the same. In this work, ΔV_T and $\Delta\beta$ will note fluctuations measured with respect to the average threshold voltage $\overline{V_T}$ and average current factor $\overline{\beta}$ of the group of matched transistors. For each unit transistor M_X in the group, $V_{TX} = \overline{V_T} + \Delta V_{TX}$ and $\beta_X = \overline{\beta} + \Delta\beta_X$. Fluctuations in V_T and β can be seen as random variations with a normal distribution and an SD given by [19], [20]

$$\sigma^2_{V_T} = \frac{A^2_{V_T}}{2WL}, \quad \frac{\sigma^2_\beta}{\beta^2} = \frac{A^2_\beta}{2WL}. \tag{8}$$

In (8), A_{VT} and A_β are two technology parameters with typical values of A_{VT} = 13-30 mV·μm and A_β = 2-4%·μm [20]. In analog design it is common to express mismatch in terms of δV_T and $\delta\beta$, the difference between V_T and β of two adjacent transistors, thus $\sigma^2_{\delta V_T} = 2\sigma^2_{V_T}$, $\sigma^2_{\delta\beta} = 2\sigma^2_\beta$[20]. Series-parallel association of MOS transistors [21] is a useful circuit technique and can be utilized to obtain improved matching between devices [25]. In Fig. 4(a) two transistors $M_{S(D)}$ are series connected; the equivalent aspect ratio $(W/L)_{eq}$ of the composite transistor is [21]

$$(W/L)_{eq} = \frac{(W/L)_S \cdot (W/L)_D}{(W/L)_S + (W/L)_D}. \tag{9}$$

Equation (9) may be extended to complex combinations of unit transistors to obtain different equivalent transistor geometries. For example, Fig. 4(c) shows measured drain current versus drain voltage for two equivalent transistors: a single unit sized $(W/L)_u = 4\ \mu$m/10 μm, and a 10×10 array of the same transistor [Fig. 4(b)]. The two plots are similar, but, because it has a longer channel, note in the upper detail that the drain-source impedance r_{ds} is much higher in the case of the composite transistor. As a rule of thumb, the output conductance of a given composite transistor will be inversely proportional to the equivalent channel length [16], [21].

The copy factor M in a current mirror is calculated as the ratio between the aspect ratios of transistors, even if $\rm M_A$ and M_B are two transistor arrays. Using (9), in the mirror of Fig. 3

$$\frac{I_{\rm in}}{I_{\rm out}} = \frac{S \cdot P}{R \cdot Q} = M \tag{10}$$

where P, R, Q, and S are the number of unit transistors in series or in parallel in each branch.

Classic current mirrors with a copy factor $M \gg 1$ [as in Fig. 5(a)] are very sensitive to mismatch offset because at the output there is a single transistor M_B, with a reduced area that

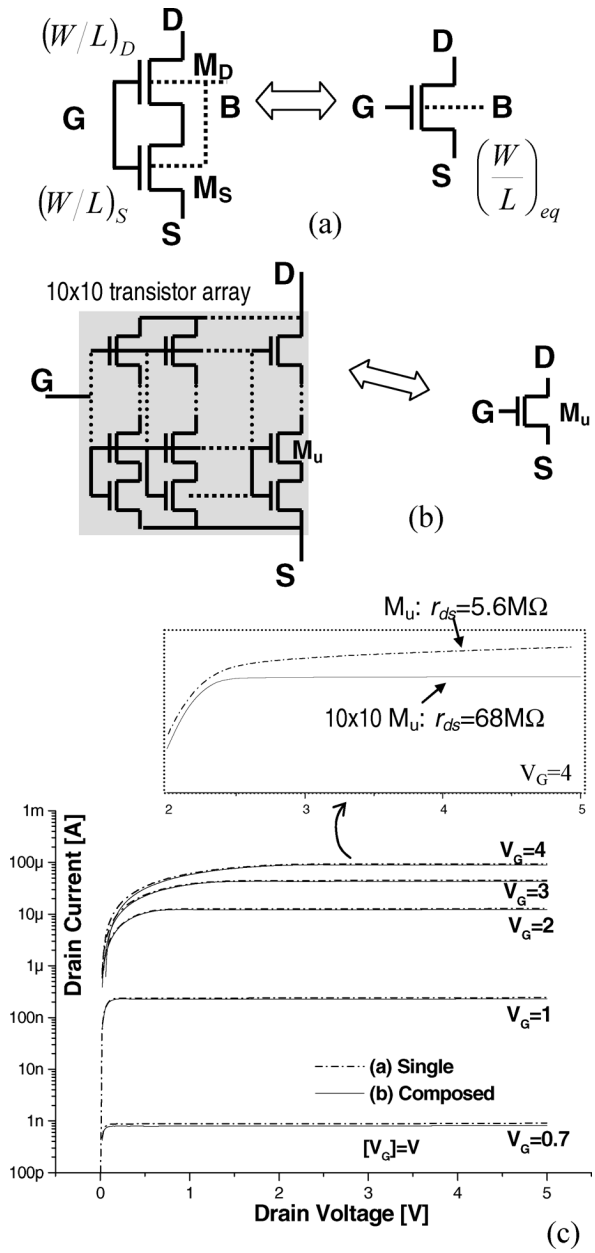

Fig. 4. (a) Two series-connected transistors and their equivalent. (b) A single M_u transistor is equivalent to a 10×10 M_u array. (c) Measured I_D-V_D curves at different gate voltage V_G for single M_u sized $(W/L)_u = 4\ \mu$m/12 μm, and a 10×10 M_u array. At the top, saturation region is magnified for $V_G = 4$ V to observe the change in r_{ds}.

according to (8) presents high variations $\Delta\beta_B$, ΔV_{TB}, in its threshold voltage and current factor. On the other branch, fluctuations $\Delta\beta_{aj}$, ΔV_{Taj} [see Fig. 5(a)] have less impact on the output current because they are noncorrelated so their effect is averaged. The composite transistors of Fig. 5(b) and Fig. 5(c), can be used to implement a current mirror with a copy factor $M = N^2$, but using the same number of unit transistors at both input and output branches of the mirror. A better matching and a reduction in random offset are expected if usual layout matching rules are followed, because a large number of unit transistors have been matched together. In this way, common centroid layout geometry is possible, even for matching composite transistors with very different aspect ratios.

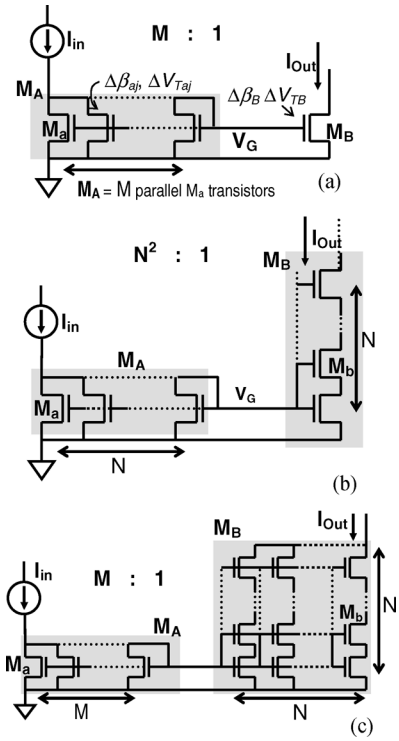

Fig. 5. Three M:1 current copiers. (a) Classic: M unit transistors in parallel, copy to a single unit transistor M_B. (b) $N = \sqrt{M}$ parallel transistors, copy to N series-stacked ones. (c) M parallel unit transistors, copy to a $N \times N$ array. All unit transistors $M_a \equiv M_b = M_u$ are sized $(W/L)_u$.

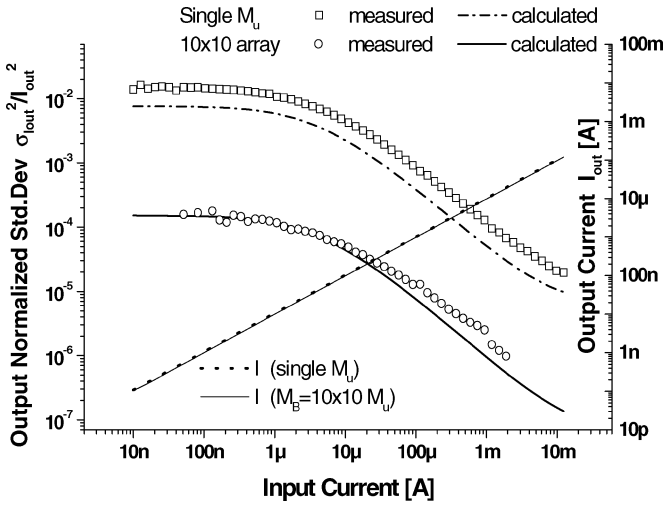

Fig. 6. Calculated and measured $I_{\rm out}$, $\sigma^2_{Iout}/I^2_{\rm out}$ in terms of the input current are shown for a 100:1 nMOS current mirror with the topologies of Fig. 5(a) ($M = 100$) and Fig. 5(c) ($M = 100$, $N = 10$). σ^2_{Iout} value was obtained from 10 samples of the circuit of the same batch.

A. Mismatch Calculation in an SP Mirror

Even with a careful layout, fluctuations $\Delta\beta_{a(b)ij}$, $\Delta V_{Ta(b)ij}$, of each unit transistor $M_{a(b)_{i,j}}$ in Fig. 3 produce an output current error term $\Delta I_{\rm out}$; thus $I_{\rm out} = I_{\rm in}/M + \Delta I_{\rm out}$. The designer—who normally has an equation for mismatch between identical unit transistors—requires a formula to estimate the standard deviation of $I_{\rm out}$. The calculation is immediate when using (8), if the model in (8) is series-parallel consistent, because the composite transistors M_A, M_B, have an area RS and PQ times, respectively, larger than the unit transistor. In effect, assuming known values for the SD in current factor and threshold voltage of composite transistors M_A, M_B of Fig. 3:

$$\sigma^2_{I_{\rm out}} = \frac{g^2_{mB}\cdot I^2_{\rm in}}{g^2_{mA}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_A + I^2_{\rm out}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_B + \frac{g^2_{mB}\cdot I^2_{\rm in}}{g^2_{mA}}\cdot\sigma^2_{V_TA} + g^2_{mB}\cdot\sigma^2_{V_TB}. \quad (11)$$

Equation (11) has been derived propagating to $I_{\rm out}$ the effect of noncorrelated fluctuations $\Delta\beta_A$, ΔV_{TA}, $\Delta\beta_B$ and ΔV_{TB} . Using (8) in (11):

$$\left(\frac{\sigma^2_{I_{\rm out}}}{I^2_{\rm out}}\right) = \left(\frac{1}{RS}+\frac{1}{PQ}\right)\cdot\left[\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{I^2_{\rm out}}\cdot\left(\sigma^2_{V_T}\right)_u\right]. \quad (12)$$

$\left(\sigma^2_\beta/\beta^2\right)_u$, $\left(\sigma^2_{V_T}\right)_u$ are the SD of threshold voltage and current factor for unit transistors. This equation relating the mismatch of an SP mirror to that of unit transistors is general; a careful derivation of (12) that does not assume the model in (8) is presented in the Appendix. The designer can use any mismatch model to calculate $\left(\sigma^2_\beta/\beta^2\right)_u$, $\left(\sigma^2_{V_T}\right)_u$ in (12).

In the example of Fig. 5, three different topologies for a current mirror to perform a M:1 current copy are shown. For a 100:1 copy, the circuit in Fig. 5(a) requires 101 unit transistors, the one in Fig. 5(b) only 20, and 200 are required for the circuit in Fig. 5(c). From (12), the standard deviation in output current fluctuation is $\left(\sigma^2_{Iout}/I^2_{\rm out}\right)_{(a)} \approx 5\left(\sigma^2_{Iout}/I^2_{\rm out}\right)_{(b)} \approx 50\left(\sigma^2_{Iout}/I^2_{\rm out}\right)_{(c)}$. In Fig. 6 calculated and measured $I_{\rm out}$, $\sigma^2_{Iout}/I^2_{\rm out}$ in terms of the input current are shown for a 100:1 nMOS current mirror with the topologies of Fig. 5(a) and (c) ($N = 10$). The σ^2_{Iout} value was obtained from 10 samples of the circuit of the same batch in 0.8 μm technology. Unit transistors were sized $(W/L)_u = 4\ \mu{\rm m}/12\ \mu{\rm m}$, and previously adjusted values for the target technology $A_{VT} = 0.03$ Vμm, $A_\beta = 0.02$ μm, were used for theoretical offset calculation with (8) and (12). A major conclusion is that $\sigma^2_{Iout}/I^2_{\rm out}$ has been substantially reduced in SP mirrors.

III. On the Design of SP Very Low Transconductors

To complete the design of the SP OTAs, some other circuit properties should be studied.

A. Linearity

Linearity in Fig. 1 can be calculated in terms of the inversion level i_{f1} of the input differential pair. The expression is [14]

$$V_{\rm Lin} = 2n\phi_t\sqrt{\frac{6\alpha\left(1+i_{f1}\right)^{3/2}}{3\left(1+i_{f1}\right)^{1/2}-1}} \quad (13)$$

where $V_{\rm Lin}$ is the input linear range defined in terms of an acceptable error α. Linearity is further extended in the case of the input topology in Fig. 2 [13] or others ([4] for example).

B. Offset in the OTA

The input pair M_1, pMOS current mirror transistors M_3, and SP current dividers (12), contribute to offset in the OTA of Fig. 1. Summing their input referred contribution

$$\sigma^2_{V_{off}} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{I^2_{D1}}{g^2_{m1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1\right] + \frac{4I^2_{D1}}{N\cdot g^2_{m1}}\left[\frac{g^2_{m2B}}{I^2_{D2B}}\left(\sigma^2_{V_T}\right)_u + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u\right] + \frac{2I^2_{D1}}{g^2_{m1}}\left[\frac{g^2_{m3}}{I^2_{D3}}\left(\sigma^2_{V_T}\right)_3 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_3\right]. \quad (14)$$

In the case of the linearized pair in Fig. 2, transistors M_4 do not introduce offset because M_4 source-drain voltage is zero at $V_{\text{in}} = 0$. But an extra offset is introduced by the current mirror M_5 and the effect of fluctuations in $M_{1A(B)}$ is slightly different. A new expression for offset is derived with a small-signal analysis:

$$\sigma^2_{V_{off}} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{I^2_{D1}}{g^2_{m1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1\right] + \frac{4I^2_{D1}}{N\cdot g^2_{m\_eff}}\left[\frac{g^2_{m2B}}{I^2_{D2B}}\left(\sigma^2_{V_T}\right)_u + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u\right] + 2\frac{I^2_{D1}}{g^2_{m\_eff}}\left[\frac{g^2_{m3}}{I^2_{D3}}\left(\sigma^2_{V_T}\right)_3 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_3\right] + 2\left[\frac{g^2_{m5}}{g^2_{m\_eff}}\left(\sigma^2_{V_T}\right)_5 + \frac{I^2_{D5}}{g^2_{m\_eff}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_5\right]. \quad (15)$$

Expressions (14) and (15) can be extended to generic SP current division of Fig. 3, changing N by $\sqrt{SP/RQ}$.

C. Noise Analysis

Using the consistent thermal and flicker noise models of [17], the output current noise of the mirror in Fig. 3 is calculated:

$$\frac{S_{I_{\text{out}}th}}{I^2_{\text{out}}} \approx 2nk_BT\left(\frac{g_{mB}}{I_{\text{out}}}\right)\left(\frac{1}{I_{\text{in}}} + \frac{1}{I_{\text{out}}}\right) \quad (16)$$

$$\frac{S_{I_{\text{out}}1/f}}{I^2_{\text{out}}} = \frac{q^2N_{otN}}{nC'^2_{\text{ox}}(WL)_u}\left(\frac{1}{RS} + \frac{1}{PQ}\right)\cdot\frac{g^2_{mB}}{I^2_{\text{out}}}\cdot\frac{1}{f}. \quad (17)$$

$S_{I_{\text{out}}th}, S_{I_{\text{out}}1/f}$, are thermal and flicker noise power spectral densities (PSDs), k_B is the Boltzmann's constant, T is the absolute temperature, $N_{otN(P)}$ are technology parameters for the flicker noise, q is the electron charge. Note that the output noise (like offset) does not significantly increase when using large SP current dividers. The input referred noise can be calculated for the OTA in Fig. 1 using (16), (17). It is assumed that $M \gg 1$ and that $M_{2B(D)}$, M_3 are in weak inversion. Thermal -$v^2_{\text{input\_}th}$-, and flicker -$v^2_{\text{input}(1/f)}$- input referred noise in the OTA are

$$v^2_{\text{input\_}th}(f) \approx \frac{4nk_BT}{G_m}\eta \quad (18)$$

$$v^2_{\text{input\_}f}(f) \approx \frac{2nk_BT}{N^*C'_{\text{ox}}}\left[\frac{N_{otP}}{(WL)_1} + \eta^2\left(\frac{2N_{otN}}{N(WL)_u} + \frac{N_{otP}}{(WL)_3}\right)\right]\frac{1}{f}. \quad (19)$$

$N^* = nC'_{\text{ox}}\phi_t/q$, the factor $\eta = \left(\sqrt{1+i_{f1}}+1\right)$, and $(WL)_1$, $(WL)_u$, and $(WL)_3$ are the gate areas of M_1, M_u, and M_3, respectively. Expressions (18) and (19) are very similar to that obtained for a simple symmetrical OTA, but here we are paying a price in noise for the linearization represented by the factor η. As in (15), these expressions can be extended to calculate input noise in OTAs using the pair of Fig. 2.

D. What is the Minimum Effective G_m Possible With This Technique?

The output branch in Fig. 1 may be biased with a current as low as a few pA or less; the only limitation being the sum of the leakage current at the source (drain) of each series transistor in $M_{2B(D)}$. In the target technology, as well as others examined, leakages in p-doped diffusions are much higher than those in an n-doped diffusion. For this reason all the presented OTAs include a pMOS differential pair, and nMOS series-parallel current mirrors. From manufacturer's data, estimated leakage current in a single source(drain) was $I_{\text{leak}} = 3\,\text{fA}$ for a $4\,\mu\text{m}\times 2\,\mu\text{m}$ n+ diffusion. The selected design criterion is that the sum of all the leakages at the output branch of the current mirror should be at least 10 times less than the bias current in the same branch (equal to I_{D1} divided by N^2)

$$\sum I_{\text{leak}} = N\cdot I_{\text{leak}} < \frac{I_{D1}}{10N^2} \quad (20)$$

which imposes a limit on the minimum achievable transconductance $G_{m\,\min}$. A 15 pS value (equivalent to a 60 GΩ resistor) was estimated for $N = 100$ and $(g_m/I_D)_1 = 5$ at the input pair, that is—although reasonable—an arbitrary worst case condition. A nonarbitrary limit for the minimum achievable transconductance should be examined according to specific restrictions in area, power consumption, and linear range (for example if no restrictions apply, the bias current can be selected as low as necessary to achieve an extremely low transconductance in detriment to the linear range). Using (1) it is possible to rewrite (20):

$$G^{3/2}_{m\,\min} > 10\cdot\left(\frac{g_m}{I_D}\right)^{3/2}_1\cdot I_{\text{leak}}\cdot\sqrt{I_{D1}}. \quad (21)$$

Consider the design of a transconductor with a specified minimum input linear range. Because in a differential pair the linear range is a function of the inversion level (13), the latter is fixed. A fixed i_{f1} in the moderate or strong inversion region (for an enhanced linearity), limits the minimum bias current because an arbitrary large transistor cannot be realized. Thus, examining (21), the minimum G_m value is a function of the circuit topology, desired linear range, and available transistor area.

Finally, as discussed in [11], leakages do not always limit the bottom current range of an MOS transistor. In modern technologies, drain current may be several pA or up to nA order for $V_{GS} = 0$ in minimum size transistors. But, large SP current mirrors as in Fig. 1 are not a problem because they use extremely

TABLE I
SEVERAL DESIGN CHARACTERISTICS OF FABRICATED SP OTAS

OTA	g_{m_pair} [nS]	M (P-Q-R-S)	W_u/L_u [μm/μm]	Area [mm^2]	Power [nW]
G_{m1}	174	72 (2-8-1-18)	4/4	0.04	116
G_{m2}	174	4900 (70-1-1-70)	4/8	0.09	113
G_{m3}	69	28 (5-5-1-28)	4/12	0.15	118
G_{m4}	69	784 (28-1-1-28)	4/12	0.15	113

Input pair transconductance, division factor, divider unit transistor size, area, and power consumption.

long $M_{2B(D)}$ transistors while M_3 transistor layout can be also narrow and long. Since the drain current at very low V_{GS} is still proportional to W/L ratio the designer can push $V_{GS} = 0$ current below leakages, even in the worst case transistors, without using the special circuit techniques in [11].

E. Frequency Response

Input time constant in SP mirrors can be calculated as in [23] using C_{gs} , C_{gb} expressions in terms of the inversion level, and including also gate overlap, and diffusion parasitic capacitances. In usual current mirrors, the input sets cut-off frequency [23], but in SP mirrors several unit transistors at the output may introduce enough parasitics to take them into account. We estimated a 3 fF parasitic for a 4 μm$\times$ 2 μm n+ diffusion in the target process. For $N = 100$ series transistor, a 600 fF capacitance will be distributed along M_{2B}, M_{2D} (Fig. 1). Such analysis is complex and becomes difficult to arrive to a general expresion; a simple rule of thumb for the designer is to place the 600 fF at the output to estimate frequency cut-off of its circuit. In Section IV-B, the 3 dB frequency for several OTAs connected as followers is shown, using a distributed parasitic capacitance model simulation. Because large input transistors were employed to reduce offset, in all cases parasitic capacitance is much small than the input capacitance of the OTA.

IV. DESIGNED OTAS AND LAYOUT TECHNIQUES

Several low and very low transconductance OTAs named G_{m1} to G_{m4} , were fabricated for test purposes. The basic design methodology is that proposed in [14] where the designer starts with a required transconductance G_m and linear range V_{Lin}. Non idealities like noise and offset are addressed using (14) to (19) depending on the topology of the input pair.

G_{m1} is a 35 pS, 160 mV linear range OTA. It uses a $g_{m1} =$ 170 ns differential input pair in the configuration of Fig. 1 (inversion level $i_{f1} = 34$), with an $N^2 = 4900$ division factor. $G_{m2} = 2.35$ nS requires also a 160 mV linear range so the differential pair of G_{m1} is reused with a 9:1 division factor obtained with the topology of Fig. 3 using $P = 8$, $Q = 2$, $R = 1$, $S = 18$. G_{m3}, G_{m4} are both 500 mV linear range OTAs with transconductances of 2.6 nS and 90 pS, respectively. A differential pair, like in Fig. 2 with $g_{m\_eff} = 69$ nS is employed (i_{f1} is still 34 but linear range is enhanced by M_4 transistor operating in the linear region [13]). Division factors are 28:1 in G_{m3}, and 784:1 in G_{m4}. In the former $P, Q, R, S = 28, 1, 5, 5$ and the latter employs 28 parallel transistors copying to 28 series transistors in the current divider. Table I resumes several design characteristics of the OTAs.

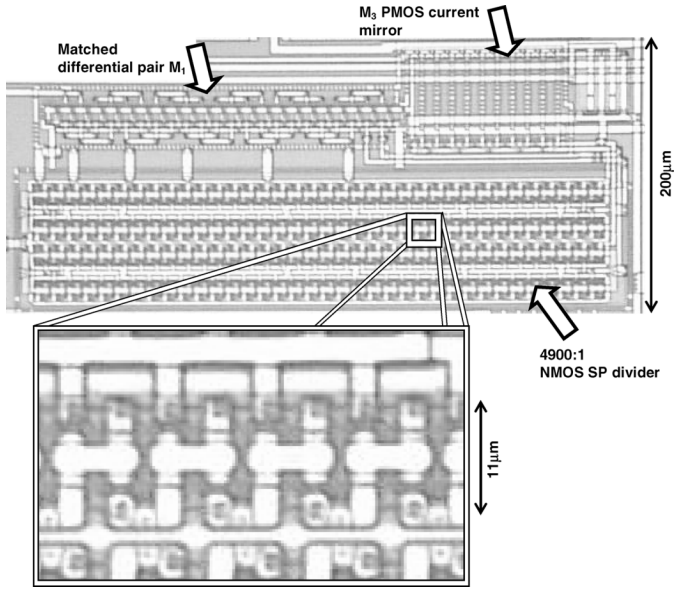

Fig. 7. Photograph of G_{m2} to observe layout techniques.

A. Layout Techniques

A careful layout plays a central role in obtaining a reduced random offset. Series-parallel current mirrors allow to apply usual matching practices [24] (including same orientation, same surroundings, same geometry), to a large number of interleaved unit transistors. In this way the mismatch impact of several effects, not only related to transistor gate area, is reduced (diffussion and etch effects, linear and nonlinear gradients, among others [24]). The layout structure used in this work for matched transistors, whether differential pair or series-parallel current mirrors was in all cases the same: a large row of equal sized transistors placed together at minimum distance, and then connected with metal wires. The layout technique can be seen in the chip photograph of Fig. 7, corresponding to G_{m2}. Particular care was taken to ensure that:

- When matching two arrays M_A, M_B, of transistors, if one unit transistor of the row corresponds to M_A, their neighbors correspond to M_B. If more than two arrays are being matched together, unit transistors are also interleaved.
- Current flow direction is always the same in unit transistors and the usual dummy structures at row ends were incorporated. Symmetry between adjacent transistors is preserved as much as possible even in the layout of the metal wires. This can be observed in the magnified zone of Fig. 7 showing nMOS unit transistors of the 4900 division factor SP mirror.
- No minimum size transistors are employed. Minimum allowed distance is preserved between unit transistors.

The row structure has the following advantages:

- A minimum extra space is used since only two dummies are required to obtain the same surroundings for all unit transistors. The gate-to-silicon area ratio is between 10 to 20% for G_{m1} to G_{m4}.
- Layout blocks are easily reusable since transistor rows can be employed in current mirrors with widely different copy

TABLE II
SEVERAL CHARACTERISTICS OF FABRICATED OTAS

OTA	Transconductance	Linearity [mV]	Offset [mV]	$\text{Offset}_{\text{max}}$ [mV]	Noise [μV_{rms}]	3dB frequency
G_{m1}	2.4nS - 2.6nS	±160	8.0 – 4.4	8.3	48 – 89	1.2kHz
G_{m2}	35pS - 33pS	±160	5.4 – 2.1	4.0	193 –160	12Hz
G_{m3}	2.4nS – 2.8nS	±550	8.8 – 9.1	21	56 – 108	300Hz
G_{m4}	89pS – 100pS	±500	9.0 – 6.8	12	190 – na	10Hz

Transconductance predicted-measured, measured linearity, predicted-measured input offset SD, maximum measured offset (10 circuit samples), predicted – measured input referred noise in the band from .3 – 10Hz, simulated 3dB frequency for the OTA connected as a voltage follower.

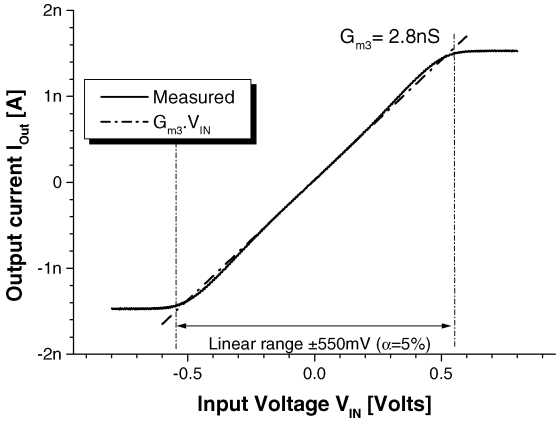

Fig. 8. Measured transfer characteristic of G_{m3}.

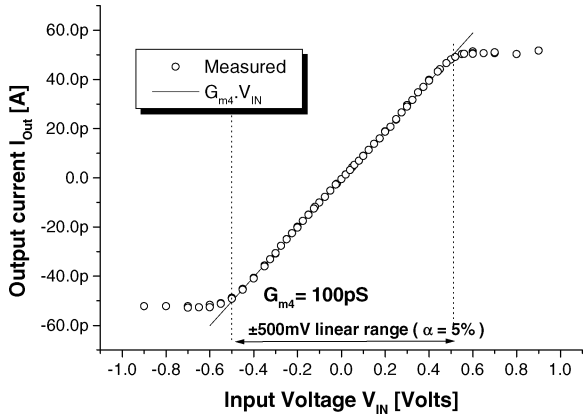

Fig. 9. Measured transfer characteristic of G_{m4}.

factors, or in a differential pair whether linearized or not, just by changing metal wire connections.

— When matching transistor arrays, common centroid geometry is preserved if each array contains the same number of interleaved unit transistors, regardless of the way they are connected.

B. Measurement Results

Several measured characteristics of G_{m1} to G_{m4} are summarized in Table II, while in Figs. 8 and 9, the measured transfer function of G_{m3}, and G_{m4} is shown. Linearity V_{Lin} was measured for a 5% error [14]. The reduced input offset of the OTAs, obtained with a moderate area and nano-power consumption even for G_{m4} of 89 nS with a ±500 mV linear range, should be highlighted. Ten circuit samples from the same batch were

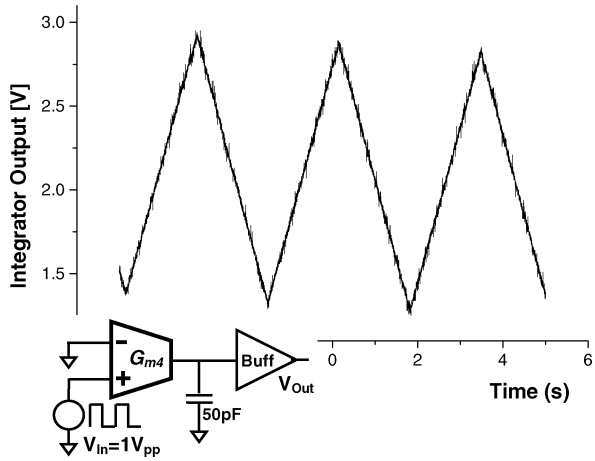

Fig. 10. Measured transient response of a 3.3-s time-constant integrator with a large 1 V_{pp} square wave at the input.

used to calculate σ_{Voff} in Table II. The transfer functions of G_{m1}, and G_{m3} were directly measured using an HP4155 semiconductor parameter analyzer, while the transfer functions of G_{m2}, and G_{m4}, and noise measurements employ the technique described in [11]. Noise figures correspond to the input referred rms voltage integrated in the band from 0.3 to 10 Hz where OTAs are intended to operate. The 3 dB frequency of the last column correspond to the 3 dB output voltage drop, when the OTA is connected as a voltage follower (OTA output and inverting input are the same node).

A 3.3-s time constant integrator, using G_{m4} and a 50 pF capacitor was also fabricated. The integrator occupies a 0.2 mm^2 area. An independently powered unit gain buffer was also incorporated to drive the output pad. The plot of Fig. 10 shows the measured transient response of the circuit to a large 1 V_{pp} square wave at the input. The plot in Fig. 11 shows the frequency response of a low pass filter based on the integrator. The 3 dB decay was measured at 0.302 Hz.

V. A COMPARATIVE SURVEY

As indicated in the introduction, several very low transconductors and large time constant G_m-C filters have been reported. In [4], Sharpeskar *et al.* combine at the input, gate degeneration, bulk driven transistors, and the so-called bump transistor technique, to achieve a transconductor of 10 nS with a linear range of ±1.7 V, a less than 20 mV input offset, and a 1 μW power consumption. In [1] several 10 nS, sub-μW OTAs using different input pair linearization techniques are

TABLE III
COMPARISON OF SEVERAL REPORTED DIVISION TECHNIQUES USED IN VERY LOW TRANSCONDUCTANCE OTAS AND LARGE TIME CONSTANT G_m-C FILTERS

Technique	Reference	Division Factor & Time contant	Offset	Comments
SP Current Division	This work	70 to 4900 3.3s	2 to 9mV SD	Low input noise, good linearity, nW power.
Voltage Division	[2]	Up to 10000 10s	Very large.	Poor linearity, small silicon area, nW power.
SP Current Division	[3]	2200 0.7s	130mV	Large offset probably due to non-symmetrical SP copy.
Capacitive Scaling & Others.	[6]	1.2s	~20mV	4th order, 1-5Hz tunable band-pass filter. ~25μW power.
Current Division/Cancellation.	[5]	1000 100ms	40mV*	10pF capacitors employed.

*random offset + 80mV systematic offset.

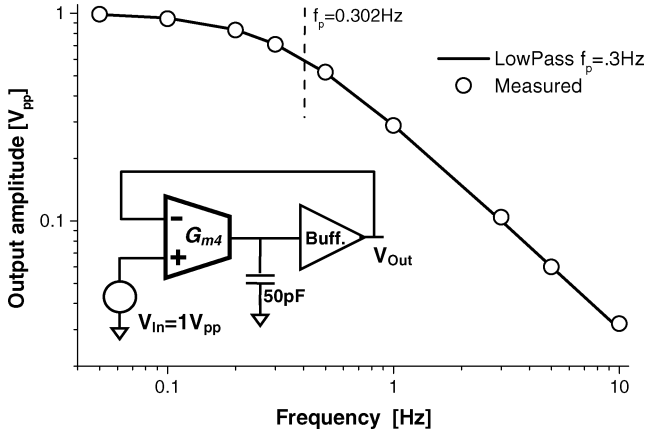

Fig. 11. Measured transfer function of the 3.3-s time constant integrator.

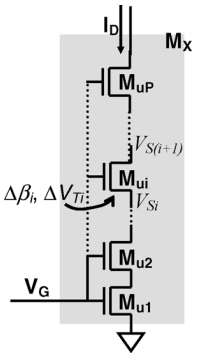

Fig. 12. A number P of series-stacked unit transistors.

compared; unfortunately no offset measurements are presented. These OTAs require the addition of some kind of division technique, like the one presented here, to achieve few Hertz or sub-Hertz range G_m-C filters. Techniques may include voltage attenuation [2], [7], capacitor scaling [9], [22], or current division/cancellation [3], [5]. Table III gives some previously reported very large time constant integrators and filters, all of them incorporating some kind of division scheme. Although the comparative study is difficult because linearity, noise, and particularly, offset, are not always measured in the same way, it is possible to conclude that the technique here presented is very efficient regarding mismatch, power consumption, and noise, without a significant overhead in silicon area.

VI. CONCLUSION

A general expression was introduced to estimate mismatch offset in series-parallel current mirrors. Extremely large current multiplication (division) factors can be obtained by means of SP mirrors, without a significant loss in terms of area, offset, or noise. Series-parallel division of current was applied in symmetrical OTAs to achieve very low transconductances with extended linear range. Sample OTAs ranging from 35 pS to 2.8 nS, and a 3.3-s time constant G_m-C integrator were designed, fabricated, and tested. The designed circuits demonstrate a very good trade-off in terms of occupied area, power consumption, linearity, noise, and input offset. All the OTAs consume around 100 nW power, and have a measured input referred offset standard deviation of less than 10 mV.

APPENDIX

In this Appendix, small-signal analysis is carried out for V_T, β fluctuations in all individual transistors of the circuit in Fig. 3. Firstly, consider in Fig. 12, a composite transistor M_X formed by a large number P of series-stacked unit transistors M_{ui}. ΔV_{Ti}, $\Delta\beta_i$ fluctuations on unit transistors affect the drain current I_{Di} and their node voltages. For each M_{ui} it is possible to write

$$\begin{aligned}\Delta I_{Di} &= \frac{\partial I_{Di}}{\partial V_{Ti}}\cdot\Delta V_{Ti} + \frac{I_{Di}}{\beta_i}\Delta\beta_i + \frac{\partial I_{Di}}{\partial V_{Si}}\cdot\Delta V_{Si} \\ &\quad + \frac{\partial I_{Di}}{\partial V_{Di}}\cdot\Delta V_{S(i-1)} \\ &= -g_{m_i}\Delta V_{Ti} + \frac{I_D}{\beta_i}\Delta\beta_i - g_{ms_i}\Delta V_{Si} + g_{md_i}\Delta V_{S(i-1)}\end{aligned} \tag{22}$$

where g_{m_i}, g_{ms_i}, g_{md_i} are gate, source, and drain transconductances of M_{ui}, respectively. Equation (22) has been derived for a generic transistor but $\Delta I_{Di} = \Delta I_D$ is constant, because the

transistors are series connected. Also, because transistors are series connected $Q'_{ID_i} = Q'_{IS_{(i-1)}}$ then $g_{ms_{(i-1)}} = g_{md_i}$ from (5), (6). Summing (22) for all the series transistors

$$P\Delta I_D = \sum_{i=1}^{P} I_D \frac{\Delta\beta_i}{\beta} - \sum_{i=1}^{P} g_{m_i} \cdot \Delta V_{Ti}. \tag{23}$$

Assuming that ΔV_{Ti}, $\Delta\beta_i$ are noncorrelated, and that $\sigma^2_{\beta_i}$, $\sigma^2_{V_T i}$ do not depend on i, we obtain

$$\begin{aligned}\sigma^2_{\Delta I_D} &= \frac{I_D^2}{P} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{\left(\sigma^2_{V_T}\right)_u}{P^2} \cdot \sum_{i=1}^{P} g^2_{m_i} \\ &\approx \frac{I_D^2}{P} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mX}}{P}\left(\sigma^2_{V_T}\right)_u. \end{aligned} \tag{24}$$

The result of the sum in (24) is not exact, it uses $\sum_{i=1}^{P} g^2_{m_i} \approx P \cdot g^2_{mX}$. This approximation assumes $P = \infty$ differential-length series transistors, and the integration procedure, and approximations in [26]

$$\begin{aligned}\sum_{i=1}^{P} g^2_{m_i} &\approx \frac{P}{L}\int_0^L g^2_m(x)\cdot dx \\ &= \frac{P\cdot\mu W I_D C'_{\text{ox}}}{nL}\int_{Q'_{IS}}^{Q'_{ID}} \frac{1}{nC'_{\text{ox}}\phi_t - Q'_I}\cdot dQ'_I \\ &\approx P\cdot g_{mB}. \end{aligned} \tag{25}$$

If a $P \times Q$ transistor array like the M_B in Fig. 3 is now introduced, fluctuations are calculated summing (24) for the parallel branches; $g_{mB} = Q \cdot g_{mX}$ and drain current is Q times larger:

$$\sigma^2_{I_D} = \frac{I_D^2}{PQ} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{PQ}\left(\sigma^2_{V_T}\right)_u. \tag{26}$$

Drain current is fixed in M_A of Fig. 3, so (26) could be better expressed in this case, as a fluctuation in V_G:

$$\sigma^2_{V_G} = \frac{I^2_{\text{in}}}{g^2_{mA}\cdot RS} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{1}{RS}\left(\sigma^2_{V_T}\right)_u. \tag{27}$$

This V_G fluctuation is then propagated to the output through M_B. Also, (26) should be summed to calculate total output current SD in Fig. 3.

$$\begin{aligned}\frac{\sigma^2_{I_{\text{out}}}}{I^2_{\text{out}}} = \frac{g^2_{mB}\cdot I^2_{\text{in}}}{g^2_{mA}\cdot PQ} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{PQ}\left(\sigma^2_{V_T}\right)_u \\ + \frac{I^2_{\text{in}}}{RS} \cdot \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{RS}\left(\sigma^2_{V_T}\right)_u. \end{aligned} \tag{28}$$

Because M_A, M_B have the same specific current then $g_{mA}/I_{\text{in}} = g_{mB}/I_{\text{out}}$ [20] . It follows that

$$\left(\frac{\sigma^2_{I_{\text{out}}}}{I^2_{\text{out}}}\right) = \left(\frac{1}{RS} + \frac{1}{PQ}\right) \cdot \left[\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{I^2_{\text{out}}} \cdot \left(\sigma^2_{V_T}\right)_u\right]. \tag{29}$$

It should be pointed out that the derivation of (29) does not assume a specific mismatch model for the MOS transistor. Either another expression for $\left(\sigma^2_\beta/\beta^2\right)_u$, $\left(\sigma^2_{V_T}\right)_u$ can be used instead of (8), or the development in the appendix can be extended to a mismatch model that considers fluctuations in other transistor parameters such as those proposed in [27] and [28].

REFERENCES

[1] A. Veeravalli, E. Sánchez-Sinencio, and J. Silva-Martínez, "Transconductance amplifiers structures with very small transconductances: A comparative design approach," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 770–775, Jun. 2002.

[2] R. Rieger, A. Demosthenous, and J. Taylor, "A 230-nW 10-s time constant CMOS integrator for an adaptive nerve signal amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1968–1975, Nov. 2004.

[3] P. Kinget, M. Steyaert, and J. Van der Spiegel, "Full analog CMOS integration of very large time constants for synaptic transfer in neural networks," *Analog Integrated Circuits and Signal Processing*, vol. 2, no. 4, pp. 281–295, Jul. 1992.

[4] R. Sarpeshkar, R. F. Lyon, and C. Mead, "A low-power wide-linear-range transconductance amplifier," *Analog Integrated Circuits and Signal Processing*, vol. 13, pp. 123–151, May 1997.

[5] J. Silva-Martínez and J. Salcedo-Suñer, "IC voltage to current transducers with very small transconductance," *Analog Integrated Circuits and Signal Processing*, vol. 13, pp. 285–293, Jul. 1997.

[6] A. Veeravalli, E. Sánchez Sinencio, and J. Silva Martínez, "A CMOS transconductance amplifier architecture with wide tuning range for very low frequency applications," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 776–781, Jun. 2002.

[7] C. D. Salthouse and R. Sarpeshkar, "A practical micropower programmable bandpass filter for use in bionic ears," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 63–70, Jan. 2003.

[8] A. Becker-Gómez, U. Cilingiroglu, and J. Silva Martínez, "Compact sub-Hertz OTA-C filter design with interface-trap charge pump," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 929–934, Jun. 2003.

[9] S. Solis Bustos, J. Silva Martínez, F. Maloberti, and E. Sánchez Sinencio, "A 60 dB dynamic range CMOS sixth-order 2.4 Hz low-pass filter for medical applications," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 1391–1398, Dec. 2000.

[10] P. Furth and A. Andreou, "Linearized differential transconductors in subtreshold CMOS," *Electron. Lett.*, vol. 31, no. 7, pp. 545–547, Mar. 1995.

[11] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.

[12] E. Sánchez Sinencio and J. Silva Martínez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," *IEE Proc. Circuits Devices Syst.*, vol. 147, no. 1, Feb. 2000.

[13] F. Krummenacher and N. Joehl, "A 4-Mhz CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 750–758, Jun. 1988.

[14] A. Arnaud and C. Galup-Montoro, "Pico-A/V range CMOS transconductors using series-parallel current division," *Electron. Lett.*, vol. 39, no. 18, pp. 1295–1296, Sep. 2003.

[15] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[16] C. Galup-Montoro, M. C. Schneider, and A. I. A. Cunha, "A current-based MOSFET model for integrated circuit design," in *Low-Voltage/ Low-Power Integrated Circuits and Systems*, E. Sánchez-Sinencio and A. Andreou, Eds. New York: IEEE Press, 1999, ch. 2.

[17] A. Arnaud and C. Galup Montoro, "Consistent noise models for analysis and design of CMOS circuits," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 10, pp. 1909–1915, Oct. 2004.

[18] C. Galup-Montoro, M. C. Schneider, H. Klimach, and A. Arnaud, "A compact model of MOSFET mismatch for circuit design," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1649–1657, Aug. 2005.

[19] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1440, Oct. 1989.

[20] P. Kinget and M. Steyaert, *Analog VLSI Integration of Massive Parallel Signal Processing Systems*. Boston, MA: Kluwer Academic, 1996.

[21] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1094–1101, Sep. 1994.
[22] J. Silva Martínez and A. Vázquez González, "Impedance scalers for IC active filters," in *Proc. IEEE ISCAS*, 1998, vol. I, pp. 151–154.
[23] A. Emira, E. Sanchez-Sinencio, and M. Schneider, "Design tradeoffs of CMOS current mirrors using one-equation for all-region model," in *Proc. IEEE ISCAS*, 2002, vol. 5, pp. 45–48.
[24] A. Hastings, *The Art of Analog Layout*. Upper Saddle River, NJ: Prentice Hall, 2001, pp. 426–442.
[25] R. Fiorelli, A. Arnaud, and C. Galup-Montoro, "Series-parallel association of transistors for the reduction of random offset in nonunity gain current mirrors," in *Proc. IEEE ISCAS*, 2004, vol. 1, pp. 881–884.
[26] A. Arnaud and C. Galup-Montoro, "A compact model for flicker noise in MOS transistors for analog circuit design," *IEEE Trans. Electron Devices*, vol. 50, pp. 1815–1818, Aug. 2003.
[27] T. Serrano-Gotarredona and B. Linares-Barranco, "CMOS transistor mismatch model valid from weak to strong inversion," in *Procs. ESSCIRC*, Sep. 2003, pp. 627–630.
[28] P. G. Drennan and C. C. McAndrew, "Understanding MOSFET mismatch for analog design," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 450–456, Mar. 2003.

Alfredo Arnaud (M'97) received the M.S. and Ph.D. degree in electronics from the Universidad de la República, Montevideo, Uruguay, in 2000 and 2004.

Since 1997, he was involved in several research and industrial projects in the field of CMOS analog design and optoelectronics. Since 2004, he has been with the Electrical Engineering Department, Universidad Católica, Montevideo, Uruguay. His current research interests include high-performance circuits for implantable medical devices and analog signal processing and MOS transistor modeling.

Rafaella Fiorelli (S'05) received the B.Sc. and M.Sc. degrees in electrical engineering from the Universidad de la República (UdelaR), Montevideo, Uruguay, in 2002 and 2005, respectively. She is currently working towards the Doctoral degree in electrical engineering.

In 2003, she joined the Electrical Engineering Institute of the UdelaR, where she is now Assistant. Her current research includes low power consumption in analog CMOS circuits and radio frequency.

Carlos Galup-Montoro (M'89) studied engineering sciences at the University of the Republic, Uruguay, and received the Engineer degree in electronics and the Doctor Engineer degree from the Institut National Polytechnique de Grenoble, France, in 1979 and 1982, respectively.

From 1982 to 1989, he was with University of São Paulo, São Paulo, Brazil, where he was involved in bipolar and MOS analog design. Since 1990, he has been with the Electrical Engineering Department, Federal University of Santa Catarina, Florianopolis, Brazil. His main research interests are device modeling and transistor-level design.