Fully Integrated Inductive Ring Oscillators Operating at V_{DD} below *2kT/q*

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Abstract — This paper presents two fully integrated inductive ring oscillators that operate with supply voltages below *2kT/q* for energy harvesting applications. Expressions for the oscillation frequency as well as the minimum transistor gain and supply voltage required for the starting up of oscillations are derived for each topology. The experimental results for two cross-coupled oscillators, with topologies comprised of a single-inductor and two-inductors per stage, are presented. The two oscillators operate with supply voltages as low as V_{DD} = 46 mV at 11.5 µW DC power and V_{DD} = 31 mV at 15 µW DC power, respectively, thus confirming the extremely low voltage operation of the prototypes integrated in a 130 nm technology.

Keywords — **Ultra-low-voltage, MOSFET ultra-low-voltage analog circuits, minimum supply voltage, energy harvesting, zero-VT transistor, ring oscillator, cross-coupled oscillator.**

1 Introduction

Motivated mainly by the need for low power consumption, reducing the supply voltage of the MOS electronic circuits has been a research aim since long time ago. In recent years, digital blocks operating at around or below *4kT/q*, as shown in [1, 2], have pushed the limit of the supply voltage closer to the Meindl limit of *2kT/q*ln(1+*n*) [3], where *k* is the Boltzmann constant, *T* is the absolute temperature, *q* is the electron charge, and *n* is the transistor slope factor. Recently, the need for alternative ways to generate power has motivated a search for further reductions in the minimum operating voltage of key analog blocks, such as rectifiers and oscillators, some of them [4, 5] operating from supply voltages below the Meindl limit for digital circuits.

Emerging applications, such as wireless sensor networks and wearable devices for medical or lifestyle purposes, require energy autonomy. Harvesting power from the environment using ultra-low-voltage (ULV) power sources, such as thermoelectric generators (TEGs), photovoltaic cells and glucose fuel cells, is an interesting approach to addressing the energy needs of these recent applications. Body-worn TEGs typically generate voltages as low as a couple of tens of mV, whereas a photovoltaic cell in the dark provides voltages of

around 100 mV [6]. A recent paper presented glucose fuel cells that generate voltages ranging from around 100 mV to 200 mV when implanted in the human body [7]. In general, in order to be appropriate for use with current electronics, all of these exciting power sources need a circuit to boost the voltage generated to a higher level.

In recent studies, ULV DC-DC converter topologies, one of which is shown in Fig.1, based on either inductive boost or charge pump converters [6, 8, 9], have been used to increase the voltage levels available from low-voltage sources. A major design challenge in ULV DC-DC converters, regardless of the topology, is to generate a signal to either turn on and off the MOS switch of an inductive boost topology or control the charge transfer of a charge pump. In order to boost the incoming voltage, some start-up solutions have been proposed, such as the use of previously-charged capacitors or batteries [8], mechanical switches [9] or an oscillator tuned after fabrication which operates at voltages above 90 mV [6]. However, a fully-integrated electronic solution which can start up with around 50 mV is not available yet.
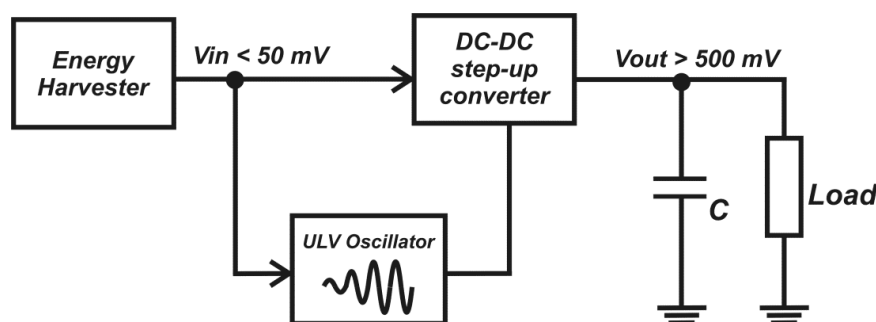
Figure 1. Step-up converter topology used with ULV energy harvested sources.

In this paper, we present the analysis, design and testing of two ULV oscillator topologies, namely the inductive ring oscillator (IRO) and the enhanced-swing ring oscillator (ESRO), both of which are suitable for energy harvesting applications, due to their low operating voltages. Experimental results for oscillators carefully laid out in a 130 nm technology demonstrated that the IRO and ESRO can operate with supply voltages as low as $2kT/q$ and $1.2kT/q$, respectively, even when using integrated inductors with quality factors of around 10.

In the design of both oscillators, zero-threshold voltage (zero-VT) MOS transistors were employed as the active devices due to their high drive capability and sufficient voltage gain at low voltages [10].

This paper is organized as follows. The inductive ring oscillator topology and the enhanced-swing ring oscillator are presented in Sections 2 and 3, respectively. Section 4 describes the design and the experimental results obtained for the two oscillators developed. Section 5 summarizes the main results of this study and details the conclusions.

2 The Inductive Ring Oscillator – IRO

Starting up a conventional ring oscillator with a power supply below 100 mV is extremely difficult [11]. The minimum value of the supply voltage, $V_{DD,min}$, is usually limited by the imbalance of the threshold voltage of PMOS/NMOS transistors of the logic inverter caused by within-die and die-to-die variations [11]. In order to arrive at an oscillator that starts up from a $V_{DD,min}$ value lower than that of the conventional ring oscillator, one can use the inductive ring oscillator topology shown in Fig. 2 [12]. This topology, which

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replaces the PMOS transistor of logic inverters with an inductor, can not only reduce $V_{DD,min}$ but also boost the amplitude of the oscillations beyond the supply voltage.
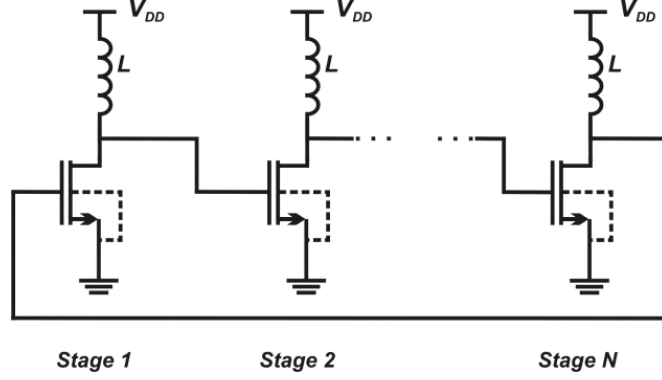

Figure 2. Schematic diagram of an N stage inductive ring oscillator [12.

The analysis of the IRO is based on the simplified small-signal equivalent circuit of a single stage of the IRO shown in Fig. 3, where g_m and g_{md} represent the gate and drain transconductances, respectively, C is the sum of all capacitances between the drain node and the ac ground, and G_P models the inductor losses. For the sake of simplicity, here we assume that the drain-to-gate capacitance C_{gd} is negligible; the complete analysis of the IRO including C_{gd} can be found in Appendix A. The transfer function of the single stage in Fig. 3 is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{g_{md}+G_P}\frac{1}{1-j\tan\phi} \tag{1}$$

$$\tan\phi = \frac{1-LC\omega^2}{\omega L\left(g_{md}+G_p\right)} \tag{2}$$

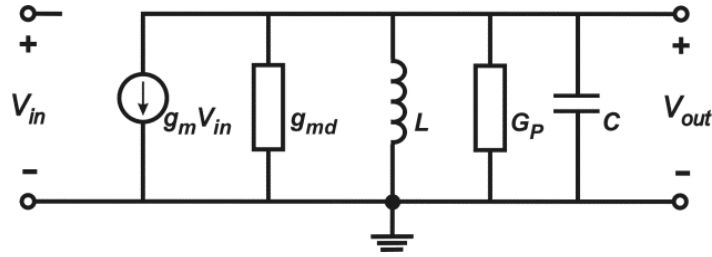where ϕ is the phase shift between the output and the input.

Figure 3. Simplified small-signal model of a single stage of the inductive ring oscillator.

The condition of loop gain equal to unity for oscillation requires the phase shift ϕ between two contiguous stages to be $\phi=2k\pi/N$, where N is the number of stages and k is an integer. Except for N=2 and 4, more than one value of the phase shift for the transfer function given by (1), *e.g.* $\phi=2\pi/3$ and $\phi=4\pi/3$ for N=3, satisfies the phase condition required for oscillation. However, as explained in [13], the circuit will oscillate at the frequency for which the voltage gain is highest. In the case of an even number of stages, the phase shift for oscillation is $\phi=\pi$, while for the case of an odd number of stages $\phi=(N-1)\pi/N$. Thus, once the number of oscillator stages has been decided upon, the phase-shift between two contiguous stages of the oscillator is found. Therefore, from (2), we can calculate the oscillation frequency ω as

$$\frac{\omega}{\omega_o} = \sqrt{1+\frac{\left(\tan\phi\right)^2}{4Q^2}} - \frac{\tan\phi}{2Q} \tag{3}$$

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where $\omega_o = 1/\sqrt{LC}$ is the resonant frequency of the LC tank and $Q=1/(g_{md}+G_P)\omega_0 L$ is the quality factor of the stage. Note that when the condition $\phi=\pi$ holds, which is the case for an even number of stages, ω equals ω_0.

The dispersion relation of a stage, which shows the dependence of ω/ω_0 on ϕ, is shown in Fig. 4. It is clear that, for $Q > 100$, we have $\omega/\omega_0 \cong 1$.
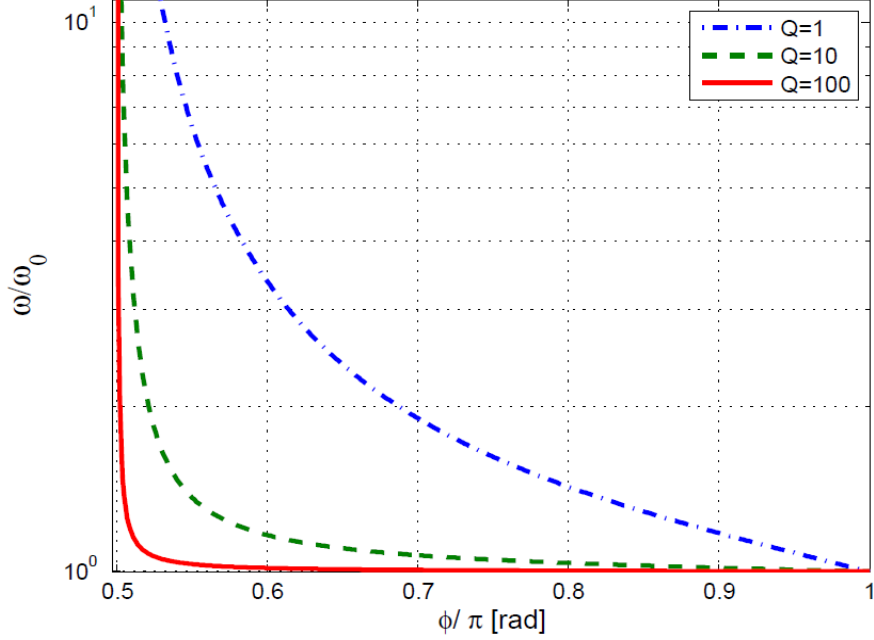

Figure 4.   The dispersion relation of a single stage of the inductive ring oscillator for different quality factors.

The requirement of gain greater than unity for the starting up of oscillations is satisfied for

$$\frac{g_m}{g_{md}+G_P}\frac{1}{\sqrt{1+(\tan\phi)^2}} > 1 \tag{4}$$

Since the relation between source, drain and gate transconductances, g_{ms}, g_{md}, and g_m, respectively, is $g_m=(g_{ms}-g_{md})/n$ [14], where n is the transistor slope factor, the minimum transistor gain g_{ms}/g_{md} required for oscillation is obtained from (4) as

$$\frac{g_{ms}}{g_{md}} = 1+n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right) \tag{5}$$

From the MOSFET model [14] described in Appendix B and the condition given by (5), it is possible to calculate the minimum supply voltage required for the start-up of the oscillator. Thus, from the expression for the drain-source voltage (V_{DS}) in Appendix B we have

$$\frac{V_{DS}}{\phi_t} = \frac{\phi_t}{2I_S}g_{md}\left(\frac{g_{ms}}{g_{md}}-1\right)+\ln\frac{g_{ms}}{g_{md}} \tag{6}$$

For each transistor in Fig. 2 we have the following dc values: $V_S=V_B=0$ and $V_G=V_D=V_{DD}$. We note from (6) that, for a fixed g_{md}, the minimum V_{DS} ($=V_{DD}$) is reached for the minimum value of the g_{ms}/g_{md} ratio given in (5). Thus, based on (5) and (6) we find that the minimum supply voltage required to start up the oscillator is

$$V_{DD} = \frac{\phi_t^2}{2I_S}ng_{md}\left(1+\frac{G_P}{g_{md}}\right)\sqrt{1+(\tan\phi)^2}+\phi_t\ln\left[1+n\sqrt{1+(\tan\phi)^2}\left(1+\frac{G_P}{g_{md}}\right)\right] \tag{7}$$

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Assuming that the transistor operates in weak inversion and that the inductor losses are negligible, the voltage supply limit of (7) is given by

$$V_{DD} = \phi_t \ln(1+n) \tag{8}$$

for the case of an even number of stages. Assuming that $n=1$, the limit given by (7) is around 18 mV at room temperature. This limit shows that the circuit can theoretically operate with one half the value of the Meindl limit [3] of digital circuits, which for a CMOS inverter is 36 mV at room temperature. This result was to be expected since the condition required for oscillation of a ring oscillator with an even number of stages (loaded with an infinite-Q tank) is that the voltage gain of the transistor equals unity. The unity gain of a transistor operating in weak inversion is obtained for a power supply of 18 mV at room temperature [10].

3 The Enhanced-Swing Ring Oscillator – ESRO

A variation of the IRO topology is shown in Fig. 5. Thanks to the inclusion of a second inductor L_2 in each stage, the ESRO topology can extend the oscillation beyond the supply voltage even operating with very low supply voltages.
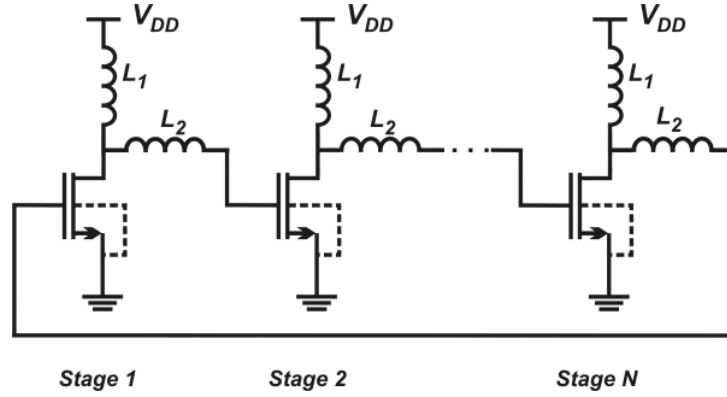

Figure 5.   Schematic diagram of an *N*-stage enhanced-swing ring oscillator (ESRO).

The simplified small-signal equivalent circuit of a single stage of the ESRO is shown in Fig. 6, where R_{S2} represents the series resistance of inductor L_2, G_{p1} is the parallel conductance of L_1, and the other symbols have the same meaning as in Fig. 3.
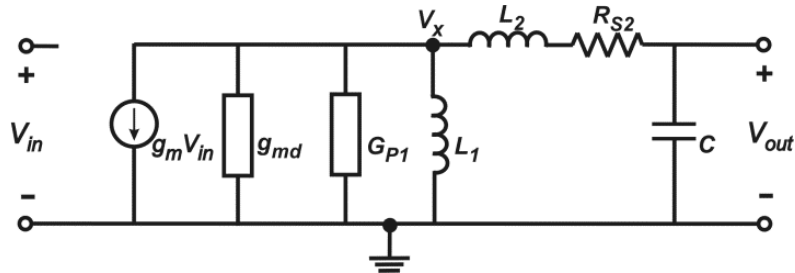

Figure 6.   Simplified small-signal model of a single stage of the ES inductive-load ring oscillator.

The transfer function of the single stage in Fig. 6 is

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{sC + \left(g_{md} + G_{p1} + \frac{1}{sL_1}\right)\left(L_2 Cs^2 + R_{S2} Cs + 1\right)} \tag{9}$$

which, for $s=j\omega$, becomes

$$\frac{V_{out}}{V_{in}} = -\frac{g_m}{\left(g_{md}+G_{p1}\right)\left(1-L_2C\omega^2\right)+\dfrac{R_{S2}C}{L_1}}\frac{1}{1+j\left(\dfrac{\left[L_1+L_2+L_1R_{S2}\left(g_{md}+G_{P1}\right)\right]C\omega^2-1}{\left(g_{md}+G_{P1}\right)\omega L_1\left(1-L_2C\omega^2\right)+R_{S2}C\omega}\right)} \tag{10}$$

The phase shift ϕ between V_{out} and V_{in} calculated from (10) is

$$\phi = \pi - \tan^{-1}\left(\frac{\left[L_1+L_2+L_1R_{S2}\left(g_{md}+G_{P1}\right)\right]C\omega^2-1}{\left(g_{md}+G_{P1}\right)\omega L_1\left(1-L_2C\omega^2\right)+R_{S2}C\omega}\right) \tag{11}$$

Considering, for the sake of simplicity, the case of a ring oscillator with an even number of stages ($\phi=\pi$), we can calculate the oscillation frequency from (11) as

$$\omega = \frac{1}{\sqrt{\left[L_1+L_2+L_1R_{S2}\left(g_{md}+G_{P1}\right)\right]C}} \tag{12}$$

which, for lossless inductors, reduces to

$$\omega = \frac{1}{\sqrt{\left(L_1+L_2\right)C}} \tag{13}$$

From (10), the greater-than-unity gain required to start up oscillations is achieved for

$$g_m > \left[\left(g_{md}+G_{P1}\right)\left(1-L_2C\omega^2\right)+\frac{R_{S2}C}{L_1}\right]\sqrt{1+\left(\tan\phi\right)^2} \tag{14}$$

Rewriting the inductor losses of L_2 as a parallel conductance G_{P2} and assuming that the inductor Q is high and that the resonant frequency can be approximated by (13), we can write (14) as

$$g_m > \left[\left(g_{md}+G_{P1}\right)\frac{1}{1+K_L}+G_{P2}\frac{K_L^2}{1+K_L}\right]\sqrt{1+\left(\tan\phi\right)^2} \tag{15}$$

where $K_L = L_2/L_1$. Rewriting (15) in terms of g_{ms} and g_{md}, the transistor gain required for oscillation must satisfy

$$\frac{g_{ms}}{g_{md}} > 1 + \left[n\left(1+\frac{G_{P1}}{g_{md}}\right)\frac{1}{1+K_L}+n\frac{G_{P2}}{g_{md}}\frac{K_L^2}{1+K_L}\right]\sqrt{1+\left(\tan\phi\right)^2} \tag{16}$$

The curves in Fig. 7 represent the minimum gain g_{ms}/g_{md} calculated from (16) for the case in which the quality factors of the inductors are equal, i.e. $G_{P1}/G_{P2}=L_2/L_1$, $n=1$, and the practical case of an even number of stages ($\phi=\pi$). As is clear from Fig. 7, there is an optimum value for the L_2/L_1 ratio that minimizes the ratio of the transconductances required for oscillation. The value for L_2/L_1 that minimizes the right-hand side of (16), for $G_{P1}/G_{P2}=L_2/L_1$, is

$$K_{L,opt} = \left.\frac{L_2}{L_1}\right|_{opt} = \frac{1}{2}\left(\sqrt{1+\frac{4g_{md}}{G_{P2}}}-1\right) \tag{17}$$
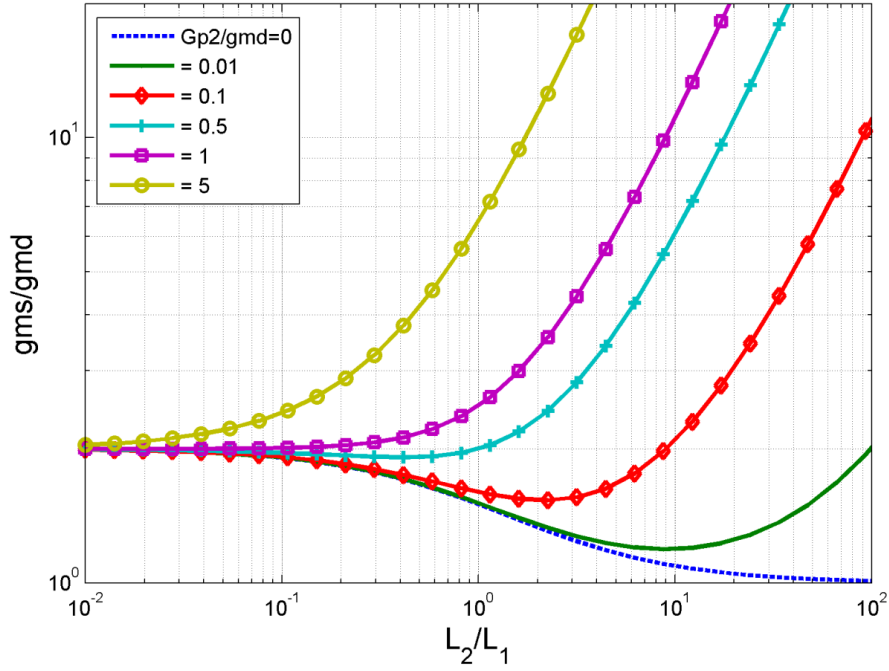
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Figure 7. Minimum transistor intrinsic gain (to start up oscillations) versus L_2/L_1 ratio with G_{P2}/g_{md} as a parameter. The inductors are assumed to have equal quality factors.

Using (17) in order to minimize the required gain g_{ms}/g_{md}, we find that

$$\left.\frac{g_{ms}}{g_{md}}\right|_{opt} = 1 + \frac{2n}{1 + K_{L,opt}} \tag{18}$$

Finally, the limit for the minimum supply voltage of the topology can be calculated assuming that the transistor operates in weak inversion and the resonant frequency can be approximated by (13), which yields

$$V_{DD,opt} = \phi_t \ln \left.\frac{g_{ms}}{g_{md}}\right|_{opt} = \phi_t \ln\left(1 + \frac{2n}{1 + K_{L,opt}}\right) \tag{19}$$

If $K_L = L_2/L_1 \gg 1$, the voltage gain of the transistor can be (much) lower than unity, but at the expense of a high g_{md}/G_{p2} ratio, as equation (17) shows. Thus, for high values of L_2/L_1 the ESRO is capable of oscillating at supply voltages well below the thermal voltage.

Figure 8 shows the calculated values for the minimum supply voltage as a function of both the number of stages and the type of topology, IRO or ESRO, using the parameters of devices in a 130 nm technology. The $V_{DD,min}$ value for the IRO was calculated from (7), while for the ESRO it was calculated by substituting (16) in (6). For the IRO topology, zero-VT transistors with $W/L=250\mu m/0.42\mu m$ and $L=100$ nH ($Q \approx 8$ at 500 MHz) were employed. For the ESRO, zero-VT transistors with $W/L=1000\mu m/0.42\mu m$, $L_1=22$ nH ($Q_1 \approx 11$ at 500 MHz), and $L_2=100$ nH ($Q_2 \approx 8$ at 500 MHz) were used for the calculations. As can be readily noted, the ESRO is capable of starting up at a V_{DD} significantly lower than that for the IRO, but at the expense of an additional inductor per stage.
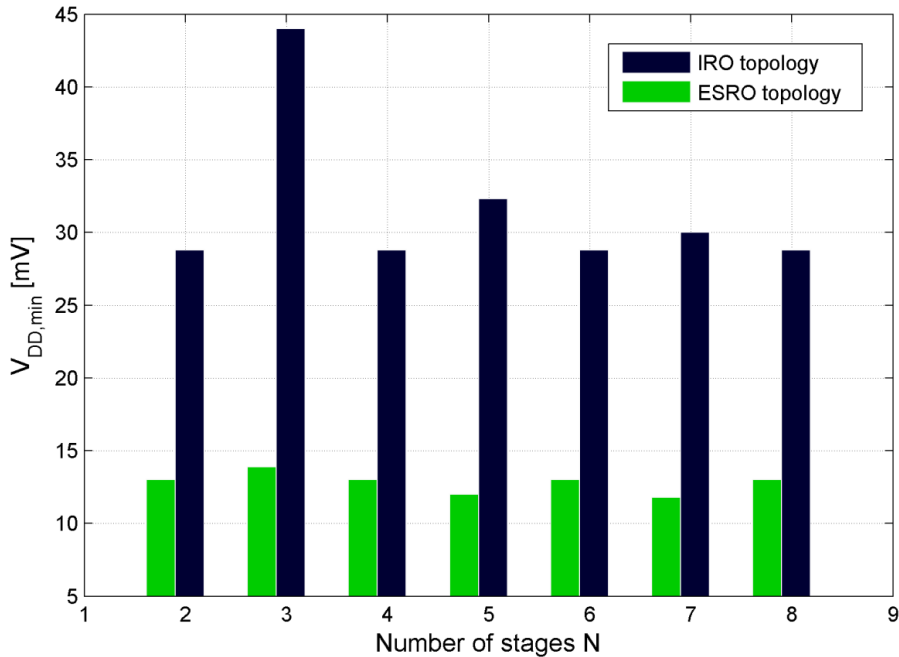
Figure 8.   Calculated values for the minimum supply voltage for the starting up of the IRO and ESRO topologies versus number of stages.

4 Design of the Oscillators and Experimental Results

In order to explore the potential of the IRO and ESRO topologies for ultra-low-voltage operation, this section describes the design of both a cross-coupled IRO and a cross-coupled ESRO. Both circuits were designed using zero-VT transistors available in the 130 nm CMOS process of IBM. Some design details as well as simulated and experimental results for each oscillator operating from supply voltages below 50 mV are given in the next section.

4.1 The two-stage inductive ring oscillator

Based on the theoretical framework presented in Section 2, we designed a two-stage IRO that operates with supply voltages of less than 50 mV. According to (5), the supply voltage is minimized when the phase shift between contiguous stages of the oscillator is equal (or close) to π. Such a phase shift can be obtained with either an even number of stages or an odd number of stages greater than 5, *e.g.* the seven-stage IRO presented in [15]. From (7), one can see that the minimum supply voltage has a strong dependence on the inductor losses. Thus, a high-Q ($Q \approx 8$) inductor at the oscillation frequency, roughly around 500 MHz, was chosen. It is then possible to calculate (or determine through simulation) the W/L ratio of the zero-VT transistor to achieve the required capacitance for the specified oscillation frequency. The characteristics of both the transistor and the inductor used in each stage of the IRO are summarized in Table 1. Differences between the simulated and experimental values for the DC current at V_{DD}=50 mV are mainly attributed to the difference between the nominal and practical values for the threshold voltage.

Table 1. Summary of device characteristics and the main simulated and experimental results for the fully integrated IRO.

Simulated Device Characteristics		IRO results	
Zero-VT transistor*	Inductor**	Simulated	Experimental
$W/L=30x6\mu m/0.42\mu m$	$L = 108$ nH	$V_{DD,min}= 38$ mV	$V_{DD,min}= 46$ mV
$V_T =71$ mV	$Q = 7.9$ @ 500 MHz	$f = 467$ MHz	$f = 410$ MHz
$I_S= 68.4$ µA	$f_{resonance}=1.13$ GHz	$I_{DC}=0.14$ mA @ $V_{DD}=50$ mV	$I_{DC}=0.26$ mA @ $V_{DD}=50$ mV
$g_{md} = 2.5$ mA/V			

*The value of g_{md} was extracted at $V_{DS} = V_{GS}= 50$ mV; V_T, I_S, and n were extracted by simulation of the gm/Id [14] curve.
**Inductor was simulated at 460 MHz;

Figure 9 shows the micrograph of the fully integrated IRO implemented in the 130 nm technology. In order to measure each oscillator phase simultaneously, we designed a symmetrical voltage buffer whose schematic diagram is shown in Fig. 10. The source degenerated topology of the buffer maintains an acceptable linearity for input signals of up to 300 mV peak-to-peak with a voltage gain of -0.75 at 400 MHz.
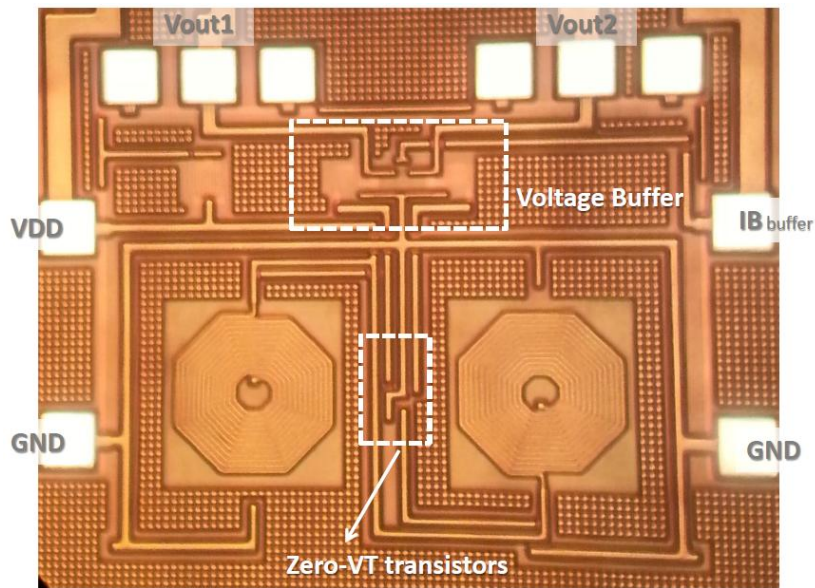

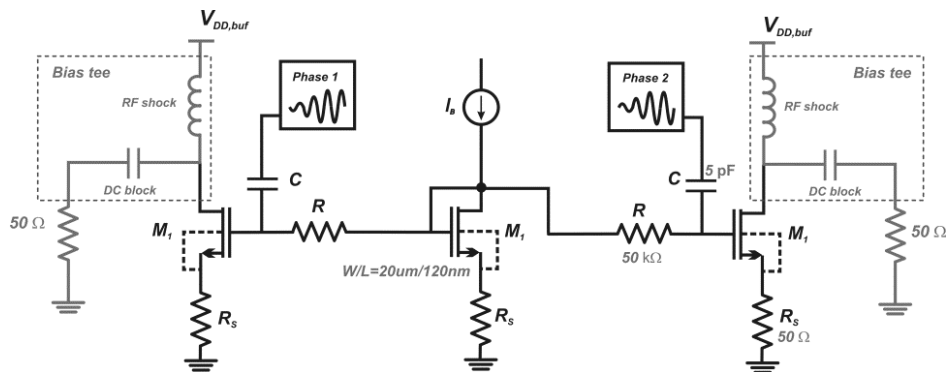Figure 9. Micrograph of the two-stage IRO in a 130 nm technology.

Figure 10. Schematic diagram of the voltage buffer.

Experimental measurements were performed in both the time and frequency domains using the digital serial analyzer Tektronix DSA 70804C and the spectrum analyzer HP 8593E. Figure 11 shows the experimental waveforms at each output of the voltage buffer, which has as inputs the two phases of the inductive ring oscillator. Figure 11 shows prototype oscillations at around 410 MHz when powered with a 45.3 mV supply.
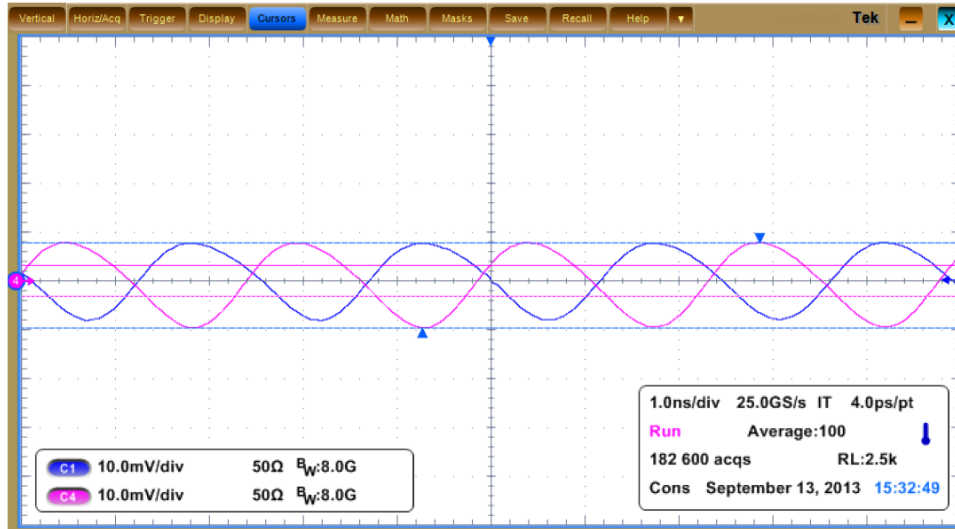

Figure 11.   Experimental waveforms at the buffer outputs for V_{DD}=45.3 mV.

The variation in the amplitude and frequency of the IRO oscillator in terms of the supply voltage is shown in Fig. 12. The peak-to-peak oscillator voltage is around 30 mV at V_{DD}=50 mV. The main simulated and experimental results for the IRO are summarized in Table 1. Despite some differences in the minimum start-up voltage and in the oscillation frequency, the agreement between the simulated and experimental curves is quite good. Since the main goal of this work is to design oscillators operating with very low supply voltages, the accuracy of the oscillation frequency is not of major concern.
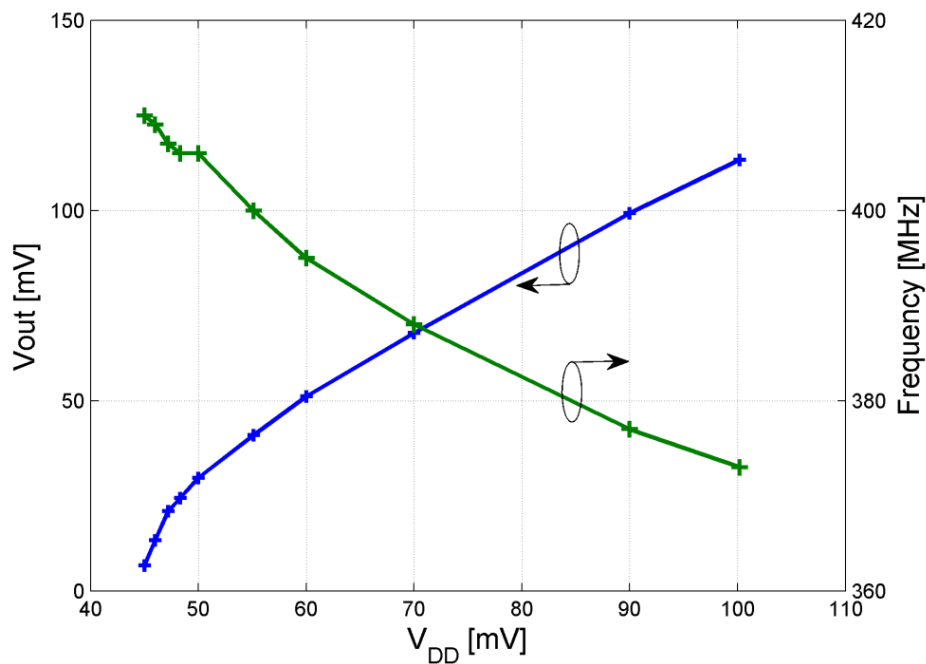

Figure 12.   Experimental peak-to-peak output voltage and oscillation frequency of the two-stage IRO versus V_{DD}.

4.2 Design of the two-stage enhanced-swing ring oscillator

Due to the use of a second inductor in each stage, the ESRO topology can boost the oscillation amplitude beyond the supply rails even when operating with very small supply voltages. Using the theoretical analysis developed in Section 3, we designed a fully integrated cross-coupled ESRO able to operate with supply voltages of around 32 mV. The inductors were designed in order to achieve a relatively high $K_L=L_2/L_1$ ratio (around 4), in order to reduce the g_{ms}/g_{md} ratio (see equation (18)) and, consequently, the minimum V_{DD} required for oscillation. Both inductors were also designed for a relatively high quality factor Q (around 8 at 400 MHz) which is close to the maximum value reached in the technology under consideration.

The theoretical optimum g_{md} was determined from expression (17), resulting in a value of around 13 mA/V after taking into account the inductor parameters of Table 2. In view of both the lack of accurate modeling for hand analysis and the parasitic elements due to the physical layout, we resorted to some fine-tuning through simulation. Subsequently, the aspect ratio W/L of the transistor was found to be 25x20µm/0.42µm for the starting up of oscillations at the lowest supply voltage.

A summary of the characteristics of the components of each stage of the ESRO is given in Table 2. As can be seen, the measurements and the simulated results in the ESRO match very closely.

Figure 13 shows the micrograph of the ESRO implemented in the 130 nm technology. In order to measure the two oscillator phases of the ESRO, the voltage buffer presented in Fig. 10 was used once again.

Table 2. Summary of device characteristics and the main simulated and experimental results for the fully integrated ESRO design.

Simulated Device Characteristics			ESRO results	
Zero-VT transistor*	Inductor L1**	Inductor L2**	Simulated	Experimental
$W/L=25x20$µm$/0.42µm$	$L_1 = 19$ nH	$L_2 = 80$ nH	$V_{DD,min}= 29$ mV	$V_{DD,min}= 31$ mV
$V_T =60.7$ mV	$Q1 = 8.7$	$Q2 =7.9$	$f = 410$ MHz	$f = 340$ MHz
$Is= 209$ µA	$f_{resonance1}=6.2$ GHz	$f_{resonance2}=1.25$ GHz	$I_{DC}=0.72$ mA @$V_{DD}=50$ mV	$I_{DC}=0.86$ mA @$V_{DD}=50$ mV
$g_{md} = 6.8$ mA/V				

*The value of g_{md} was extracted at $V_{DS} = V_{GS} =30$ mV; V_T, I_S, and n were obtained by simulation of the gm/Id [14] curve.
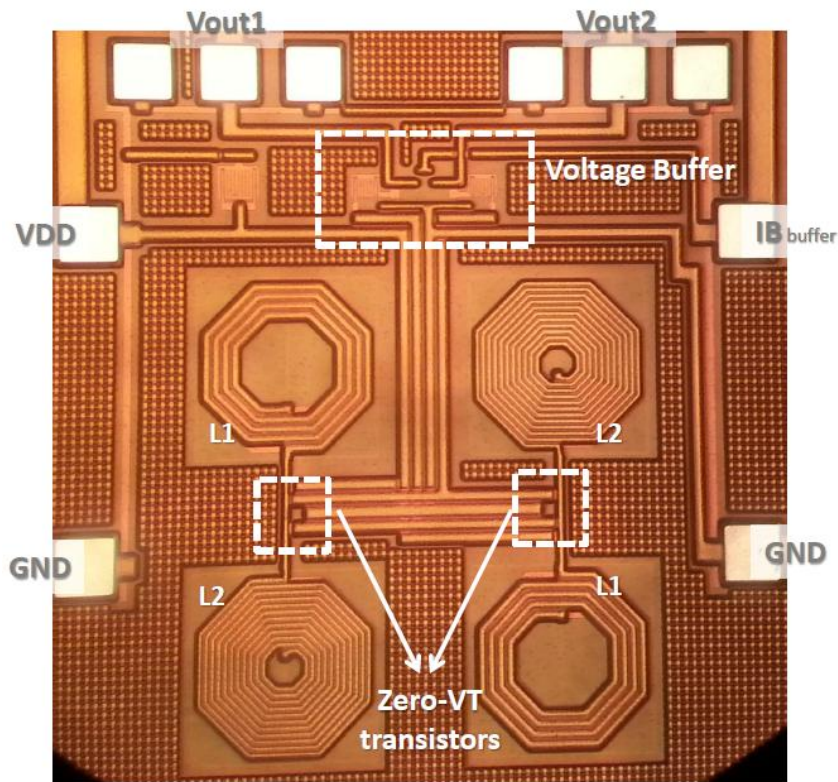
**Inductors were simulated at 400 MHz

Figure 13. Micrograph of the two-stage ESRO in the 130 nm technology.

Figure 14 shows the measurement setup for the characterization of the oscillators while Figure 15 shows the waveforms at the buffer outputs. Despite the somewhat different amplitude of the waveforms, the remarkable feature of this circuit is that it starts to oscillate at around 340 MHz from a supply voltage as low as 31 mV.
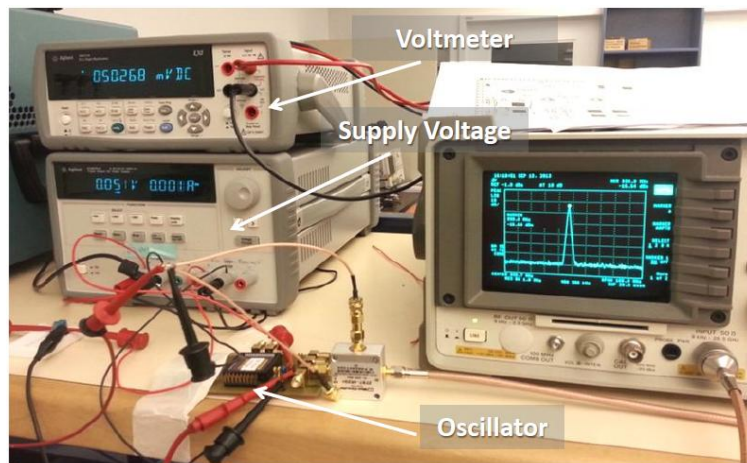

Figure 14. Measurement setup for the characterization of the oscillators. The picture shows the testing of the fully-integrated ESRO powered with a 50 mV power supply.
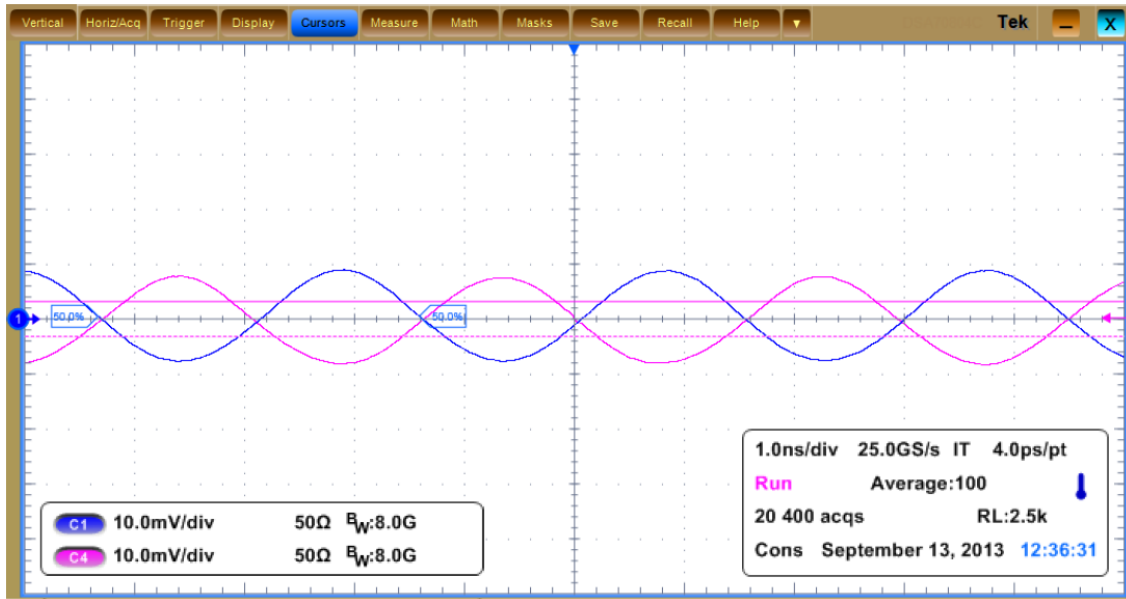
Figure 15.   Waveforms at the output of the voltage buffer in which the inputs are the two phases of the ESRO, for V_{DD}=32 mV.

The variation in the amplitude and frequency of the ESRO in terms of the supply voltage is illustrated in Fig. 16. For V_{DD}=50 mV the oscillator output voltage is around 130 mV peak-to-peak. The minimum supply voltage for the starting up of oscillations is 31 mV at room temperature. To the best of our knowledge, this is the lowest supply voltage reported to date for the running of a fully integrated oscillator in a conventional CMOS technology, at room temperature.
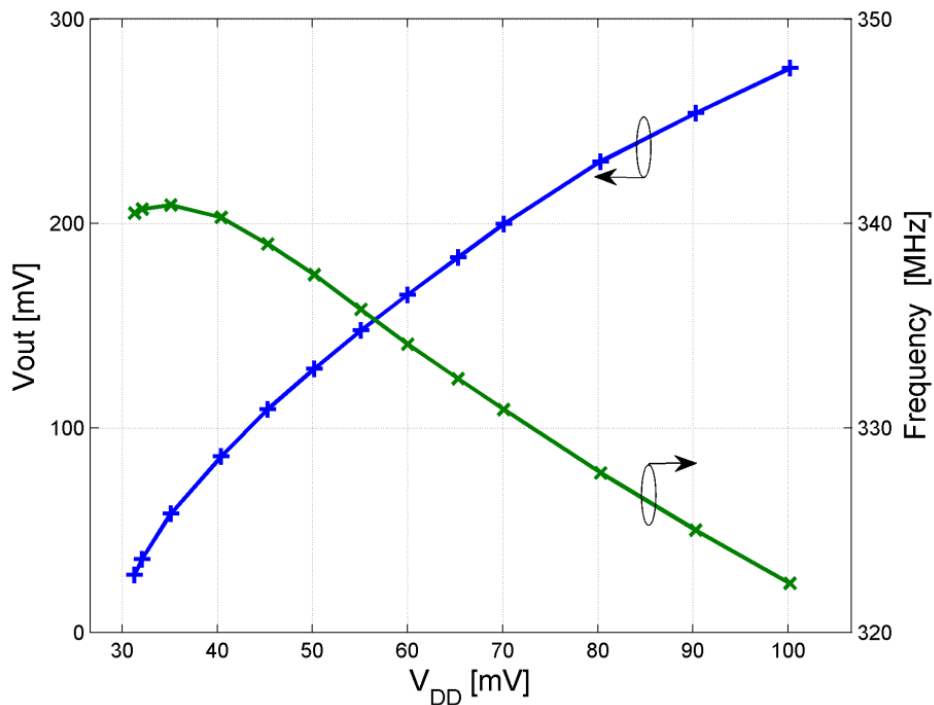

Figure 16.   Experimental peak-to-peak output voltage and frequency of the two-stage ESRO in terms of V_{DD}.

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5 Summary and conclusions

We have presented above two oscillator topologies, namely the inductive-load (IRO) and the enhanced-swing (ESRO) ring oscillators, which can operate with very low supply voltages. Analysis of the IRO topology revealed that it can operate with supply voltages of the order of the thermal voltage kT/q (around 26 mV at room temperature). On the other hand, the ESRO is able to operate with supply voltages below the thermal voltage, but at the expense of a second inductor per stage. Experimental results on a test chip in a 130 nm CMOS technology demonstrated that the IRO and the ESRO can operate with supply voltages as low as 46 mV and 31 mV, respectively. Instrumental to the design of the ultra-low-voltage oscillators is the availability of native (zero-VT) MOSFETs, which have a high drive capability at low voltages due to the low (or zero) threshold voltage. Both the IRO and the ESRO are suitable for energy harvesting applications, such as DC-DC converters operating with very low voltages. The oscillators we developed can operate with a thermoelectric generator attached to the human body [16] and other energy sources for which the available voltage is in the range of tens of mV.

Appendix A – Oscillation frequency of the inductive ring oscillator with the inclusion of C_{gd}

The circuit of a single stage of the inductive ring oscillator, as well as its small-signal model with the inclusion of the gate-drain capacitance C_{gd}, is shown in Fig. 17, where the symbols have the same meaning as in Fig. 3.
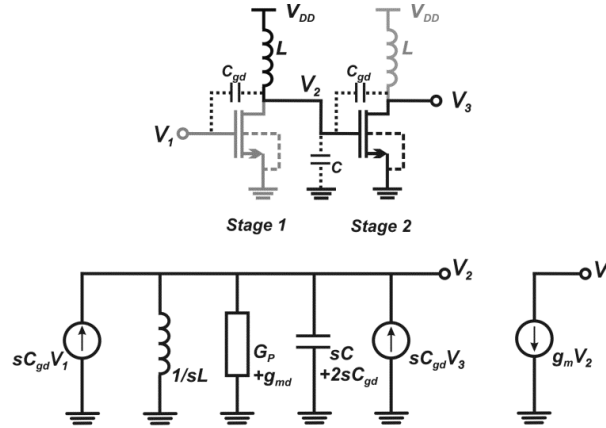

Figure 17. The inductive ring oscillator and the corresponding small-signal model of a single stage.

The phase shift ϕ between two adjacent stages of the ring oscillator is given by $\phi=2k\pi/N$, where N is the number of stages and k is an integer. Since the node voltages in Fig. 17 are related as $V_2=V_1e^{j\phi}$ and $V_3=V_2e^{j\phi}$, we can redraw the small-signal circuit of Fig. 17 as shown in Fig. 18, with $C_T=C+2C_{gd}(1\text{-}cos\ \phi)$.
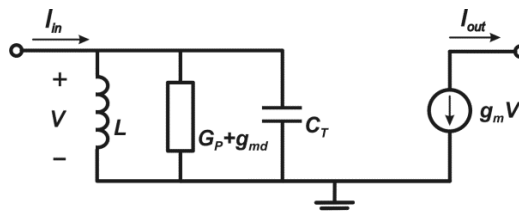

Figure 18. Small-signal model equivalent to a single stage of the inductive ring oscillator.

Thus, the transfer function of the single stage in Fig. 18 is given by

$$\frac{I_{out}}{I_{in}}(s) = -\frac{g_m}{g_{md} + G_P + \dfrac{1}{sL} + sC_T} \tag{A1}$$

In this case, the resonant frequency ω_0 is given by $\omega_0^2 L C_T = 1$. For an even number of stages $\phi = \pi$ and thus $C_T = C + 4C_{gd}$.

Appendix B – MOSFET model

The MOSFET model used throughout this paper is the Unified Current Control Model (UICM) [14], in which the current I_D is written as a combination of the forward (I_F) and reverse (I_R) currents

$$I_D = I_F - I_R = I_S\left(i_f - i_r\right) \tag{B1}$$

I_S is the specific current, a parameter slightly dependent on the gate voltage, but here assumed to be independent of the gate voltage, i_f and i_r are the normalized forward and reverse currents, respectively, and

$$\frac{V_P - V_{SB(DB)}}{\phi_t} = \ln\left(\sqrt{1+i_{f(r)}} - 1\right) + \sqrt{1+i_{f(r)}} - 2 \tag{B2}$$

$$V_P = \frac{V_{GB} - V_T}{n} \tag{B3}$$

where V_P is the pinch-off voltage, V_T is the threshold voltage, and n is the slope factor, assumed to be independent of the gate voltage. The differentiation of the current with respect to V_S, V_D, and V_G allows us to write

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_f} - 1\right) \tag{B4}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_r} - 1\right) \tag{B5}$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{n} \tag{B6}$$

The drain-source voltage V_{DS} can be expressed in terms of i_f and i_r using (B2). The resulting expression for V_{DS} can be subsequently written in terms of the transconductances making use of (B4) and (B5), which yields

$$\frac{V_{DS}}{\phi_t} = \ln\left(\frac{\sqrt{1+i_f} - 1}{\sqrt{1+i_r} - 1}\right) + \sqrt{1+i_f} - \sqrt{1+i_r} = \ln\frac{g_{ms}}{g_{md}} + \frac{\phi_t}{2I_S}\left(g_{ms} - g_{md}\right) \tag{B7}$$

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