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Fully integrated signal conditioning of an accelerometer for implantable pacemakers

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Abstract This paper shows the development of a fully integrated G_m-C 0.5–7 Hz bandpass amplifier (gain $G = 400$), for a piezoelectric accelerometer to be employed in rate adaptive pacemakers. The circuit, fabricated in a standard 0.8 micron CMOS technology, operates with a power supply as low as 2 V, consumes 230 nA of current, and has only a 2.1 μV_{rms} input referred noise. Detailed circuit specifications, measurements, and a system performance comparative analysis are presented. The physical activity system includes a fully integrated G_m-C rectifier and 3-second time average. Fully integrated very low frequency circuits were implemented with the aid of series-parallel current division in symmetrical OTAs. OTAs as low as 33 pS (equivalent to a 30 GΩ resistor) were designed, fabricated, and tested.

Keywords Low power design · CMOS analog integrated circuits · Sensors · Bandpass filters · Cardiac pacemaker

1 Introduction

Low power consumption is crucial in the case of pacemakers, the most widespread active implant, where batteries need to last for years [1]. Since the replacement of batteries requires a surgical, albeit simple procedure, the need arises for minimizing power consumption to extend device lifetime. On the other hand, circuits must be extremely reliable since they may be life supporting devices for the patient. The design of complex but reliable circuits restricted to a few micro-Amperes of current consumption is a major quest for the pacemaker manufacturer. Modern cardiac pacemakers are nowadays complex electronic circuits performing several sensing, control, and stimulation functions [1, 2] to reestablish a normal rhythm to a diseased heart. These functions may include cardiac sensing channels, cardiac stimuli, battery sensing, telemetry, and also physical activity sensing [1–3] the latter being the focus of this work. Physical activity sensing is a measurement used in the so-called adaptive pacemakers, which regulate the heart stimulation rate according to the requirements of the patient. A simple but robust solution for activity sensing, is the use of an accelerometer to register body movement. Because it is non-invasive (the sensing device is placed inside the pacemaker without direct contact with the human body), this is the preferred technique used in most rate adaptive pacemakers sometimes complimented with sensors for other parameters such as ventilation rate, venous O_2 saturation, or body impedance [1].

This study is concerned with the design of an activity sensing integrated circuit based on a commercial piezoelectric accelerometer. The specified signal chain for the circuit is shown in Fig. 1. Its objective is to give at the output a voltage proportional to the average of the modulus of the mechanical movement of the patient during the previous 3 seconds, filtered in the signal band from 0.5 to 7 Hz. The circuit consist of 2nd order bandpass filter-amplifier stage, followed by a rectifier, and a 3-second time average. The task of Fig. 1 appears simple, but it becomes difficult when dealing with normal pacemaker power consumption restrictions. Because human body motion signals are of very low frequency, the passive components, (capacitors and resistors) for a traditional filter become too large to integrate [4]. To integrate the system in Fig. 1 (excluding the sensor) in a single ASIC,

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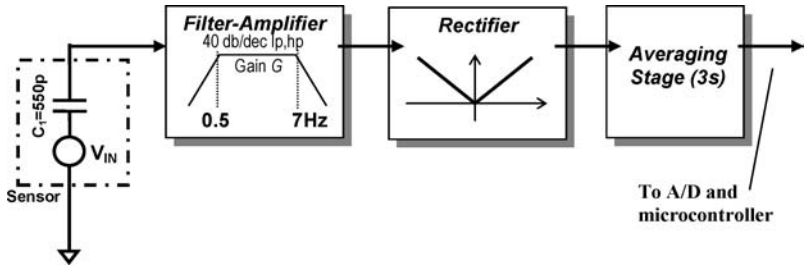

Fig. 1 The signal chain of the (physical) activity sensing circuit

the selected circuits were continuous-time G_m-C filters [5], and series-parallel current division transconductors (OTAs) [6, 7] were employed to achieve the required transconductances (as small as the inverse of a 30 GΩ resistor and with up to ±500 mV linear range).

The critical block in the signal chain of Fig. 1 is the bandpass filter-amplifier because at the rectifier and time averaging stage, noise is no longer critical and the transfer function is much simpler. Throughout this paper the focus will be on the bandpass amplifier, and the complete design and test measurements for this stage will be presented. A very simple rectifier and time averaging design was also simulated to evaluate total system area and power consumption. In the following section, circuit specifications are presented and the bandpass-amplifier design and topology are shown in Section 3. Measurements are presented in Section 4 while a performance comparison between this and other similar filters is given in Section 5.

2 The sensing element and system specifications

Several kinds of sensors exist [8, 9] for sensing acceleration, but we will limit the analysis to piezoelectric ones [8], because they fulfill size and power consumption requirements for implantable devices. The sensing material is an isolator and thus the equivalent circuit of the transducer is a capacitor. The input source can be considered either as a charge generator or as a voltage source in series with the capacitor, as in Fig. 1. A miniature single axis accelerometer was selected and in Table 1 specifications are given. The charge sensitivity and capacitance of the sensor are 1.5 pC/g, and 550 pF, respectively, which is equivalent to 3.5 mV/g sensitivity in the connection scheme of Fig. 1. For implantable applications, a piezoelectric transducer is an ideal choice because it has no power consumption of its own. However, the signal conditioning circuit presents several challenges:

Table 1 Piezoelectric sensor data provided by the manufacturer

Specification	Min	Typ	Max
Charge sensitivity (pC/g)	1.4	1.9	2.4
Capacitance		550 pF	
Transverse response			5%
Resistance (25°C)	10 GΩ		
Resistance (150°C)	100 MΩ		
Mechanic resonance		9 kHz	

- At 0.5 Hz, the 550 pF sensor capacitance represent a 580 MΩ series impedance. Also note in Fig. 1 that the upper node of the accelerometer is floating unless the measuring circuit provides some kind of virtual ground or DC bias connection.
- Although a pacemaker is a self-contained circuit in a titanium case very similar to an ideal Faraday cage, capacitive or inductive coupled noise may strongly affect the sensor due to its enormous impedance.
- The circuit must operate at low voltage, with extremely low power consumption, it must be low-noise and have a reduced offset.
- All these restrictions ideally must be overcome without the use of external passive components.

The most common range of accelerations present at chest level due to normal human exercise is 0.007 g_{peak} to 0.34 g_{peak} [2]. The frequency band of the signal, 0.5 Hz to 7 Hz, corresponds to values reported in [1] for several studies on acceleration for various activities for the human body. Owing to the force of gravity, physical activity acceleration signals may be accompanied by much higher steps of up to at least ±1 g that should be removed. A 2.8 V (nominal) lithium-iodine battery [1, 10] normally powers modern pacemakers. Battery voltage decays with time and the pacemaker should be fully operational down to a 2 V power supply to guarantee a reasonable time from the low battery condition detection to pacemaker substitution [1, 2]. Depending on their functionality and artificial pace rate, modern pacemarkers may consume in the order of 10 to 100 μW power. Unlike other circuit blocks, the acceleration sensor is always turned on in rate adaptive pacemakers, up to the end of battery life condition detection. Thus, activity sensing circuit must operate down to 2 V with a power consumption budget in the order of a μW [2, 3]. In Table 2, a summary of specifications for the bandpass amplifier is given. Noise specifications correspond to an in-band rms value equal to the rms voltage produced by the minimum 0.007 g acceleration input to be detected (typ. 24 μV_{peak}). A gain G of 400 is selected

Table 2 Circuit specifications for the bandpass filter-amplifier

Specification	Requirement
Supply voltage	2.8–2.0 V
Acceleration range	0.007–0.34 g_{peak}
Input voltage range	(24 μV_{peak} – 1.2 mV_{peak})
Power consumption	$\sim$ 1 μA[a]
Frequency response	0.5–7 Hz Bandpass 40 dB/dec
Input referred noise	<12 μV_{rms}
Output offset[b]	<5 mV
Total gain	400
Others	No external components
	Relaxed tolerance in gain and pole position

[a] Whole system of Fig. 1.

[b] Output offset defined as DC output for null input signal.

so that this minimum input signal gives an output voltage higher than the maximum estimated 5 mV output offset (see Section 3.2).

3 Circuit description and design methodology

The selected bandpass filter topology is shown in Fig. 2. It has two cascade single-ended stages with a total gain of $G = 385$, a preamplifier stage with a gain of $G_1 = 46.4$ formed by G_{m1}, G_{m2}, G_{m3}, C_1, C_2, and a gain stage with a gain of $G_2 = 8.4$ formed by G_{m4}, G_{m5}, G_{m6}, C_3, C_4. Each stage is composed of a lowpass gain structure (given by $G_{m1(4)}$, $G_{m2(5)}$, $C_{2(4)}$) similar to that proposed in [11] for a capacitive microphone, and a DC cancellation loop (given by $G_{m3(6)}$, $C_{1(3)}$). Capacitors are of the double poly type, and note that in Fig. 2 the sensor capacitance itself is used in the filter, taking advantage of the 550 pF equivalent capacitance. The $G_{m3} - C_1$ DC cancellation loop also provides a virtual ground for the upper node of the accelerometer, eliminating the need for any biasing resistor connected to the sensor. The transfer function $H_{1(2)}(\omega)$ of each stage of the amplifier is of the bandpass type [5]:

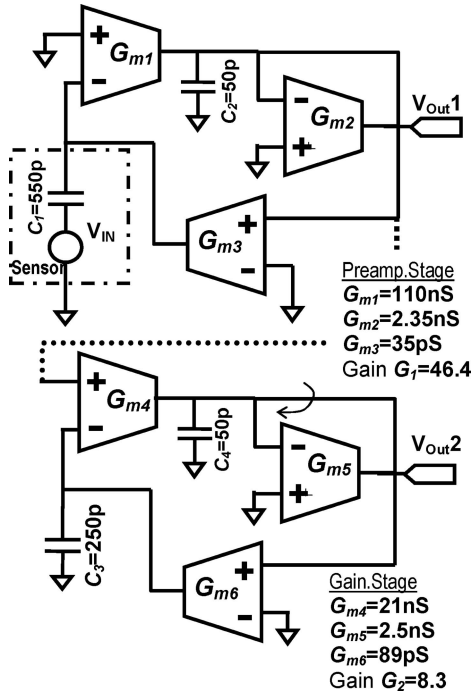

Fig. 2 Circuit topology of the bandpass filter-amplifier

$$H_{1(2)} = \frac{Q\omega_0}{k} \cdot \frac{j\omega \cdot \omega_0/Q}{\omega_0^2 + j\omega \cdot \omega_0/Q - \omega^2} \tag{1}$$

with quality factor Q, and center frequency ω_0 given by :

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m3}}{C_1C_2}} \approx \sqrt{\frac{G_{m4}G_{m6}}{C_3C_4}} \approx 1.88 \text{ Hz},$$
$$Q = \sqrt{\frac{G_{m1}G_{m3}C_2}{G_{m2}^2C_1}} \approx \sqrt{\frac{G_{m4}G_{m6}C_4}{G_{m2}^2C_3}} \approx 0.25 \tag{2}$$

k is defined as $k = \frac{G_{m3(6)}}{C_{1(3)}}$ and the gain at the center frequency of each stage is $G_{1(2)} = \frac{G_{m1(4)}}{G_{m2(5)}}$. The system was simulated to be stable with a 68° phase margin. The capacitors, and OTAs G_{m1} to G_{m6}, where designed with the following criteria:

- Noise is critical, mostly determined by the input OTA G_{m1}, thus G_{m1} was designed to minimize noise, according to the area and the current consumption budget [12].
- As much gain as possible was assigned to the preamplifier.
- G_{m6} has a minimum offset oriented design (see offset discussion in Section 3.2) and $C_3 = 250$ pF was selected as the highest reasonable value.
- The rest of the capacitors have the value of 50 pF, while OTAs G_{m2} to G_{m6} were designed using the methodology proposed in [7] according to their required linear range and transconductance.

The capacitors are double poly type; they are made of two stacked poly layers with an outer guard ring connected to ground, but without any dummy structure or matching geomtry to reduce the occupied area.

Finally, at the output of each stage (V_{Out1}, V_{Out2}), unity gain buffers were placed to drive output pads for test purposes.

3.1 OTAs description

G_{m1} is a standard symmetrical OTA with large input transistors sized $W/L = 120$ μm/10 μm and also large current mirrors, transistors sized $W/L = 35$ μm/30 μm, to reduce flicker noise. Only 7 nA bias current was necessary

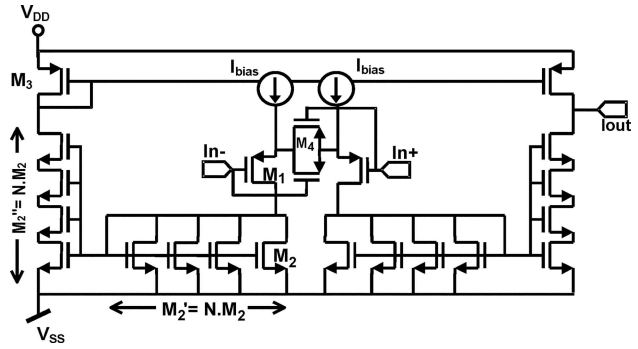

Fig. 3 Circuit schematic for G_{m6} including series-parallel current division and linearized differential input pair

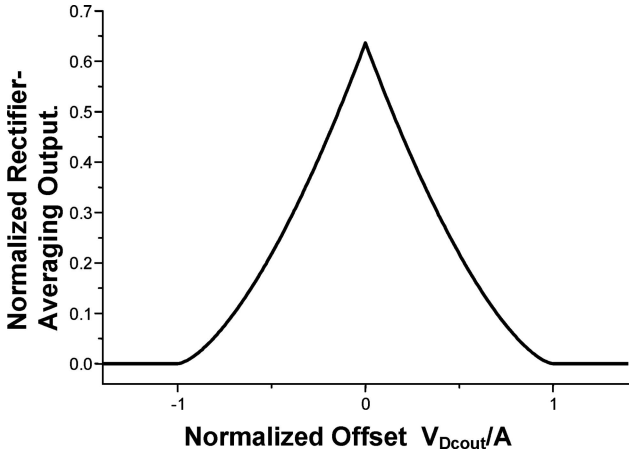

Fig. 4 Time average of a rectifier output in terms of offset voltage, considering an input sine wave signal of arbitrary frequency and amplitude A. Both offset and output are normalized with respect to A. At zero offset, the output is the expected $2/\pi$ average of a rectified sine wave; the output falls to zero if the offset is larger than A. Note on the y-axis the output is referred to as the offset voltage: output $= \langle|\text{offset} + \text{input signal}|\rangle - |\text{offset}|$

to push thermal noise below flicker noise. The rest of the transconductors were implemented using series-parallel current division [6, 7].

For a maximum input signal of 1.2 mV_p, ± 60 mV linear range is required at the input of G_{m2}, G_{m3}, G_{m4} and ± 470 mV at the input of G_{m5}, G_{m6}. G_{m6} requires a very low input offset, very low transconductance, and large linear range; its architecture is shown in Fig. 3. It is a symmetrical OTA with a linearized input pair [13] and a series-parallel current division factor $N^2 = 784$. The effective transconductance is calculated as $G_{m6} = g_{m\_eq}/N^2$, where $g_{m\_eq} = 70$ nS is the equivalent transconductance of the linearized input pair. The input transistors M_1 are sized $W/L = 10\ \mu$m/130 μm, biased with 21 nA current in moderate inversion with a current factor [14] $i_f = 20$. Transistors M_4 are sized $W/L = 5\ \mu$m/520 μm, M_2 unit transistors are $W/L = 4\ \mu$m/12 μm, and M_3 transistors are $W/L = 20\ \mu$m/60 μm.

Since their required linear range is narrower, G_{m2}, G_{m3}, G_{m4}, are implemented with non-degenerated differential input pairs but the same topology in Fig. 3; in all cases M_1 is sized $W/L = 5\ \mu$m/110 μm, with a current factor $i_f = 34$. Current division factor to the output are respectively 72 for G_{m2} (M_2" = 8 series; M_2' = 9 parallel), 4900 for G_{m3} (M_2" = 70 series; M_2' = 70 parallel), and 8 for G_{m4}. Since the required division factor for G_{m4}, or G_{m5} is not too high, transistor M_2" is composed of a rectangular array of unitary transistors. The copy division factor of the NMOS current mirror M_2": M_2' in G_{m4} (assuming a circuit analogous to that in Fig. 3) is obtained with M_2' as an array of 28 unitary transistors in parallel while, M_2" is composed of a 7-parallel-by-2-series array of unitary transistors sized $W/L = 4\ \mu$m/12 μm each (M_2" in this case is equivalent to a $3\frac{1}{2}$ parallel array of unit transistors [15]). These particular numbers were chosen in order to reuse other layout blocks of the circuit.

Because their inputs are the same (see Fig. 2), it was possible that G_{m5}, and G_{m6} share the same large area differential pair and M_2' transistor, with a different output branches.

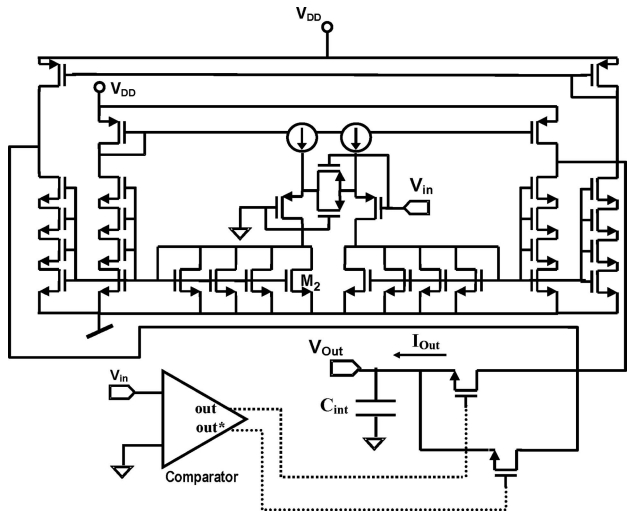

Fig. 5 Proposed scheme for a rectifier-tranconductor G_{mR} connected to an integrating capacitor. A comparator, depending on the sign of the input, determines which of the two output currents charges the capacitor

The topology is similar to that in Fig. 5 but M_2" geometry is different in G_{m5}, and G_{m6} and thus the copy factor. G_{m5} copy factor is 28:1, obtained with a 5 by 5 array of unitary transistors for M_2".

3.2 Offset analysis and discussion

The circuit in Fig. 2 can be seen as a bandpass filter with a capacitive coupled input. But because the $G_{m6} - C_3$ DC cancellation loop is not perfect, a null input signal will produce a small DC voltage output $V_{DC\ out}$. $V_{DC\ out}$ is the bandpass output offset.

For DC operation G_{m6} cannot have an output current, thus:

$$I_{Out\,6} = G_{m6}\,(V_{DC\,out} - V_{Os6}) = 0 \tag{3}$$

where $I_{Out\,6}$ and V_{Os6} are G_{m6} output current and input referred offset, respectively. Thus, output offset $V_{DC\,out}$ is equal to V_{Os6}. The input referred offset of the bandpass amplifier V_{Os} is defined dividing $V_{DC\,out}$ by the total gain G:

$$V_{Os} = \frac{V_{DC\,out}}{G} = \frac{V_{Os6}}{G} \tag{4}$$

Note that the input referred offsets of G_{m1} to G_{m5} are removed by the final cancellation loop. Thus, the design of G_{m6} is critical in terms of offset and linearity due to the large signal amplitude at V_{Out2} (Fig. 2).

Circuit offset will determine overall system precision. In effect, $|V_{DC\,out}|$ is observed at the output of the system in Fig. 1, with a null or very low acceleration input (ideal rectifier assumed). This is because:

$$\langle |V_{DC\,out} + A.\sin(\omega t)| \rangle \cong \langle |V_{DC\,out}| \rangle \quad \text{if} \quad A < |V_{DC\,out}| \tag{5}$$

where $\langle \cdots \rangle$ denotes time average, A is signal amplitude at the bandpass output, and ω is an arbitrary frequency in the signal band. The minimum signal that causes a change in the system output is such that A is larger than $|V_{DC\,out}|$. Clearly, if $V_{DC\,out} = 0$, an arbitrary low signal would be detectable. In the plot of Fig. 4 it is shown how the output of the system in Fig. 1 varies depending on the normalized offset voltage $|V_{DC\,out}|/A$. Note that for $|V_{DC\,out}| > A$ the output falls to zero. The bandpass-amplifier should be provided with appropriate gain, and guarantee a sufficient low offset, so that the bandpass output corresponding to the minimum 0.007 g acceleration is high enough to be detected. For an estimated 5 mV total offset, a gain of $G = 400$ was selected and so the minimum signal is twice this value (10 mV).

3.3 Dispersion analysis and discussion

It is necessary to estimate how much the spread in the technology parameters affect the transfer function of the bandpass-amplifier. From the datasheet of the target CMOS process, double poly capacitance per unit area is expected to spread $\pm 8\%$ around a 1.8 fF/μm^2 typical value. On the other hand an approximately $\pm 25\%$ spread was assumed for OTAs, obtained from simulating the gate transconductance g_m of a single PMOS transistor in moderate inversion, using three different BSIM3v3 models provided by the manufacturer (typical, worst case slow, worst case fast). Fluctuations affect the center frequency, gain, and Q of the filter. Considering the spread of the capacitances and conductances mentioned above, Eq. (2) gives a center frequency between 1.4 Hz and 2.5 Hz. While the gain may be software-corrected at the pacemaker microcontroller, it should be discussed whether variations in ω_0 and Q from one chip to another affect the system performance.

A worst case analysis probably overestimates the fluctuation in the position of zeros and poles. It is interesting to note here that the integrated circuits from two different fabrication batches, reported in this study and in [16], have a center frequency and quality factor very close to the specified ones. If still required, an automatic or trimmable tuning scheme acting on the bias current of one or several OTAs to set the appropriate ω_0 and Q value is possible. However, for the sake of simplicity, a tuning scheme was discarded to preserve low circuit area and power consumption, and because the application here presented does not require a precise transfer function.

3.4 Circuit noise analysis and discussion

Most gain was assigned to the preamplifier stage thus it determines total noise. The power spectral density (PSD) of the input referred noise voltage $S_{vn}(f)$ in the preamplifier stage is:

$$S_{vn}(f) = S_{v_{Gm1}}(f) + \frac{S_{v_{Gm2}}(f)\cdot G_{m2}^2}{G_{m1}^2} + \frac{S_{v_{Gm3}}(f)\cdot G_{m3}^2}{(j\omega C_1)^2} \tag{6}$$

where $S_{v_{Gm1}}(f)$, $S_{v_{Gm2}}(f)$, $S_{v_{Gm3}}(f)$, are the input noise voltage PSD of each OTA. From (6), most of the noise in the passband from 0.5 to 7 Hz, is introduced by G_{m1}. At low frequencies, both thermal and flicker noise should be considered. All the OTAs use large transistors like G_{m1} to reduce the impact of mismatch offset, and larger bias currents, but their input noise voltage is larger because of the reduced transconductance value. The noise contribution of G_{m2} to G_{m6} was verified to be negligible integrating (6) in the band of interest. In Table 3 some noise measurements of individual OTAs are shown.

The input rms noise voltage to measure in the whole circuit is:

$$V_{n\_rms} = \frac{1}{G}\sqrt{\int_0^\infty |H(f)|^2 \cdot S_{VG_{m1}}(f)\cdot df} \tag{7}$$

Where $H(f) = H_1 \cdot H_2$ is the second order bandpass-filter amplifier transfer function ($\omega = 2\pi f$). Using (7), the expected input noise voltage was 3.3 μV_{rms}, slightly larger than the measured value in Section 4.

Table 3 Measurement results for fabricated transconductors: calculated (measured) transconductance, linear range V_{Lin} (defined as in [7] for a error $\alpha < 5\%$), calculated (measured) input referred noise in the signal band, measured input referred offset, calculated current, and total area, for the OTAs. G_{m5},G_{m6} share the input pair but use different output current mirrors

OTA	Transc	Linearity V_{Lin}(mV)	Input noise. (μV_{rms})	Input Offset σ_{Voff} (mV)	Current Cons.(nA)	Area (mm^2)
G_{m1}	110(110)nS	60	5 (4)	1.1	14	.019
G_{m2}	2.35(2.58)nS	150	42	4.4	43	.040
G_{m3}	35(33)pS	150	163(130)	2.1	42	.092
G_{m4}	21 nS	150			47	.051
G_{m5}	2.4(2.8)nS	500		9.1	44	.18
G_{m6}	89(100)pS	500		6.8		

3.5 The effect of leakage currents

The above presented design requires the use of pA bias currents in certain transistors. Maximum leakage currents were estimated in 6 fA for a 4 μm $\times$ 2 μm n+ diffusion in the target technology at 37°C. The design criterion was to preserve accumulated leakages in any branch of series transistors, below 10% of their bias current (relaxed to 20% in G_{m3}). It should be pointed that parasitic diode leakages do not always set the bottom current range of an MOS transistor [17]. In modern technologies, drain current may be several pA or up to nA order for $V_{GS} = 0$ in minimum size transistors. But, large current mirrors as in Fig. 3 are not a problem because they use extremely long M_2" transistors while M_3 transistor was designed also narrow and long. Since the drain current at very low V_{GS} is still proportional to W/L ratio, the designer can push $V_{GS} = 0$ current below leakages, without using the special circuit techniques in [17].

Measurements in the following section were performed at room temperature but the operation of the circuit, power consumption, and output offset, were also tested at 37°C without a significant change.

3.6 Integrated rectifier

A fully integrated rectifier and time average circuit, utilizing the same circuit blocks previously employed in the bandpass amplifier, is shown in Fig. 5. It is composed of a modified G_{m6} transconductor, which incorporates a second output branch toggling the connections of the mirrors so the output current at both outputs have the same modulus but opposite signs. A comparator with the aid of two MOS switches selects which of the outputs will be the effective current output of the transconductor. Thus, the modified OTA, comparator, and switches, act together as a voltage to current rectifier providing an output $I_{\text{out}} = |G_{m6} \cdot V_{\text{in}}|$. This rectifying OTA will be referred to as G_{mR}. In the plot of Fig. 6, the simulated transfer function (output current vs. input voltage) of G_{mR} is shown. The comparator used for the simulation is simply

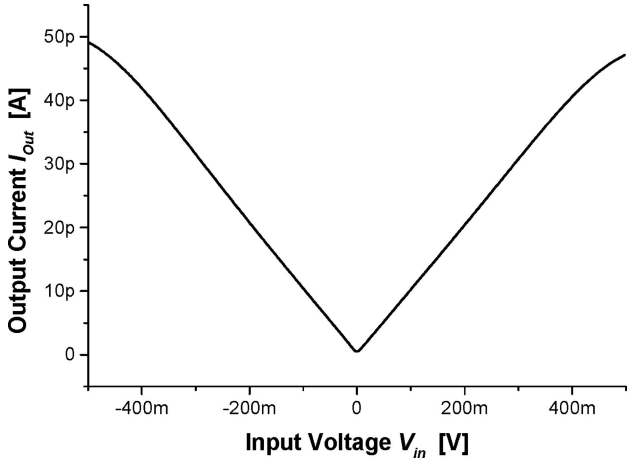

Fig. 6 Simulated transference of the rectifying OTA G_{mR}.

G_{m1}. Finally, G_{mR} is connected to an integrating capacitor C_{int}. The circuit is simulated considering that a discharge switch is shunted with C_{int} and closed every 3 seconds. A 260 pF C_{int} was chosen for an appropriate output voltage swing.

4 Filter measurement results

The previously described bandpass filter-amplifier was fabricated in a 0.8 μm CMOS technology, and tested. In Fig. 7 a microphotograph of the circuit occupying only 0.7 mm^2 is shown. Figure 8 shows the expected and measured transfer function of the filter. The center frequency was measured as 1.8 Hz. The simple circuit in Fig. 9 was used to simulate the accelerometer using an external function generator, because a calibrated movement generator was not available. The voltage divider R_A-R_B allows us to comfortably simulate input voltages from a few μV to a few mV. Measured input referred noise was 2.1 μV_{rms} and measured total current was 229 nA. A summary of the bandpass filter-amplifier characteristics is shown in Table 4. The graph in Fig. 10 shows the time response of the filter-amplifier with the accelerometer

Table 4 Measured bandpass amplifier characteristics

Specification	Value
Bandpass frequency	40 dB/dec 0.5–7 Hz
Gain	390
Input referred noise	2.1 μV_{rms}
Operating voltage	2.0–2.8 V
Current consumption	229 nA
Occupied area	0.78 mm^2
Input referred offset	18 μV[a]

[a]Input referred offset defined in Eq. (4).

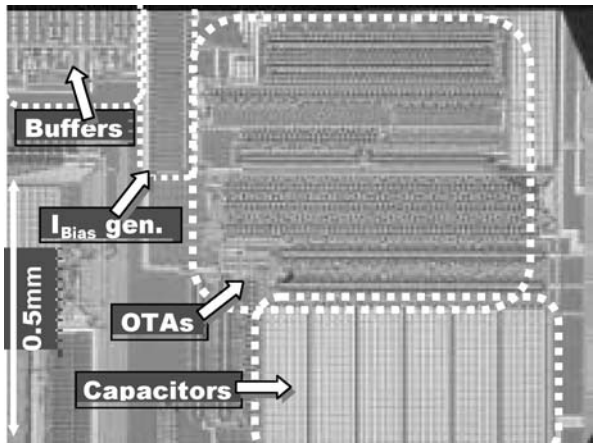

Fig. 7 A microphotograph of the fabricated circuit. OTAs, capacitors, (test) buffers, and the bias current generation block

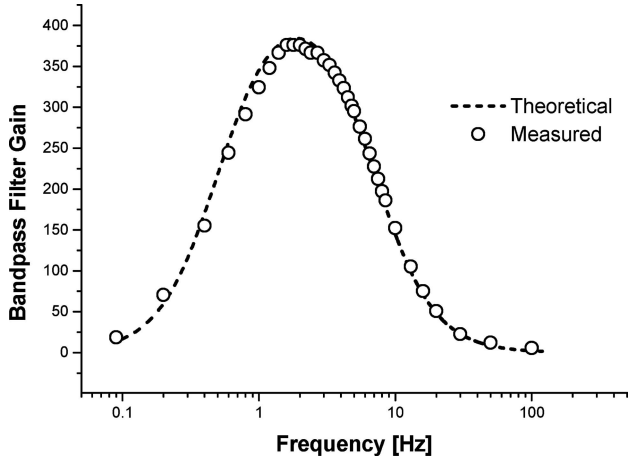

Fig. 8 Measured filter response

connected to its input, while shaking the whole system at approximately 2 Hz.

Isolated transconductors were also fabricated for test purposes. Several measured and calculated characteristics are summarized in Table 3. It should be highlighted that the reduced input offset of the OTAs is obtained with moderate area and power consumption, even for the case of a transconductor of only 33 pS, or G_{m6} of 89 nS with a ± 500 mV linear

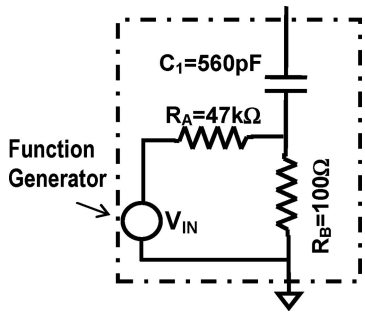

Fig. 9 A simple circuit used to emulate the sensor output with a standard function generator

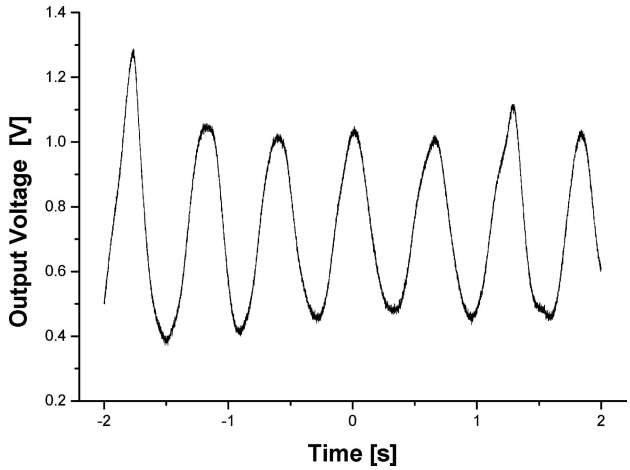

Fig. 10 Filter output while shaking the system at approximately 2 Hz with the piezoelectric accelerometer connected at the input

range. Ten circuit samples from the same batch were used to calculate σ_{Voff} in Table 3.

Finally, the accelerometer connected to the fabricated bandpass amplifier, with the addition of an external full-wave rectifier and 15 s time averaging, was inserted into a battery-powered closed container to do a field test of the activity sensing system. The circuit was strapped at chest level while doing different physical activities to check whether it is capable of distinguishing between them. The output voltage was registered with the aid of a small pocket multimeter.

Table 5 Activity estimation measurements using the fabricated circuit and external rectifier and 15 s time average

Physical activity	Syst. output (mV)
Sleeping	0
Working on a computer	30
Walking (slow)	44
Walking (normal)	86
Walking (fast)	210
Climbing up stairs	95
Going down stairs	82
Climbing up stairs (fast)	200
Running (10 km/h)	423

Table 6 Comparative analysis of the system here presented (#1); two other implementations of the same system (#2, #3); and two high performance filters for implantable devices (#4, #5). For the evaluation of the system in row (#1), the results in Table 4 have been used with the addition of the simulation results for G_{mR}-C rectifier and time averaging

Circuit description	Technique	Discrete elements	Input noise	Gain	Current consumption	Supply voltage	Area (mm^2)
(**#1**) - 0.5–7 Hz 2nd.order bandpass + rectifier + time averaging	G_m-C using series-parallel current division OTAs	no	2.1 μV_{rms}	400	300 nA	2–2.8 V	1.2
(**#2**) - 0.5–7 Hz 1st order bandpass + rectifier + time averaging. [3]	Continuous- time filter using combined techniques	10	18 μV_{rms}	2900	2.5 μA + 500 nA sensor	2–2.8 V	1.82
(**#3**) - 0.5–7 Hz 1st order bandpass + rectifier. [18]	Switched Capacitors	2 for time averaging	n.a	510	1.3 μA + 1.5 μA sensor	2–2.8 V	9
(**#4**) - Sixth order, 2.4 Hz lowpass filter. [19]	G_m-C using special OTAs and scaled capacitors	no	<50 μV_{rms}	0.3	3.3 μA	3 V	1
(**#5**) - 3rd. Order bandpass filter around 110 Hz. [20]	Switched Capacitors & Continuous-time preamp	4	6.9 μV_{rms}	50–750	1 μA	2–2.8 V	1.9

The results are summarized in Table 5. Measurement results are consistent with a circuit adequate for inclusion in a high performance rate adaptive pacemaker [2, 3].

5 Conclusions

New design techniques for very low frequency analog filters were tested in the design of a fully integrated G_m-C, 0.5–7 Hz, CMOS bandpass filter-amplifier. Large time constants were obtained using series-parallel division of current in symmetrical OTAs to achieve low transconductances with an extended linear range. The measured and predicted performance of the filter resulted in a very good solution in terms of power consumption, noise, offset, and occupied area. The low input referred noise, and power consumption should be highlighted. A complete accelerometer-based activity sensing system using this filter was tested while carrying out different physical activities, demonstrating that it is suitable for incorporation in modern rate adaptive pacemakers.

A comparative analysis is shown in Table 6, where the main characteristics of several micro-power filters are summarized. The first row relates to the activity sensing circuit here presented, including the bandpass amplifier, and rectifier-time average stage of Section 3.6. Row (#2) gives data from an activity sensing circuit using continuous-time techniques but requiring a large number of external components [3]. Row (#3) contains information on a switched-capacitor filter, rectifier, and time averaging used for the same purpose, based on a piezoresistive accelerometer [18]. The three circuits are different approaches to the same problem but the G_m-C filter using series-parallel current division shows a considerable reduction in power consumption and input noise, while using no external elements. The occupied area has been reduced but the circuits in rows (#2, #3) were fabricated in a 2.4 μm technology. Regarding power consumption and noise, it is possible to assume that in a very low frequency filter, the technology does not have much impact on circuit performance. Rows (#4, #5) contain information about two filters, which are intended to form part of biomedical devices, and have a set of specifications close to those of the physical activity sensing circuit. The first is a 2.4 Hz low pass filter, presented by Solis Bustos et al. [19] using combined continuous-time techniques. The circuit is compact in area while implementing a high order transfer function with a 60-dB dynamic range performance. This filter requires more power consumption and input noise is higher in comparison to the filter in row (#1). The reason for this may be the use of capacitor scaling, and partial current cancellation OTAs. The data in row (#5) correspond to a low-power front end for a pacemaker atrial sensing channel [20]. It is a bandpass filter-amplifier centered at 110 Hz, with several special characteristics. The circuit combines a continuous-time preamplifier-antialiasing stage at the input, followed by a 3rd order switched capacitor stage. Four external discrete elements are used in the filter but the use of at least 2 external ones is mandatory in an atrial sensing channel for safety purposes. The filter also takes advantage of high resistivity poly layers to implement MΩs resistors in the preamplifier. The resulting circuit is compact in area, with a very low power consumption, and a very low input referred noise (observe that the bandwidth of this filter is approximately 9 times that of the filter in row (#1)). In this case the reduced noise is possible due to the low flicker noise in the bandpass frequency.

An overall conclusion is that the system here presented improves the performance of previously designed activity sensing circuits in [3, 18]. Its performance is also comparable to other high-end modern filters with similar specifications [19, 20]. The main advantage of G_m-C filters is that they are

extremely simple allowing a reduced power consumption, circuit area, and noise.

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