Journal of
Low Power Electronics and Applications

MDPI

Article

Bridging the Gap between Design and Simulation of Low-Voltage CMOS Circuits †

Cristina Missel Adornes *, Deni Germano Alves Neto, Márcio Cherem Schneider and Carlos Galup-Montoro

Department of Electrical and Electronics Engineering, Federal University of Santa Catarina, Florianópolis 88040-900, Brazil; deni.alves@posgrad.ufsc.br (D.G.A.N.); m.c.schneider@ufsc.br (M.C.S.); carlos@eel.ufsc.br (C.G.-M.)

* Correspondence: cristina.m.adornes@posgrad.ufsc.br

† This paper is an extended version of our paper published in 2021 IEEE Nordic Circuits and Systems Conference (NorCAS).

Abstract: This work proposes a truly compact MOSFET model that contains only four parameters to assist an integrated circuits (IC) designer in a design by hand. The four-parameter model (4PM) is based on the advanced compact MOSFET (ACM) model and was implemented in Verilog-A to simulate different circuits designed with the ACM model in Verilog-compatible simulators. Being able to simulate MOS circuits through the same model used in a hand design benefits designers in understanding how the main MOSFET parameters affect the design. Herein, the classic CMOS inverter, a ring oscillator, a self-biased current source and a common source amplifier were designed and simulated using either the 4PM or the BSIM model. The four-parameter model was simulated in many sorts of circuits with very satisfactory results in the low-voltage cases. As the ultra-low-voltage (ULV) domain is expanding due to applications, such as the internet of things and wearable circuits, so is the use of a simplified ULV MOSFET model.

Keywords: ACM model; MOSFET modeling; circuit simulation; ultra-low voltage

Citation: Adornes, C.M.; Alves Neto, D.G.; Schneider, M.C.; Galup-Montoro, C. Bridging the Gap between Design and Simulation of Low-Voltage CMOS Circuits. *J. Low Power Electron. Appl.* **2022**, *12*, 34. https://doi.org/10.3390/jlpea12020034

Academic Editors: Orazio Aiello and Andrea Acquaviva

Received: 16 February 2022
Accepted: 5 May 2022
Published: 16 June 2022

1. Introduction

The design and simulation of integrated circuits (IC) are assisted by compact MOSFET models, which started to be developed in the 1960s [1] for long-channel devices. The technological progress promoted the down-scaling of semiconductor devices, giving rise to short-channel effects and their interference in circuit performance; thereby, these short-channel effects were incorporated into the existing long-channel based models to improve circuit-design efficiency.

Although BSIM [2,3] has been broadly used as the main MOSFET model to simulate MOS circuits in EDA tools, the complexity of its calculations and numerous parameters have opened a gap between circuit simulations and designs by hand [4,5], which has complicated the understandings of how the main MOSFET parameters relate to simulation results. Therefore, it is in designers' interest to have models founded on physics available in the simulator, such as those based on the inversion charge.

In the fast expanding ultra-low-voltage domain [6], some short-channel effects, such as velocity saturation, are not relevant; thus, a simplified MOSFET model can be satisfactory for circuit design. Targeting the increasing number of ultra-low-voltage designs [7–12], this work proposes a four-parameter model (4PM) based on the all-region advanced compact MOSFET model (ACM) [13].

In this work, the 4PM was carried out with the description language Verilog-A to easily simulate circuits in the commercial Cadence® Virtuoso® simulator, which implements BSIM 4.5 through a private propriety interface [14]. Hardware description languages

(HDLs), such as Verilog-A, are interchangeable with different simulators and assist designers in describing circuits and systems in a variety of behavioral modeling levels. We chose Verilog-A because it combines simplicity, functionality and portability [14].

The paper is structured as described in the following lines. Section 2 briefly introduces the four-parameter model (4PM). Section 3 describes the methods employed to extract the model's parameters and describes the extraction results of the parameters with temperature and process variations. Section 4 describes how to carry out the 4PM in Verilog-A for its inclusion in Cadence. Section 5 presents the results of the simulations carried out by using BSIM or the 4PM in Verilog-A. Four circuits designed according to the ACM model were simulated: a CMOS inverter, a ring oscillator, a self-biased current source and a common source amplifier. Conclusions are drawn in Section 6.

2. The Four-Parameter Model (4PM)

The advanced compact MOSFET (ACM) model describes static and small-signal low-frequency characteristics of MOS transistors in all regions of operation [13]. ACM employs three main transistor parameters: the specific current I_S, the threshold voltage V_{T0} and the slope factor n, which are usually sufficient to design a broad amount of circuits.

Nevertheless, the four-parameter model herein also employs drain-induced barrier lowering (DIBL), a secondary effect [13]. In spite of being a very pronounced effect for short-channel transistors, the DIBL cannot be ignored for long-channel transistors in weak inversions. For long-channel transistors in strong inversions (out of the scope of this work), DIBL is overshadowed by channel-length modulation.

In the long-channel ACM model [13], the drain current I_D in Figure 1 is split into the forward term I_F and the reverse term I_R, both of them dependent on the voltage V_{GB}. The component I_F also depends on V_{SB}, while I_R depends on V_{DB}. This source-drain symmetry is given by using (1).

$$I_D = I_F - I_R = I_S\,(i_f - i_r\,) \tag{1}$$

The specific current I_S, depicted in (2), is influenced by the device's geometry and technological parameters, such as the carrier mobility μ, C_{ox}, the slope factor n and temperature through the thermal voltage ϕ_t.

$$I_S = \mu C_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{2}$$

The relationship between the voltages at the device terminals and the normalized inversion charge density at the source (drain) $q_{IS(D)}$ is established by using the normalized form of the unified charge-control model (UCCM) in (3).

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{IS(D)} - 1 + \ln q_{IS(D)} \tag{3}$$

The pinch-off voltage V_P can be approximated by using (4), where V_{T0} is the equilibrium threshold voltage that corresponds to the gate voltage for which $V_P = 0$ and for which σ is the magnitude of the DIBL coefficient. In the four-parameter model, the DIBL effect must comply with the MOSFET symmetry.

$$V_P = \frac{V_{GB} - V_{T0} + \sigma V_{DB} + \sigma V_{SB}}{n} \tag{4}$$

Equation (5) gives the definition of the normalized inversion charge, which is the inversion charge (Q_I) normalized to the pinch-off charge ($-nC_{ox}\phi_t$).

$$q_{IS(D)} = \frac{Q_I}{-nC_{ox}\phi_t} \tag{5}$$

$$q_{IS(D)} = \sqrt{1 + i_{f(r)}} - 1 \tag{6}$$

The voltage-to-inversion level relationship is established by applying (6) to (3), which results in (7a,b), also known as the unified current-control model (UICM). For design purposes, $i_f < 1$ characterizes an operation in a weak inversion (WI), while for $i_f > 100$, it is assumed there is an operation in a strong inversion (SI). For inversion levels between 1 and 100, it is said that the transistors operate in moderate inversion (MI).

$$I_{F(R)} = I_S F\left[\frac{V_P - V_{S(D)}}{\phi_t}\right] \tag{7a}$$

$$F^{-1} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{7b}$$

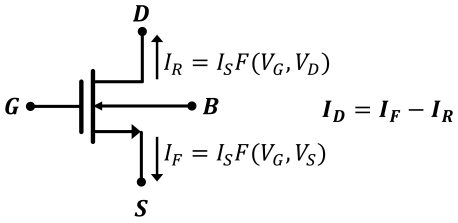

Figure 1. Symbol of an n-channel MOSFET transistor and its four terminals: gate (G), source (S), drain (D) and bulk (B). Source-drain symmetry illustrated by using currents.

2.1. Small-Signal Transconductances

Small-signal transconductances are essential for both the design of integrated circuits and the extraction of the four transistor parameters. Figure 2 presents the low-frequency small-signal model for MOSFET in which the variation of the drain current is expressed by using (8), where g_{mg}, g_{ms}, g_{md} and g_{mb} are, respectively, the gate, source, drain and bulk transconductances given by using (9); v_g, v_s, v_d and v_b represent small variations in the gate, source, drain and bulk voltages, respectively.

$$i_d = g_{mg} v_g - g_{ms} v_s + g_{md} v_d + g_{mb} v_b \tag{8}$$

$$g_{mg} = \frac{\partial I_D}{\partial V_G}; g_{ms} = -\frac{\partial I_D}{\partial V_S}; g_{md} = \frac{\partial I_D}{\partial V_D}; g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{9}$$

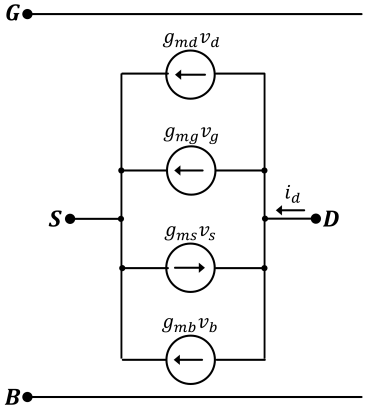

Figure 2. Low-frequency small-signal model of the MOSFET.

The relationships between the transconductances and the inversion levels are obtained by applying the partial derivatives of (9) to the UICM along with (1).

The transconductance-to-current ratios, in terms of inversion level, are given by using expressions (10)–(12) in which $I_{D,sat}$ stands for the approximation of the drain current in the saturation region, where $i_r << i_f$ [13].

$$\phi_t \frac{g_{ms}}{I_{D,sat}} = \left(1 - \frac{\sigma}{n}\right) \frac{2}{\sqrt{1+i_f}+1} \tag{10}$$

$$\phi_t \frac{g_{md}}{I_{D,sat}} = \left(\frac{\sigma}{n}\right) \frac{2}{\sqrt{1+i_f}+1} \tag{11}$$

$$\phi_t \frac{g_m}{I_{D,sat}} = \left(\frac{1}{n}\right) \frac{2}{\sqrt{1+i_f}+1} \tag{12}$$

2.2. Dynamic Model

The dynamic model of MOS transistors includes intrinsic and extrinsic capacitances. Figure 3 presents a simplified dynamic model that includes both the intrinsic and extrinsic parts.

In Figure 3a, the extrinsic capacitance $C_{gse(de)}$ includes an unavoidable overlap between the gate and the source (drain) diffusion and fringing capacitances, while the substrate-source (drain) junctions modeled by (nonlinear) diode capacitances correspond to $C_{bse(de)}$. A more complete model for the extrinsic part should include parasitic resistances as well [15].

The field effect of MOS transistors occurs in the intrinsic part between the source and drain. The classical MOSFET model in Figure 3b contains five capacitances added to the small-signal model of Figure 2.

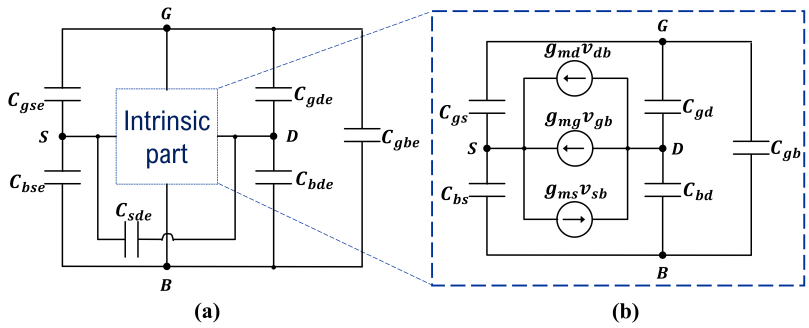

Figure 3. MOSFET dynamic model with (**a**) extrinsic and (**b**) intrinsic parts [13].

The calculation of the intrinsic capacitance coefficients is based on the unified charge-control model (UCCM) and on the quasi-static charge conserving model [13]. The effect of the DIBL parameter on the five intrinsic capacitances is summarized in expressions (15)–(19) in which C_{gs0} and C_{gd0} are the gate-source and gate-drain capacitances of the long-channel model, respectively. In (13) and (14), $\alpha = \frac{1+q_{iD}}{1+q_{iS}}$ is the channel linearity factor.

$$C_{gs0} = \frac{2}{3} WLC_{ox} \frac{1+2\alpha}{(1+\alpha)^2} \frac{q_{iS}}{1+q_{iS}} \tag{13}$$

$$C_{gd0} = \frac{2}{3} WLC_{ox} \frac{\alpha^2+2\alpha}{(1+\alpha)^2} \frac{q_{iD}}{1+q_{iD}} \tag{14}$$

$$C_{gs} = \left(1 - \frac{\sigma}{n}\right) C_{gs0} - \frac{\sigma}{n} C_{gd0} \tag{15}$$

$$C_{gd} = \left(1 - \frac{\sigma}{n}\right) C_{gd0} - \frac{\sigma}{n} C_{gs0} \tag{16}$$

$$C_{gb} = \left(1 - \frac{1}{n}\right)(WLC_{ox} - C_{gs0} - C_{gd0}) + \frac{2\sigma}{n}[(n-1)WLC_{ox} - C_{gs0} - C_{gd0}] \quad (17)$$

$$C_{bs} = (n-1)C_{gs} \quad (18)$$

$$C_{bd} = (n-1)C_{gd} \quad (19)$$

Figure 4 presents plots of the five intrinsic capacitances normalized to C_{ox} as functions of the pinch-off voltage. The curves were obtained for an NMOS transistor with $\frac{W}{L} = \frac{0.6\ \mu m}{0.3\ \mu m}$ and $V_{DS} = 1$ V.

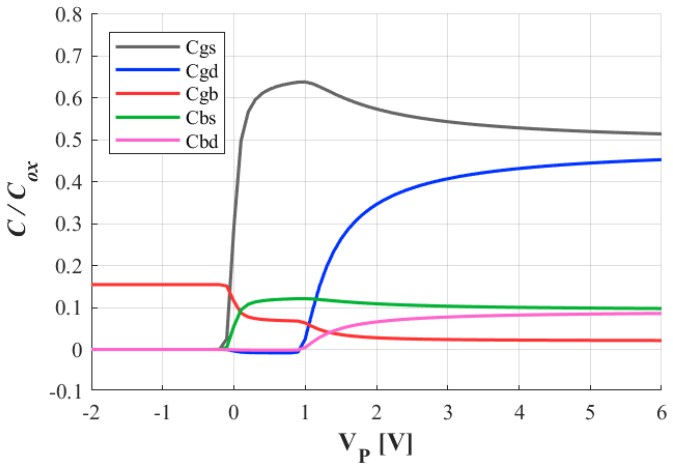

Figure 4. Capacitances (15)–(19) normalized to C_{ox} versus the pinch-off voltage for $V_{DS} = 1$ V.

3. Parameter Extraction

The accuracy of the transistor's characteristics depends on both the model and the accuracy of the parameters. The model's parameters should be easily and accurately extracted; otherwise, the model will not be successful [14]. Thus, this section presents the methods to extract the four transistor parameters.

3.1. Extraction of Threshold Voltage (V_{T0}), Specific Current (I_S) and Slope Factor (n)

The values of the threshold voltage (V_{T0}), the specific current (I_S) and slope factor (n) were extracted from the g_m/I_D curve [16] illustrated in Figure 5b, which was measured with the circuit configuration in Figure 5a.

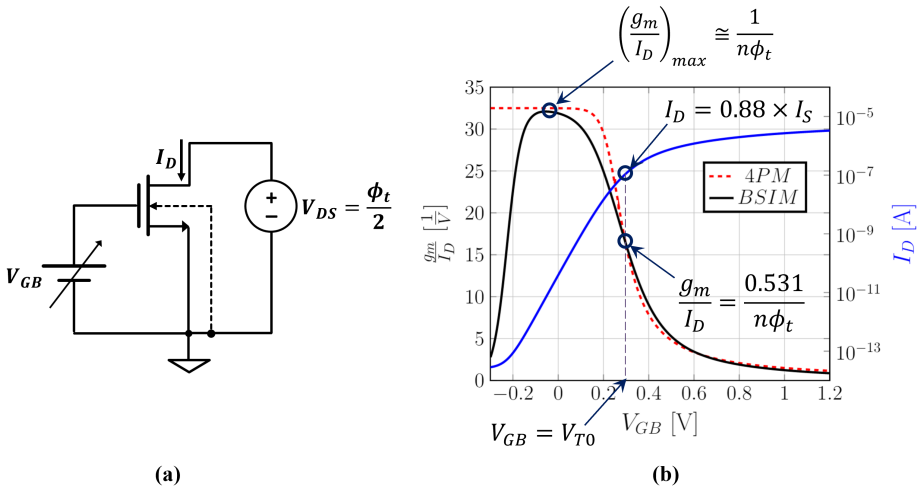

Figure 5. (**a**) Circuit to extract parameters from (**b**) the g_m/I_D and I_D curves.

Based on the method described in [16], the values of the threshold voltage and the specific current were determined through the g_m/I_D characteristic written in (20), which was valid for all regions of operation.

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_G} = \frac{2}{n\phi_t(\sqrt{1+i_f}+\sqrt{1+i_r})} \tag{20}$$

$$\frac{V_{DS}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{21}$$

Expression (21) is obtained by applying the UICM to the drain and source terminals. For $i_f = 3$ and $V_{DS} = \frac{\phi_t}{2}$, expression (21) results in $i_r = 2.12$; under these conditions, V_{T0} corresponds to the gate voltage at which $g_m/I_D = 0.531(g_m/I_D)_{max}$, while I_S corresponds to $I_D/0.88$, where I_D is the drain current at $V_{GB} = V_{T0}$. The method described for the extraction of the values of V_{T0} and I_S assumes that the variation of the slope factor with the gate voltage is negligible. The slope factor (n) can be extracted from (22), which is the asymptotic value of the g_m/I_D curve in a weak inversion. The points used to determine V_{T0}, I_S and n are shown in Figure 5b.

$$\left(\frac{g_m}{I_D}\right)_{max} \approx \frac{1}{n\phi_t} \tag{22}$$

The DIBL factor (σ) does not appear in (20) because the short-channel effects, namely DIBL, velocity saturation and channel length modulation are not relevant in the linear region. Consequently, the extraction of V_{T0}, I_S and n in the linear region is also valid for short-channel devices.

3.2. Extraction of Drain-Induced Barrier-Lowering Factor (σ)

The DIBL factor σ is a small-signal parameter that affects the intrinsic voltage gain of the common source amplifier. Figure 6 presents a schematic to determine the common-source intrinsic gain (CSIG) and the equivalent small-signal model [17] of the amplifier.

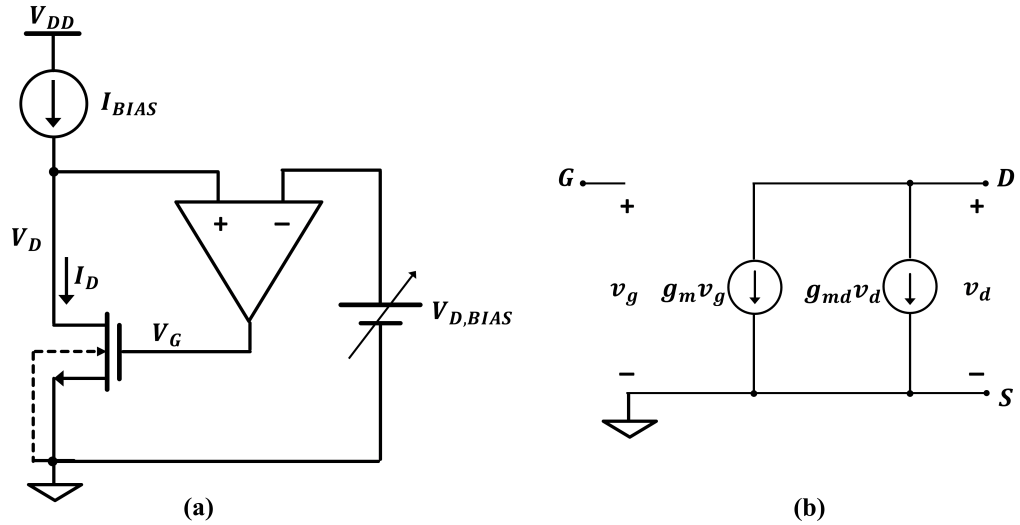

Figure 6. (**a**) Circuit to determine the CSIG and (**b**) its equivalent small-signal model.

In saturation, the use of the transconductance-to-current characteristics (11) and (12) yields the CSIG in (23).

$$A_{V,CS} = \frac{v_d}{v_g} = -\frac{g_m}{g_{md}} = -\frac{1}{\sigma} \tag{23}$$

To determine the common-source intrinsic gain through a simulation, an ideal operational amplifier was included, as shown in Figure 6a, to set the DC operating point required for the small-signal measurement.

3.3. Extraction Results

The g_m/I_D and CSIG methods presented herein were used to extract the four parameters of each transistor used throughout this work. The four parameters were also extracted for various temperatures and corners of process variation.

Figure 7 shows the dependence of the parameters of the 4PM on the temperature of an NMOS transistor with $\frac{W}{L} = \frac{1\ \mu m}{0.3\ \mu m}$. As expected, the threshold voltage is a linearly decreasing function of the temperature [18], whereas the DIBL factor increases linearly with temperature [19,20]. The slope factor is, for practical purposes, independent of the temperature. The dependence of the specific current on the temperature is, in general, not predictable due to uncertainty in the variation of the mobility with the temperature.

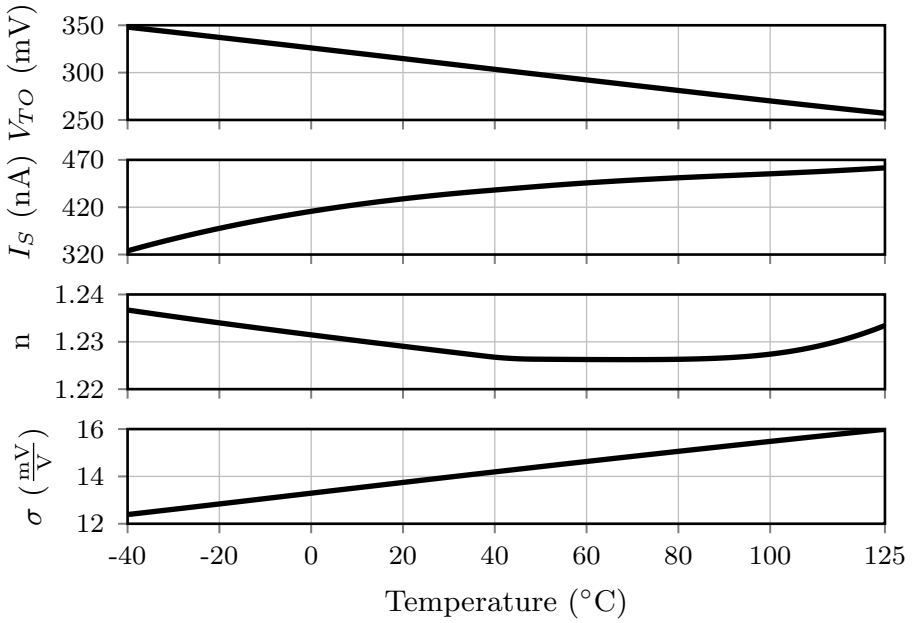

Figure 7. Parameters of the 4PM vs. temperature of a medium (nominal) V_T NMOS transistor with $W/L = 1\ \mu m/0.3\ \mu m$.

Tables 1 and 2 summarize the extracted values for NMOS and PMOS long-channel ($\frac{W}{L} = \frac{1\ \mu m}{1\ \mu m}$) and short-channel ($\frac{W}{L} = \frac{1\ \mu m}{0.3\ \mu m}$) transistors, respectively, from a 0.18 µm technology. The four parameters were extracted at room temperature for extreme corners (slow and fast) and for the typical (nominal) condition.

Table 1. Extracted parameters for medium-V_T NMOS/PMOS transistors with $\frac{W}{L} = \frac{1\ \mu m}{1\ \mu m}$.

Transistor	Slow		Nominal		Fast	
	NMOS	**PMOS**	**NMOS**	**PMOS**	**NMOS**	**PMOS**
V_{TO} **[mV]**	316	−239	291	−211	266	−183
I_S **[nA]**	99	35	111	40	124	45
n	1.19	1.18	1.20	1.18	1.22	1.17
$\sigma[\frac{mV}{V}]$	5.9	18	5.9	18	5.9	19

Table 2. Extracted parameters for medium-V_T NMOS/PMOS transistors with $\frac{W}{L} = \frac{1\ \mu m}{0.3\ \mu m}$.

Transistor	Slow		Nominal		Fast	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
V_{TO} [mV]	338	−272	311	−239	283	−206
I_S [nA]	313	81	420	106	543	137
n	1.24	1.17	1.23	1.18	1.22	1.17
$\sigma[\frac{mV}{V}]$	14	19	14	20	14	20

As expected, the parameters that varied the most were threshold voltage and specific current. The threshold voltage varied 8.6% in relation to the nominal value of the NMOS transistors and 13.3% in relation to the PMOS transistors. The specific current varied around 13% in relation to the nominal value in long-channel transistors and up to 29.3% in short-channel transistors. The effects of these variations in a circuit are presented in Section 5.

4. Including the 4PM in Cadence

To simulate MOS circuits through the 4PM in a commercial simulator, the model was carried out in Verilog-A, an HDL that describes the electrical behavior of analog devices, circuits and systems. The Verilog-A compiler handles every required interaction between the model and the simulation software. Furthermore, Verilog-A supports various functions to assist in descriptions, such as standard mathematical functions, transcendental and hyperbolic functions as well as a set of statistical functions [14].

The inversion levels in the UICM (7) simplify the design of various MOS circuits; however, for a simulator, the voltages at the device's terminals are the inputs, while the current flowing through the device is the output.

When solving (7) for the drain current, a transcendental equation arises, which can be solved numerically. Nonetheless, the simulator solves the equations point by point; thus, iterative calculations to find the solution of one single point waste time and processing power.

Siebel [21] explored some algorithms to improve the implementation of (7) in simulators, reaching the conclusion that algorithm 443 [22] finds an accurate solution for the drain current in only one iteration.

Algorithm 443 solves transcendental equations of the form $x = we^w$. To resemble such a form, the UCCM in (3) can easily be rewritten as (24).

$$e^{\left(\frac{V_P - V_{S(D)B}}{\phi_t} + 1\right)} = q_{IS(D)} e^{q_{IS(D)}} \tag{24}$$

Owing to the similarity of (24) to $x = we^w$, algorithm 443 is employed to determine the drain current by following a few steps: first, the normalized forward and reverse charge densities $q_{IS(D)}$ are determined; then, by applying their values in (6), we obtain the respective inversion levels $i_{f(r)}$, which, at last, are applied in (1), resulting in the drain current I_D. A sample of the Verilog-A description is presented in Appendix A to clarify how algorithm 443 was implemented to solve (24).

For the dynamic model, expressions (13)–(19) were implemented in Verilog-A just after the drain current was calculated. The overlap capacitances were also included as extrinsic capacitances. The transconductances were used as design parameters that could easily be derived from the current–voltage relation, namely UICM.

Model Results

For the sake of comparisons with BSIM 4.5 results, the four-parameter model described in Verilog-A was simulated employing single transistors in typical conditions at room temperature. Figures 8 and 9 present the $I_D \times V_{GS}@V_{DS} = 200$ mV and $I_D \times V_{DS}@V_{GS} = 200$ mV,

respectively, for long-channel ($\frac{W}{L} = \frac{1\ \mu m}{1\ \mu m}$) and short-channel ($\frac{W}{L} = \frac{1\ \mu m}{0.3\ \mu m}$) transistors. Note that in both figures, ACM refers to the 4PM.

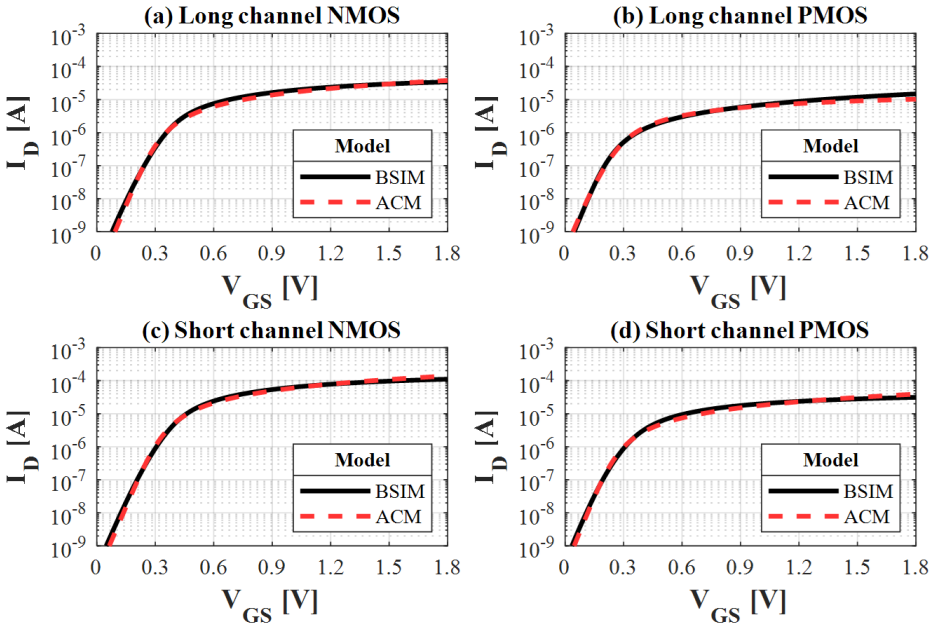

Figure 8. $I_D \times V_{GS}$ @ $V_{DS} = 200$ mV for (**a**) medium (nominal) V_T long-channel NMOS and (**b**) PMOS transistors and for (**c**) medium (nominal) V_T short-channel NMOS and (**d**) PMOS transistors.

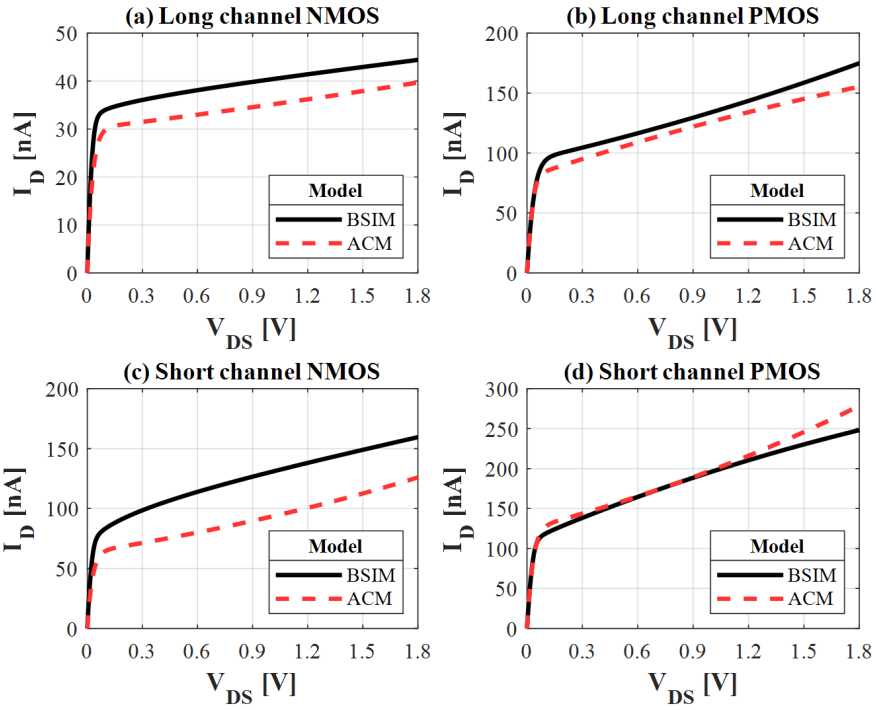

Figure 9. $I_D \times V_{DS}$ @ $V_{GS} = 200$ mV for (**a**) medium (nominal) V_T long-channel NMOS and (**b**) PMOS transistors and for (**c**) medium (nominal) V_T short-channel NMOS and (**d**) PMOS transistors.

Simulations carried out for V_{DS} and V_{GS} with 100 mV, 500 mV and 1 V led to current–voltage characteristics similar to those in Figures 8 and 9; therefore, they were not included herein.

Overall, the Verilog-A simulation for long- and short-channel transistors provided results close to BSIM's. Notably, for high values of V_{DS}, the drain current of the 4PM

drifts away from BSIM's due to effects that are not taken into account in the ACM model used herein.

5. Circuit Examples and Simulation Results

Four circuits were simulated through either the 4PM in Verilog-A descriptions or BSIM 4.5 [23]: the classic CMOS inverter, an 11-stage ring oscillator, a self-biased current source (SBCS) and a common-source amplifier.

5.1. CMOS Inverter

The CMOS inverter in Figure 10 is a versatile and simple circuit employed in various ULV digital circuits [6,8] and analog building blocks, such as amplifiers and oscillators [10,24].

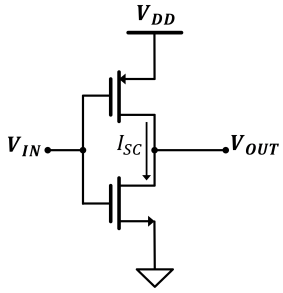

Figure 10. The classic CMOS inverter.

Well-designed CMOS inverters usually present a perfect balance between the N and P networks, which means that in the voltage transfer curve, the mid-point voltage corresponds to $V_{OUT} = V_{IN} = V_{DD}/2$. The CMOS inverter herein was designed to be balanced for the supply voltage V_{DD} = 100 mV, room temperature and typical process parameters.

For this particular design, we chose transistors with threshold voltages lower than those of the standard transistor, which favors them in the design of ULV circuits. They are called medium-V_T transistors, and their minimum channel length is 300 nm in this 0.18 µm technology. The PMOS and NMOS transistors were designed with channel lengths of $L_P = L_N = 300$ nm and widths of $W_P = W_N = 600$ nm. The values in Table 3 correspond to the extracted parameters of these medium-V_T transistors for the simulation through the 4PM in Verilog-A.

Table 3. Corner-extracted parameters for medium-V_T NMOS/PMOS transistors with $\frac{W}{L} = \frac{600\text{ nm}}{300\text{ nm}}$.

Transistor	Slow		Nominal		Fast	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
V_{TO} [mV]	339	−308	309	−269	280	−230
I_S [nA]	206	70	280	89	366	111
n	1.25	1.25	1.24	1.25	1.23	1.24
$\sigma[\frac{\text{mV}}{\text{V}}]$	15	22	15	23	15	23

The design was validated through a DC analysis in Cadence® by using each model (4PM and BSIM 4.5) separately. The results of the DC simulations for five different supply voltages V_{DD}s at room temperature and typical conditions are depicted in Figure 11, which includes the voltage transfer characteristic (VTC), small-signal gain and short-circuit current (I_{SC}). From Figure 11, it can be verified that the ACM model with only four parameters is sufficient to properly describe the electronic behavior of the classic CMOS inverter in the ULV domain.

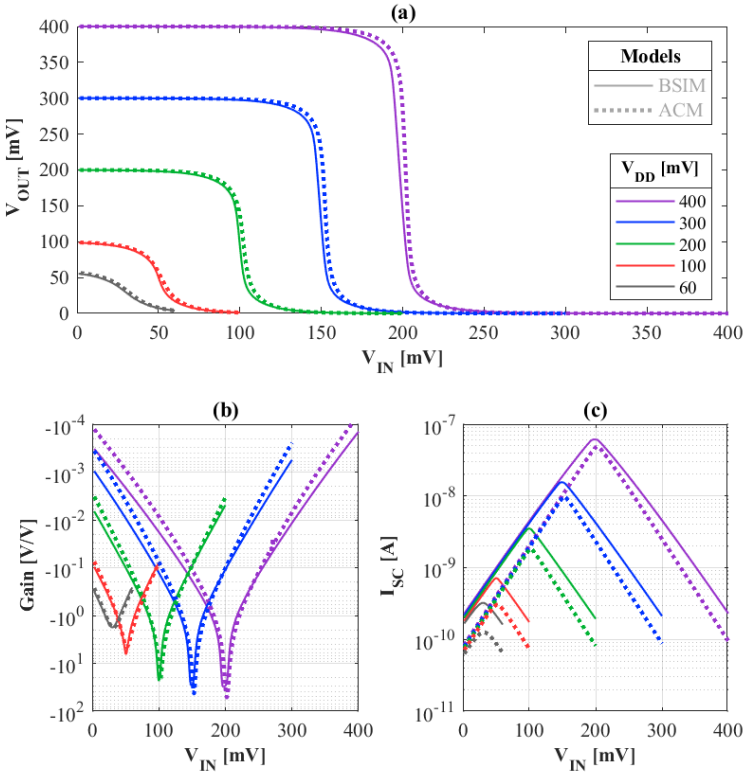

Figure 11. CMOS inverter results of (**a**) voltage-transfer characteristic (VTC), (**b**) small-signal gain and (**c**) short-circuit current.

Figure 12 presents the VTC curves for the CMOS inverter across the corners of process variation for both BSIM and the 4PM at supply voltages of 100 mV and 300 mV and a temperature of 300 K. Even with variations of up to 15% and 30% in the threshold voltage and specific current, respectively, the 4PM clearly adapts to the corners and follows BSIM since the four parameters were extracted for each corner.

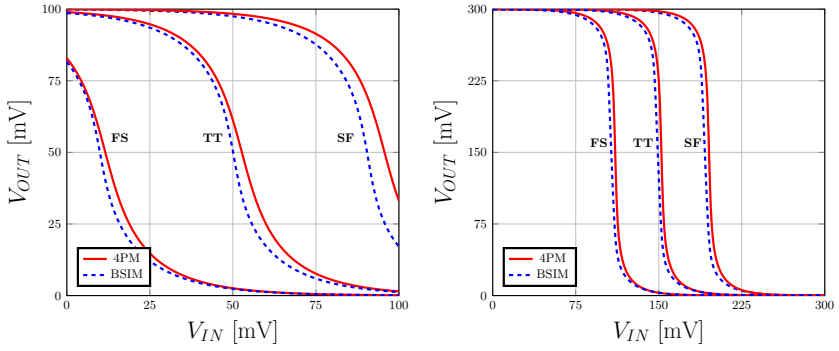

Figure 12. Voltage-transfer characteristics of the CMOS inverter using BSIM and the 4PM across the corners of process variation. (**a**) V_{DD} = 100 mV. (**b**) V_{DD} = 300 mV.

5.2. Ring Oscillator

In Figure 13, the ring oscillator comprises N CMOS inverters in a loop and the load capacitance C_L in between stages, which includes external capacitors that load each node, along with the transistors' intrinsic and extrinsic capacitances presented in Section 2.2. The load capacitance is crucial to set the frequency of oscillation and is critical for the successful start-up of the oscillator.

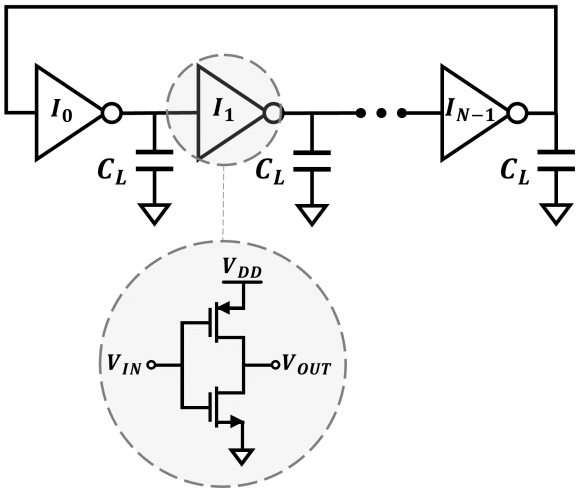

Figure 13. Ring oscillator.

According to [24], in order to facilitate the start-up of the ring oscillator in the ultra-low-voltage domain, the minimum gain required to establish a condition of oscillation can be reduced by increasing the number of stages in the ring oscillator. We chose the number of stages $N = 11$, which corresponds to a minimum voltage gain of 1.04 V/V for the start-up of oscillations.

Figure 14 presents the voltage signal at one of the stages of the ring oscillator for the supply voltage V_{DD} of 100 mV. Table 4 summarizes the frequencies obtained through the use of either ACM or BSIM for various V_{DD} values without the inclusion of any external capacitor.

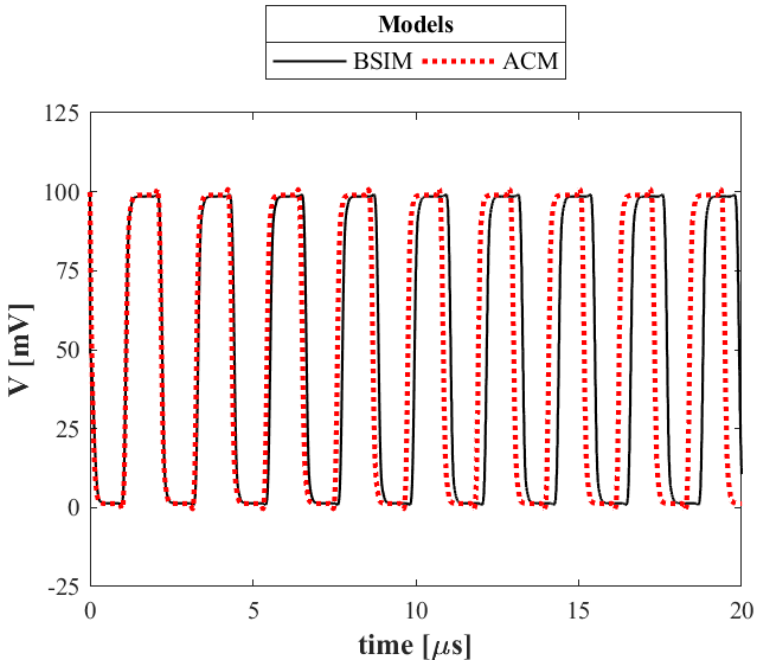

Figure 14. Voltage signal in the time domain at one of the stages of the oscillator. Results for BSIM and 4PM simulations at 100 mV of supply voltage.

Table 4. Oscillation frequency at various VDDs obtained through time-domain simulations of the 11-stage ring oscillator without external C_L.

V_{DD}	BSIM	4PM	$\frac{f_{4PM}}{f_{BSIM}}$
400 mV	81.3 MHz	187.2 MHz	2.30
300 mV	23.7 MHz	52.1 MHz	2.20
200 mV	3.79 MHz	5.87 MHz	1.55
100 mV	452 kHz	463 kHz	1.02
60 mV	198 kHz	177 kHz	0.89

As expected, due to a lack of extrinsic capacitances associated with fringing and diode junctions [15] in the implemented dynamic model, the frequency of oscillation using the 4PM was higher than BSIM's overall. Table 4 shows that the oscillation frequency obtained through the 4PM diverged from the frequency obtained through BSIM at $V_{DD} = 300$ mV and 400 mV for more than 200%, which suggests that the implemented dynamic model lacks sufficient information to provide frequency results closer to BSIM's in these voltages.

To further evaluate the difference in the oscillation frequency, we added the external capacitor $C_L = 1\ pF$ between stages. Figure 15 presents the oscillation frequency at supply voltages from 60 mV to 400 mV.

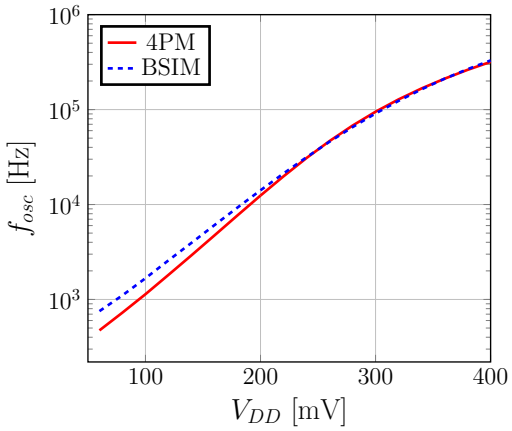

Figure 15. Oscillation frequency vs. the supply voltage V_{DD}.

From Figure 15 and Table 5, it can be seen that the inclusion of high-value external capacitors attenuated the effect of the capacitances inherent to the ring oscillator on the frequency response and, consequently, improved the ACM's accuracy in relation to BSIM for voltages from 200 mV to 400 mV. However, it deteriorated the results for voltages below 100 mV. Overall, the 4PM delivers a time/frequency domain result that closely matches BSIM's.

Table 5. Oscillation frequency at various V_{DD}s obtained through time-domain simulations of the 11-stage ring oscillator with external $C_L = 1\ pF$.

V_{DD}	BSIM	4PM	$\frac{f_{4PM}}{f_{BSIM}}$
400 mV	329.4 kHz	316.2 kHz	0.96
300 mV	91.0 kHz	94.4 kHz	1.04
200 mV	14.1 kHz	12.3 kHz	0.87
100 mV	1.67 kHz	1.12 kHz	0.67
60 mV	753 Hz	469 Hz	0.62

These results suggest the capacitances in BSIM have a strong dependence on the supply voltage, a dependence which was not incorporated in the implemented extrinsic

dynamic model, hence the observed difference in the oscillation frequency at various supply voltages.

In addition, the computational efficiency was verified by comparing the CPU transient simulation time required to simulate the oscillator with the external $C_L = 1\ pF$ at the supply voltage $V_{DD} = 300$ mV, which provides signals with similar frequencies for BSIM and ACM ($f_{ACM}/f_{BSIM} = 1.04$). The total CPU time required to run the transient analysis with BSIM was 76.25 s, while the same simulation required a total CPU time of 55.64 s using the 4PM in Verilog-A, representing 73% of the time BSIM used, which is very significant when it comes to several long simulation runs.

5.3. Self-Biased Current Source (SBCS)

The design of the self-biased current source (SBCS) in Figure 16, for the output current $I_{OUT} = 100$ nA and supply voltage $V_{DD} = 1.8$ V, was based on the ACM model [25–27].

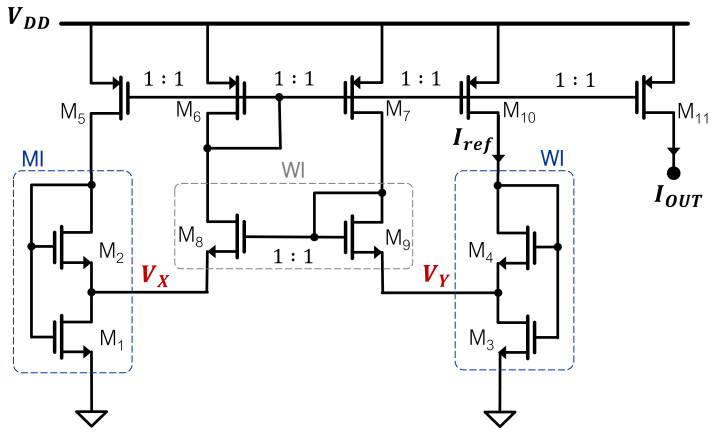

Figure 16. Self-biased current source (SBCS) circuit.

The core of the SBCS in Figure 16 is the self-cascode MOSFET (SCM), composed of transistors M_1 and M_2, which operate in a moderate inversion. Transistors M_3 and M_4 form the second SCM biased in a weak inversion to generate the proportional to absolute temperature (PTAT) voltage V_Y [26,27].

Transistors $M_{2(4)}$ are in a saturation, while $M_{1(3)}$ is in a triode; therefore, $I_{D2} \cong I_{S2} i_{f2}$ and $I_{D1} = I_{S1}(i_{f1} - i_{r1}) = I_{ref}(N+1)$. Since $V_{P1} = V_{P2} = V_P$ and $V_{D1} = V_{S2}$, we have $i_{r1} = i_{f2}$.

The specific current I_S can also be written as $I_S = I_{SH} S$, where I_{SH} is the sheet normalization current and S is the aspect ratio $\frac{W}{L}$, which, combined with (1), yields the relationship (25).

$$\alpha_{12(34)} = \frac{i_{f1(3)}}{i_{f2(4)}} = 1 + \frac{S_2(4)}{S_1(3)}\left(1 + \frac{1}{N}\right) \tag{25}$$

The SCM intermediate voltage $V_{X(Y)}$ relates to the inversion level through the design Equations (26) and (27), which can be directly derived from the ACM using (7) and (25).

$$\frac{V_X}{\phi_t} = \sqrt{1 + \alpha_{12} i_{f2}} - \sqrt{1 + i_{f2}} + ln\left(\frac{\sqrt{1 + \alpha_{12} i_{f2}} - 1}{\sqrt{1 + i_{f2}} - 1}\right) \tag{26}$$

$$\frac{V_Y}{\phi_t} = \ln \alpha_{34} \tag{27}$$

To simplify the design, we chose $i_{f2} = 15$ and $S_1 = S_2$, which results in $\alpha_{12} = 3$. From this starting point, it is sufficient to extract the sheet normalization current of M_2, as shown in Section 3.1, and to use (1) to determine the aspect ratio. Once V_X is determined,

α and the inversion levels of the other transistors can be calculated, along with their aspect ratios.

Table 6 summarizes the sizes, series/parallel associations and inversion levels of the transistors. Table 7 presents the four parameters extracted for the three transistors used in the SBCS.

Table 6. Sizes and and inversion levels of the transistors of the SBCS.

Transistor	$\frac{W}{L} \times \frac{N_{parallel}}{N_{series}}$	i_f
$M_{1,2}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{1}{4}$	15
M_3	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{20}{1}$	0.32
M_4	$\frac{4.0\ \mu m}{2.0\ \mu m} \times \frac{40}{1}$	0.01
$M_{8,9}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{35}{1}$	0.1
$M_{5-7,10,11}$	$\frac{0.5\ \mu m}{2.0\ \mu m} \times \frac{1}{1}$	10

Table 7. Extracted parameters of transistors used in the SBCS.

Transistor	NMOS		PMOS
W [µm]	0.5	4.0	0.5
L [µm]	2.0	2.0	2.0
I_S [nA]	29	63	10
V_{T0} [mV]	423	444	−428
n	1.27	1.27	1.31
σ [mV/V]	2.2	2.4	6.5

The DC simulation results in Figure 17 were obtained through the use of either BSIM or the 4PM for a voltage sweep on V_{DD} from 0 to 1.8 V. Both models yielded similar results for I_{OUT}, V_X and V_Y. The SBCS started up for supply voltages above 650 mV. The average values of V_X and V_Y for a V_{DD} higher than 650 mV were approximately 86 mV and 81 mV, respectively, which were very close to the calculated value of 88 mV. The design of the SBCS can be improved and optimized; however, the main goal herein was to compare the results of the 4PM with those of BSIM.

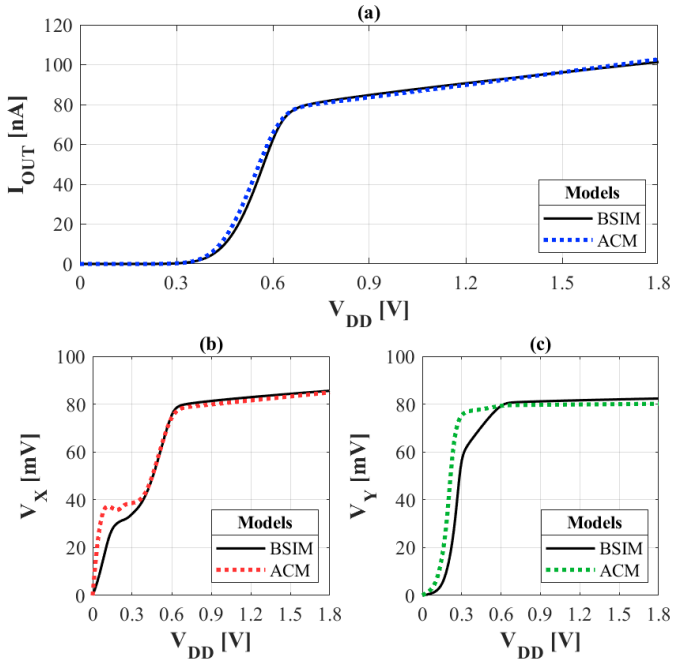

Figure 17. Results of DC analysis for voltage sweep on V_{DD}: (**a**) output current, (**b**) V_X and (**c**) V_Y.

5.4. Common-Source Amplifier

The common-source amplifier in Figure 18 was designed to demonstrate the suitability of the 4PM in the frequency domain in comparison to BSIM. The amplifier was designed for a maximum gain at a frequency of 2 MHz, a bias current of 200 nA and a supply voltage of 1.8 V.

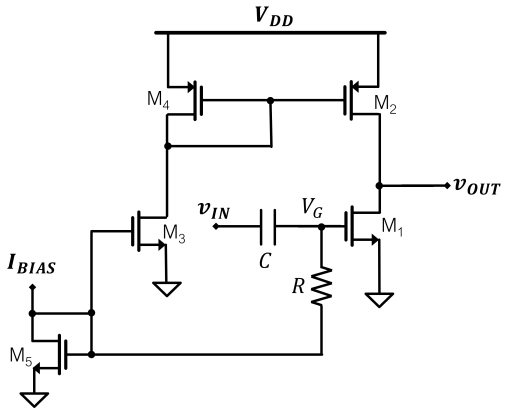

Figure 18. Common-source amplifier.

Table 8 presents the transistors' dimensions and extracted parameters employed in the design. The resistor R of 500 kΩ isolates the node V_G from the bias circuit, while the capacitor C of 150 fF blocks the DC level from the input signal at V_G.

Table 8. Transistor dimensions for the common-source amplifier and extracted parameters.

Transistor	$M_{1,3,5}$	$M_{2,4}$
W [μm]	2.0	0.5
L [μm]	0.18	2.0
I_S [nA]	2000	10
V_{T0} [mV]	518	−428
n	1.36	1.31
σ [mV/V]	21.8	6.5

An AC simulation from 1 kHz to 10 GHz was run for a capacitive load of 10 fF. The results using BSIM and 4PM are depicted in Figure 19, where it is evident that the 4PM managed to follow the BSIM curves in the AC simulation.

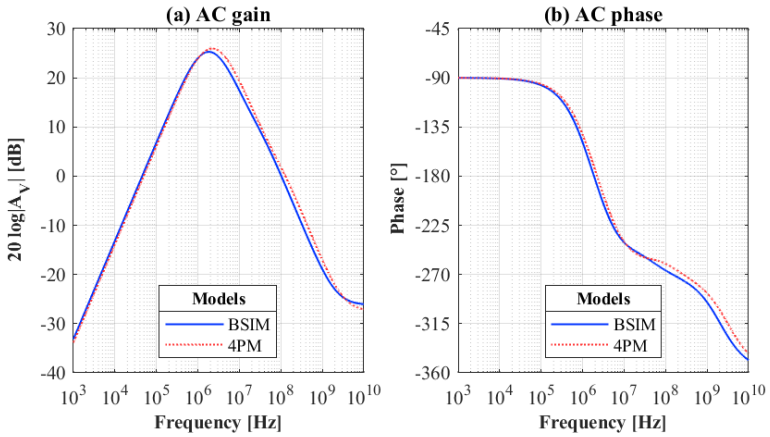

Figure 19. Frequency response of the common-source amplifier using BSIM and 4PM: (**a**) open-loop gain in dB and (**b**) phase.

The center frequency for the 4PM was around 2.14 MHz with a peak gain of 26 dB, while BSIM presented a maximum gain of 25.3 dB at 1.9 MHz. The phase curves presented in Figure 19 show that the 4PM managed to follow BSIM very closely. Two poles were found at 700 kHz and 4.7 MHz for BSIM and at 850 kHz and 5.5 MHz for the 4PM. These differences were expected since the 4PM in Verilog-A does not consider the complete dynamic transistor model.

6. Conclusions

The simulation results of MOS circuits depend on the accuracy of both the MOS model and the extracted transistors' parameters.

The authors of [28] employed an ACM expression of charge density to calculate currents but did not extract the required parameters that should be available in the simulator. Nonetheless, despite using VHDL (the hardware description language VHSIC) to facilitate the widespread use of the model in other simulators, the charge density equations are not familiar to most designers; thus, a gap between hand-design and simulation remains.

This paper introduced a truly compact MOS model composed of only four parameters—enough to describe the DC and small-signal low-frequency characteristics of MOSFET. The 4PM in Verilog-A was used to calculate the current from the UICM, which contains parameters familiar to IC designers. This is significant because a first-order understanding of the MOSFET model along with its associated parameters is indispensable for IC designers since the MOSFET parameters of simulators are numerous and most of them are quite hard to understand.

Besides presenting the 4PM, this paper also introduced the extraction methods employed to obtain accurate parameters, reflected in the consistent results obtained through the simulations of different circuits presented in Section 5.

The four-parameter model is a minimalist model that helps electronic engineers to design MOS circuits and to rapidly find approximate solutions to the circuits' electrical behavior in a way that the troubleshooting can easily be done by directly relating the design parameters to the obtained results before fine tuning through more complex and time-consuming simulations.

The 4PM is particularly useful for the design by hand of low-voltage circuits because fewer parameters are required for accurate results while still maintaining a foundation in physics. Therefore, all things considered, the 4PM helps to bridge the gap between the hand design and simulation of MOS circuits.

Author Contributions: Conceptualization, C.G.-M. and M.C.S.; methodology, C.G.-M., M.C.S., C.M.A. and D.G.A.N.; software, C.M.A. and D.G.A.N.; validation, C.M.A. and D.G.A.N.; writing—original draft preparation, C.M.A. and D.G.A.N.; writing—review and editing, C.G.-M. and M.C.S.; visualization, C.M.A. and D.G.A.N.; supervision, C.G.-M.; funding acquisition, C.G.-M. and M.C.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the Brazilian agencies CAPES (finance codes 001 and print #698503P) and CNPq.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data are contained within the article.

Acknowledgments: The authors would like to thank the Brazilian agencies CAPES and CNPq for supporting this work.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretations of data; in the writing of the manuscript, or in the decision to publish the results.

Abbreviations

The following abbreviations are used in this manuscript:

4PM	Four-parameter model
ACM	Advanced compact MOSFET model
BSIM	Berkeley short-channel IGFET model
CMOS	Complementary metal-oxide semiconductor
CSIG	Common-source intrinsic gain
DC	Direct current
DIBL	Drain-induced barrier lowering
EDA	Electronic design automation
HDLs	Hardware description languages
MI	Moderate inversion
MOSFET	Metal-oxide semiconductor field-effect transistor
PTAT	Proportional to absolute temperature
SBCS	Self-biased current source
SCM	Self-cascode MOSFET
SI	Strong inversion
UCCM	Unified charge-control model
UICM	Unified current-control model
ULV	Ultra-low voltage
VHDL	VHSIC hardware description language
VTC	Voltage transfer characteristic
WI	Weak inversion

Appendix A. Verilog-A Implementation

In Verilog-A, the current flowing from Terminal A to Terminal B is defined using the syntax I(A,B), and the voltage between these two terminals is defined as V(A,B). Therefore, it is very straightforward to set equations and associate voltages and currents.

The sample below contains a definition of the pinch-off voltage in (4), followed by an implementation of Algorithm 443 regarding the source (subscript S) terminal. In the full description, the calculations are performed for both source and drain (subscript D) terminals, which are analogous.

```
analog begin
PhiT = $vt($temperature); // thermal voltage
VP = (V(G,B) - VTH + sigma*V(D,S) + sigma*V(S,B))/n;
// Equation (4), pinch-off voltage

// Condition to calculate WnS
X = exp(((VP - V(S,B))/PhiT)+1);

        if(X < 0.7385) begin
                numeratorS = X + (4/3)*X*X;
                denominatorS = 1 + (7/3)*X+(5/6)*X*X;
                WnS = numeratorS/denominatorS;
        end

        else begin
                numeratorS = log(X)*log(X)+2*log(X)-3;
                denominatorS = 7*log(X)*log(X) + 58*log(X) +127;
                WnS = log(X) - 24*(numeratorS/denominatorS);
        end

// Calculating ZnS
ZnS = log(X) - WnS - log(WnS);

// Calculating EnS
TermC = ZnS/(1 + WnS);

numeratorES = (2*(1+WnS)*(1+WnS+(2/3)*ZnS)-ZnS);
denominatorES = 2*(1+WnS)*(1+WnS+(2/3)*ZnS)-2*ZnS;
```

```
29
30  EnS = TermC*(numeratorES/denominatorES);
31
32  // Finding the qis and ifS
33  qiS = WnS*(1+EnS); // normalized inversion charge at source
34  ifS = (qiS + 1)*(qiS + 1) - 1; // Equation (6), forward inversion level
```

Note that the methodology used to calculate the inversion charges (lines 6–33) is from [22], and we used several variables throughout the description to facilitate the implementation. Afterward, the drain current is calculated from the results of the source, and drain calculations as shown in the sample below. The syntax and guidelines are detailed in [14].

```
1  //Calculating ID
2  I(D,S) <+ IS*(ifS-irD); // Equation (1),drain-current
```

References

1. Sah, C.-T. A history of MOS transistor compact modeling. In Proceedings of the NSTI Nanotech, Anaheim, CA, USA, 8–12May 2005; pp. 347–390.
2. Liu, W. *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*; Wiley: Hoboken, NJ, USA, 2001.
3. Singh, Y.; Venugopalan, S.; Karim, M.A.; Khandelwal, S.; Paydavosi, N.; Thakur, P.; Niknejad, A.M.; Hu, C.C. NiknBSIM Industry standard compact MOSFET models. In Proceedings of the European Solid-State Device Research Conference (ESSDERC), Bordeaux, France, 17–21 September 2012; pp. 46–49.
4. Brews, J.R. MOSFET hand analysis using BSIM. *IEEE Circuits Devices Mag.* **2006**, *21*, 28–36. [CrossRef]
5. Jespers, P.G.A.; Murmann, B. *Systematic Design of Analog CMOS Circuits*; Cambridge University Press: Cambridge, UK, 2017.
6. Aunet, S. Ultra low voltage sub-100 mV Vdd CMOS. In Proceedings of the19th IEEE International New Circuits and Systems Conference (NEWCAS), Toulon, France, 13–16 June 2021.
7. Bryant, A.; Brown, J.; Cottrell, P.; Ketchen, M.; Ellis-Monaghan, J.; Nowak, E. Low-power CMOS at Vdd = 4kT/q. In Proceedings of the Device Research Conference. Conference Digest (Cat. No. 01TH8561), Notre Dame, IN, USA, 25–27 June 2001; pp. 22–23.
8. Lotze, N.; Manoli, Y. A 62 mV 0.13 µm CMOS standard-cellbased design technique using Schmitt-trigger logic. *IEEE J. Solid-State Circuits* **2011**, *47*, 47–60. [CrossRef]
9. Choi, J.; Aklimi, E.; Shi, C.; Tsai, D.; Krishnaswamy, H.; Shepard, K.L. Matching the power, voltage, and size of biological systems: A nWscale, 0.023-mm^3 pulsed 33-GHz radio transmitter operating from a 5 kT/q-supply voltage. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2015**, *62*, 1950–1958. [CrossRef]
10. Ballo, A.; Pennisi, S.; Scotti, G.; Venezia, C. A 0.5 V Sub-Threshold CMOS Current-Controlled Ring Oscillator for IoT and Implantable Devices. *J. Low Power Electron. Appl.* **2022**, *12*, 16. [CrossRef]
11. Palumbo, G.; Scotti, G. A Novel Standard-Cell-Based Implementation of the Digital OTA Suitable for Automatic Place and Route. *J. Low Power Electron. Appl.* **2021**, *11*, 42. [CrossRef]
12. Centurelli, F.; Della Sala, R.; Monsurrò, P.; Scotti, G.; Trifiletti, A. A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers. *J. Low Power Electron. Appl.* **2022**, *12*, 12. [CrossRef]
13. Galup-Montoro, C.; Schneider, M.C. *MOSFET Modeling for Circuit Analysis and Design*; World Scientific: Singapore, 2007.
14. Technologies, A. Verilog-A Reference Manual. 2004. Available online: https://edadownload.software.keysight.com/eedl/ads/2011_01/pdf/verilogaref.pdf (accessed on 1 August 2021).
15. Tsividis, Y.; McAndrew, C. *Operation and Modeling of the MOS Transistor*; Oxford University Press: Oxford, UK, 2011.
16. Siebel, O.F.; Schneider, M.C.; Galup-Montoro, C. MOSFET threshold voltage definition, extraction and some applications. *Microelectron. J.* **2012**, *43*, 329–336. [CrossRef]
17. Hiblot, G. DIBL–compensated extraction of the channel length modulation coefficient in MOSFETs. *IEEE Trans. Electron Devices* **2018**, *65*, 4015–4018. [CrossRef]
18. Vittoz, E.A. MOS Transistor: Model and modes of operation. In *MEAD Course on "Advanced Analog CMOS IC Design"*; EPF-Lausanne: Lausanne, Switzerland, 2019.
19. Fikry, W.; Ghibaudo, G.; Dutoit, M. Temperature dependence of drain-induced barrier lowering in deep submicrometre MOSFETs. *Electron. Lett.* **1994**, *30*, 911–912. [CrossRef]
20. Chen, Z.; Wong, H.; Han, Y.; Dong, S.; Yang, B.L. Temperature dependences of threshold voltage and drain-induced barrier lowering in 60 nm gate length MOS transistors. *Microelectron. Reliab.* **2014**, *54*, 1109–1114. [CrossRef]
21. Siebel, O.F. *Um Modelo Eficiente do Transistor MOS Para o Projeto de Circuitos VLSI*; Universidade Federal de Santa Catarina: Florianopolis, Brazil, 2007.
22. Fritsch, F.N.; Shafer, R.E.; Crowley, W.P. Algorithm 443: Solution of the transcendental equation wew=x. *Commun. AMC* **1973**, *16*, 123–124.
23. Department of Electrical Engineering and Computer Science, UC Berkeley. *BSIM4v4.5.0 Technical Manual*; Department of Electrical Engineering and Computer Science, UC Berkeley: Berkeley, CA, USA, 2004.

24. Ferreira, J.V.T. *Analysis, Design and Test of Ultra-Low-Voltage CMOS Ring Oscillators*; Universidade Federal de Santa Catarina: Florianopolis, Brazil, 2019.
25. Antúnez-Calistro, G.; Siniscalchi, M.; Silveira, F.; Rossi-Aicardi, C. Variability-Aware Design Method for a Constant Inversion Level Bias Current Generator. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 2027–2036. [CrossRef]
26. Heim, P.; Schultz, S.R.; Jabri, M.A. Technology-independent biasing technique for CMOS analogue micropower implementations of neural networks. In Proceedings of the 6th Australian Conference on Neural Networks, Sydney, Australia, 6–8 February 1995; pp. 9–12.
27. Olmos, A.; Boas, A.V.; Soldera, J. A Sub-1V Low Power Temperature Compensated Current Reference. In Proceedings of the 2007 IEEE International Symposium on Circuits and Systems (ISCAS), New Orleans, LA, USA, 27–30 May 2007; pp. 2164–2167.
28. Fonseca, A.K.T.B.; de Souza, F.R. Behavioral modeling of the Advanced Compact MOSFET (ACM) model with VHDL-AMS. In Proceedings of the 2008 Joint 6th International IEEE Northeast Workshop on Circuits and Systems and TAISA Conference, Montreal, QC, Canada, 22–25 June 2008; pp. 169–172.