Analysis of the Rectifier Circuit Valid Down to Its Low-Voltage Limit

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***Abstract*—This paper describes a simple analytical model of the rectifier circuit valid down to very low voltage operation (input voltage below the thermal voltage). Steady-state and transient analyses of the rectifier with the diode described by an exponential I-V characteristic are presented. We provide formulas for the dc output voltage level, the output voltage ripple, and the power conversion efficiency. We also give a compact expression for the charging time of the load capacitor. The models of the rectifier and the voltage doubler for input voltages down to the thermal voltage are verified with simulations and measurements using circuits built with off-the-shelf 1N4148 diodes.**

***Index Terms*—AC-DC converters, energy harvesting, low voltage rectifiers.**

I. Introduction

VOLTAGE multipliers are extensively used in both dc/dc [1], [2] and ac/dc converters [3]–[12]. The former are used for generating voltages higher than the supply voltage, while the latter are often used in low-input-voltage applications such as wireless sensor networks or RFID tag chips. The amplitude of the RF input voltage is usually within hundreds or even tens of mV [3], [10]–[12].

The purpose of this paper is to provide an analysis of rectifiers employed for energy harvesting. The analysis is correct down to input voltages smaller than the thermal voltage. We show expressions that can be employed to optimize the efficiency of multistage rectifiers, which directly affects the energy-harvesting tag range [5].

Section II presents the steady-state analysis of the rectifiers. In Section III we derive an explicit equation for the power conversion efficiency. In Section IV, we present the transient analysis. Section V reports the simulation and experimental results.

II. Steady-State Analysis of Rectifier Circuits

In general, voltage multipliers are a cascade of elementary stages such as that shown in Fig. 1 [1], [7]. Consequently, the performance of a multistage rectifier can be inferred from an analysis of the one-stage voltage multiplier (doubler) in Fig. 1, which will be the main focus of this paper. For the analysis we will make the following assumptions: i) the input is a symmetric square wave; ii) the diode is described by the Shockley equation; iii) the load current is constant.

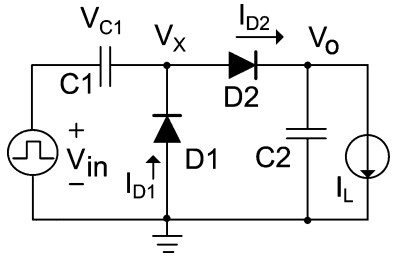

Fig. 1. Schematic of the voltage doubler analyzed herein.

The Shockley equation, used throughout this paper, can be applied to either pn-junction or Schottky diodes or diode-connected MOSFETs operating in weak inversion. The assumption of a square-wave input makes the calculations of the dc output voltage and of the settling time during startup extremely simple. Additionally, the main results obtained for a square-wave input are similar to those for a sine-wave input, as can be noted through a comparison of the results in this paper with those in [12].

A. Half-Wave Rectifier

Let us assume that the input signal is a symmetric square wave, with a 50% duty cycle, as shown in Fig. 2. We also assume that the diode in Fig. 2 can be characterized through the Shockley (exponential) model

$$I_D = I_S\left[e^{\frac{V_D}{n\phi_t}} - 1\right] \tag{1}$$

where $V_D = V_{in} - V_o$, n is the ideality factor, ϕ_t is the thermal voltage, and I_S is the diode saturation current. The average value of the diode current over a complete cycle of the input signal equals the load current, i.e.,

$$\frac{1}{T}\int_{-T/2}^{T/2} I_D dt = I_L \tag{2}$$

$$\int_{-T/2}^{0} \exp\left(\frac{-V_P - V_o}{n\phi_t}\right)dt + \int_{0}^{T/2} \exp\left(\frac{V_P - V_o}{n\phi_t}\right)dt = \left(1 + \frac{I_L}{I_S}\right)T. \tag{3}$$

Manuscript received January 28, 2011; revised April 18, 2011 and June 21, 2011; accepted June 22, 2011. Date of publication August 15, 2011; date of current version January 11, 2012. This work was supported in part by CNPq of the Brazilian Ministry of Science and Technology. This paper was recommended by Associate Editor G. Palumbo.

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Digital Object Identifier 10.1109/TCSI.2011.2161366

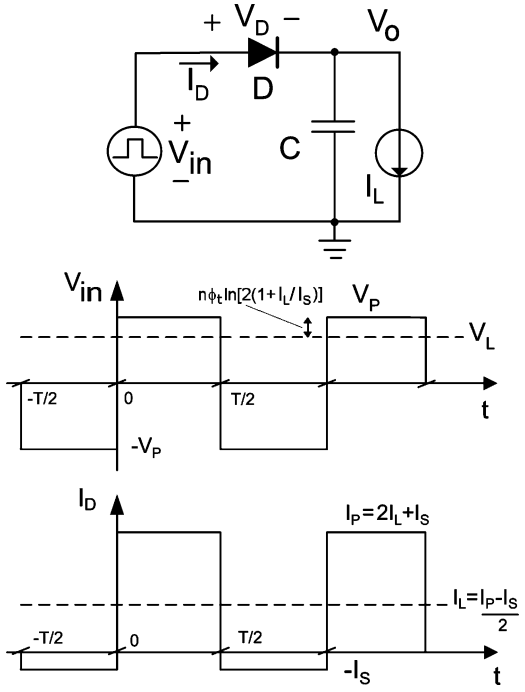

Fig. 2. Half-wave rectifier and voltage and current waveforms.

Assuming that the value of the load capacitance is large enough to preclude any significant variation in V_o, the solution of (3) is given by

$$\frac{V_o}{n\phi_t} = \frac{V_L}{n\phi_t} = \ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_S}\right] \tag{4}$$

where V_L represents the dc value of V_o. For low values of both the input voltage, $V_P/n\phi_t < 1$, and load current, $I_L/I_S \ll 1$, (4) reduces to

$$\frac{V_L}{n\phi_t} \cong \frac{1}{2}\left(\frac{V_P}{n\phi_t}\right)^2. \tag{5}$$

Thus, for low input voltage values the rectifier operates as a power detector [13] and with high values for the input signal, i.e., $V_P/n\phi_t > 1$, the dc output voltage is

$$V_L \cong V_P - n\phi_t \ln\left[2(1+I_L/I_S)\right]. \tag{6}$$

Thus, the load voltage equals V_P minus the forward voltage drop across D, through which a current equal to I_P flows. Note that for the peak detector ($I_L = 0$) there is a diode voltage drop of $n\phi_t \ln 2$ due to the forward current through the diode, which in this case equals the reverse diode current I_S.

B. Voltage Multipliers

As in the case of the half-wave rectifier, we assume that the capacitances of the voltage doubler in Fig. 1 are sufficiently high to avoid significant changes in the stored charges. Since the average currents through the capacitors are equal to zero, the dc currents that flow through D1 and D2 are both equal to I_L. The loop composed of D1, C1, and the signal generator is a half-wave rectifier where the average current through D1 equals I_L. Therefore, the voltage V_{C1} stored in C1 is a dc voltage given by (4), i.e.,

$$\frac{V_{C1}}{n\phi_t} = \ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_S}\right]. \tag{7}$$

The nodal voltage V_X is equal to the sum of the square-wave input and V_{C1}. Therefore, the dc output voltage of the doubler is equal to the value calculated for the half-wave rectifier plus V_{C1}. Thus, for identical diodes, the dc output voltage of the doubler is

$$\frac{V_L}{n\phi_t} = 2\ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_S}\right]. \tag{8}$$

We can extend this result to an N-diode (N/2-stage) rectifier. Assuming, for simplicity, that all the diodes in the rectifier are identical, it follows that

$$\frac{V_L}{n\phi_t} = N\ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_S}\right], \tag{9}$$

which, for $V_P/n\phi_t > 1$, simplifies to

$$V_L \cong N\left\{V_P - n\phi_t \ln\left[2(1+I_L/I_S)\right]\right\}. \tag{10}$$

C. Performance Degradation Due to Parasitic Capacitance

So far we have assumed that the capacitance associated with node V_X is negligible. However, in a true implementation, the sum of all unwanted stray capacitances contributes to reducing the effective voltage across diode D1 [1], which leads to a decrease in the dc load voltage. For the sake of simplicity, let us assume that the parasitic capacitance C_P at node V_X is linear. To calculate its effect on the dc load voltage, we invoke the charge conservation principle, which yields

$$\frac{V_L}{n\phi_t} = 2\ln\left[\frac{\cosh(\alpha_P V_P/n\phi_t)}{1+I_L/I_S}\right]; \quad \alpha_P = \frac{C_1}{C_1+C_P}. \tag{11}$$

Therefore, the effect of the parasitic capacitance on the load voltage is equivalent to a reduction in the input voltage, proportional to the attenuation factor α_P [1], [7].

III. Power Conversion Efficiency

The PCE of the voltage doubler is the output power divided by the input power. The latter is the sum of the output power and the power loss due to diodes D1 and D2 in Fig. 1. The power loss due to D1 and D2 is

$$P_{\text{loss}} = \frac{1}{T}\int_{-T/2}^{T/2}\left[-V_X I_{D1} + (V_X - V_L)I_{D2}\right]dt. \tag{12}$$

Since the dc voltages across C1 and C2 are equal to $V_L/2$ and V_L, respectively, with V_L given by (8), we can readily find that

$$P_{\text{loss}} = -V_L I_L + 2(I_L + I_S)V_P \tanh(V_P/n\phi_t). \tag{13}$$

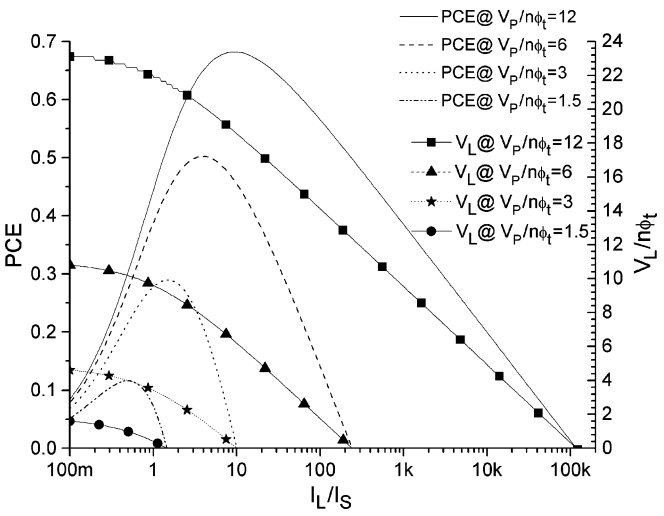

Fig. 3. Power conversion efficiency and load voltage of the voltage doubler versus normalized load current for values of $V_P/n\phi_t$ equal to 1.5, 3, 6, and 12.

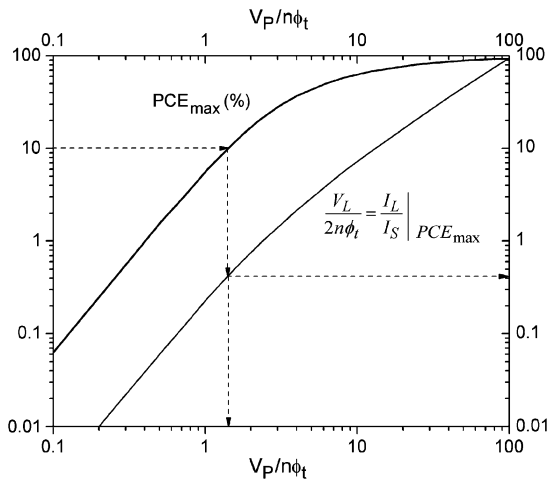

Fig. 4. Numerical calculation of the maximum power conversion efficiency (PCE) and dc load voltage of the voltage doubler versus the magnitude of the input voltage.

The PCE is thus written as

$$\text{PCE}=\frac{P_{\text{out}}}{P_{in}}=\frac{n\phi_t/V_P}{\left(1+\frac{I_S}{I_L}\right)\tanh(V_P/n\phi_t)}\ln\left[\frac{\cosh(V_P/n\phi_t)}{1+I_L/I_S}\right], \tag{14}$$

which, for $V_P/n\phi_t > 1$, can be rewritten as

$$\text{PCE}=\frac{P_{\text{out}}}{P_{\text{out}}+P_{\text{loss}}}\cong\frac{1-\frac{n\phi_t}{V_P}\ln\left[2(1+I_L/I_S)\right]}{(1+I_S/I_L)}. \tag{15}$$

Fig. 3 shows the dependence of both PCE and V_L on the load current for some values of the magnitude of the input signal. Note that the dc output voltage and the load current are both normalized to diode parameters $n\phi_t$ and I_S, respectively. The results shown in Fig. 3 can be used to determine the size of the diodes for a given technology.

For a fixed input voltage, the PCE reaches its maximum for a given value of the ratio of the load current to the saturation current, e.g., $I_L/I_S \cong 4$ for $V_P/n\phi_t = 6$. This maximum is essential for the design of an efficient voltage multiplier. From (14) we find that the value of I_L/I_S at which the PCE is at its maximum is given by

$$\left.\frac{I_L}{I_S}\right|_{\text{PCE}_{\max}}=\ln\left[\frac{\cosh(V_P/n\phi_t)}{1+\left.\frac{I_L}{I_S}\right|_{PCE_{\max}}}\right] \tag{16}$$

or, equivalently

$$\left.\frac{I_L}{I_S}\right|_{\text{PCE}_{\max}}=\frac{V_L}{2n\phi_t}. \tag{17}$$

The result in (17) simply shows that the voltage doubler achieves its maximum efficiency for a dc load current equal to the diode saturation current times a factor which is the dc load voltage normalized to $2n\phi_t$. This result can be extrapolated to an N-stage multiplier through the modification of the normalization factor to $Nn\phi_t$.

Now, inserting the values of I_L/I_S given by (16) and the relationship between V_L and V_P given by (9), we can plot the maximum PCE in terms of V_P, as shown in the graph of Fig. 4. The voltage doubler can operate with an efficiency of 10% for input voltages as low as $1.5n\phi_t$. However, the available load current in this case is around 40% of the saturation current. To operate efficiently with a load current of the order of several times the saturation current, the input voltage must be of the order of several tens of millivolts. One way to improve the rectifier efficiency is to choose a diode with $n \cong 1$. Also, whenever possible, the diode saturation current should be designed to operate the voltage doubler (multiplier) close to the maximum PCE point given by (17) (for an N-stage multiplier simply substitute N for 2 in (17)). This choice may, however, depending on the case, cause an increase in the parasitic capacitance of the diode which counteracts the beneficial effect [7].

IV. Transient Response and Ripple

A. Half-Wave Rectifier During Startup

For the transient analysis, let us assume that the capacitor is initially discharged and that the load current is zero during startup. In each cycle, the charge ΔQ transferred from the source to the capacitor is

$$\begin{aligned}\Delta Q&=\int_{t-T/2}^{t+T/2} I_D dt\\&=I_S\left[\int_{t-T/2}^{t} e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}dt+\int_{t}^{t+T/2} e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}dt-T\right].\end{aligned} \tag{18}$$

Assuming that the variation in the output voltage over one cycle is $\ll n\phi_t$, (18) can be simplified as

$$\frac{\Delta Q}{I_S T}=\frac{e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}+e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}}{2}-1 \tag{19}$$

Therefore, after one cycle, the variation in the capacitor voltage becomes

$$V_o(t+T)=V_o(t)+\frac{\Delta Q}{C} =V_o(t)+\frac{I_S T}{C}\left[\frac{e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}+e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}}{2}-1\right]. \quad (20)$$

The differential equation that describes the transient behavior is then

$$\frac{\Delta V_o}{T}=\frac{V_o(t+T)-V_o(t)}{T}\cong\frac{dV_o}{dt} =\frac{I_S}{C}\left[\frac{e^{\left(\frac{-V_P-V_o}{n\phi_t}\right)}+e^{\left(\frac{V_P-V_o}{n\phi_t}\right)}}{2}-1\right]. \quad (21)$$

The solution of (21), a linear differential equation for $\exp(-V_o/n\phi_t)$, is

$$e^{(V_o/n\phi_t)}-1=[\cosh(V_P/n\phi_t)-1]\,[1-e^{-t/\tau_0}] \quad (22)$$

where $\tau_0=C/g_{d0}$. $g_{d0}=I_S/n\phi_t$ is the diode conductance for $I_D=0$.

The time T_S required to charge the capacitor up to a voltage equal to V_{fin}, according to (22), is

$$e^{T_S/\tau_0}=\frac{\cosh(V_P/n\phi_t)-1}{\cosh(V_P/n\phi_t)-e^{(V_{fin}/n\phi_t)}}. \quad (23)$$

Let us now assume that the final voltage $V_{fin}=V_L$, with V_L given by (4). This corresponds to charging the capacitor from 0 up to V_L and making use of a wake-up circuit, which connects the load immediately after the output voltage has reached V_L (see Fig. 7 for details). In this case, the settling time T_S is

$$\frac{T_S}{\tau_0}=\ln\frac{(1+I_S/I_L)\,[\cosh(V_P/n\phi_t)-1]}{\cosh(V_P/n\phi_t)} =\ln\left[1+\frac{I_S}{I_L}\right]\left(1-\frac{I_S}{I_S+I_L}e^{-V_L/n\phi_t}\right) \quad (24)$$

which, for $I_L/I_S\gg 1$ and $V_L>n\phi_t$, becomes

$$T_S\cong\tau_0\frac{I_S}{I_L}=C\frac{n\phi_t}{I_L}. \quad (25)$$

The settling time given by (25) is equal to the product of the load capacitance and the dynamic resistance of a diode through which a dc current equal to the load current flows.

B. Output Voltage Ripple of the Half-Wave Rectifier

According to Fig. 2, during the negative half-cycle of the input the capacitor discharges at a rate equal to the load current plus the reverse current I_S. Thus, the voltage ripple is

$$\Delta V\cong\frac{T}{2C}(I_L+I_S) \quad (26)$$

The analysis of the ripple for any V_P is given in Appendix 1.

C. Settling Time and Output Voltage Ripple of the Voltage Doubler

The output voltage ripple is essentially the same as in the half-wave rectifier, i.e., it is given by (26).

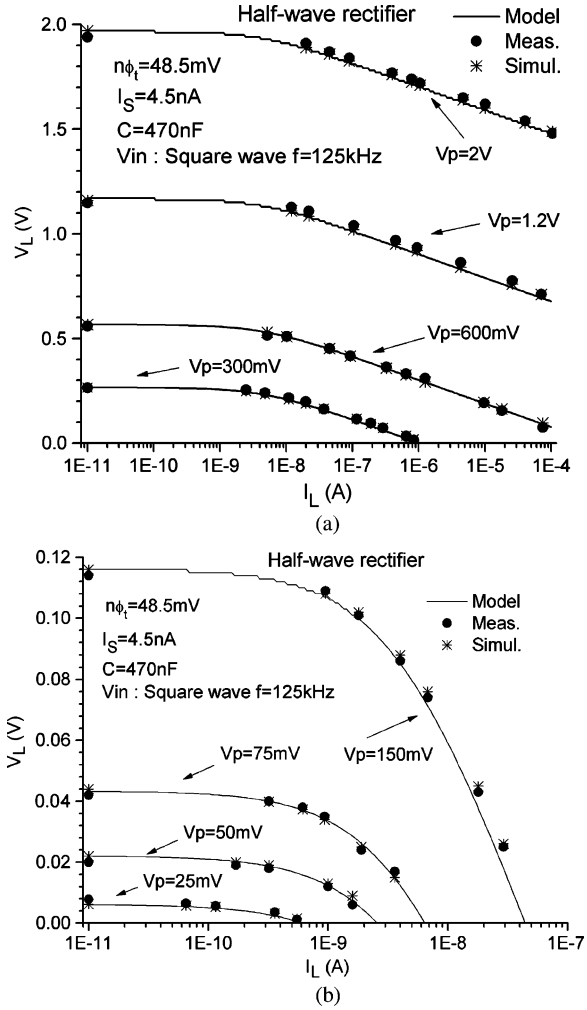

Fig. 5. DC output voltage of the half-wave rectifier versus load current for: (a) $V_P=0.3$, 0.6, 1.2, and 2 V; (b) $V_P=25$, 50, 75, and 150 mV.

The model for the settling time is more complicated than for the half-wave rectifier because a pair of coupled differential equations needs to be solved. For the case of $V_P=300$ mV, the simulation showed that the settling time is around twice the value given by (25), which was derived for the half-wave rectifier.

V. Simulation and Experiment

In order to check the validity of the model, we simulated and measured the performance of both the half-wave rectifier and the voltage doubler.

For the measurements we employed off-the-shelf 1N4148 diodes and 470 nF capacitors. The experimentally extracted parameters for the diodes are $I_S=4.5$ nA and $n\phi_t=48.5$ mV.

Fig. 5 shows the dependence of the dc output voltage of the half-wave rectifier on the load current, for several values of the magnitude of the input signal. The solid lines represent (4), which, as expected, fits very well both the simulated and experimental results. The ripple voltage ΔV is, except for very high load current values, a small fraction of $n\phi_t$ since we used a large capacitance. For $V_P/n\phi_t>1$ the output voltage is

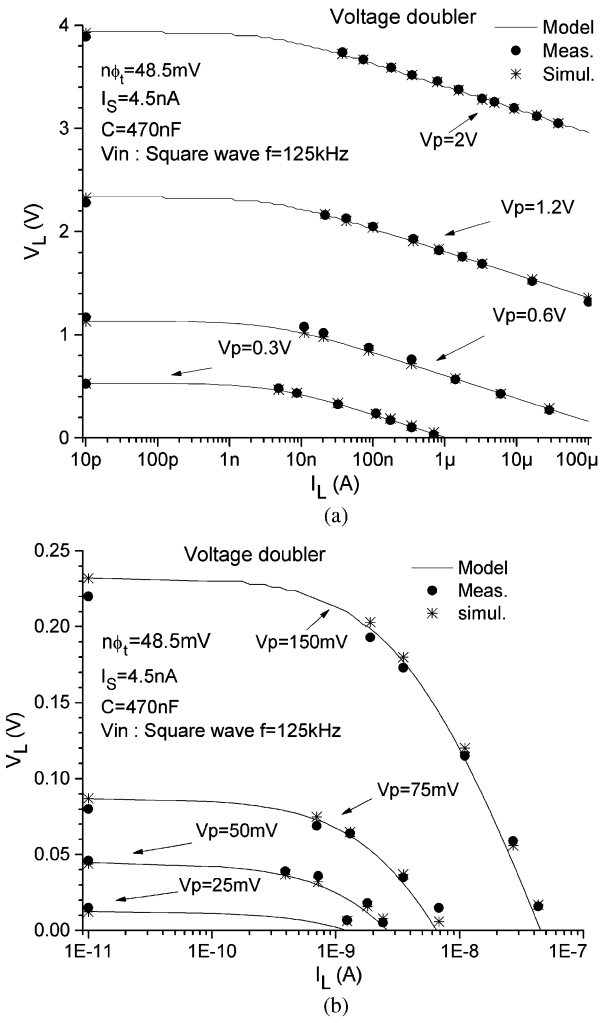

Fig. 6. DC output voltage of the voltage doubler versus load current for (a) $V_P = 0.3$, 0.6, 1.2, and 2 V; (b) $V_P = 25$, 50, 75, and 150 mV.

equal to the peak value of the input voltage reduced by the term $n\phi_t \ln[2(1+I_L/I_S)]$, as predicted by (6). On the other hand, for $V_P/n\phi_t < 1$ the dc output voltage is proportional to the input voltage squared [13], reduced by the term $n\phi_t \ln(1 + I_L/I_S)$. When $I_L/I_S \ll 1$, we have $V_L \cong V_P^2/(2n\phi_t)$, which, for $V_P = 25$ mV, gives $V_L = 6.4$ mV, a value very close to the experimental result in Fig. 5(b).

Fig. 6 shows the dependence of the dc output voltage of the voltage doubler on the load current, for values of V_P ranging from 25 mV to 2 V. The experimental and simulated results clearly indicate an excellent fitting of the model.

In order to verify the correctness of the transient model during startup, we measured the output voltage for different values of the input voltage. Fig. 7 shows the analytical [(22)], simulated, and experimental transient waveforms for $V_P/n\phi_t = 6$ and $I_L = 0$. The measured settling time T_S for $I_L/I_S = 8.2$ is of the order of 52 ms, which is very close to the value of 57 ms calculated from (25).

Table I gives a comparison of the settling time obtained from the simulation and from the analytical result in (24), for three values of the input voltage.

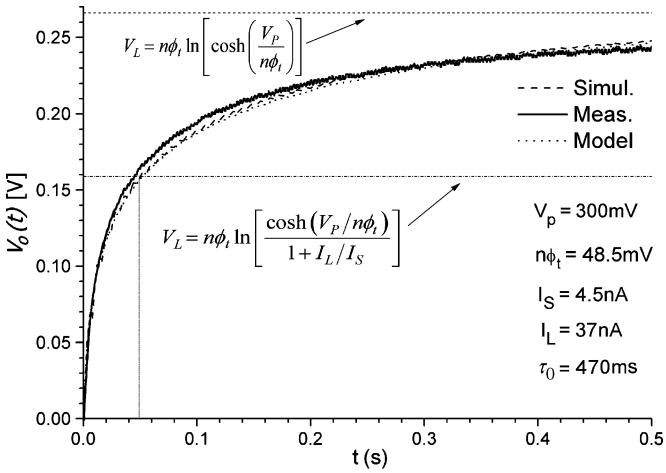

Fig. 7. Transient response of the half-wave rectifier for $V_P/n\phi_t = 6$, at no load, nominal C = 47 nF. The broken line $V_o = 0.16$ V corresponds to $I_L/I_S \cong 8.2$. The measured settling time in this case is approximately 52 ms while the theoretical settling time is $T_S \cong \tau_0/8.2 \cong 57$ ms.

TABLE I
SETTLING TIME OF THE HALF-WAVE RECTIFIER. PARAMETERS ARE $I_S = 4.5$ nA, $n\phi_t = 48.5$ mV, AND $C = 47$ nF. T_S IS IN MS

V_P (mV)	I_L (nA)	T_S (simulation)	T_S (eqn (24))	T_S (experiment)
100	10	43	42	-
150	10	146	140	120
200	20	91	86	-
300	37	62	56	52

VI. CONCLUSIONS

We have presented an analytical model of the rectifier circuit in which the nonlinear device follows the diode Shockley (exponential) equation. The model is correct for input voltages down to below the thermal voltage. Expressions for the dc output voltage, voltage ripple, transient during startup, and power conversion efficiency were derived. Theoretical results are supported by simulations and measurements. The expressions presented herein represent a valuable tool for the optimization of voltage multipliers operating down to their low-voltage physical limit.

APPENDIX I
DERIVATION OF THE VOLTAGE RIPPLE

Let us now assume for the half-wave rectifier that V_o is not constant. The diode current is then written as

$$I_D = I_L + C\frac{dV_o}{dt} = I_S\left[e^{\left(\frac{V_{in}-V_o}{n\phi_t}\right)} - 1\right]. \qquad \text{(A1.1)}$$

Equation (A1.1) can be rewritten as

$$\left(1+\frac{I_L}{I_S}\right)e^{\frac{V_o}{n\phi_t}} + \frac{C}{I_S}n\phi_t\frac{d\left(e^{\frac{V_o}{n\phi_t}}\right)}{dt} = e^{\frac{V_{in}}{n\phi_t}}. \qquad \text{(A1.2)}$$

The solution of (A1.2) can be obtained by integration in the intervals $[-T/2, t]$ and $[t, T/2]$, where $V_{in} = -V_P$ and $V_{in} = V_P$, respectively. Under steady-state conditions we have $V_o(-T/2) = V_o(T/2)$; applying this boundary condition

and the continuity condition at $t = 0$, we can find the (two) integration constants, thus obtaining

$$\left(1+\frac{I_L}{I_S}\right)e^{\frac{V_o}{n\phi_t}} = e^{-\frac{V_P}{n\phi_t}} + \frac{\left(e^{\frac{V_P}{n\phi_t}} - e^{-\frac{V_P}{n\phi_t}}\right)e^{-\frac{t}{\tau}}}{1+e^{\frac{T}{2\tau}}} \quad \text{(A1.3)}$$

for $-T/2 < t < 0$ and

$$\left(1+\frac{I_L}{I_S}\right)e^{\frac{V_o}{n\phi_t}} = e^{\frac{V_P}{n\phi_t}} - \frac{\left(e^{\frac{V_P}{n\phi_t}} - e^{-\frac{V_P}{n\phi_t}}\right)e^{-\frac{t}{\tau}}}{1+e^{-\frac{T}{2\tau}}} \quad \text{(A1.4)}$$

for $0 < t < T/2$. In (A1.3) and (A1.4), $\tau = C/g_d$ with $g_d = (I_S + I_L)/n\phi_t$.

The ripple ΔV in the output voltage can be calculated from (A1.3), resulting in

$$\Delta V = V_o(-T/2) - V_o(0) = n\phi_t \ln\left[\frac{\cosh(V_P/n\phi_t + T/4\tau)}{\cosh(V_P/n\phi_t - T/4\tau)}\right]. \quad \text{(A1.5)}$$

For $T/4\tau \ll 1$, (A1.5) can be simplified to

$$\Delta V \cong n\phi_t \frac{T}{2\tau}\tanh(V_P/n\phi_t). \quad \text{(A1.6)}$$

Finally, for $V_P/n\phi_t > 1$, we have

$$\Delta V \cong \frac{T}{2C}(I_L + I_S), \quad \text{(A1.7)}$$

which is the result expected for the ripple of a capacitor discharged at a constant current equal to $I_L + I_S$ during a time interval equal to $T/2$.

Appendix II
Equivalence Between Sine and Square Inputs for the Rectifier

So far, we have analyzed the ac/dc converter assuming that the input signal is a square wave. In many cases, the input signal closely resembles a sine-wave input. In order to make use of the analysis provided in this paper, we introduced a definition of equivalence between sine and square waves for the rectifier. We assume here that a sine wave with peak value equal to V_A is equivalent to a square wave of magnitude V_P if, under the same load condition, they produce the same dc output voltage. For a sine-wave input, the load current is

$$\frac{1}{T}\int_0^T i_D dt = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S e^{(V_A\cos\theta - V_L)/n\phi_t} d\theta - I_S = I_L. \quad \text{(A2.1)}$$

Expression (A2.1) can be rewritten as

$$\frac{V_L}{n\phi_t} = \ln\left[\frac{I_0(V_A/n\phi_t)}{1+I_L/I_S}\right] \quad \text{with} \quad I_0(z) = \frac{1}{2\pi}\int_{-\pi}^{\pi} e^{z\cos\theta} d\theta. \quad \text{(A2.2)}$$

$I_0(z)$ is the modified Bessel function of the first kind [14].

As in Section II-A, we have assumed in the derivation of (A2.2) that the output voltage V_o is approximately constant. Now we compare (A2.2) with (4) and apply the definition of equivalence between sine and square waves, which leads to

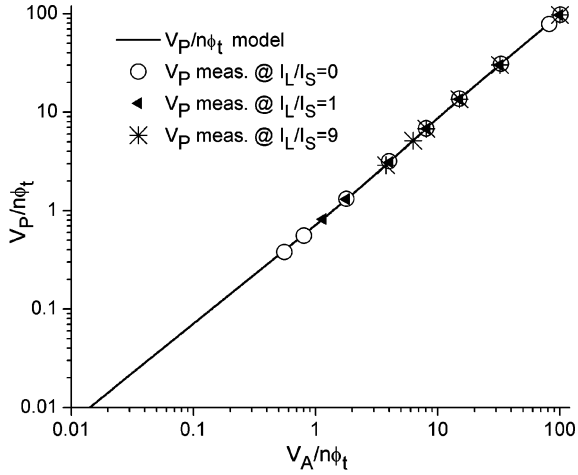

Fig. 8. Equivalence between sine and square waves. V_A is the peak value of the sine wave and V_P is the magnitude of the square wave.

$$I_0(V_A/n\phi_t) = \cosh(V_P/n\phi_t). \quad \text{(A2.3)}$$

Thus, a sine wave is equivalent to a square wave if the relationship between their magnitudes is given by (A2.3), which is illustrated in Fig. 8. It is interesting to note that, for $V_A/n\phi_t \ll 1$, we have

$$V_A/n\phi_t \cong \sqrt{2}V_P/n\phi_t \quad \text{(A2.4)}$$

whereas for $V_A/n\phi_t \gg 1$,

$$\frac{V_A}{n\phi_t} - \frac{\ln(V_A/n\phi_t)}{2} \cong \frac{V_P}{n\phi_t} + \ln(\sqrt{\pi/2}). \quad \text{(A2.5)}$$

The last approximation is a consequence of the asymptotic approximations $I_0(z) \cong e^z/\sqrt{2\pi z}$ for large z and $\ln[\cosh(x)] \cong x - \ln 2$ for large x.

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