Ultra-Low-Voltage Operation of CMOS Analog Circuits: Amplifiers, Oscillators, and Rectifiers

C. Galup-Montoro, *Member, IEEE*, M. C. Schneider, *Member, IEEE*, and M. B. Machado, *Student Member, IEEE*

***Abstract*—This letter presents MOS analog circuits that can operate with very low supply voltages. Operation of the MOS transistor in the triode region is emphasized owing to the limited voltages available. Special attention has been given to the properties of the zero-VT transistor due to its high drive capability at low voltages. Simulation and measurement results for a Colpitts oscillator prototype set up around a zero-VT MOSFET demonstrated that the oscillator operates with supply voltages lower than the thermal voltage kT/q. Finally, ultra-low-voltage rectifiers using diodes or diode-connected MOSFETs operating in weak inversion are analyzed.**

***Index Terms*—Colpitts oscillator, energy harvesting, MOSFET analog circuits, rectifier circuit, ultra-low-voltage circuits, zero-VT transistor.**

I. Introduction

As STATED by Prof. J. Rabaey, ultra-low-power circuit design is synonymous with ultra-low-voltage (ULV) circuit design [1]. The need for portable and greener computing is at the origin of ULV digital circuits operating with supply voltages in the range of 100–400 mV (see, for example, [2] and references therein). There is still room for further supply voltage reductions since the fundamental supply voltage limit for the proper operation of a CMOS inverter is 2 (ln2) $(kT/q) = 36$ mV for MOS devices with a subthreshold slope of 60 mV/decade [3]. For analog circuits, the minimum practical supply voltage has generally been considered to be higher than the minimum necessary for the operation of digital circuits [4], but rectifiers and voltage multipliers have appeared recently as an exception to this rule. In effect, recent studies [5], [6] motivated by energy harvesting show that rectifiers and voltage multipliers can operate efficiently even with input voltages below the thermal voltage kT/q.

The specificity of ULV circuits, powered by supply voltages of, for instance, below 100 mV, is related to the fact that there is not enough voltage headroom to operate MOS transistors in saturation. For this reason, we will review MOSFET modeling in the triode region in Section II. In Section III, we summarize the operation of the ideal common-source and common-gate amplifiers operating in the triode region and in weak inversion (WI), which is the most appropriate inversion level for efficient ULV operation.

The choice of appropriate technology is of paramount importance for ULV circuits. Enhancement-mode devices, such as MOS transistors with threshold voltage in the range of 0.3–0.5 V, operate with very low current density for supply voltages below 100 mV and thus are of very limited practical utility. On the other hand, depletion-mode devices, such as MOSFETs or JFETs, can supply relatively high-current densities for low supply voltages, but they present two drawbacks: they are neither available in conventional technologies nor provide enough voltage gain for low voltages. In between enhanced and depletion devices, MOS transistors with zero or near-zero threshold voltage are particularly suitable for ULV circuits due to their current drive capability and sufficient voltage gain at very low supply voltages. Section IV summarizes the characteristics of zero-VT MOSFETs.

In Section V, we show that analog circuits, such as oscillators built around zero-VT MOSFETs, can operate with supply voltages below kT/q, a result previously reported in [7].

For ULV design, it is mandatory to use the correct physical parameter of the devices. For a diode, for example, the saturation current I_S is the appropriate physical parameter and not the threshold voltage, which is meaningless for ULV circuit design. In Section VI, we summarize ULV operation of rectifiers implemented with diodes or diode-connected MOSFETs operating in WI.

II. MOSFET Modeling for ULV Operation

WI (or close to WI) is very attractive for ULV circuits since the transistor voltage gain is maximum for the available bias voltage. In WI, conservation of the purely diffusive drain current along the channel [8], [9] leads to

$$I_D = \mu n C'_{ox} \phi_t^2 e^1 \frac{W}{L} e^{\frac{V_G - V_T}{n\phi_t}} \left(e^{-\frac{V_S}{\phi_t}} - e^{-\frac{V_D}{\phi_t}} \right) \qquad (1)$$

where V_G, V_S, and V_D are the gate, source, and drain voltages referred to the bulk, respectively; μ is the mobility; C'_{ox} is the oxide capacitance per unit area; n is the slope factor; W/L is the aspect ratio; and $\phi_t = kT/q$ is the thermal voltage where k is the Boltzmann constant, q is the elementary charge, and T is the absolute temperature.

ULV analog design needs the careful calculation of the source (g_{ms}), drain (g_{md}), and gate (g_m) transconductances,

Manuscript received July 5, 2012; revised September 14, 2012; accepted October 23, 2012. Date of publication December 24, 2012; date of current version February 1, 2013. This brief was recommended by Associate Editor M. Alioto.

C. Galup-Montoro and M. C. Schneider are with the Departamento de Engenharia Eletrica, Universidade Federal de Santa Catarina, 88040-900 Florianopolis-SC, Brazil (e-mail: marcio@eel.ufsc.br).

M. B. Machado is with the Departamento de Engenharia Eletrica, Universidade Federal de Santa Catarina, 88040-900 Florianopolis-SC, Brazil. He is also with the Instituto Federal Sul-Rio-Grandense, RS, Brazil.

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2012.2231042

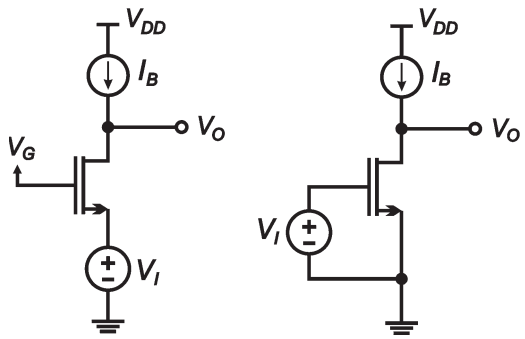

Fig. 1. Ideal common-gate and common-source amplifiers. I_B is an ideal current source.

which can be readily calculated from (1) as

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = \mu n C'_{ox}\phi_t e^1 \frac{W}{L} e^{\frac{V_G - V_T}{n\phi_t}} e^{\frac{-V_S}{\phi_t}} \tag{2}$$

$$g_{md} = \frac{\partial I_D}{\partial V_D} = \mu n C'_{ox}\phi_t e^1 \frac{W}{L} e^{\frac{V_G - V_T}{n\phi_t}} e^{\frac{-V_D}{\phi_t}}. \tag{3}$$

Neglecting the variation of n with V_G, the combination of (1)–(3) yields

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{n}. \tag{4}$$

Equation (4) represents the two essential features of the MOSFET operating in the triode region: 1) The channel is represented by two anti-parallel current sources controlled by the source and drain voltages and 2) A gate voltage variation appears in the channel attenuated by n, which models the capacitive divider constituted by the oxide and depletion capacitances.

III. Ideal Common-Gate and Common-Source Amplifiers

Using the model of the previous section for the MOSFET operating in WI in the triode region, the voltage gains of the common-gate and common-source topologies shown in Fig. 1 are, respectively

$$A_{v,cg} = \frac{v_o}{v_i} = \frac{g_{ms}}{g_{md}} = e^{\frac{qV_{DS}}{kT}} \tag{5}$$

$$A_{v,cs} = \left|\frac{v_o}{v_i}\right| = \frac{g_m}{g_{md}} = \frac{1}{n}\left(e^{\frac{qV_{DS}}{kT}} - 1\right). \tag{6}$$

For the common-source amplifier, the voltage gain equals unity for $V_{DS} = (kT/q)\cdot\ln(1+n)$. Regenerative logic circuits require a voltage gain of at least unity for their proper operation. Therefore, in the case of the "symmetric" CMOS inverter, the minimum supply voltage $V_{DD} = 2\cdot(kT/q)\cdot\ln(1+n)$ deduced in [3] can be directly derived from (6). For ideal MOSFETs (i.e., with zero depletion capacitance, $n = 1$) $V_{DD\,\min} = 36$ mV at room temperature.

On the other hand, the common-gate amplifier provides a voltage gain of greater than unity for $V_{DS} > 0$. As will be seen later in this paper, this property of the common-gate amplifier is very useful for lowering the supply voltage limit for the operation of oscillators.

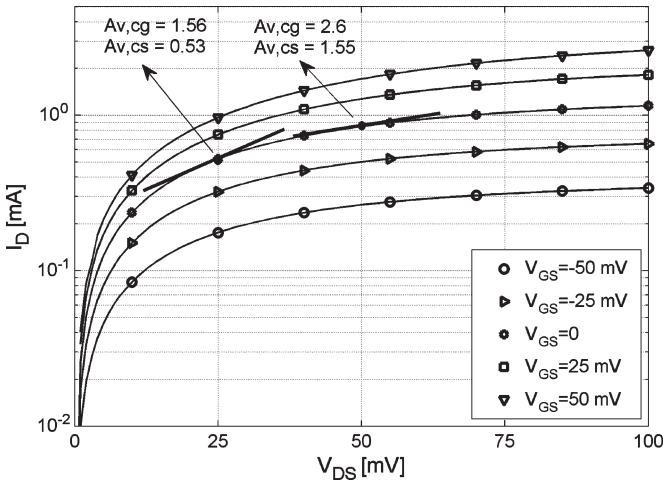

Fig. 2. $I_D \times V_{DS}(V_S = V_B)$ characteristics for a zero-VT transistor with $W/L = 2500\ \mu$m$/420$ nm. The values of the common-gate and common-source gains are 1.56 and 0.53, respectively, for $V_{GS} = 0$ V and $V_{DS} = 25$ mV.

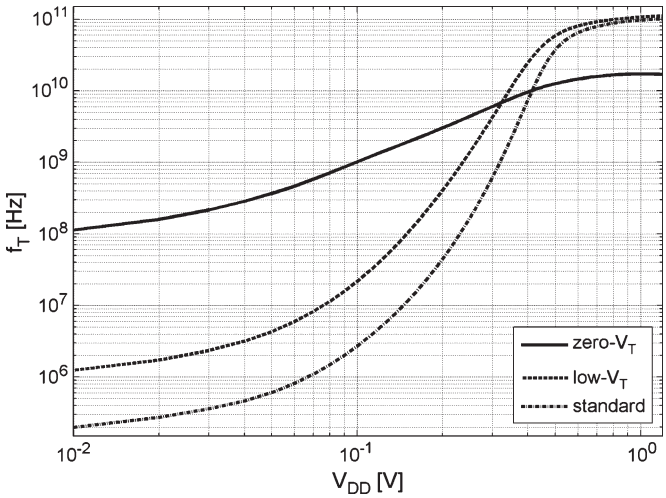

Fig. 3. First-order approximation of the intrinsic cutoff frequency of the zero-VT ($W/L = 3\ \mu$m$/0.42\ mu$m), low-VT ($W/L = 0.84\ \mu$m$/0.12\ \mu$m), and standard transistors ($W/L = 0.84\ \mu$m$/0.12\ \mu$m) of a 0.13 μm CMOS technology. The transconductance g_m was simulated for $V_S = V_B = 0$ and $V_D = V_G = V_{DD}$.

IV. Zero-VT MOSFETs

MOS transistors with zero or near-zero threshold voltage are particularly suitable for ULV circuits due to their current drive capability and sufficient voltage gain at very low supply voltages, as shown in Fig. 2.

In order to compare the usefulness of MOS transistors in relation to the available supply voltage, we can use the ratio of the drain current to the transistor gate area as a figure of merit or, equivalently, the transconductance-to-gate capacitance ratio g_m/C_{ox}, which is proportional to the unit gain or cutoff frequency f_T of the device. Fig. 3 shows the value of f_T for zero-VT, low-VT, and standard transistors in terms of the supply voltage for minimum-channel-length devices of a 0.13 μm CMOS technology. Nominal threshold voltages are 5, 245, and 340 mV, respectively. Current densities I_D/W for the three types of transistors with $V_{GS} = V_{DS} = 50$ mV are around 300 nA$/\mu$m, 980 pA$/\mu$m, and 140 pA$/\mu$m, respectively.

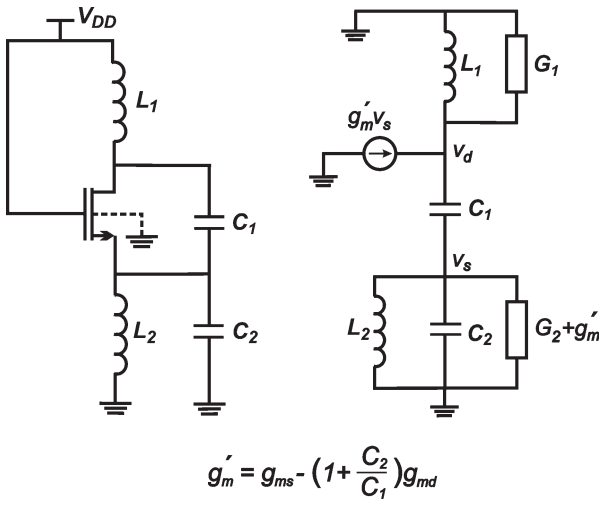

Fig. 4. Schematic of the ES Colpitts oscillator and its simplified small-signal model.

The graphs for the first-order approximation of the intrinsic cutoff frequency in Fig. 3 clearly show the advantage of the zero-VT transistor over the low-VT and standard transistors for low supply voltages in applications where high-current drive capability and/or high-frequency operation is a must. Note that for supply voltages below 50 mV, the zero-VT transistor is faster than the low-VT transistor by two orders of magnitude and almost three orders of magnitude faster than the standard transistor. On the other hand, for supply voltages of some hundreds of mV, the speed of the zero-VT transistor becomes lower than those of the other two transistors since its channel length is around three times the length of the channel of the other two transistors.

Two important applications that employ zero-VT transistors, a ULV oscillator and a ULV rectifier, are shown next.

V. ULV Colpitts Oscillator

In the conventional Colpitts oscillator [10], the supply voltage is divided between the active device and a DC current source (or resistor) connected to the active device. In order to apply all of the available bias voltage to the transistor, we adopted the topology of Fig. 4, in which L_2 substitutes the DC current source of the conventional Colpitts oscillator. This topology is called the enhanced-swing (ES) Colpitts oscillator because inductors L_1 and L_2 in series with the transistor channel allow the source/drain terminals to swing beyond the supply rails [11]. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

A. Circuit Analysis

The detailed analysis of the ES Colpitts is cumbersome [12] owing to the second tank composed of L_2 and C_2. In order to obtain some insight for circuit design, we adopted the simplified approach of considering the capacitive feedback divider (C_1 and C_2) as a transformer-like network with a turns ratio of $1 : C_1/(C_1 + C_2)$[10]. The resulting simplified second-order resonator circuit is shown in Fig. 5.

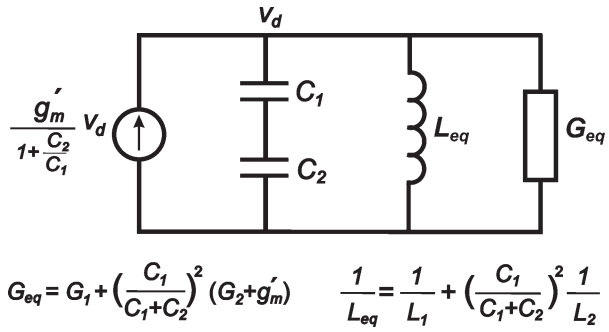

Fig. 5. Second-order small-signal model of the ES Colpitts oscillator.

As is clear from the equivalent circuit of Fig. 5, the oscillator start-up condition is achieved when the real part of the tank conductance is negative, which gives

$$g_{ms} > \left(1+\frac{C_2}{C_1}\right) g_{md} + \frac{C_1}{C_2} G_2 + \left(2+\frac{C_1}{C_2}+\frac{C_2}{C_1}\right) G_1. \quad (7)$$

The above expression is a generalization of the result presented in [7], since it explicitly includes the effect of the losses of L_2 on the start-up condition. For the classical Colpitts oscillator, in which the transistor operates in saturation, G_2 and g_{md} can be neglected. Thus, the transconductance necessary for oscillation is given by the last term in (7), which has a minimum value of $4G_1$ when $C_1 = C_2$. The optimum value of the capacitor ratio that minimizes (7) extends the result of [7] as shown below

$$\frac{C_2}{C_1} = \sqrt{\frac{G_1 + G_2}{g_{md} + G_1}}. \quad (8)$$

In the hypothetical case of ideal inductors and capacitors ($G_1 = G_2 = 0$), it follows from (7) that the open-loop gain (g_{ms}/g_{md} times $C_1/(C_1 + C_2)$) must be greater than unity. In this hypothetical case, for which the losses are only due to the transistor, the limit for the minimum supply voltage for oscillation startup, which is obtained by combining (5) and (7), is

$$V_{DD\,\mathrm{lim}} = \frac{kT}{q} \ln\left(1 + \frac{C_2}{C_1}\right). \quad (9)$$

For $C_1 = C_2$, V_{DDlim} equals the voltage drop of a transistor at the Meindl limit [3], but for $C_2 < C_1$, the value of V_{DDlim} given by (9) is below it. Condition (9) would be observed for high-quality-factor passive devices, as is clear from (7).

For the oscillator in Fig. 4, assuming that the drain voltage is a sinusoidal signal of peak amplitude A_d and that the drain current $i_D \geq 0$ at all times, we should have $v_{DS} \geq 0$, which implies that

$$V_{DD} - A_d(1 - \alpha) \geq 0 \quad (10)$$

where $\alpha = C_1/(C_1 + C_2)$. Therefore, in the limit case, the maximum value of the amplitude of oscillation is

$$A_{d,\max} = \frac{V_{DD}}{1 - \alpha}. \quad (11)$$

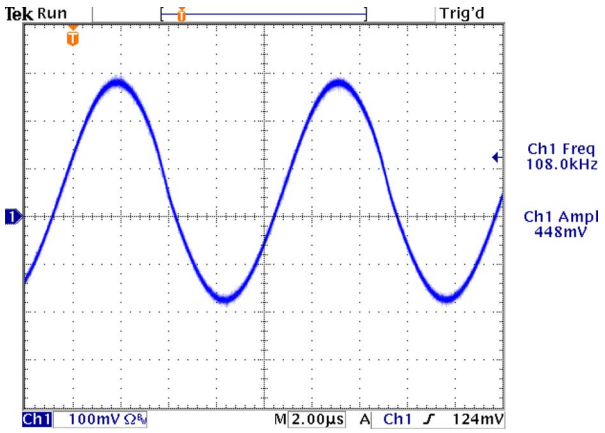

Fig. 6. Experimental drain voltage of the ES Colpitts oscillator of Fig. 4 for $V_{DD} = 15$ mV and $C_2/C_1 = 0.12$ ($C_1 = 3.6$ nF, $C_2 = 0.44$ nF) with a temperature of around 23 °C.

B. Experimental Results

We designed a zero-VT transistor with a large aspect ratio (2500 μm/420 nm) in a 130-nm technology. The zero-VT transistor along with a large aspect ratio were chosen for obtaining a high transconductance (10 mA/V) at very low voltages ($V_{DS} = 10$ mV and $V_{GS} = 0$ V), which is appropriate for many designs. In relation to the transistors, this 130-nm technology can be regarded as ideal for ULV applications, since a technology with a shorter channel length could introduce more drawbacks than benefits for ULV operation. On the other hand, passive devices, particularly inductors, have low quality factors. Due to the losses of on-chip inductors, the minimum supply voltage to sustain oscillations (at 800 MHz) in an integrated Colpitts oscillator is around 50 mV. In this paper, in order to explore the ULV design space, we combined the integrated transistor with off-chip passive devices. The nominal inductances of the inductors are 10 mH with quality factors of around 90. Several combinations of values of C_1 and C_2 were chosen to explore the low-voltage limit of operation of the oscillator, while keeping the oscillation frequency at around 110 kHz.

Fig. 6 shows the drain voltage oscillation obtained experimentally for $C_2/C_1 = 0.12$ and a supply voltage of 15 mV. The peak-to-peak drain voltage is around 400 mV. The simulation results indicated a minimum supply voltage of 8 mV.

VI. Rectifier at ULV

Rectifiers are the basic building blocks of voltage multipliers, essential components for energy-harvesting circuits. The voltage level available from ambient energy sources (excluding light) is generally below 100 mV. The purpose of this section is to analyze the rectifier for input voltages that can be as low as the thermal voltage.

To simplify the mathematics, let us assume that the input signal for the rectifier of Fig. 7 is a symmetric square wave, with a 50% duty cycle. We will also assume that the diode can be characterized through the Shockley (exponential) model, as

$$I_D = I_S \left[e^{\frac{qV_D}{nkT}} - 1 \right]. \tag{12}$$

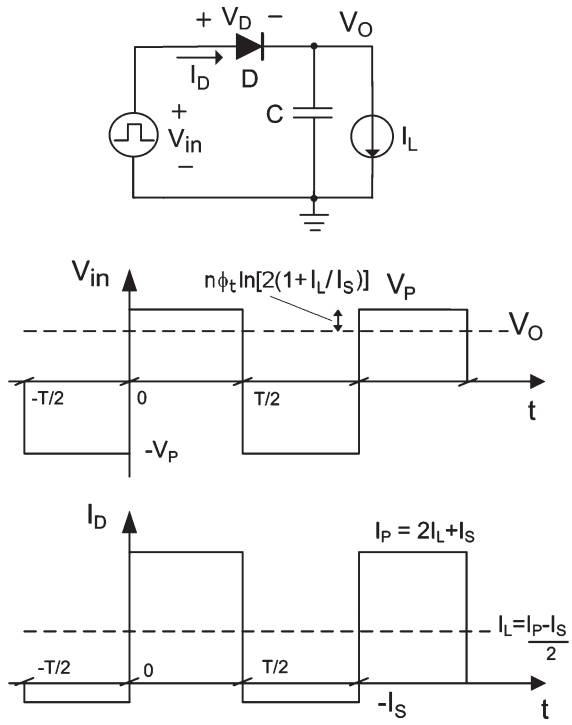

Fig. 7. Half-wave rectifier and voltage and current waveforms.

We will focus on the useful case in which the load capacitance is large enough to assure a nearly constant output voltage. In this case, the steady-state operation of the circuit, for a peak input voltage greater than the thermal voltage, is illustrated in Fig. 7. As is clear from the figure, the diode forward current must be $2I_L + I_S$ in order to make the average diode current equal to the load current I_L. Thus, the voltage drop in the diode, according to (12), is

$$V_{on} = n\frac{kT}{q} \ln\left(1 + \frac{I_P}{I_S}\right) = n\frac{kT}{q} \ln\left(1 + \frac{2I_L + I_S}{I_S}\right). \tag{13}$$

Consequently, the output voltage of the rectifier is

$$V_0 \cong V_P - n\frac{kT}{q} \ln\left[2(1 + I_L/I_S)\right]. \tag{14}$$

In some electronic circuits, I_S can be as low as 1 fA and I_L as large as 1 mA. Assuming that $n = 1$, we obtain, in this case

$$V_{on} = 26 \cdot \ln(2 \cdot 10^{12}) \cong 796 \text{ mV}$$

which is a typical voltage drop for a silicon diode. On the other hand, in a low-power/low-voltage application we can have, e.g., $I_S = I_L = 1$ μA. For $n = 1$ we obtain

$$V_{on} = 26 \cdot \ln(4) = 36 \text{ mV}.$$

Thus, the voltage drop in a forward-biased diode can be of the order of the thermal voltage, which is appropriate for low-voltage and low-power circuits. For such low voltages, (14) is not accurate but nevertheless gives the correct order of magnitude (for details, see [6]).

A particularly interesting case of application of the rectifier is the peak detector for which $I_L = 0$. In this case, the output voltage is simply

$$V_0 \cong V_P - n\frac{kT}{q} \ln 2. \tag{15}$$

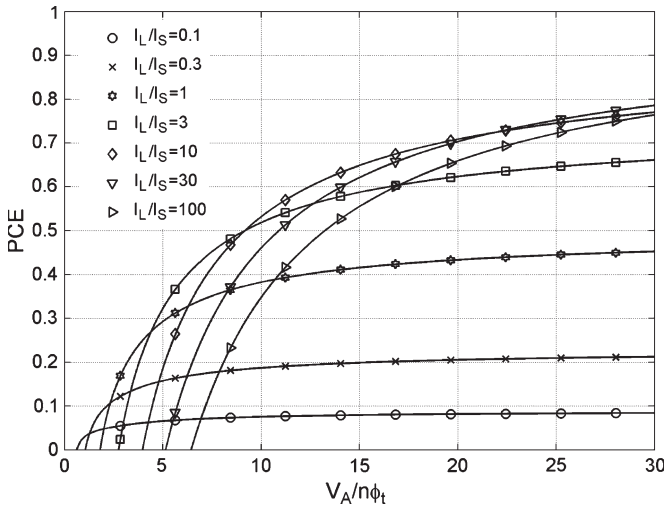

Fig. 8. Power conversion efficiency of a half-wave rectifier.

As we have seen in Sections III and V, the voltage drop $(kT/q) \cdot \ln 2$ appears in the models of other circuits, such as amplifiers and oscillators operating at ULV.

We note here that the results of the rectifier circuit for a sine wave input are similar to those obtained for a square wave input (for details, see [6]).

The output voltage of the circuit in Fig. 7 for a sine wave input with peak value equal to V_A[6] is given by

$$\frac{V_o}{n\phi_t} = \ln\left[\frac{I_0(v_a)}{i_l + 1}\right] \tag{16}$$

where $v_a = V_A/n\phi_t$, $i_l = I_L/I_S$, and I_0 is the modified Bessel function of the first kind of order zero. The power conversion efficiency (PCE) of the half-wave rectifier in Fig. 7, which can be derived from the considerations given in [6], is

$$PCE = \frac{P_{out}}{P_{in}} = \frac{1}{v_a}\frac{i_l}{i_l + 1}\frac{I_0(v_a)}{I_1(v_a)}\ln\left[\frac{I_0(v_a)}{i_l + 1}\right]. \tag{17}$$

I_1 is the modified Bessel function of the first kind of order one. The PCE given by (17) is graphically shown in Fig. 8 in terms of the normalized input voltage, considering the load current as a parameter. For small input voltages, say below $3n\phi_t$, the saturation current of the diode must be considerably higher than the load current for an acceptable output, but the PCE is very low. For energy harvesting, a PCE of 50% (or even less) can be acceptable since the energy is available for free.

In integrated circuits, the diodes are usually implemented using MOS transistors. The different possible diode-connected MOSFET topologies were discussed in detail in [13]. For ultra-low-voltage rectifiers, zero-VT-MOSFETs [5] as well as standard threshold transistors in deep wells in the DTMOS connection have been used [14].

VII. Conclusion

We have briefly discussed amplifiers, oscillators, and rectifiers operating at ULV using an exponential law for the nonlinear device (diode and MOSFET). We found that the minimum supply voltage for the proper operation of these circuits can be below the Meindl limit for logic inverters. We proposed the use of zero-VT MOSFET for the operation of ULV analog circuits. Moreover, we discussed the use of high-quality-factor passives and the ES Colpitts topology for a ULV oscillator. Experimental results showed that the resulting oscillator can operate with supply voltages below $kT/q \cdot (\ln 2)$.

Acknowledgment

The authors would like to thank Prof. F. Rangel de Sousa for his help with the Colpitts oscillator experiment, MOSIS for the fabrication of the devices, and the Brazilian Federal Government agencies CNPq and CAPES for the partial funding of this study.

References

[1] J. Rabaey, *Low Power Design Essentials*. New York: Springer-Verlag, 2009.

[2] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[3] J. D. Meindl and A. J. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1515–1516, Oct. 2000.

[4] E. A. Vittoz, "Weak inversion in analog and digital circuits," in *Proc. CCCD Workshop*, Lund, Sweden, Oct. 2003, pp. 1–33.

[5] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micropower CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.

[6] A. J. Cardoso, L. G. de Carli, C. Galup-Montoro, and M. C. Schneider, "Analysis of the rectifier circuit valid down to its low-voltage limit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 106–112, Jan. 2012.

[7] F. Rangel de Sousa, M. B. Machado, and C. Galup-Montoro, "A 20 mV Colpitts oscillator powered by a thermoelectric generator," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seoul, Korea, May 2012, pp. 2035–2038.

[8] C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *J. Anal. Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, Jul. 1995.

[9] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge, U.K.: Cambridge Univ. Press, 2010.

[10] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, MA: Addison-Wesley, 1971.

[11] A. C. Heiberg, T. W. Brown, T. S. Fiez, and K. Mayaram, "A 250 mV, 352 μW GPS receiver RF front-end in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 938–949, Apr. 2011.

[12] T. W. Brown, F. Farhabakhshian, A. G. Roy, T. S. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential Colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1782–1795, Aug. 2011.

[13] S. Voldman, F. Assaderaghi, J. Mandelman, L. Hsu, and G. Shahidi, "Dynamic threshold body-and gate-coupled SOI ESD protection networks," in *Proc. EOS/ESD*, 1997, pp. 210–220.

[14] Y.-K. Teh, F. Mohd-Yasin, F. Choong, M. I. Reaz, and A. V. Kordesch, "Design and analysis of UHF micropower CMOS DTMOST rectifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 2, pp. 122–126, Feb. 2009.