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CMOS multiplier based on the relationship between drain current and inversion charge

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Abstract: The authors propose a four-quadrant multiplier based on a core cell that exploits the general relationship between the saturation current of an MOS transistor and the source inversion charge density, valid from weak to strong inversion. The advantages of the proposed circuit are simplicity, low distortion and feasibility of low-voltage operation. Experimental results in a 0.35 μm CMOS prototype indicate 1 mA consumption for 1 MHz bandwidth, and distortion level below 1% for an input current of 80% of the full-scale range. The multiplier core area is around 10 000 μm^2.

1 Introduction

Analogue multipliers are important sub-circuits with application in filtering, neural networks, electronic instrumentation and modulators, among others. A good review on MOS multipliers is presented in [1], although limited to voltage-mode architectures with MOS transistors operating only in strong inversion (quadratic $I–V$ characteristic). Several other more recent papers such as [2–9] have also proposed CMOS circuits for the implementation of analogue multiplication.

Current-mode multipliers [5–9] have been more attentively addressed in the last 10 years, because of their promising features regarding power consumption, supply voltage, bandwidth, dynamic range and circuit complexity. The current-mode approach uses either the quadratic behaviour of $I–V$ characteristics in strong inversion [3–6] or their exponential behaviour in weak inversion [7, 8].

In this paper as well as in our recent work described in [10, 11], we follow the new approach to analogue multipliers of [9], which is not based on a specific current–voltage law. As in [9], we use the general relationship between the saturation current and the inversion charge density at the source. This law is valid from weak to strong inversion, being slightly affected by mobility degradation because of transversal electric field. Consequently, the approach used here does not have the limitations of the use of the quadratic or exponential laws, which are valid in strong and weak inversion, respectively, but not in between.

2 Squarer circuit architecture

2.1 Fundamentals

The core cell of the proposed multiplier is a current-mode squarer circuit.

Applying the sum of two input signals to a squarer circuit, the output signal comprises a component that is proportional to their product, among other undesirable components that should be eliminated by a cancellation scheme (Section 3).

In this work, the operating principle of the current-mode squarer circuit is based on the quadratic dependence of the forward saturation current I_F of an MOS transistor on the inversion charge density at the source regardless of the inversion level (weak, moderate or strong) [12–15]. The

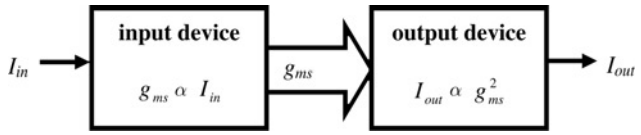

Figure 1 *Principle of proposed squarer circuit*

inversion charge density is not directly available for circuit design but we can use the source transconductance g_{ms}, which is proportional to it according to the Pao–Sah model [16].

The squarer circuit consists basically of two devices, as illustrated in Fig. 1: an input device operating in the triode region at constant drain-to-source voltage, which converts the input current to a gate voltage and an output device operating in saturation, which converts the gate voltage back to a current. Provided that the input device operates linearly, it converts the input current (linearly) to the source transconductance. On the other hand, the output current is a quadratic function of the source transconductance.

To derive the fundamental relationship associated with the squarer circuit, let us impose the input device to operate in the very beginning of the triode region, that is, at a low drain-to-source voltage. In this case, we may assume the following relationship between the drain current (I_D) and the drain-to-source voltage (V_{DS})

$$g_{ms} \cong \frac{I_D}{V_{DS}} \tag{1}$$

for $V_{DS} \ll V_{DSSAT}$, where V_{DSSAT} is the saturation voltage, dependent upon the inversion level in moderate and strong inversion and about 100 mV in weak inversion.

The input device is an MOS transistor operating in the linear region with very small and current-independent V_{DS}, so that its source transconductance is proportional to the input current. The same gate, source and bulk voltages are applied to both the input and output devices, which implies the same source transconductances for both devices since they have the same aspect ratios. Such an arrangement, here named forward-current mirror, is detailed in Section 2.2.

2.2 Forward-current mirror

The principle described in the previous section is implemented by the current squarer illustrated in Fig. 2, where transistors M_1 and M_3 are the input and output devices, respectively. In order to obtain a better insight on the operation of this circuit, we invoke here the advanced compact MOSFET (ACM) model [14], revisited in Appendix 1.

In the derivation that follows, we assume that the transistor sets (M_B, M_2) and (M_A, M_1, M_3) in Fig. 2 are matched.

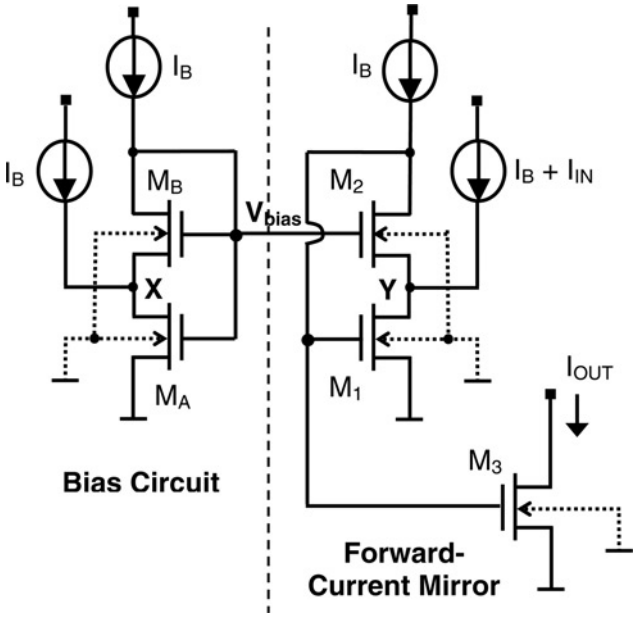

Figure 2 *Core cell of the analogue multiplier (squarer circuit)*

As will be shown in Appendix 2, the function of the bias circuit in Fig. 2 is to provide an appropriate (and constant) voltage at node Y, which is a replica of the voltage at node X. Since the voltage at node X can be easily made proportional-to-absolute temperature (PTAT), for the sake of convenience, we will use the notation $V_X = K\phi_t$ throughout the paper. Since the drain currents of the saturated transistors M_2 and M_B are the same and since their gates are connected, then $V_Y = V_X = K\phi_t$ as long as we assume that the modulation of the drain current is negligible in saturation.

In Fig. 2, M_1 is assumed to operate at constant and low drain-to-source voltage, that is, $V_Y \ll V_{DSSAT}$, with V_{DSSAT} defined by (14). Thus, according to (1)

$$g_{ms1} \cong \frac{I_{D1}}{V_Y} = \frac{2I_B + I_{IN}}{K\phi_t} \tag{2}$$

According to (9) and (13a) from Appendix 1

$$i_{f1} = \frac{I_{F1}}{I_{S1}} = \frac{\phi_t}{I_{S1}}\left(\frac{\phi_t}{4I_{S1}} g_{ms1}^2 + g_{ms1}\right) \tag{3}$$

where I_{F1}, i_{f1} and g_{ms1} are the forward saturation current, the normalised forward saturation current and the source transconductance of M_1, respectively, ϕ_t is the thermal voltage and I_{S1} is the specific current of M_1 given by (8) in Appendix 1.

Since transistors M_1 and M_3 share common gate, source and bulk terminals, the forward inversion levels i_{f1} and i_{f3} are equal. Assuming that M_3 operates in saturation and therefore its forward saturation current ($I_{F3} = I_{S3} i_{f3}$) is much greater than its reverse saturation current ($I_{R3} = I_{S3} i_{r3}$), the substitution of

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approximation (2) into (3) gives

$$I_{OUT} = I_{S3} i_{f1} = I_{S3}\left[\left(\frac{2I_B + I_{IN}}{2KI_{S1}} + 1\right)^2 - 1\right] \quad (4)$$

Therefore the output current I_{OUT} is a replica of the forward saturation current of M_1. Owing to this property, the pair M_1–M_3 can be called a forward-current mirror. Along with the desired quadratic term, I_{OUT} contains a linear term and a dc level associated with the bias current, which can be eliminated by a cancellation scheme (Section 3).

2.3 Design considerations

The input of the core cell $I_B + I_{IN}$ is a unidirectional current provided by a single p-channel transistor, that is, $|I_{IN}| \leq I_B$. In principle, this condition could be violated as long as the current flowing through M_1 is greater than zero ($2I_B + I_{IN} \geq 0$). However, it would be hard to sink a current from the core cell by means of an n-channel transistor operating in the saturation region since the voltage at node Y is typically lower than 100 mV, not high enough to saturate transistors operating even in weak inversion. Therefore in order to keep the current sources unidirectional, we must have $|I_{IN}| \leq I_B$ for a symmetrical input signal I_{IN}.

If transistor M_1 operates in weak inversion ($i_{f1} \leq 1$), the linear term in (4) prevails over the quadratic term. Although the linear term in (4) is eliminated by an appropriate combination of four squarer circuits (Section 3), the efficiency of this elimination relies on the matching of the squarer circuits. Thus, the operation of the proposed multiplier should not be deep in weak inversion.

An important design feature of the squarer circuit is the minimum power supply voltage to keep the transistors in the appropriate operating region, which is given by

$$V_{DDmin} = V_{CS} + V_{G1max} \quad (5a)$$

where V_{DDmin} is the minimum power supply voltage, V_{G1max} is the maximum gate voltage of M_1 and V_{CS} is the minimum required voltage between the terminals of the current source I_B for its proper operation.

The maximum gate voltage of M_1, V_{G1max}, results from the maximum input current, I_{INmax}, which is assumed equal to I_B. Thus, applying (12a) and (11) of Appendix 1 to transistor M_1, we obtain

$$\frac{V_{G1max} - V_{T0}}{n\phi_t} \cong \frac{V_{P1\,max}}{n\phi_t} = \sqrt{1 + i_{f1max}} - 2 + \ln\left(\sqrt{1 + i_{f1\,max}} - 1\right) \quad (5b)$$

The inversion level i_{f1max} is, in turn, computed from (12b) of Appendix 1

$$\frac{V_Y}{\phi_t} = K = \sqrt{1 + i_{f1\,max}} - \sqrt{1 + i_{r1\,max}} + \ln\left(\frac{\sqrt{1 + i_{f1\,max}} - 1}{\sqrt{1 + i_{r1\,max}} - 1}\right) \quad (5c)$$

where

$$i_{r1\,max} = i_{f1\,max} - \frac{I_{D1\,max}}{I_{S1}} = i_{f1\,max} - \frac{3I_B}{I_{S1}} \quad (5d)$$

If the current source I_B is implemented by a single p-channel transistor, V_{CS} is the source-to-drain saturation voltage of this transistor. The minimum supply voltage can be reduced by reducing the inversion levels of the current sources and of the transistors of the core cell at the expense of accuracy. The core cell of the proposed multiplier is able to operate at low supply voltages as a result of operating transistor M_1 in the linear region.

For instance, with $I_B = 10\,\mu A$, $(W/L)_A = 5$ and $(W/L)_B = 1$ (aspect ratios of transistors M_A and M_B, respectively), $V_{DDmin} = 1.2$ V in TSMC 0.35 μm CMOS technology and $V_{DDmin} = 0.95$ V in TSMC 0.18 mm CMOS technology.

3 Current-mode multiplier

According to the expression of the output current of the proposed squarer circuit, (4), any linear combination of two signals, I_X and I_Y, applied as the input current I_{IN}, originates the product $I_X I_Y$ along with other undesired terms. In order to eliminate these undesired terms, we adopt here a well-known cancellation scheme [1], shown in Fig. 3. The complete configuration of the multiplier in Fig. 3 comprises four squarer circuits, sharing the same bias circuit. The outputs of the squarer circuits are added in pairs and one of the resulting values is subtracted from the other for the cancellation of the undesirable terms. The resulting output current I_{OUT}, using (4) for each squarer cell in Fig. 3 with $I_{S3} = I_{S1}$, is

$$I_{OUT} = I_{OUTA} + I_{OUTD} - (I_{OUTB} + I_{OUTC}) = 2I_X I_Y/(K^2 I_{S1}) \quad (6)$$

It is important to note that in order to keep the input current of all core cells unidirectional, we must have $|I_X| + |I_Y| \leq I_B$.

The complete multiplier illustrated in Fig. 3 requires a few ancillary circuits, among which is the current subtractor. In this work, we have adopted as current subtractor the circuit described in [3], which represents a trade-off between complexity and symmetry. Although the output current components $I_{OUTA} + I_{OUTD}$ and $I_{OUTB} + I_{OUTDC}$ do not flow through identical paths, as more complex circuits

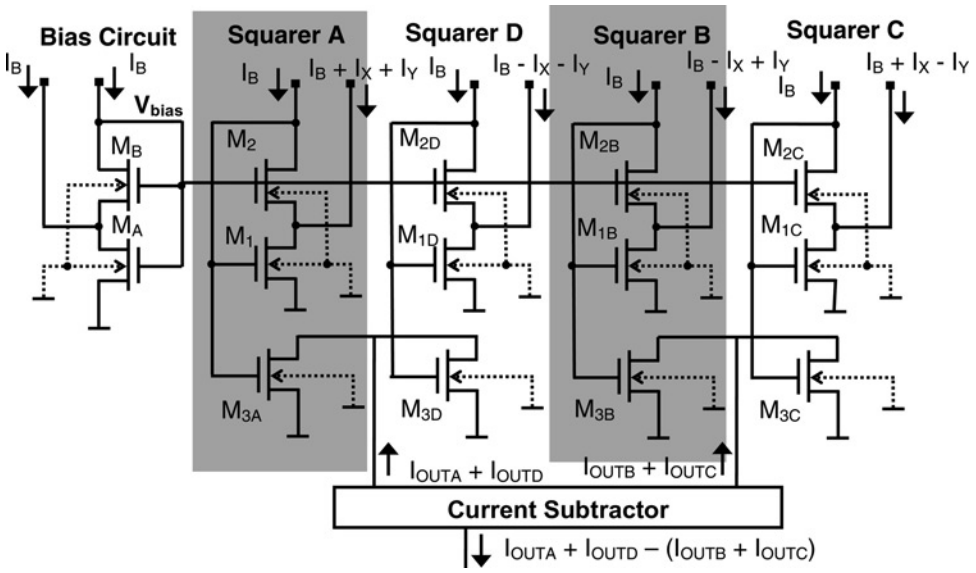

Figure 3 *Block diagram of the analogue multiplier*

should provide, the four squarer cells of Fig. 3 are symmetrically loaded.

Furthermore, accurate current mirrors are needed to generate replicas of I_X and I_Y and the corresponding symmetric signals. The topology of the current mirrors here used and illustrated in Fig. 4 is similar to the one presented in [3].

4 Experimental results

A design example of the multiplier was implemented in the 0.35 μm technology of TSMC as shown in Fig. 5. The multiplier core cell is shown inside a dashed rectangle. For the n-channel transistor, the threshold voltage V_{T0} is equal to 0.54 V, the slope factor n is approximately equal to 1.3, and the sheet specific current $I_{SQ} = I_S/(W/L)$ is equal to 72 nA (W and L are the channel width and length, respectively). In our design, we have adopted $I_B = 10$ μA and for each core cell: $i_{fA} = i_{f1} = i_{f3} = 197$, $i_{fB} = i_{f2} = i_{f3} = 140$, $W_A = W_1 = W_3 = 19.2$ μm, $W_B = W_2 = 4$ μm and $L = 4$ μm for all transistors in Fig. 3. We have chosen long-channel devices in order to reduce short-channel effects as well as to improve matching. In our example, the minimum supply voltage for proper operation of the circuit is around 1.6 V.

Some experimental features of the design example are presented in this section as well as some related simulation results obtained through circuit simulator SMASH [17], using BSIM 3v3.1.

The experimental and simulated transfer characteristics of the squarer prototype, along with (4), are shown in Fig. 6. The fitting of the experimental results by (4) is quite good.

Fig. 7 shows the measured dc current transfer characteristics of the multiplier for constant current at input

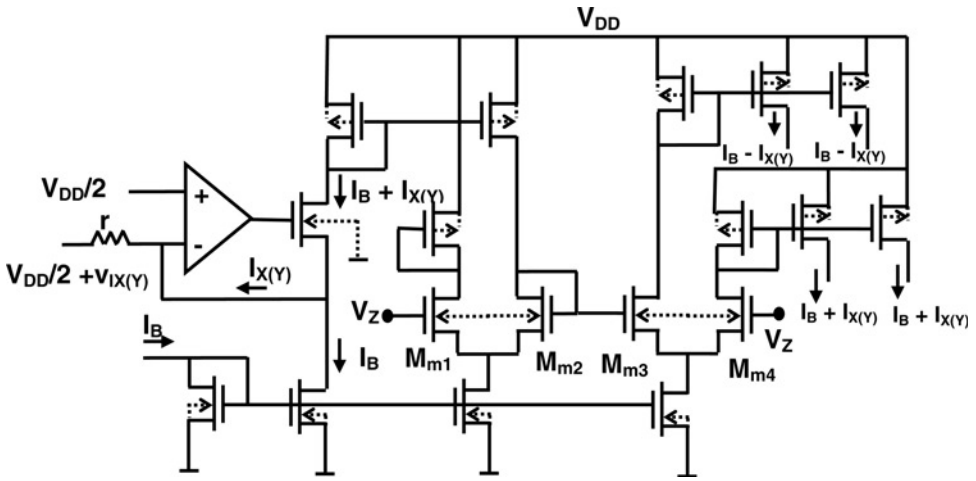

Figure 4 *Current-to-voltage converter and current mirrors*

V_Z is a constant voltage and $v_{IX(Y)} = rI_{X(Y)}$

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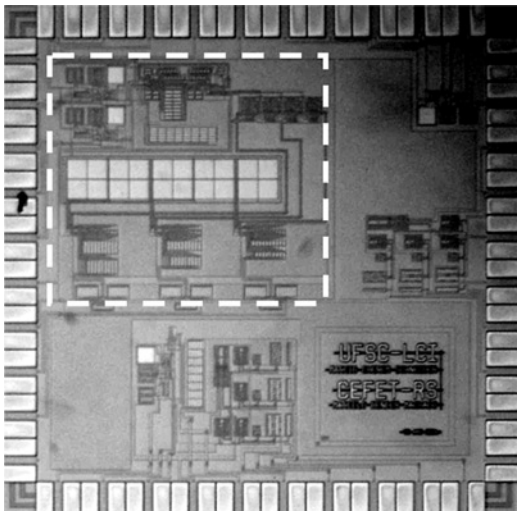

Figure 5 *Micrograph of proposed multiplier implemented in the 0.35 μm technology of TSMC*

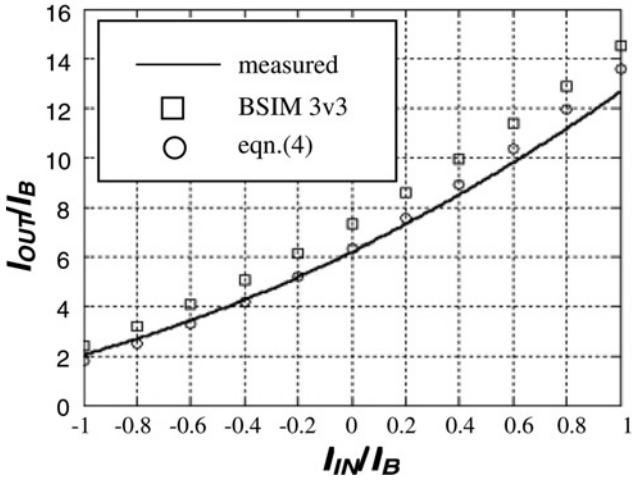

Figure 6 *Transfer characteristic of the squarer in 0.35 μm technology: measured (solid line), simulated with BSIM 3v3 (squares) and calculated in (4) (circles)*

X and I_Y varying in the range ±5 μA. The linearity of the multiplier, later confirmed by measurements of harmonic distortion (Table 1), is remarkably high for an input current up to 5 μA.

Fig. 8 shows the simulated and experimental frequency response of the multiplier for 5 μA dc at input X and peak amplitude equal to 5 μA at input Y. The −3 dB frequency of the multiplier is around 1 MHz.

Fig. 9 shows the experimental performance of the multiplier as an amplitude modulator for the case in which a 5 Hz sine wave modulates a 100 Hz carrier.

In Table 1 the experimental and simulated performances of the multiplier prototype here proposed are summarised.

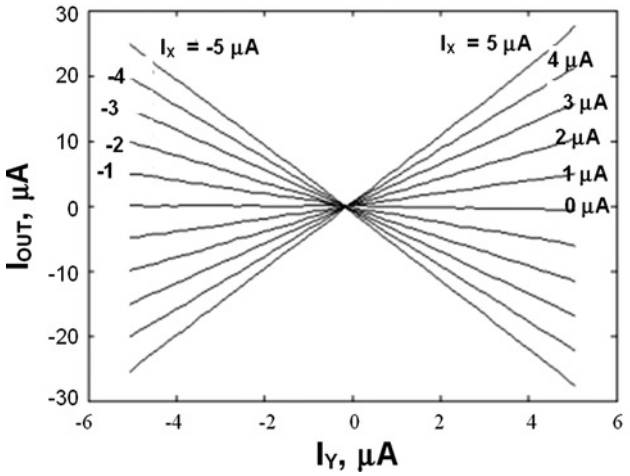

Figure 7 *Experimental dc transfer characteristics of the multiplier (I_B = 10 μA)*

Table 1 Experimental and simulated performance of multiplier prototype in CMOS 0.35 μm technology, input range of ±5 μA

Feature	Experimental	Simulated
supply voltage, V	3	3
THD (amplitude: 86% range, frequency: 100 kHz)[a], %	1.0	0.53
−3 dB bandwidth, MHz	1	1
power consumption (*V–I* converter not included)	1 mA	700 μA
area, μm^2	10 000	10 000

[a] I_X = 5 μA dc and peak of I_Y equal to 4.3 μA

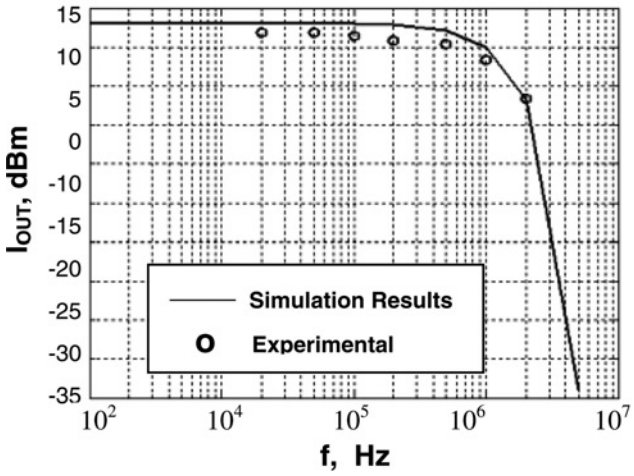

Figure 8 *Simulated and experimental frequency response of the integrated multiplier in 0.35 μm technology for I_B = 10 μA and I_X = 5 μA (V–I input converter included)*

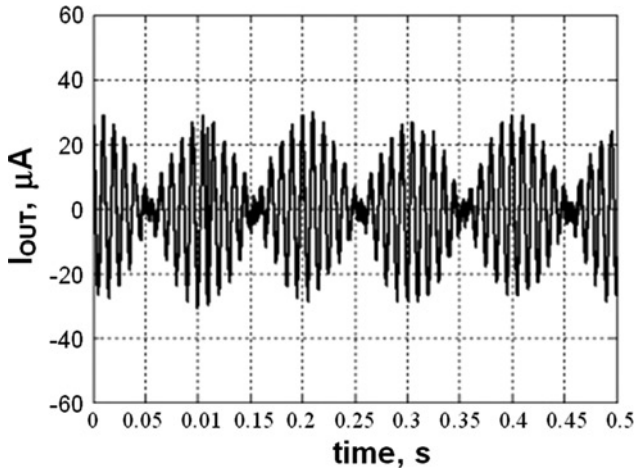

Figure 9 *Multiplier as an amplitude modulator (measured data)*

10 μA pp/100 Hz at input X and 10 μA pp/5 Hz at input Y, $I_B = 10$ μA

In our prototype, the supply voltage is almost twice the computed minimum value (1.6 V) in order to more easily dimension the ancillary circuitry. Lower voltage operation of the multiplier is possible with a consequent reduction in power consumption.

Drain-induced barrier lowering (DIBL) is of minor impact in the performance of the proposed multiplier, since M_1 in Fig. 2 operates with constant drain and source voltages. Channel length modulation (CLM) affects the output current and slightly affects node voltage V_Y in Fig. 2. In the case of V_Y, the effect of the input current on V_{G1} is transferred to node Y after being attenuated by the voltage gain of M_2 in the common-gate configuration. The CLM effect can be reduced in the core cell by either increasing the devices channel lengths, at the expense of frequency response, or using cascoded transistors with the need for higher supply voltage.

In the formalism of Section 2, constant specific current has been assumed, which is not true. Two factors contribute to the variation of the specific current, namely the slope factor and the mobility, both functions of the gate voltage. It can be seen in (4) that the quadratic term is proportional to the ratio $I_{S3}/(I_{S1})^2$. Since the gates of M_1 and M_3 in Fig. 2 are connected together, their specific currents are linearly related. Therefore the quadratic term is inversely proportional to I_{S1}. As a consequence, the scaling factor of the quadratic term varies with the input current since the gate voltage of M_1 is modulated by the input current. However, the dynamic range of the current that flows through M_1 is equal to 3. This variation of the current results in a significant variation of the gate voltage only for very high inversion levels, where the variation of the slope factor is extremely low, but the mobility variation because of the transverse field can be relatively important. Thus, only for very high inversion levels the core cell is affected by mobility degradation.

Both the linear and quadratic terms [see (4)] of the core cell are associated with components of the cell and, are thus, susceptible to deviations. Consequently, this cancellation scheme (as well as any other similar scheme) is very sensitive to mismatch of the cells. The need of four matched core cells may be avoided by adopting a switched-current structure [18], which in turn reduces the frequency range and increases circuit complexity.

5 Comparison with other architectures

In order to compare the proposed multiplier with other current-mode CMOS multipliers available in the literature, we have accomplished a few tests through circuit simulator SMASH [17], using BSIM 3v3.1. The architectures proposed in [8], where all transistors should operate in weak inversion, and in [5], where all transistors should

Table 2 Comparison between simulated performances of current mode multipliers in CMOS 0.25 μm technology, input range of ±5 μA

Feature	Sub-threshold mode [8] Nominal	Strong inversion mode [5] Nominal	Transconductance based (proposed)		
			Nominal	−5%[a]	+5%[b]
THD (80% range, 10 kHz), %	0.78	1.28	0.12	0.14	0.17
−3 dB bandwidth for small signals, MHz	3.3	30	36	32.4	23.2
−3 dB bandwidth for large signals, MHz	3	1	20	18	14
power consumption, mW	0.2	0.5	1.0	1.07	0.98
active area, μm^2	8918	2265	8554		

[a]Variation of −5% on nominal technological parameters. [b]Variation of +5% on nominal technological parameters

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operate deep in strong inversion, as well as the architecture described in this work have been redesigned in the 0.25 μm technology of TSMC. For this technology, the n-channel transistor presents a threshold voltage V_{T0} equal to 0.41 V, a slope factor n approximately equal to 1.33 and a sheet specific current $I_{SQ} = I_S/(W/L)$ equal to 110 nA; these parameters derived from a fitting of simulated characteristics to ACM model expressions.

For all designs, we have adopted supply voltages of ±1.25 V and have assumed maximum amplitude of input currents equal to 5 μA. Therefore the biasing currents have been dimensioned to allow a total swing of ±10 μA in each input terminal. In the squarer circuit of Fig. 2, we have determined $I_B = 10$ μA, $W_A = W_1 = 8$ μm, $W_B = W_2 = 32$ μm, $W_3 = 5.6$ μm and $L = 4$ μm for all transistors.

The simulation results concerning total harmonic distortion (THD) analysis, −3 dB bandwidth, power consumption and active area are summarised in Table 2. The nominal parameters of BSIM 3.3v1 have been used in the simulation of the three multipliers and a variation of ±5% on these parameters has been applied to the proposed architecture.

For evaluating THD at 80% input range, I_X is a 10 kHz sinusoidal signal with amplitude equal to 4 μA and I_Y is a constant current of 4 μA. The −3 dB bandwidth has been determined through simulator ac analysis, according to which all transistors are modelled as linear devices for small signal operation. Since these circuits are designed for large signal operation and harmonic distortion is not taken into account in ac analysis, −3 dB bandwidth has also been estimated through transient analysis, with I_X as a sinusoidal signal of variable frequency and amplitude equal to 4 μA and with constant $I_Y = 4$ μA.

By examining the simulation results in Table 2, it should be noticed that at the expense of twice the power consumption of the strong inversion mode architecture [5] and almost the same area of the weak inversion mode architecture [8], the proposed multiplier exhibits the best performance regarding harmonic distortion and bandwidth. It has been also verified through Monte Carlo analysis that the proposed circuit is far less sensitive to threshold voltage mismatching than the other two architectures.

6 Conclusion

We presented a four-quadrant CMOS current-mode multiplier capable of operating at low voltage supplies. Its main advantages are the simplicity and feasibility of low-voltage operation, low distortion and low sensitivity. The multiplier functionality has been experimentally verified for a prototype implemented in 0.35 μm CMOS technology.

Comparison with sub-threshold mode [8] and strong inversion mode [5] architectures, through simulation results, revealed that the proposed multiplier has a better performance regarding bandwidth, THD and sensitivity to threshold voltage mismatching, with comparable consumption of power and silicon area.

Finally, it should be observed that this work is based on a very recent design approach: the exploitation of the quadratic relationship between the MOSFET saturation current and the source inversion charge density. This new approach opens interesting possibilities for the conception of analogue signal processing circuits.

7 Acknowledgments

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9 Appendix 1

The main expressions of the MOSFET model [14] used in this study are

$$I_D = I_S(i_f - i_r) \tag{7}$$

$$I_S = \mu C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} \tag{8}$$

$$i_{f(r)} = q'^2_{IS(D)} + 2q'_{IS(D)} \tag{9}$$

$$q'_{IS(D)} = -\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t} \tag{10}$$

$$V_P = \left(\sqrt{V_G - V_{FB} + \frac{\gamma^2}{4}} - \frac{\gamma}{2}\right)^2 - 2\phi_F \cong \frac{V_G - V_{T0}}{n} \tag{11}$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{12a}$$

$$V_{DS} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + \ln\left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1}\right) \tag{12b}$$

$$g_{ms} = -\frac{\partial I_D}{\partial V_S} = \frac{2I_S}{\phi_t} q'_{IS} \tag{13a}$$

$$g_{ms} = \frac{2I_S}{\phi_t}\left(\sqrt{1 + i_f} - 1\right) \tag{13b}$$

$$V_{DSSAT} = \phi_t\left(\sqrt{1 + i_f} + 3\right) \tag{14}$$

where I_D is the drain current, i_f (i_r) is the normalised forward (reverse) saturation current, I_S is the specific current, ϕ_t is the thermal voltage, n is the slope factor, μ is the carrier mobility, C'_{ox} is the oxide capacitance per unit area, $Q'_{IS(D)}$ is the inversion charge density at source (drain), $q'_{IS(D)}$ is the normalised inversion charge density at source (drain), V_P is the pinch-off voltage, V_G is the gate-to-bulk voltage, $V_{S(D)}$ is the source(drain)-to-bulk voltage, V_{T0} is the threshold voltage, g_{ms} is the source transconductance, V_{DSSAT} is the drain-to-source saturation voltage, W is the channel width and L is the channel length.

10 Appendix 2

The drain-to-source voltage V_X across transistor M_A in Fig. 1 is calculated using the following set of equations, based on the ACM model (Appendix 1). Such voltage is transferred to node Y through a transistor (M_2) operating under the same inversion level as M_B.

Applying (12a) of Appendix 1 to transistor M_B, we obtain

$$\frac{V_{PB} - V_X}{\phi_t} = \sqrt{1 + i_{fB}} - 2 + \ln\left(\sqrt{1 + i_{fB}} - 1\right) \tag{15a}$$

Since M_B is in saturation, then $i_{fB} \gg i_{rB}$ and, according to (7) of Appendix 1, the inversion level at source of M_B is $i_{fB} = I_B/I_{SB}$.

Since the source of M_B is connected to the drain of M_A, the inversion level at the drain of M_A is equal to the inversion level at the source of M_B, that is, $i_{rA} = i_{fB}$. Therefore according to (7) of Appendix 1, the inversion

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level at source of M_A (in non-saturation, in general) is

$$i_{fA} = \frac{2I_B}{I_{SA}} + \frac{I_B}{I_{SB}} \tag{15b}$$

Finally, we can apply (12a) to M_A, for which $V_{SA} = 0$

$$V_{PA}/\phi_t = \sqrt{1 + i_{fA}} - 2 + \ln\left(\sqrt{1 + i_{fA}} - 1\right) \tag{15c}$$

Since the gates of M_A and M_B are connected together, $V_{PA} = V_{PB}$. Replacing V_{PB} in (15a) by the expression of V_{PA} in (15c), we solve for V_X, which gives

$$\begin{aligned} V_X/\phi_t = K = &\sqrt{1 + \frac{I_B}{I_{SA}}\left(2 + \frac{I_{SA}}{I_{SB}}\right)} - \sqrt{1 + \frac{I_B}{I_{SB}}} \\ &+ \ln\left(\sqrt{1 + \frac{I_B}{I_{SA}}\left(2 + \frac{I_{SA}}{I_{SB}}\right)} - 1\right) \\ &- \ln\left(\sqrt{1 + \frac{I_B}{I_{SB}}} - 1\right) \end{aligned} \tag{16}$$

If current source I_B is obtained through a specific current generator, that is, if I_B is proportional to the specific current I_S, as described in [19, 20], then V_X is PTAT.