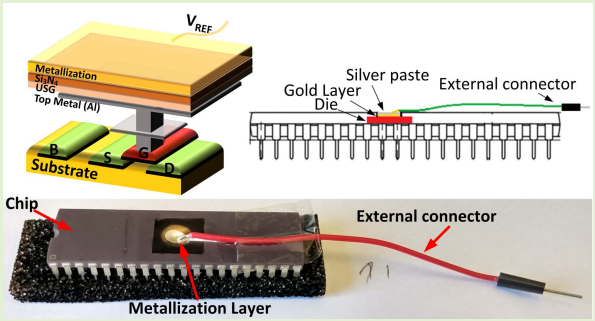
A CMOS Test Chip With Simple Post-Processing Steps for Dry Characterization of ISFET Arrays

Rodrigo Wrege, Celso Peter, Bruno N. Wesling, Carlos R. Rambo, *Member, IEEE*, Márcio Cherem Schneider, *Senior Member, IEEE*, and Carlos Galup-Montoro, *Senior Member, IEEE*

***Abstract*—ISFETs (ion sensitive field effect transistors) are ion solid-state sensors based on MOSFETs (metal oxide semiconductor field effect transistors) applied in many areas including ion imaging, detection of viruses and bacteria and DNA sequencing. ISFETs implemented in standard CMOS technology adopt the inherent Si_3N_4 passivation as the sensing layer, and benefit from a high integration level with no need of post-processing steps. However, this implementation is associated with non-idealities such as output temporal drift, capacitive attenuation of the input signal and random offsets in the threshold voltage due to trapped charges. Most of these non-idealities, which require better understanding, are characterized through biasing a reference electrode immersed in a solution in contact with the passivation layer. To remove electrochemical effects from the measurements, this paper proposes a dry test where the wet test setup is replaced with a sputtered gold thin film that provides electrical contact with the ISFETs. Dry tests were performed in arrays of n-ISFETs and p-ISFETs from chips fabricated in a standard 180 nm high voltage CMOS technology. The intra-die threshold voltages of the n-ISFETs and p-ISFETs presented, on average, similar offsets, but their die-to-die fluctuation was high. Wet tests on an n-ISFET and a p-ISFET of two non-metalized chips indicated sensitivities of 38 mV/pH and 46 mV/pH, respectively. The dry test introduced herein allows the electrical parameters of ISFETs to be determined without the interference of chemical contributions as well as the charges trapped in the passivation layer to be estimated.**



***Index Terms*— Dry test, ISFET, modeling, sputtering, trapped charge, threshold voltage.**

I. Introduction

WHEN a viral infection such as dengue, zika and covid-19 spreads around the world, an instrument for rapid diagnosis that is affordable, portable, accurate and easy to use is an important tool for contagious disease control. An electronic platform with specific techniques, such as amplification of pathogen ribonucleic acid, and sensors allow both the rapid detection of the virus in biological samples (e.g., human blood, urine or saliva) and the communication of the results to a cloud system to improve analysis within the health system [1].

A suitable sensor for this sort of application is the ISFET (ion sensitive field effect transistor), which is a small structure based on the MOSFET (metal oxide semiconductor field effect transistor) capable of measuring the ionic concentration of solutions. Since its inception in 1970 by Bergveld [2], the ISFET has been used in different areas including food analysis [3], detection of viruses [4] and bacteria [5], ion imaging [6], DNA sequencing [7] and DNA methylation detection for early cancer screening [8]. With the advent of the extended-gate technique in 1999 [9], ISFETs started to be realized with unmodified CMOS (complementary metal oxide semiconductor) processes, eliminating the post-processing steps needed in the early fabrication methods.

The extended-gate technique expanded the sensor application to lab-on-chip platforms and allowed the integration of high-density arrays with more than 1000 sensors per die [10], with small dimensions, thus requiring less reagents and reducing the testing costs. Additionally, the extended-gate technique allows mass production at low cost and the coexistence of

Manuscript received October 2, 2020; accepted October 29, 2020. Date of publication November 3, 2020; date of current version January 15, 2021. This work was supported in part by the Brazilian governmental agencies CAPES (Finance Code 001), in part by Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), in part by the ITT Chip, and in part by the Chipus Microeletronics S.A. The associate editor coordinating the review of this article and approving it for publication was Dr. Amitava Chatterjee. *(Corresponding author: Rodrigo Wrege.)*

Rodrigo Wrege, Bruno N. Wesling, Carlos R. Rambo, Márcio Cherem Schneider, and Carlos Galup-Montoro are with the Department of Electrical and Electronics Engineering, Federal University of Santa Catarina (UFSC), Florianópolis 88040-900, Brazil (e-mail: rodrigowrege@gmail.com; brneckel@gmail.com; carlos.rambo@ufsc.br; marcio.cherem.schneider@gmail.com; carlosgalup@gmail.com).

Celso Peter is with the ITT Chip, UNISINOS, São Leopoldo 93022-750, Brazil (e-mail: cepeter@unisinos.br).

Digital Object Identifier 10.1109/JSEN.2020.3035627

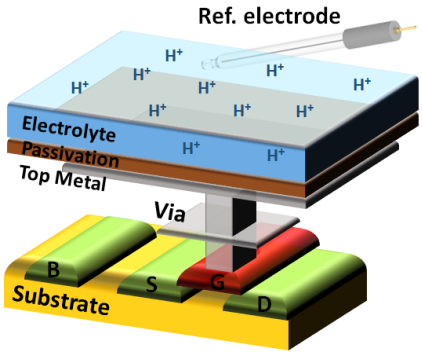


Fig. 1. ISFET structure in a standard CMOS technology.

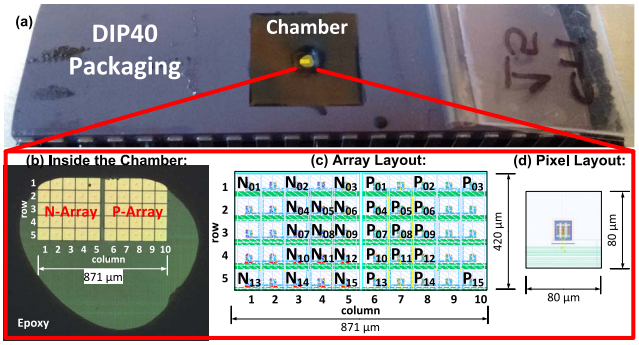


Fig. 2. (a) The chip encapsulated in DIP40, (b) details of the epoxy chamber, (c) array layout with identification of devices, and (d) pixel layout.

the sensor readout and bias circuitry on the same chip. These characteristics, along with low power consumption, paved the way to implementing ISFETs in portable devices, which are mostly desirable for point-of-care applications.

The extended-gate technique consists of connecting the MOSFET gate (in red in Fig. 1), which is left floating, to the top metal that is in contact with the passivation layer, usually silicon nitride (Si_3N_4). In an ISFET, the passivation layer in direct contact with the solution functions as a sensing membrane. An external reference electrode (usually Ag/AgCl) immersed in the solution serves as the gate terminal of the ISFET (Fig. 1). Despite the benefits of using a standard CMOS process, the use of the passivation layer as a sensing membrane presents some challenges due to non-idealities, namely, fluctuations in the threshold voltage due to trapped charges, temporal output drift influenced by device size, the solution and the reference electrode, and input capacitive attenuation due to the capacitive divider formed by the passivation, oxide and depletion capacitances [11], [12]. In spite of the use of techniques such as circuit level compensations, differential measurements and ultraviolet exposition [11] to mitigate the effects of these non-idealities, most of them still need to be better understood and characterized.

The ISFET threshold voltage varies in response to the solution pH, as described using the Gouy-Chapman-Stern and site-binding theories [13]. The current-voltage characteristic of the ISFET is modelled through the combination of these two theories with the transistor model, which in this paper is the advanced compact MOSFET (ACM) model [14].

Besides the ion sensitivity, for which the maximum is theoretically $2.3\phi_t$/pH (=59 mV/pH at 25°C) [13], where ϕ_t is the thermal voltage, other ISFET electrical parameters related to the passivation layer and the MOS transistor must be characterized to achieve an appropriate design. The conventional characterization of ISFETs is affected by the electrochemistry of the solution, changes in the reference electrode potential due to leakage currents, which affects the temporal output drift [12], and the degradation of the passivation layer due to long-term contact with the solution [11].

In order to remove these electrochemical effects from the measurements, this paper proposes a dry test by replacing the wet test elements (solution and electrode) with a sputtered gold (Au) film, for the characterization of the ISFET electrical parameters, such as the capacitive attenuation, trapped charges, slope factor and specific current. This is a complementary tool for ISFET analysis, given that the conventional wet test is still needed to determine the pH sensitivity.

II. Materials and Methods

A. The Fabricated Chip

The chip, designed with Virtuoso® and fabricated in a standard 180 nm high voltage CMOS technology, consists of an array with 15 p-ISFETs, 15 n-ISFETs, 1 p-MOSFET and 1 n-MOSFET. The ISFETs and the MOSFETs employ thick oxide transistors (12.5 nm oxide thickness, supporting V_{GS} up to 5.5 V, mainly used for input/output pins) with a gate width (W) and length (L) of 9 μm and 1.8 μm, respectively, and top metal area A_{pass} of 80 μm x 80 μm, which results in $A_{pass} = 395A_{mos}$ ($A_{mos} = W^*L$). The total area of the die is 2.28 mm x 2.28 mm with a sensing area of 871 μm x 420 μm at the die center. In order to facilitate access to the components, the die was packaged (Fig. 2), as described in the next subsection. The available n-ISFETs and p-ISFETs of the array are identified as N01 to N15 and as P01 to P15, respectively, as in Fig. 2c (the remaining devices are dummy elements). The pixel dimensions are shown in Fig. 2d.

The technology employed has six metal layers and a passivation layer of Si_3N_4 on top of undoped silicate glass (USG), with typical thicknesses of 500 nm and 900 nm, respectively, and relative dielectric constants of 7.5 and 4.2, respectively. The MOSFET gate oxide capacitance (C_{ox}) is 44 fF, calculated using the relative dielectric constant of 3.9 for silicon dioxide, the specified oxide thicknesses of 12.5 nm and A_{mos}. The passivation capacitance values for the Si_3N_4 (C_{SiN}) and USG (C_{USG}) layers, for the previously specified A_{pass}, thicknesses and dielectric constants, are 849 fF and 264 fF, respectively. The total passivation capacitance (C_{pass}) is the series association of the capacitances of the Si_3N_4 and USG layers:

$$C_{pass} = \frac{C_{SiN}C_{USG}}{C_{SiN} + C_{USG}} = 201\text{fF} \quad (1)$$

B. Chip Packaging

The die was wire bonded in a DIP40 (dual in-line package with 40 pins) with an open cavity (die is uncovered), as shown

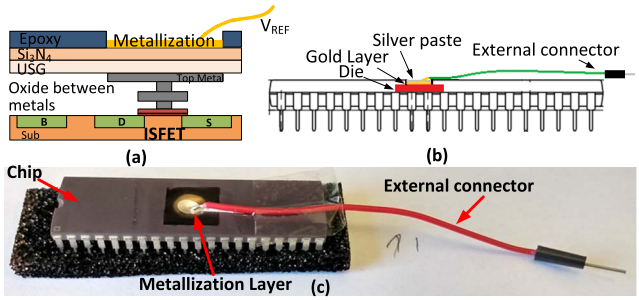


Fig. 3. (a) Cross section of a metalized ISFET; (b) diagram of the die encapsulated in DIP40 package, and (c) encapsulated chip.

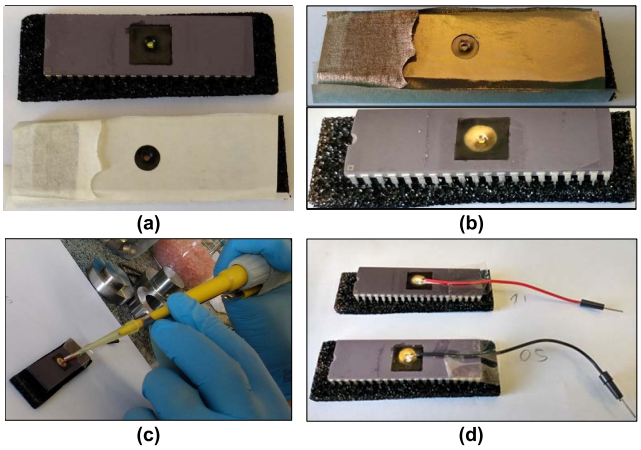


Fig. 4. Au metallization process: (a) mask application, (b) removing the mask after the sputtering, (c) applying the silver paste, (d) final assembly.

in Fig. 2a. In order to protect the pads and bonding wires, epoxy was applied to them only, leaving the top plates of the ISFETs exposed (Fig. 2b). The resulting chamber (diameter of 1 mm, height of 0.5 mm) allows different solutions or other materials to be applied.

In order to check the integrity of the electrical connections after the epoxy deposition, the devices were visually inspected using X-ray images and electrically tested through measuring the bulk/source and bulk/drain junctions of the ISFETs.

C. Gold Sputtering for Dry Tests

In order to carry out the dry test proposed herein, an Au layer was deposited on the chamber to provide electrical contact with the floating gates. Sputtering, a commonly technique used to deposit sensing films in ISFETs [15], was employed to form the thin film with neutral Au particles [16]. Illustrations of the ISFET cross section with a metallization layer and the encapsulated chip are shown in Fig. 3.

Fig. 4 shows the main steps employed for the Au metallization. Firstly, a mask was applied, consisting of a tape with a central hole (Fig. 4a), to block the Au deposition in areas other than the top of the ISFET arrays. The chip was kept in anti-static foam. In the next step, the source material (Au) and the substrate (the chip, in this case) were placed in parallel plates of the sputtering chamber. The Au DC sputtering was performed using a SPI-Module sputter coater with the parameters given in TABLE I, giving rise to an Au film thickness

TABLE I
DEPOSITION PARAMETERS FOR AU

Parameter	Value
Sputter target	Au
Substrate temperature	25 °C
Deposition time	120 s
Target to substrate distance	5 cm
Cathode voltage	-1000 V
Cathode current	20 mA

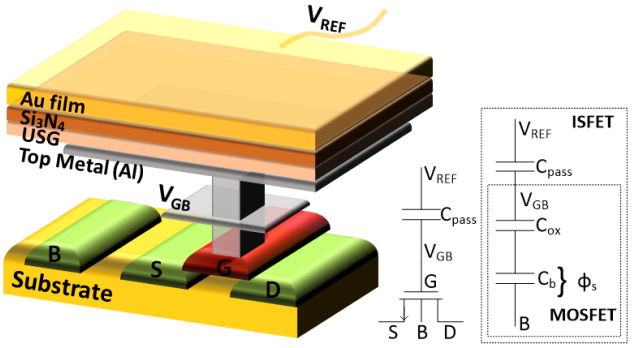


Fig. 5. Cross-section illustration, schematic showing MOSFET, and capacitive model of an ISFET with a metallization layer.

of around 40 nm, according to the following equation:

$$d = KIVt \tag{2}$$

where d is the film thickness in angstroms, K is 0.17 for Au mixed with argon (Ar), I is the plasma current in mA, V is the inter-electrode voltage in kV and t is the sputtering time in s.

After the sputtering process had been completed, the mask was removed, leaving only the ISFETs and some parts of the epoxy covered with Au (Fig. 4b). An external connector was glued to the Au layer with a conductive silver paste (Electrotube SCP003), as Fig. 4c shows. To improve the robustness for manipulation, the connector was also glued to the DIP40 package using Loctite Super Bonder (Fig. 4d).

III. ANALYSIS OF METALIZED ISFETS

Fig. 5 shows an illustration of an ISFET with a metallization Au layer for its gate along with its capacitive model. The *dry gate* ISFET characteristics are modified with respect to those of the MOSFET due to the following factors. Firstly, the ISFET *dry gate* is made of a gold layer, whereas polysilicon is used for the MOSFET gate. The different materials for the gates translate into different gate work functions [17]. Secondly, the ISFETs have a capacitive coupling between the external contact (V_{REF}) and the floating gate terminal (V_{GB}); therefore, the voltage V_{GB} is attenuated with respect to V_{REF}. Thirdly, the connection of the polysilicon floating gate to the Al top metal generates a contact potential.

The advanced compact model (ACM) of the MOSFET [14] was extended to the ISFET in a previous paper [18]. In the following, we use the ACM model to derive a set of equations for application to the *dry gate* ISFET. The drain current I_D

is given in terms of the forward and reverse inversion levels (i_f and i_r, respectively) [14] by:

$$I_D = I_S(i_f - i_r) \tag{3}$$

with I_S being the normalization current given by:

$$I_S = \mu C'_{ox} n_{mos} \frac{\phi_t^2}{2} \frac{W}{L} \tag{4}$$

where μ is the carrier mobility, C'_{ox} the oxide capacitance per unit area, n_{mos} the MOSFET slope factor, ϕ_t the thermal voltage (around 26 mV at room temperature), W the transistor width and L the transistor length.

The terminal voltages are related to the forward and reverse inversion levels by:

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \tag{5}$$

where V_S and V_D are the source and drain voltages, respectively, and V_P is the pinch off voltage:

$$V_P = \frac{V_{GB} - V_{Tmos}}{n_{mos}} \tag{6}$$

where V_{GB} is the gate voltage and V_{Tmos} is the MOSFET threshold voltage. In the case of the *metal-gate* ISFET, (6) can be written as:

$$V_P = \frac{V_{REF} - V_{TISF\_met}}{n_{ISF\_met}} \tag{7}$$

where V_{TISF_met} and n_{ISF_met} are the threshold voltage and slope factor of the *metal-gate* ISFET, which will be derived in the next subsections. The combination of equations (3) and (5) gives the transconductance-to-current ratio (g_m/I_D), where g_m is dI_D/dV_G (for the MOSFET) or dI_D/dV_{REF} (for the ISFET).

$$\frac{g_m}{I_D} = \frac{1}{n\phi_t} \frac{2}{\sqrt{1 + i_f} + \sqrt{1 + i_r}} \tag{8}$$

In (8), n is n_{mos} or n_{ISF_met} (for the MOSFET or ISFET, respectively).

A. Slope Factor

The MOSFET slope factor is given [14] by:

$$n_{mos} = 1 + \frac{C_b}{C_{ox}} \tag{9}$$

where C_b is the depletion capacitance. Thus, considering the passivation capacitance (Fig. 5), the slope factor of the metalized ISFET is:

$$n_{ISF\_met} = 1 + \frac{C_b}{C_{eff}} \tag{10}$$

where C_{eff} is the series association of capacitances C_{ox} and C_{pass}:

$$\frac{1}{C_{eff}} = \frac{1}{C_{ox}} + \frac{1}{C_{pass}} \tag{11}$$

Summarizing, there is an increase in the slope factor of the ISFET compared to that of the MOSFET due to the passivation capacitance. Since the Gouy-Chapman capacitances from the electrochemical interface are much higher than C_{ox} and C_{pass}, (11) can also be used for wet tests [19].

B. Threshold Voltage

The MOSFET threshold voltage (V_{Tmos}) is given [14] by:

$$V_{Tmos} = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F} \tag{12}$$

where ϕ_F is the bulk Fermi potential and γ the body-effect factor, related to the slope factor by [14]:

$$\gamma = 2(n_{mos} - 1)\sqrt{2\phi_F} \tag{13}$$

V_{FB} is the flat band voltage given by:

$$V_{FB} = \phi_{MS} - \frac{Q_o}{C_{ox}} \tag{14}$$

Q_o is the equivalent charge at the interface oxide-semiconductor and ϕ_{MS}, designated as the contact potential [20], is the difference between the work functions per electron charge of the gate and semiconductor materials given by

$$\phi_{MS} = \phi_{poly} - \phi_{sc} = \phi_{poly} - \left[\chi + \frac{E_g}{2q} + \phi_t \ln \left(\frac{N_a}{n_i} \right) \right] \tag{15}$$

where ϕ_{poly} and ϕ_{sc} are the work functions per electron charge of the polysilicon gate and the semiconductor, respectively, χ the semiconductor electron affinity per electron charge (4.05 V for Si), E_g the silicon band gap (1.12 eV), q the electron charge, N_a the substrate doping and n_i (10^{10} cm^{-3} at 25°C) the intrinsic carrier concentration in the silicon [21].

The ISFET threshold voltage is defined in a similar way to that of the MOSFET, *i.e.*, at the threshold condition the surface potential φ_S at the semiconductor equals $2\phi_F$. For this surface potential, the semiconductor charge is equal to $-\gamma C_{ox}\sqrt{2\phi_F}$.

Similarly to the MOSFET, the gate voltage needs to be equal to the flat-band voltage ($V_{FB,ISF}$) to compensate both the difference in the work functions of the materials employed in the ISFET and charges Q_o and Q_{pass}, where Q_{pass} is the equivalent charge trapped at the interface between the passivation layer and the top metal of the technology.

$$V_{FB,ISF} = \phi_{Au} - \phi_{sc} + \phi_{poly} - \phi_{met} - \frac{Q_o}{C_{eff}} - \frac{Q_{pass}}{C_{pass}} \tag{16}$$

where ϕ_{Au} and ϕ_{met} are, respectively, the work functions of gold and aluminum, the latter being the metal of the bottom of the passivation layer. The term Q_{pass}/C_{pass} represents the offset in the flat-band voltage due to the charges trapped at the passivation.

Assuming that the flat-band voltage is equal to zero, a voltage V_{REF} must be applied to the ISFET Au gate, such that the surface potential ϕ_S equals $2\phi_F$. At this surface potential, the semiconductor charge is equal to $-\gamma C_{ox}\sqrt{2\phi_F}$; therefore, the value of V_{REF} is given by

$$\frac{C_{pass} C_{ox}}{C_{pass} + C_{ox}} (V_{REF} - 2\phi_F) = \gamma C_{ox} \sqrt{2\phi_F} \tag{17}$$

Finally, superimposing the results from equations (16) and (17) we find that the threshold voltage of the *metal-gate* ISFET is

$$V_{TISF\_met} - 2\phi_F = \phi_{Au} - \phi_{met} + \phi_{poly} - \phi_{sc} + \frac{1}{C_{eff}} \left(-Q_o + \gamma C_{ox} \sqrt{2\phi_F} \right) - \frac{Q_{pass}}{C_{pass}} \tag{18}$$

Note the similarity between the result of (18) and the threshold voltage of the MOSFET. In the ISFET, another contact potential, between Au and Al (top metal), is included. The effects of both the oxide charge and the semiconductor charge are, in the ISFET, coupled to the Au gate by means of C_{eff}, rather than C_{ox} (as in the case of the MOSFET). Equation (18) can be rewritten in terms of the MOSFET threshold voltage as:

$$V_{TISF\_met} = \phi_{Au} - \phi_{met} + \frac{C_{pass} + C_{ox}}{C_{pass}} V_{Tmos} - \frac{C_{ox}}{C_{pass}} \left(2\phi_F + \phi_{poly} - \phi_{sc}\right) - \frac{Q_{pass}}{C_{pass}} \quad (19)$$

Equation (19) can be expressed as:

$$V_{TISF\_met} = \phi_{Au} - \phi_{met} - \frac{Q_{pass}}{C_{pass}} + V_{Tmos} + \frac{\gamma\, C_{ox}\sqrt{2\phi_F} - Q_o}{C_{pass}} \quad (20)$$

The work functions per electron charge for Au, Al, and heavily doped n^+poly (n-MOSFET) and p+poly (p-MOSFET) silicon gates are: $\phi_{Au} = 5.1$ V, $\phi_{met} = 4.28$ V, $\phi_{n+poly} = 4.15$ V and $\phi_{p+poly} = 5.27$ V, respectively [22].

IV. Results and Discussion

The test setup was configured with the Agilent 4156C semiconductor parameter analyzer and the Agilent 16442A test fixture. The threshold voltage, the specific current and the slope factor were extracted with the g_m/I_D methodology described in [14].

The $I_D x V_{REF}$ and $g_m/I_D x V_{REF}$ curves for the ACM model, implemented in Matlab®, are compared with measurement results for an n-ISFET (Fig. 6a) and a p-ISFET (Fig. 6b). The extracted parameters for the n-ISFET under test are $V_{TISF\_met} = 3.32$ V, $I_S = 231$ nA and $n_{ISF\_met} = 2.72$ while for the p-ISFET they are $V_{TISF\_met} = -0.75$ V, $I_S = 73.2$ nA and $n_{ISF\_met} = 2.41$. The model and the experimental results are in close agreement.

Fig. 7 presents the spatial distribution of the threshold voltage (V_t) across the n-ISFET and p-ISFET arrays, for four chips. Device malfunctions were mainly caused by open connections in the bonding wires due to the epoxy deposition. Histograms of the threshold voltages are shown in Fig. 8. Threshold voltage dispersions are mainly caused by fluctuations in trapped charges.

In floating gate devices, charges are trapped in the gate and mostly in the passivation layer during the fabrication process, causing offsets in the threshold voltage. Using the model developed and practical results, it is possible to estimate this charge. TABLE II presents the offset considering the value of V_{TISF_met}, assuming that there are no charges ($Q_{pass} = 0$ C) at the passivation layer, and the mean values of V_{TISF_met} measured on different chips. The value of V_{TISF_met} for $Q_{pass} = 0$ C was calculated using (20) with mean values of V_{Tmos} equal to 1.012 V and -1.213 V, and n_{mos} of 2.50 and 2.01, measured on 15 dies for the n-MOSFETs and the p-MOSFETs, respectively, and $|2\Phi_F| = 0.8$ V.

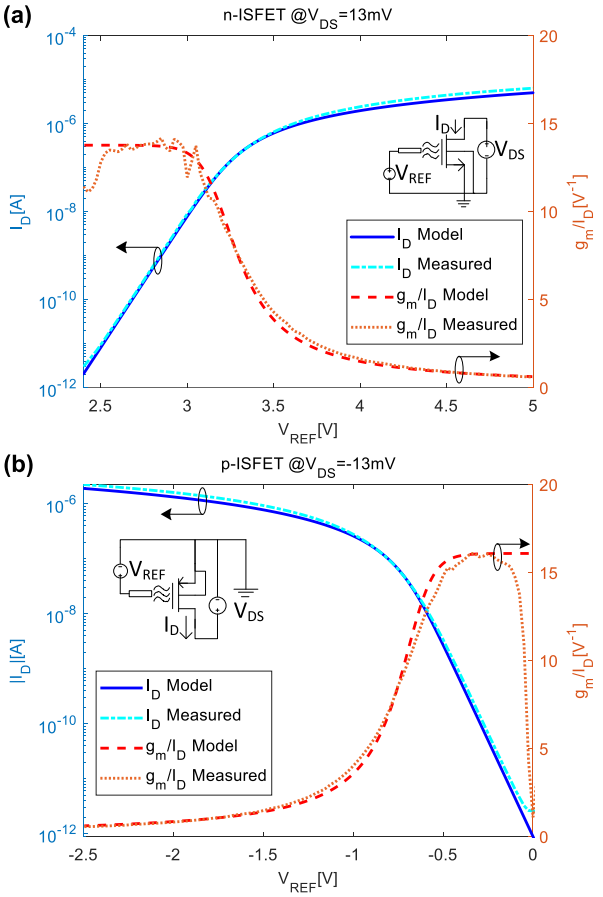


Fig. 6. $I_D \times V_{REF}$ and g_m/I_D x V_{REF} of model and measurements for (a) an n-ISFET and (b) a p-ISFET.

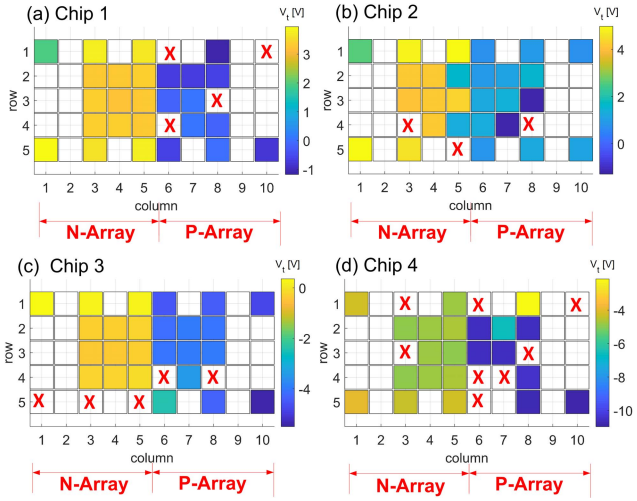


Fig. 7. Spatial variation of threshold voltage across the array after the dry characterization of four chips ("X" means failed device; empty spaces are dummy elements).

Thus, the resulting V_{TISF_met} values, assuming $Q_{pass} = 0$ C, were 2.38 V for the n-ISFETs and −0.76 V for the p-ISFETs. Defining offset as the difference between the theoretical value of the threshold voltage for $Q_{pass} = 0$ C and the measured values, the value of Q_{pass} can be readily calculated using (20).

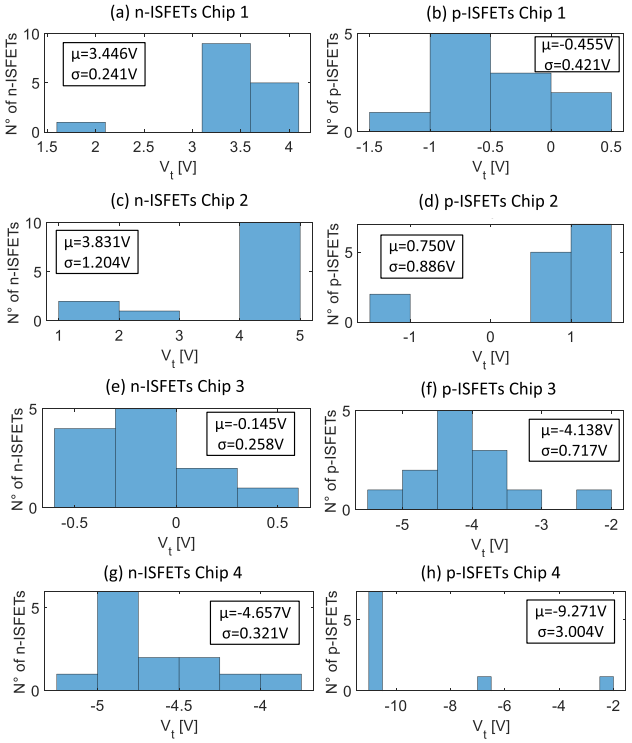


Fig. 8. Histograms of the threshold voltages measured on the n-ISFET and p-ISFET arrays of four chips.

TABLE II
ESTIMATION OF THE OFFSET IN THRESHOLD VOLTAGE DUE TO TRAPPED CHARGES AT PASSIVATION

	n-ISFETs			p-ISFETs		
Sample	V_t [V] μ meas.	**Offset [V]**	Q_{pass} [fC]	V_t [V] μ meas.	**Offset [V]**	Q_{pass} [fC]
Chip 1	3.45	**1.07**	**-214**	-0.46	**0.30**	**-61**
Chip 2	3.83	**1.45**	**-292**	0.75	**1.51**	**-303**
Chip 3	-0.15	**-2.53**	**508**	-4.14	**-3.38**	**680**
Chip 4	-4.66	**-7.04**	**1414**	-9.27	**-8.51**	**1711**

TABLE III
ISFET THRESHOLD VOLTAGE DISPERSION COMPARED WITH PREVIOUSLY PUBLISHED VALUES

Ref.	**Year**	**Technology**	**Threshold voltage dispersion**	**ISFET type**	**Test type**
[9]	1999	Atmel-ES2 1.0 μm	6.4 ± 1.4 V (linear gate) -7.0 ± 0.8 V (Interdigitated)	N	wet (pH 7)
[25]	2008	AMS 0.35 μm	-4 to -1 V	P	wet (pH 7.4)
[26]	2011	0.35-μm 2P3M CMOS	-14 to +8 V	P	wet (pH 7)
This work *	2020	SilTerra 180nm HV	-5.02 to 4.97 V (N) -10.97 to 1.50 V (P)	N and P	dry (gold)

*Measured across four chips (approximately 120 ISFETs).

For the chips under analysis, one can note close values for the charges trapped at the passivation layer for n-ISFETs and p-ISFETs on the same die. However, the inter-die fluctuation of the threshold voltage offset is relatively high, ranging from

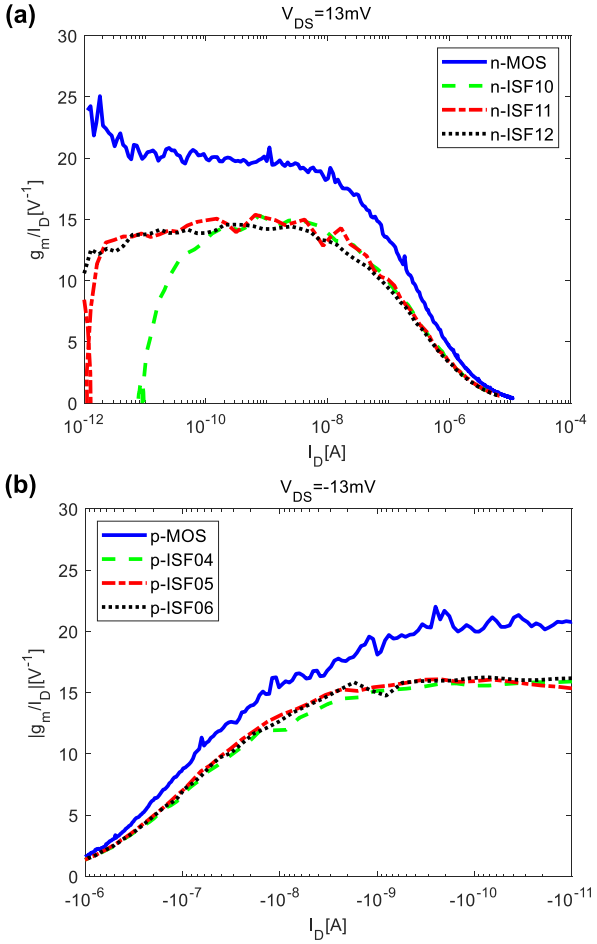


Fig. 9. Measured $g_m/I_D x I_D$ curves for the MOSFET and ISFETs of (a) n-type and (b) p-type.

approximately −8.5 V to 1.5 V, which is an indication of significant differences in the amount of passivation charges of each die.

Different methods have been reported to measure the threshold voltage offsets, usually using the conventional wet setup. The offset estimation includes removal of the passivation using laser [19] and reactive ion etching [23], and comparison between MOSFETs and ISFETs curves [24]. For example, offset estimations of −1.32 V for one n-ISFET [19] and inter-die averages between −1 V and 4 V for n-ISFETs with different geometries [24] have been reported. In contrast to the procedures employed in the researches described in [19], [23] and [24], the method presented herein is neither destructive nor affected by chemical potentials, and it can cover the whole die area, thus being suitable for the characterization of ISFET arrays.

TABLE III shows ISFETs threshold voltage dispersion obtained in this work compared with the values reported in the literature. It can be observed that the dispersion in the ISFETs threshold voltages of this work is comparable with those reported in other publications for different technologies.

The insertion of the mean values for the measured n_{mos} of n-MOSFETs and p-MOSFETs of 15 dies (2.50 and 2.01, respectively) in (10) results in slope factors of 2.82 and 2.23

TABLE IV
MEAN MEASURED AND THEORETICAL SLOPE FACTORS AND $(g_m/I_D)_{max}$ FOR ISFETS OF 3×3 CENTRAL ARRAYS OF FOUR DIES

	n-ISFETs		p-ISFETs	
	slope n	$(g_m/I_D)_{max}$	slope n	$(g_m/I_D)_{max}$
Measured (μ)	3.10	12.42	2.74	14.05
Theoretical	2.82	13.64	2.23	17.25

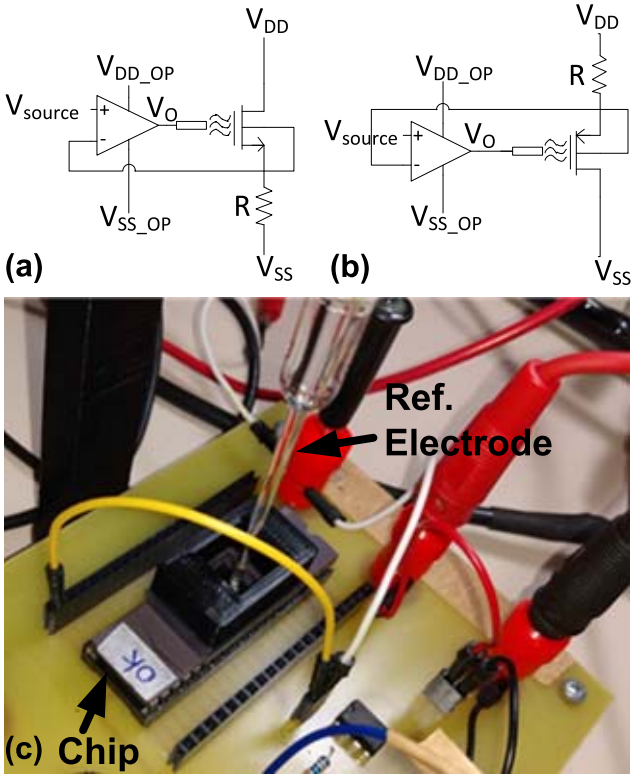


Fig. 10. Readout circuit used to measure pH sensitivity: (a) n-ISFET schematic. (b) p-ISFET schematic. (c) Implementation.

for the n-ISFETs and p-ISFETs, respectively. The increase in the slope factor (n) decreases the maximum transconductance efficiency ($(g_m/I_D)_{max}$), according to the following equation [14], [27]:

$$(g_m/I_D)_{\max} = \frac{1}{n\phi_t} \tag{21}$$

As expected, the transconductance-to-current ratios of the n-type and p-type ISFETs are smaller than those of the nMOS and pMOS transistors, as shown in Fig. 9.

TABLE IV shows the mean values obtained from the measurements and the theoretical values for the slope factor and $(g_m/I_D)_{max}$ for ISFETs of four chips in the 3×3 central array (devices 04-12, for better matching). The differences between the measured and theoretical values indicate possible capacitance deviations from the typical values used for the calculations.

In this design the passivation capacitance is dominant in relation to the oxide capacitance ($C_{pass} \approx 5C_{ox}$) and thus the slope factor and, consequently, the g_m/I_D characteristics of the ISFETs and MOSFETs are very close, as can be inferred from (10). Therefore, making the passivation capacitance dominant over the oxide capacitance results in an ISFET with a higher g_m/I_D value, close to that of a MOSFET [19].

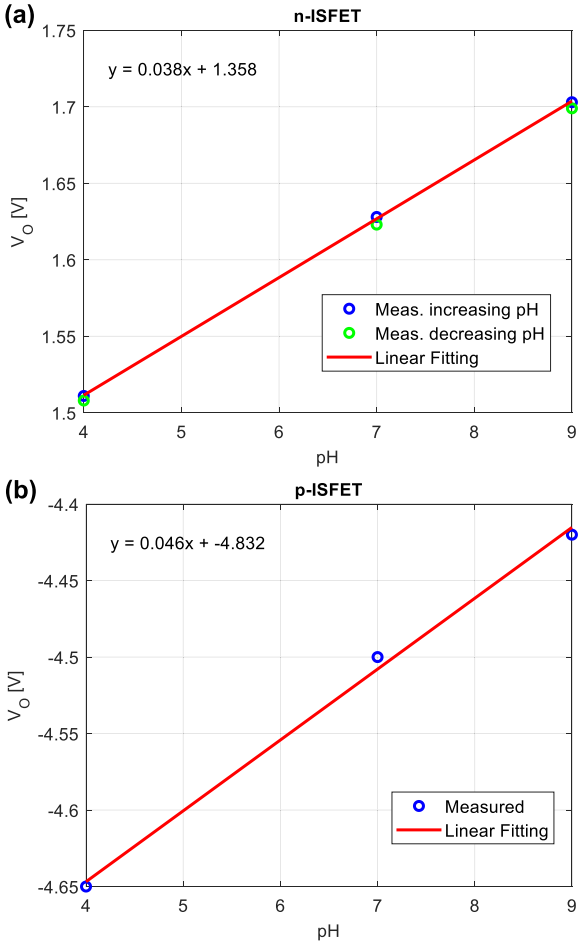


Fig. 11. pH sensitivity: (a) n-ISFET. (b) p-ISFET.

A discrete readout circuit was built to measure the pH sensitivities of both p- and n-channel ISFETs (Fig. 10). Measurements were taken over one minute for each sample of 650 μL of pH (4, 7, and 9) buffers. The ISFET was biased with a tiny Ag/AgCl reference electrode. A large chamber (glued at the top of the chip) and an electrode support were 3D printed in the Laboratório de Prototipagem/Fiocruz-PR. After each measurement, the chip was cleaned twice. The cleaning process consisted in (i) immersing the top of the chip with Mili-Q water during 1 minute, (ii) removing the cleaning solution, (iii) drying the top of the with a wiper, and (iv) letting it dry for 1 more minute.

Wet tests indicated a sensitivity of 38 mV/pH for an n-ISFET of one chip and 46 mV/pH for a p-ISFET of another chip (Fig. 11), which are close to the values obtained from simulations in our previous work [18]. The n-ISFET was measured by both increasing and decreasing values of pH, while the p-ISFET was measured only for increasing values of pH.

After several hours of testing, we were faced with unstable responses, which prevented us to characterize the full array of each chip.

The readout circuit was designed to generate a current I_D of 8 μA, using the following parameters: $V_{DD\_OP} = -V_{SS\_OP} = 15$ V, $V_{DD} = -V_{SS} = 2.5$ V, $V_{source} = 0$ V, $R = 300$ kΩ and the TL072 for the operational amplifier. Since $I_D = I_S.i_f$ for a saturated device, and knowing that the average specific current measured in 4 chips using the dry test ($Is = 200$ nA for n-ISFETs and $Is = 55$ nA for p-ISFETs) the corresponding inversion levels (i_f) are 40 and 145 for the n-ISFET and the p-ISFET, respectively. Using once again the UICM, eq. (5), the output voltage (V_O), which is the gate voltage of the ISFET, is given by:

$$V_O = V_{TISF} + n_{ISF}\phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right] + V_{source} \quad (22)$$

Using the measured values of n_{ISF} (TABLE IV) and V_O at pH 7 (Fig. 11), results in $V_{TISF} = 1.13$ V and $V_{TISF} = -3.6$ V for the tested n-ISFET and p-ISFET, respectively. These values are within the measured V_{TISF} ranges using the dry test (TABLE III).

V. Conclusion

This paper proposes a dry test for the characterization of the design parameters of ISFETs. The dry test avoids the influence of both the chemical characteristics of the aqueous solutions and the reference electrode in the measurements. The *dry gate* was realized through a DC sputtered Au film for the electrical contact with the floating gate. The ISFETs were fabricated in a standard 180 nm high-voltage technology, and encapsulated using DIP40 and epoxy to create a chamber. Several n-type and p-type devices on different dies were measured. Comparison of measurements and simulation results using the ACM model adapted to the *dry gate* ISFET are in close agreement. Trapped charges were estimated by physically modelling the metalized ISFETs. The n-ISFETs and p-ISFETs of the same die presented, on average, a similar offset, mainly caused by the trapped charge. However, inter-die measurements of the trapped charge differed considerably. Wet tests on an n-ISFET and a p-ISFET of non-metalized chips indicated pH sensitivities close to expected values. The proposed dry test can be used as a complementary tool for ISFET analysis and characterization, since the conventional wet test is still needed for the full characterization, in particular to determine the pH sensitivity. Through the improvement of the metallization process and the external connection, the setup proposed herein could be extended to unpackaged devices resulting in a less expensive and more rapid characterization of ISFET parameters, such as the threshold voltage, trapped charges, and capacitive attenuation. Summarizing, the dry test introduced herein can be used for a separate analysis of the chemical and electrical contributions to ISFET characteristics.

Acknowledgment

The authors would like to thank the CEO M. Pessatti, Dr. W. Prodanov and other technical staff from Chipus for numerous technical discussions, Professor A. Pasa for post-processing advice, S. Maraschin and A. Schuck from ITT Chip for the epoxy chamber development, Dr. L. Blanes, M. Stracke, V. de Oliveira and G. Mendonça from Fiocruz-PR for the support during wet tests.

References

[1] A. Au, N. Moser, J. Rodriguez-Manzano, and P. Georgiou, "Live demonstration: A mobile diagnostic system for rapid detection and tracking of infectious diseases," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018. p. 1.

[2] P. Bergveld, "Development of an ion-sensitive solid-state device for neurophysiological measurements," *IEEE Trans. Biomed. Eng.*, vols. BME–17, no. 1, pp. 70–71, Jan. 1970.

[3] P. Bergveld, "Thirty years of ISFETOLOGY: What happened in the past 30 years and what may happen in the next 30 years," *Sens. Actuators B, Chem.*, vol. 88, no. 1, pp. 1–20, 2003.

[4] N. Moser *et al.*, "Live demonstration: A CMOS-based ISFET array for rapid diagnosis of the zika virus," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, p. 1.

[5] M. L. Pourciel-Gouzy, W. Sant, I. Humenyuk, L. Malaquin, X. Dollat, and P. Temple-Boyer, "Development of pH-ISFET sensors for the detection of bacterial activity," *Sens. Actuators B, Chem.*, vol. 103, nos. 1–2, pp. 247–251, Sep. 2004.

[6] B. Nemeth, M. S. Piechocinski, and D. R. S. Cumming, "High-resolution real-time ion-camera system using a CMOS-based chemical sensor array for proton imaging," *Sens. Actuators B, Chem.*, vols. 171–172, pp. 747–752, Aug. 2012.

[7] J. M. Rothberg *et al.*, "An integrated semiconductor device enabling non-optical genome sequencing," *Nature*, vol. 475, pp. 348–352, 2011.

[8] M. Kalofonou and C. Toumazou, "Semiconductor technology for early detection of DNA methylation for cancer: From concept to practice," *Sens. Actuators B, Chem.*, vol. 178, pp. 572–580, Mar. 2013.

[9] J. Bausells, J. Carrabina, A. Errachid, and A. Merlos, "Ion-sensitive field-effect transistors fabricated in a commercial CMOS technology," *Sens. Actuators B, Chem.*, vol. 57, nos. 1–3, pp. 56–62, Sep. 1999.

[10] N. Moser, L. Keeble, J. Rodriguez-Manzano, and P. Georgiou, "ISFET arrays for lab-on-chip technology: A review," in *Proc. 26th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2019, pp. 57–60.

[11] N. Moser, T. S. Lande, C. Toumazou, and P. Georgiou, "ISFETs in CMOS and emergent trends in instrumentation: A review," *IEEE Sensors J.*, vol. 16, no. 17, pp. 6496–6514, Sep. 2016.

[12] C. G. Jakobson, M. Feinsod, and Y. Nemirovsky, "Low frequency noise and drift in ion sensitive field effect transistors," *Sens. Actuators B, Chem.*, vol. 68, nos. 1–3, pp. 134–139, Aug. 2000.

[13] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld, "A novel description of ISFET sensitivity with the buffer capacity and double-layer capacitance as key parameters," *Sens. Actuators B, Chem.*, vol. 24, nos. 1–3, pp. 201–205, Mar. 1995.

[14] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. New York, NY, USA: Cambridge Univ. Press, 2010.

[15] S. Sinha, R. Mukhiya, R. Sharma, P. K. Khanna, and V. K. Khanna, "Fabrication, characterization and electrochemical simulation of AlN-gate ISFET pH sensor," *J. Mater. Sci., Mater. Electron.*, vol. 30, no. 7, pp. 7163–7174, Apr. 2019.

[16] R. F. Pierret, *Semiconductor Device Fundamentals* vol. 2. Reading, MA, USA: Addison-Wesley, 1996.

[17] A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York, NY, USA: Wiley, 1967.

[18] R. Wrege, M. C. Schneider, J. Goncalves Guimaraes, and C. Galup-Montoro, "ISFETs: Theory, modeling and chip for characterization," in *Proc. IEEE 10th Latin Amer. Symp. Circuits Syst. (LASCAS)*, Feb. 2019, pp. 109–112.

[19] P. Georgiou and C. Toumazou, "ISFET characteristics in CMOS and their application to weak inversion operation," *Sens. Actuators B, Chem.*, vol. 143, no. 1, pp. 211–217, Dec. 2009.

[20] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006.

[21] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2009.

[22] B. Kumar, B. K. Kaushik, and Y. S. Negi, "Perspectives and challenges for organic thin film transistors: Materials, devices, processes and applications," *J. Mater. Sci., Mater. Electron.*, vol. 25, no. 1, pp. 1–30, Jan. 2014.

[23] N. Moser, C. Panteli, K. Fobelets, and P. Georgiou, "Mechanisms for enhancement of sensing performance in CMOS ISFET arrays using reactive ion etching," *Sens. Actuators B, Chem.*, vol. 292, pp. 297–307, Aug. 2019.

[24] M. Sohbati and C. Toumazou, "Dimension and shape effects on the ISFET performance," *IEEE Sensors J.*, vol. 15, no. 3, pp. 1670–1679, Mar. 2015.
[25] M. J. Milgrew and D. R. S. Cumming, "Matching the transconductance characteristics of CMOS ISFET arrays by removing trapped charge," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1074–1079, Apr. 2008.
[26] Y. Liu, P. Georgiou, T. Prodromakis, T. G. Constandinou, and C. Toumazou, "An extended CMOS ISFET model incorporating the physical design geometry and the effects on performance and offset variation," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4414–4422, Dec. 2011.
[27] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge, U.K.: Cambridge Univ. Press, 2017.

Rodrigo Wrege received the B.E. degree in electrical engineering from the Federal Institute of Technology Sul-Rio-Grandense (IFSUL), Brazil, in 2015, the IC Brazil qualification in analog integrated circuits design from NSCAD Microeletronics, Brazil, in 2016, and the M.S. degree in electrical engineering from the Federal University of Santa Catarina (UFSC) in 2018, where he is currently pursuing the Ph.D. degree in electrical engineering.

Celso Peter received the B.S. degree in electrical engineering from Pontifical Catholic University, Porto Alegre, Brazil, in 1986. He is currently working with the Unisinos Semiconductor Institute (itt Chip) as a Coordinator. Expert in microelectronics and electronic manufacturing with large experience in industry, spent the last ten years as Quality, Process, and Engineering Manager. More than 20 years of experience in microelectronics in the areas of IC manufacturing process development, clean room technology, quality, and project management.

Bruno N. Wesling born in Grão-Pará, Brazil, in August 1993. He received the B.E. degree in electronic engineering and the M.S. degree in electrical engineering from the Federal University of Santa Catarina in 2017 and 2020, respectively.

Carlos R. Rambo (Member, IEEE) born in Porto Alegre, Brazil, in December 1970. He graduated in physics at the University of São Paulo, Brazil, in 1994. He received the Ph.D. degree in materials science and engineering from the University of São Paulo in 2001. He then worked as a postdoc at the University of Erlangen, Germany, from 2002 to 2005. He is an Associate Professor with the Department of Electrical and Electronic Engineering, Federal University of Santa Catarina, Brazil, where he works since 2010. He has been working on the development of hybrid nanostructured composites for electronic applications.

Márcio Cherem Schneider (Senior Member, IEEE) received the B.E. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina (UFSC), Brazil, in 1975 and 1980, respectively, and the Ph.D. degree in electrical engineering from the University of São Paulo, São Paulo, Brazil, in 1984. In 1976, he joined the Electrical Engineering Department, UFSC, where he is currently a Professor. In 1995, he spent a one-year sabbatical at the Electronics Laboratory of the Swiss Federal Institute of technology, Lausanne. In 1997 and 2001, he was a Visiting Associate Professor with Texas A&M University.

Carlos Galup-Montoro (Senior Member, IEEE) studied engineering sciences at the University of the Republic, Montevideo, Uruguay, and electronic engineering at the National Polytechnic School of Grenoble (INPG), France. He received the degree in electronics and the Ph.D. degree from INPG, in 1979 and 1982, respectively.

From 1982 to 1989, he worked at the University of São Paulo, Brazil. Since 1990, he has been with the Electrical Engineering Department, Federal University of Santa Catarina, Florianópolis, Brazil, where he is currently a Professor. In the second semester of the academic year 1997-1998, he was a Research Associate with the Analog Mixed Signal Group, Texas A&M University. He was a Visiting Scholar with UC Berkeley from 2008 to 2009 and with IMEP/INPG in the first trimester of 2017.