Analysis and Design of a Fully-Integrated Colpitts Oscillator Operating at Ultra-Low-Voltages

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Abstract — This paper presents an enhanced-swing Colpitts oscillator that operates from supply voltages below $4kT/q$. The oscillation frequency, start-up condition, and amplitude of oscillation were analyzed. The condition for the minimum voltage gain, extended to the minimum supply voltage, required for operation of the Colpitts oscillator is derived. Measurement results obtained for a prototype integrated in the IBM 130 nm technology demonstrate the operation of the oscillator with 86 mV of supply voltage.

***Index Terms*- Ultra-low-voltage circuits, ultra-low-voltage oscillators, MOSFET analog circuits, zero-VT transistor, energy harvesting.**

1. Introduction

Emerging applications like wireless sensor networks and implantable medical devices, which require self-powered solutions, have increased dramatically. Ambient energy-harvesting sources such as mechanical vibrations, thermal gradients, light or RF signals provide important alternatives for powering silicon-based electronics [1]. The voltage level available from ambient energy sources (excluding light) is generally below 100 mV. The operation of electronics at very low voltages results in advantages such as an increase in the time available for active operation and a reduction in the standby power of the circuit [2].

Ultra-low-voltage (ULV) oscillators are particularly useful for circuits powered by energy harvesting devices such as thermoelectric generators. In effect, the attainment of a dc supply voltage of the order of 500 mV or more for powering state-of-the-art electronics from very low dc voltages requires a time-varying signal usually obtained from an oscillator, as shown in the conceptual scheme of the ULV dc-dc converter in Fig. 1. However, the generation of oscillations from ultra-low voltages is extremely difficult [3], [4]. In recent years

some researchers have addressed this subject with the use of, for example, mechanical switches [3], a post-fabrication tuned oscillator [4], or bulky transformers [5]. Some works [5], [6], [7] have presented oscillators operating with supply voltages in the range of tens of millivolts using off-chip high-quality passive devices, but the design of fully-integrated oscillators operating from dc voltages of the order of 100 mV or down continues to be an unsolved problem.

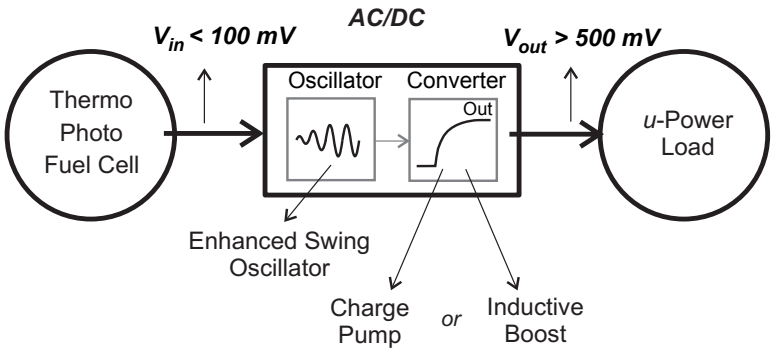


Fig. 1. Architecture of a DC step-up converter.

In this paper we present a fully-integrated Colpitts oscillator in which the inductors have a quality factor Q of around 10. The oscillator is capable of operating down to supply voltages below $4kT/q$. The oscillator employs a zero-threshold-voltage (zero-VT) MOS transistor due to its high drive capability at very low supply voltages. In order to increase the amplitude swing beyond the supply voltage and ground, we employed the Enhanced Swing Colpitts Oscillator (ESCO) [7][8].

The paper is organized as follows. Section 2 presents the oscillation frequency and start-up conditions for the enhanced swing Colpitts oscillator. In Section 4 we describe the oscillator design methodology and report experimental results. Section IV shows a comparison between our results and those reported for state-of-the-art oscillators, while Section V concludes the paper.

2. The Enhanced Swing Colpitts Oscillator (ESCO)

The schematic of the conventional Colpitts oscillator is given in Fig. 2. We will discuss some of its limitations for ultra-low-voltage applications before analyzing the enhanced swing Colpitts oscillator (ESCO).

When the voltage swing is large and the current source enters the triode region for a fraction of the period, the voltage drop across the current source can be close to zero. Thus, the minimum voltage at the source and also at the drain is around zero volts (ground level). Consequently, the maximum drain voltage for a sinusoidal peak-to-peak voltage swing is less than $2V_{DD}$, which is an important drawback of the Colpitts oscillator in Fig. 2.

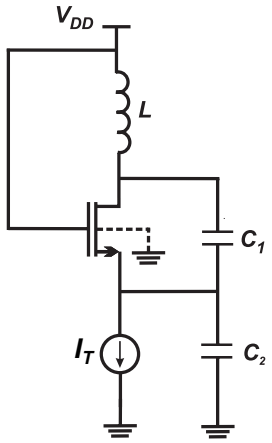


Fig. 2. Conventional Colpitts oscillator (notation for the current source: I_T).

In order to circumvent the limitations of the conventional Colpitts oscillator, one can use the ESCO [8] shown in Fig. 3. This circuit is capable of boosting the oscillation amplitude beyond the supply rails. In the small-signal model of the ESCO of Fig. 3, g_{ms} and g_{md} represent the source and drain transconductances [9]. The transistor capacitance C_{gs} can be absorbed into C_2. G_1 and G_2 model the losses of inductors L_1 and L_2, respectively.

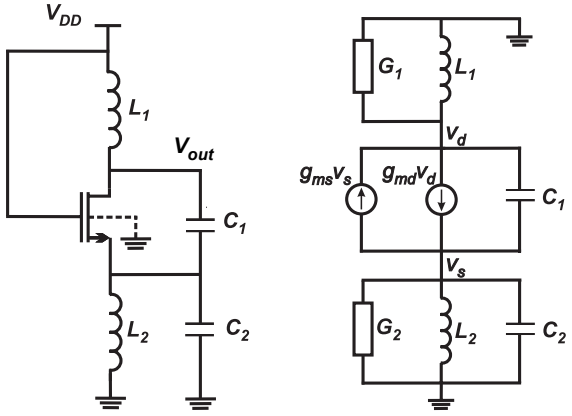


Fig. 3. Schematic of the ESCO and its small-signal model

The exact analysis of the ESCO, which is somewhat complicated, is carried out in Appendix A where the oscillation frequency is calculated as

$$\omega_0^2 L_1 C_{eq} = 1 \tag{1}$$

with C_{eq} given in Appendix A.

In order to find the requirements regarding the transistor parameters for oscillation, we will first model the circuit in Fig. 3. using the relationship between the source and drain voltages.

A. Relationship between source and drain voltages

In order to develop a simple model for the oscillator we make the following assumptions: (i) As in [6], the Q value of the resonator is so high that all current harmonics other than the fundamental are filtered out; thus, both drain and source voltages are sinusoidal signals; (ii) the non-linear capacitances are a small part of

the nodal capacitances; for practical purpose they are assumed to be independent of dc voltages.

A graphical interpretation of the voltage gain V_d/V_s can be obtained as follows. Disregarding the losses of the passive devices and the transistor current, the Kirchhoff's current law (KCL) applied to the small-signal circuit of Fig. 3 leads to equations (2) and (3)

$$\frac{V_d}{V_s} = \frac{L_1}{L_2}\left(\omega^2 C_2 L_2 - 1\right) \tag{2}$$

$$\frac{V_d}{V_s} = 1 + \frac{C_2}{C_1}\left(1 - \frac{1}{\omega^2 C_2 L_2}\right) \quad . \tag{3}$$

These two equations, which give the relationship between the drain and source potentials in terms of the angular frequency ω are shown in Fig. 4. As can be seen in the figure, for a specified L_1/L_2 ratio the curves intersect at two points. However, as stated in the Appendix A, only the higher frequency, which results in a positive V_d/V_s ratio, is a valid solution.

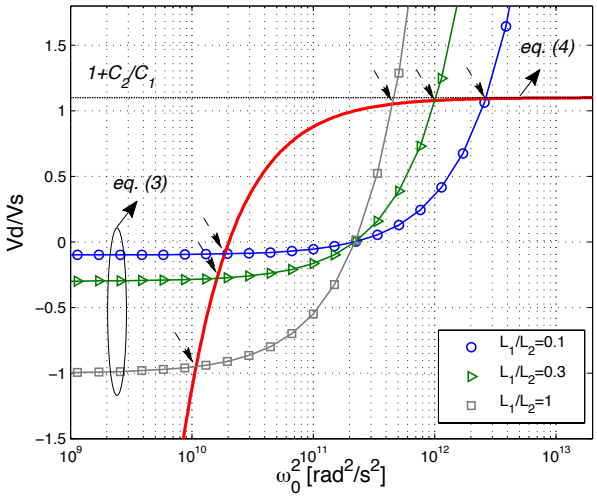


Fig. 4. V_d/V_s ratio in terms of ω^2, for the cases where L_1/L_2 = 0.1, 0.3, and 1, with C_2/C_1=0.1.

As is clear from Fig. 4, as a first order approximation we can consider the voltage ratio V_d/V_s given by the capacitive divider C_1-C_2 as $V_d/V_s = 1+C_2/C_1$ [11], but this approximation is unsuitable for design since the effect of inductors L_1 and L_2 is not modeled.

A much better approximation for the voltage ratio [6], [10] is

$$\frac{V_d}{V_s} = a \cong -\frac{L_1}{L_2}\left(1 - \omega_0^2 L_2 C_2\right) \quad . \tag{4}$$

As we will see in the following, to operate the ESCO with high swing for low supply voltages the value of a must be chosen relatively close to unity, which is achieved when $C_2/C_1 \ll 1$. Using the value of ω_0 calculated in Appendix A, the value of a when it is close to unity is given [6] by

$$a_{C_2 \ll C_1} = 1 + \frac{C_2/C_1}{1 + L_1/L_2} \quad . \tag{5}$$

After calculating the value of a, we can model the oscillator circuit as in Fig. 5. [12].

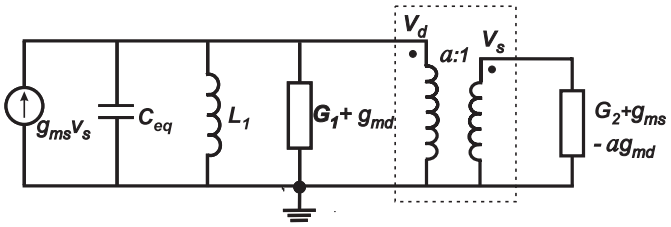


Fig. 5. ESCO with capacitive divider modeled as a transformer.

B. Minimum transistor gain required for oscillation start-up

For the occurrence of oscillation, the transistor must be able to compensate the losses of the passive components. Referring the conductance connected to the secondary winding to the primary winding, the requirement for oscillation is written as

$$g_{ms}V_s = g_{ms}\frac{V_d}{a} > \left[G_1 + g_{md} + \frac{1}{a^2}\left(G_2 - ag_{md} + g_{ms}\right)\right]V_d \quad , \tag{6}$$

or, equivalently

$$g_{ms} > ag_{md} + \frac{a^2 G_1}{(a-1)} + \frac{G_2}{(a-1)} \quad . \tag{7}$$

The value a_{opt} which minimizes the right hand side term of Eq. (7) is

$$a_{opt} = 1 + \sqrt{\frac{G_1 + G_2}{G_1 + g_{md}}} \quad . \tag{8}$$

From equations (5) and (8), after selecting g_{md}, L_1 and L_2, the ratio C_2/C_1 can be determined. Assuming that the quality factors of the inductors are equal, *i.e.* $G_1/G_2=L_2/L_1$, the value of C_2/C_1 that minimizes the right hand side of Eq. (7) is

$$\left.\frac{C_2}{C_1}\right|_{opt} = \left(1 + \frac{L_1}{L_2}\right)^{3/2} \sqrt{\frac{G_1/g_{md}}{1 + G_1/g_{md}}} \quad . \tag{9}$$

The substitution of Eq. (8) into Eq. (7) yields the optimized minimum value for the intrinsic gain

$$\frac{g_{ms}}{g_{md}} > 1 + 2\frac{G_1}{g_{md}} + 2\sqrt{\left(1 + \frac{L_1}{L_2}\right)\left(1 + \frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}} \quad . \tag{10}$$

C. Minimum supply voltage required for oscillation start-up

The minimum supply voltage required for oscillation start-up should be such that the condition imposed by inequality (10) is satisfied, *i.e.* the transistor gain g_{ms}/g_{md} must be high enough to compensate the losses in the passive components. The solution for the minimum supply voltage can be obtained using, for example, the MOSFET model described in [9] together with the limit imposed by inequality (10). Assuming the dc values $V_S=V_B=0$ and $V_G=V_D=V_{DD}$, for a fixed g_{md} the minimum V_{DS} (= V_{DD}) is reached by combining the expression for the drain-source voltage (V_{DS}) given by [9]

$$\frac{V_{DS}}{\phi_t}=\sqrt{1+i_f}-\sqrt{1+i_r}+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)=\frac{\phi_t}{2I_S}\left(g_{ms}-g_{md}\right)+\ln\frac{g_{ms}}{g_{md}} \tag{11}$$

and Eq. (10) of the minimum transistor gain g_{ms}/g_{md}. In (11), where I_S refers to the specific current, while i_f and i_r are the forward and reverse inversion levels. Thus, for $G_1/G_2=L_2/L_1$, we can write

$$\frac{V_{DD}}{\phi_t}>\frac{\phi_t}{2I_S}g_{md}\left(2\frac{G_1}{g_{md}}+2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}}\right)+\ln\left(1+2\frac{G_1}{g_{md}}+2\sqrt{\left(1+\frac{L_1}{L_2}\right)\left(1+\frac{G_1}{g_{md}}\right)\frac{G_1}{g_{md}}}\right) \tag{12}$$

Under the assumptions $C_2/C_1<<1$, operation of the MOSFET in the subthreshold region, and negligible losses in the inductors, equations (5), (7) and (11) can be combined to obtain the minimum supply voltage of the ESCO as

$$\frac{V_{DD}}{\phi_t}>\ln\left(1+\frac{C_2/C_1}{1+1/k_L}\right)\cong\frac{C_2/C_1}{1+L_1/L_2} \tag{13}$$

Theoretically, as Eq.(13) shows, the ESCO can oscillate at very low supply voltages. In practice, however, the unavoidable losses, the parasitic capacitance of the drain node and operation of the transistor in moderate or strong inversion will contribute to increasing the value of V_{DD} given by Eq. (13). Some simulated and experimental results for the minimum supply voltage, including losses and considering operation of the transistor in moderate inversion, will be given in Section III.

D. Amplitude of oscillation

Assuming, as in [6], that the Q value of the resonator is high enough for all current harmonics other than the fundamental to be filtered out and that the source voltage is a fraction $1/a$ of the drain voltage, we can write

$$v_D=V_{DD}+A_d\cos\theta \tag{14}$$

$$v_S=\frac{1}{a}A_d\cos\theta \tag{15}$$

Therefore, the minimum value of v_{DS} is

$$v_{DS,\min}=V_{DD}-A_d\left(1-1/a\right) \tag{16}$$

For the ESCO in Fig. 3. , assuming that the drain current $i_D \geq 0$ for all time we should have[1] $v_{DS} \geq 0$, which implies that

$$V_{DD} - A_d\left(1 - 1/a\right) \geq 0 \quad . \tag{17}$$

Therefore, in the limit case, the maximum value of the amplitude of oscillation is

$$A_{d,\max} = \frac{V_{DD}}{1 - 1/a} \quad . \tag{18}$$

As we will see below, the value of a can be relatively close to unity, which means that the ESCO can potentially provide amplitude of oscillation which is several times higher than the supply voltage.

E. Effect of the output load

For some applications, the oscillator is loaded by a lossy circuit. The effect of this load on the minimum transistor gain (g_{ms}/g_{md}) required to start up the oscillator can be taken into account. Considering the ESCO shown in Fig. 6, with the output load modeled as a conductance G_O, the minimum g_{ms}/g_{md} of the transistor to start-up the oscillator can be rewritten from Eq. (7) as

$$\frac{g_{ms}}{g_{md}} > a + \frac{a^2}{(a-1)}\frac{G_1 + G_O}{g_{md}} + \frac{1}{(a-1)}\frac{G_2}{g_{md}} \quad . \tag{19}$$

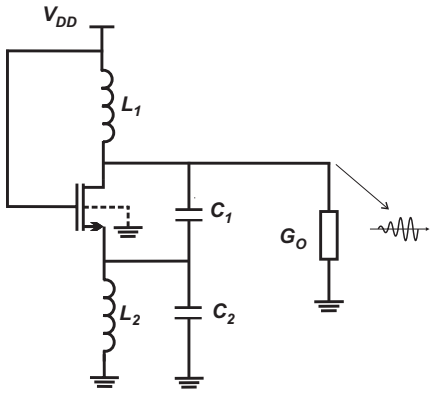


Fig. 6. Schematic diagram of the ESCO with the load modeled as a conductance G_O.

The curves in Fig. 7. represent the gain g_{ms}/g_{md} calculated from Eq. (19) for the case in which $G_1 = G_2 = G$, $L_2 = 2L_1$ and $C_1 = 2C_2$. As is clear from Fig. 7. , the influence of G_O on the minimum transistor gain required for oscillation can be mitigated by increasing g_{md} through transistor widening.

[1] In fact, the value of v_{DS} can be negative for a short time interval.

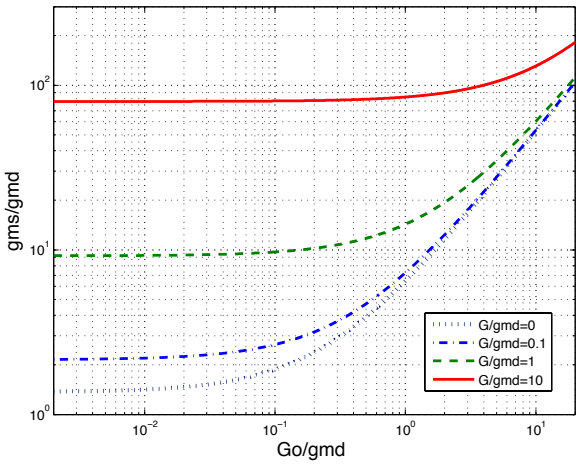


Fig. 7. Calculated minimum transistor gain, from Eq. (19) in terms of the output conductance G_O.

3. DESIGNS AND RESULTS

Based on the analysis presented in Section II, an ESCO was designed for operation at 800 MHz. High-quality integrated inductors (Q>10) with the inductances selected according to maintain the specified oscillation frequency, with the inductances indicated in Fig. 8. , were designed. The oscillator employs a wide zero-VT transistor (W/L=1500µm/420nm) to provide enough drive capability to compensate the inductor losses. The transistor was built as a parallel association of 300x5µm-width transistors.

It is worth noting that the drain transconductance of the zero-VT transistor operating at low voltages with V_G=V_D is almost bias-independent. To demonstrate this, in a way similar to what has been done in [10], consider the transistor model described in [9], at the same bias voltages of the MOSFET in Fig. 3. , *i.e.* V_S=V_B and V_G=V_D=V_{DD}. Assuming that n=1, the unified current control model [9] applied to the drain terminal yields

$$\frac{-V_T}{\phi_t} = \left[\sqrt{1+i_r} - 2 + \ln\left(\sqrt{1+i_r} - 1\right)\right] \quad . \tag{20}$$

Thus, the reverse inversion level (i_r) is, at least for low voltages, almost independent of the gate voltage. If, in addition, the value of V_T is exactly zero, the solution of (20) corresponds to i_r = 3, and the value of g_{md} calculated from [9]

$$g_{md} = -\frac{\partial I_D}{\partial V_D} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_r} - 1\right) \tag{21}$$

is g_{md}=$2I_S$ / ϕ_t , where I_S is the specific current of the transistor defined in [9]. Therefore, in a first-order approximation, the g_{md} value is dependent only on the specific current I_S, and the thermal voltage ϕ_t. This result is used for a back-of-the-envelope calculation of g_{md}.

Once the inductors and transistor parameters are known, the capacitive feedback can be readily determined from Eq. (9), which, in our design, yields an optimum capacitive ratio ≈ 0.7. From (1) and (A4), after some adjustment to account for parasitic capacitances due to layout, values of C_1=6 pF and C_2=3.5 pF were selected.

A schematic diagram of the oscillator is shown in Fig. 8. A tapered inverter chain was chosen for the

buffer since it presents a small capacitive load to the oscillator. In Fig. 8. the inductor parameters (simulated at 800 MHz) and the MOSFET capacitances are indicated. The layout of the circuit, as well as a micrograph of the chip implemented in the IBM 130 nm technology, is shown in Fig. 9.

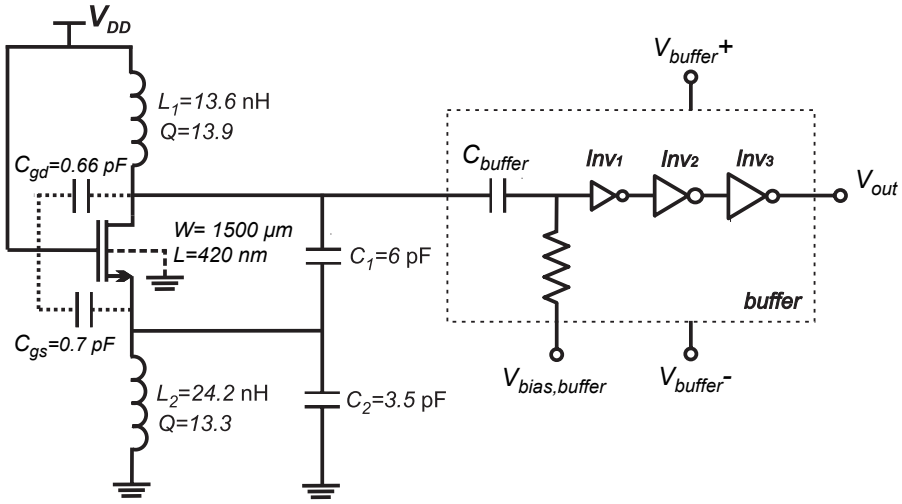


Fig. 8. Schematic diagram of the ESCO along with the voltage buffer.

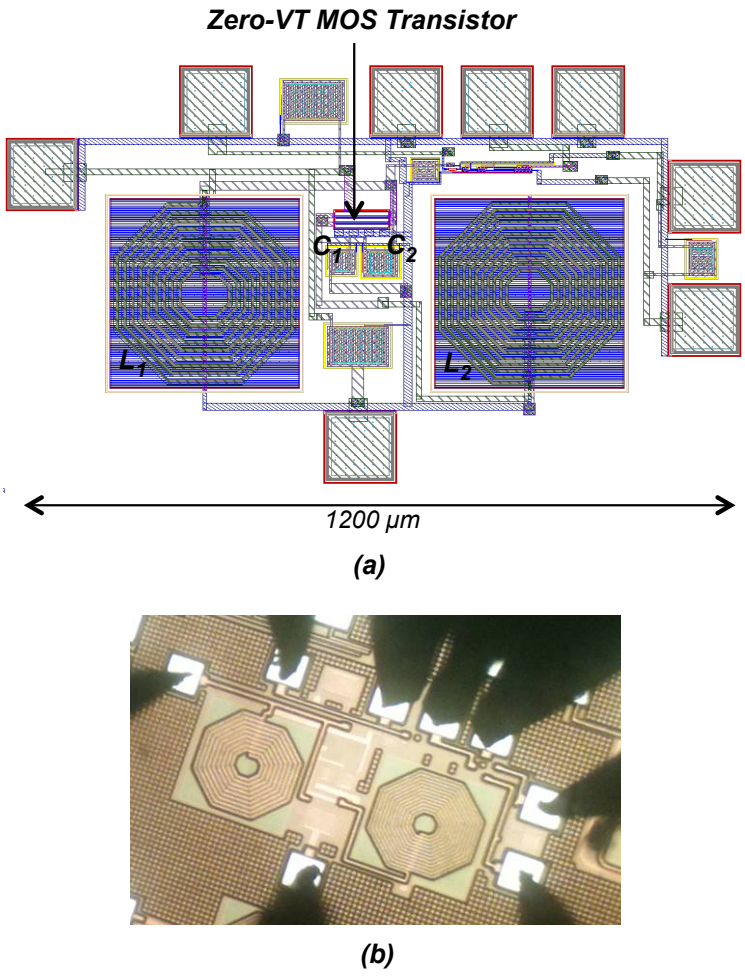


Fig. 9. (a) Layout and (b) micrograph of the fully-integrated ESCO fabricated in the IBM 130 nm technology.

A. Simulations

Post-layout simulations were run for the ESCO of Fig. 8. The minimum supply voltage to start up the oscillator and the oscillation frequency (at the start-up) simulated with the corners of the technology are shown in Fig. 10. *SS* means slow NMOS and PMOS, *FF* means fast NMOS and PMOS and *TT* means typical NMOS and PMOS. *FFF* and *SSF* are the functional corner parameter values that predict the +/- 3-σ limit of some critical electrical parameters such as *Idsat* and *Vtsat*, both defined by the technology. Except for the corner *FFF*, the simulation results show that $V_{DD,min}$ is less than 100 mV. Also, the maximum frequency deviation relative to the *TT* case is less than 5%.

The variations in the amplitude and frequency of the ESCO in terms of the supply voltage are illustrated in Fig. 11. As can be seen in the curves obtained from the post-layout, for V_{DD} = 100 mV the oscillator output peak-to-peak voltage is around 350 mV.

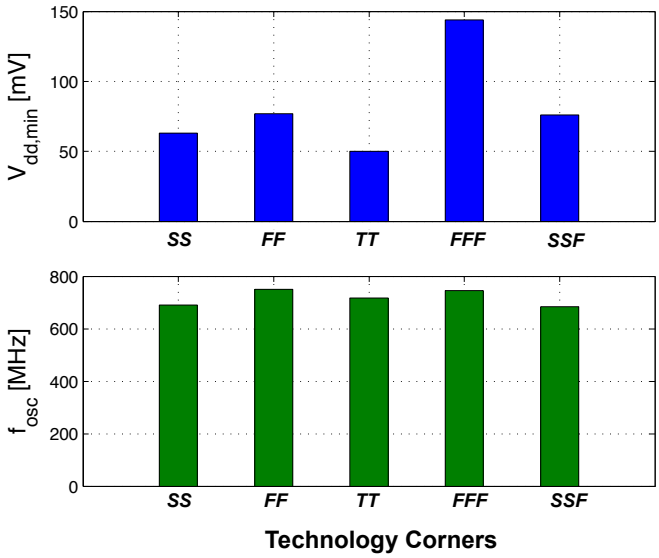


Fig. 10. Post-layout simulations of the minimum supply voltage to start-up the ESCO of Fig. 8. for the technology corners.

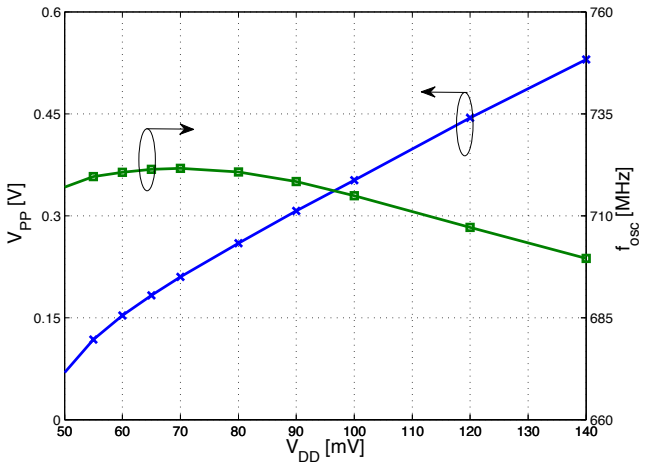


Fig. 11. Simulated (post layout) peak-to-peak output voltage and frequency of the ESCO of Fig. 8. in terms of V_{DD}.

B. Measurements

The setup used to test the oscillator is shown in Fig. 12. As can be seen in this figure, the circuit can oscillate with supply voltages below 100 mV, starting up from around 86 mV, while the calculation based on Eq. (12) gives a minimum supply voltage of 56 mV. The main results obtained with the fully-integrated ESCO are summarized in Table I. The calculated values were taken from the simulated parameters detailed in Fig. 8. , without taking into account the parasitic elements due to the layout. The spectrum for the oscillator biased at V_{DD}=86 mV is shown in Fig. 13.

Table I. Summary of the main results for the fully-integrated ESCO.

	Calculated	*Post-layout simulated*	*Experimental*
Frequency	850 MHz	715 MHz	706 MHz
$V_{DD,min}$	56 mV	50 mV	86 mV
P_{DC}*	-	0.165 mW	0.21mW

* P_{DC} measured at V_{DD} = 100 mV

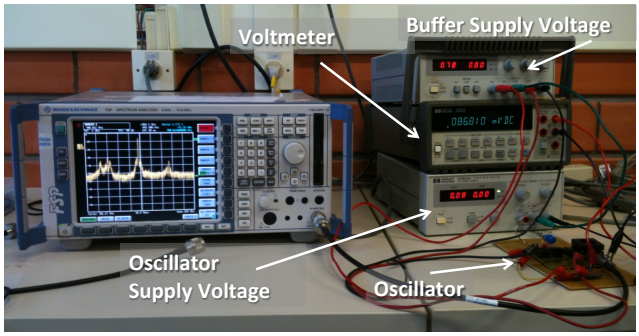


Fig. 12. Setup used to test the fully-integrated ESCO.

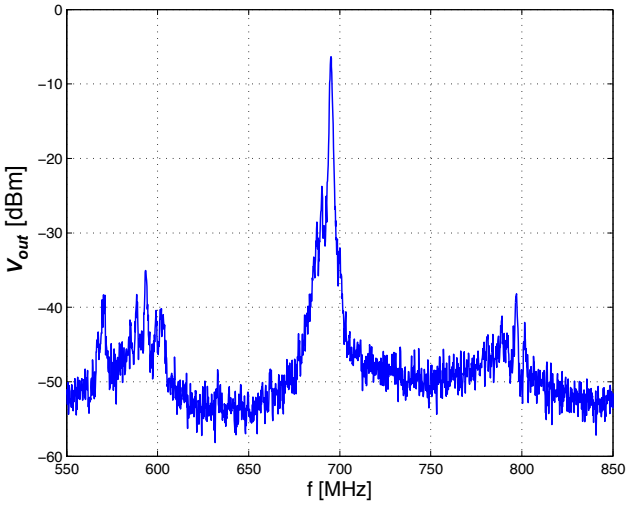


Fig. 13. Spectrum for the ESCO for V_{DD} = 86 mV.

The extracted transconductances of the zero-VT transistor biased with $V_G=V_D=V_{DD}$ and $V_S=V_B$ are shown in Fig. 14. As can be seen, for low supply voltages ($V_{DD}<$ 100 mV) the drain transconductance is almost bias-independent. Also, it is worth noting that the transistor presents a gain of $g_{ms}/g_{md} > 2$ when operating from voltages above 50 mV. In comparison with the simulation, the experimental value of g_{md} is around two times higher. This difference can be mainly assigned to a difference in the value of V_T of the simulated device with respect to the real device.

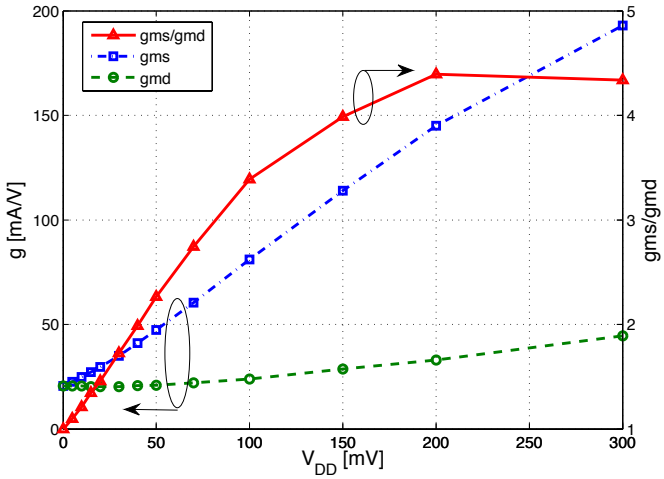


Fig. 14. Experimental transconductances of the zero-VT transistor (W/L=300x5µm/0.48µm), for $V_S=V_B=0$ and $V_G=V_D=V_{DD}$.

4. DISCUSSION

In recent years, many papers on ultra-low-voltage oscillators have been published. References [5], [13], [14] and [15] present fully integrated oscillators operating at a few GHz and with supply voltages of hundreds of mV, as can be seen in Table II. CMOS ring oscillators operating around or below 100 mV of V_{DD} using a post-fabrication tuned oscillator or an experimental process employing NMOS and PMOS zero-VT transistors are presented in [4] and [16], respectively. In [17] a fully integrated oscillator that starts up from 56 mV of supply voltage, at the cost of the area of seven inductors, is presented.

The minimum V_{DD} for sustained oscillations of the ESCO presented herein, 86 mV, is considerably higher than the value of 20 mV in reference [7], but it is worth noting that the Colpitts oscillator in [7] uses high-quality off-the-shelf components and oscillates at 100 kHz whereas the oscillator presented here is fully integrated and operates at 700 MHz. A comparison between fully-integrated oscillators operating at ultra-low-voltages in some representative papers available in the technical literature is presented in Table II. As can be seen, we present a fully-integrated oscillator which, besides starting up at a supply voltage of 86 mV, is implemented in CMOS standard technologies without the need for post-fabrication tuning.

Table II. Comparison between some state-of-the-art fully-integrated oscillators operating at ultra-low voltages.

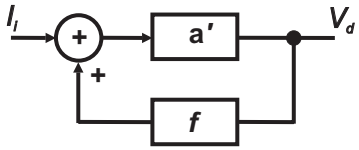
	$V_{DD,min}$	f_{osc}	P_{DC}	*Tech.*
[4]	95 mV	330 kHz	-	65 nm
[5]	400 mV	4.9 GHz	1.92 mW	0.13 µm
[13]	400 mV	5.6 GHz	1.1 mW	0.18µm
[14]	350 mV	1.4 GHz	1.46mW	0.18 µm
[15]	300 mV	3.58 GHz	0.22 mW	0.13 µm
[16]	200 mV	20 MHz	-	Experimental technology
[17]	56 mV	500 MHz	-	0.13 µm
This work	86 mV	700 MHz	0.21 mW	0.13 µm

5. CONCLUSIONS

We have presented a fully-integrated prototype of a Colpitts oscillator in which the active component is a zero-VT MOSFET. The high transconductance-to-capacitance ratio of the zero-VT MOSFET at low supply voltages makes it a very powerful component in ULV applications. The Colpitts oscillator designed in this study operates down to a supply voltage of 86 mV. The circuit functionality was verified in a prototype fabricated in the IBM 130 nm CMOS technology. Experimental results have shown that the circuit is suitable for energy harvesting applications, either as a start-up oscillator, for instance, to provide a kick-up input voltage for a boost converter, or to deliver the input signal to a voltage multiplier to energize low-power circuits.

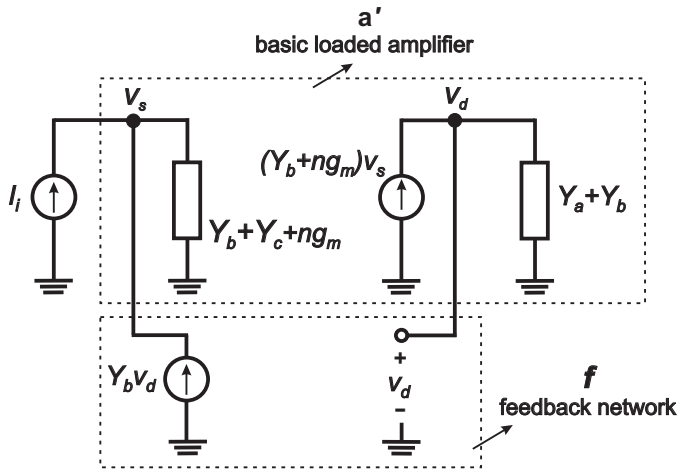
Appendix A – Feedback analysis of the ESCO

An accurate analysis of the Colpitts oscillator can be carried out with the use of feedback theory. In order to analyze the ESCO, it was represented in the standard block diagram in Fig. A1. Parameters a' and *f* of this figure are determined from the ideal feedback amplifier of Fig. A2 (shunt-shunt configuration), which is an appropriate representation of the oscillator in Fig. 3.



$$A = \frac{V_d}{I_i} = \frac{\mathrm{a}'}{1 - \mathrm{a}'f}$$

Fig. A1. Ideal feedback configuration of an amplifier.



$$Y_a = G_1 + \frac{1}{sL_1} + sC_p \qquad \text{a}' = \frac{Y_b + ng_m}{(Y_a + Y_b)(Y_b + Y_c + ng_m)}$$

$$Y_b = g_{md} + sC_1 \qquad f = Y_b$$

$$Y_c = G_2 + \frac{1}{sL_2} + sC_2$$

Fig. A2. Small-signal model of the Colpitts oscillator of Fig. 3.

The open loop gain a'f is given by

$$\text{a}'f = \frac{\left(g_{md} + sC_1 + ng_m\right)}{\left(G_1 + \frac{1}{sL_1} + sC_p + g_{md} + sC_1\right)} \text{x} \frac{\left(g_{md} + sC_1\right)}{\left(ng_m + G_2 + \frac{1}{sL_2} + sC_2 + g_{md} + sC_1\right)}, \tag{A1}$$

where C_p represents the sum of all capacitances between the drain node and the ac ground.

Taking into account the Barkhausen criterion, a necessary condition for oscillation is

$$\omega_0^4 L_1 L_2 C_1 \left(C_p + C_2 + \frac{C_p C_2}{C_1}\right) - \omega_0^2 L_1 L_2 \left(G_1 n g_m + G_1 G_2\right) - \omega_0^2 L_1 L_2 \left(G_1 g_{md} + G_2 g_{md} + \frac{C_p + C_1}{L_2} + \frac{C_1 + C_2}{L_1}\right) + 1 = 0, \tag{A2}$$

which gives the solutions for the frequency of oscillation shown in (A3), where $\Delta C = L_1\left[G_1\left(ng_m + g_{md} + G_2\right) + G_2 g_{md}\right]$ is an equivalent capacitance that represents the effects of the losses as well as those of the transistor on the resonant frequency. ω_o is independent of tank losses and, consequently, is only dependent on the capacitor and inductance values if $\Delta C << C_1 + C_2 + C_1/k_L$. In fact, two solutions can be found for the frequency of oscillation; however, only the high frequency of oscillation is possible. The reason for this is that, for the lower frequency of oscillation, the source and drain voltages are 180^o out-of-phase.

Since the transistor voltage gain V_d/V_s is positive, the loop gain will be negative at the lower frequency; thus, the circuit cannot oscillate at the lower frequency.

$$\omega_0^2 L_1 C_1 = \frac{\dfrac{C_1+C_p}{C_1} + k_L \dfrac{C_1+C_2+\Delta C}{C_1} \pm \sqrt{\left(k_L \dfrac{C_1+C_2+\Delta C}{C_1} - \dfrac{C_1+C_p}{C_1} \right)^2 + 4k_L \left[\dfrac{C_1^2 + \left(C_1+C_p\right)\Delta C}{C_1^2} \right]}}{2k_L \left[\dfrac{C_2+C_p}{C_1} + \dfrac{C_2 C_p}{C_1^2} \right]} \quad \text{(A3)}$$

For negligible C_p and ΔC, Eq. (A3) reduces to

$$\omega_0^2 L_1 C_2 = \frac{1 + k_L \left(1 + \dfrac{C_2}{C_1}\right) + \sqrt{\left[k_L \left(1 + \dfrac{C_2}{C_1}\right) - 1 \right]^2 + 4k_L}}{2k_L} \quad . \quad \text{(A4)}$$

Since $\omega_0^2 L_1 C_{eq} = 1$ it follows from (A4) that

$$C_{eq} = \frac{(C_1+C_2)\dfrac{L_2}{L_1} + C_1 - \sqrt{\left[(C_1+C_2)\dfrac{L_2}{L_1} - C_1 \right]^2 + 4\dfrac{L_2}{L_1} C_1^2}}{2} \quad \text{(A5)}$$

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