Federal University of Santa Catarina – Electrical Engineering Department

AN ULTRA-LOW-POWER SELF-BIASED CURRENT REFERENCE

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Contents

1. Introduction

- **References:**
  - **Voltage:** $V_{ref} \rightarrow \phi_t, V_{G0}$
  - **Current:** $I_{ref} \rightarrow V_{ref}/R, \mu C'_{ox} \phi_t^2$

  Required for:

- A/D and D/A conversion
- Biasing (analog and digital circuits)

1. Introduction

Objective:

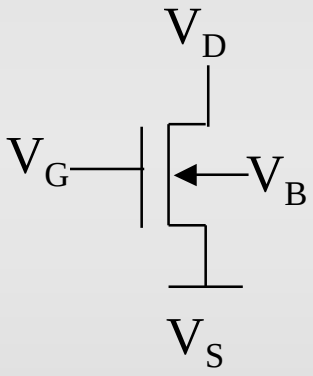
- **Design a CMOS current reference for low-voltage & ultra-low-power applications**

Characteristics of the current reference:

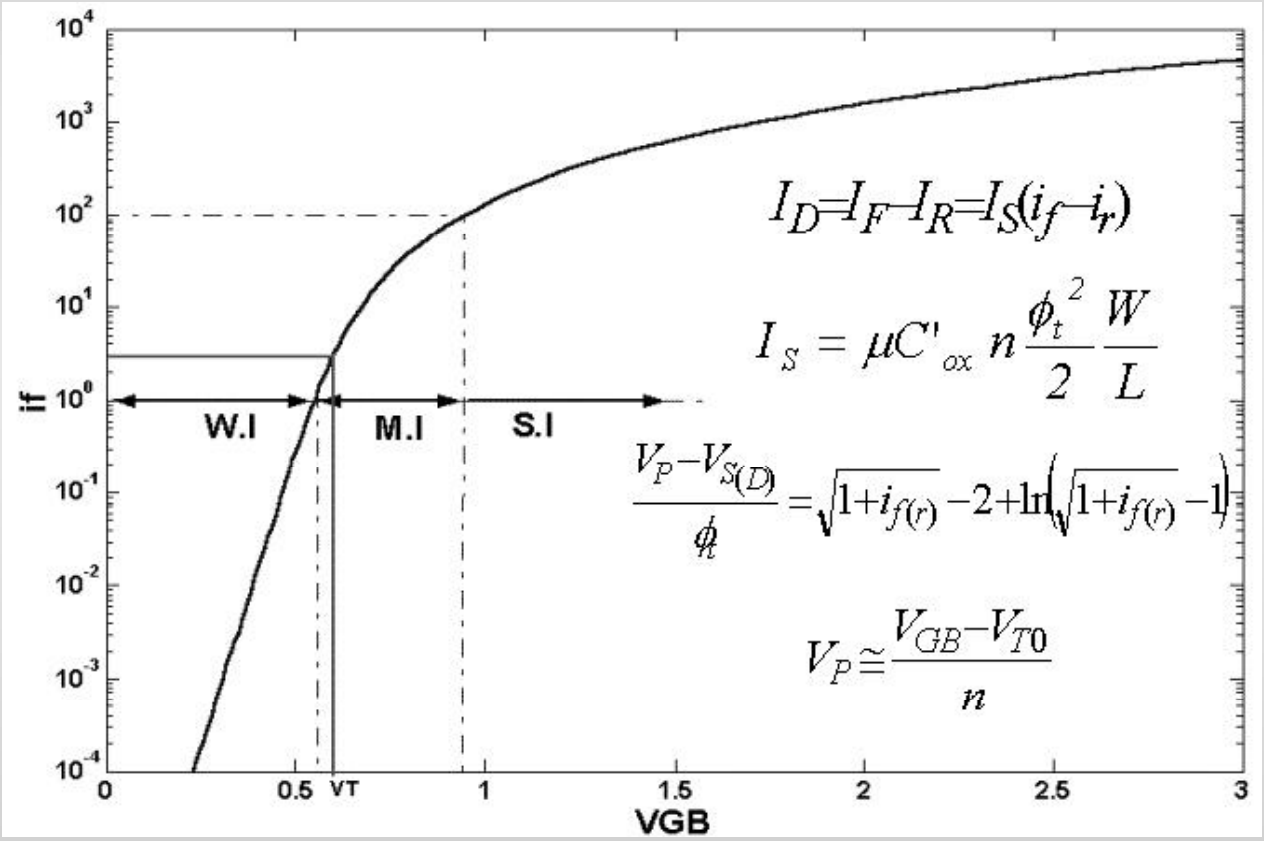
1. **Autonomous;**
2. **Low consumption;**
3. **Simple to design.**

2. Basic concepts

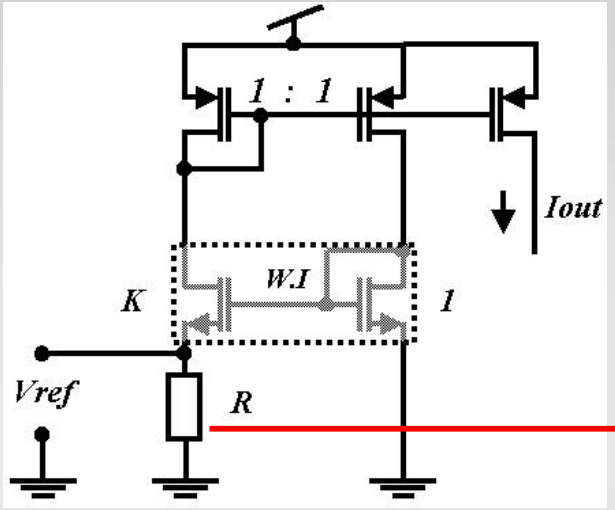
ACM model

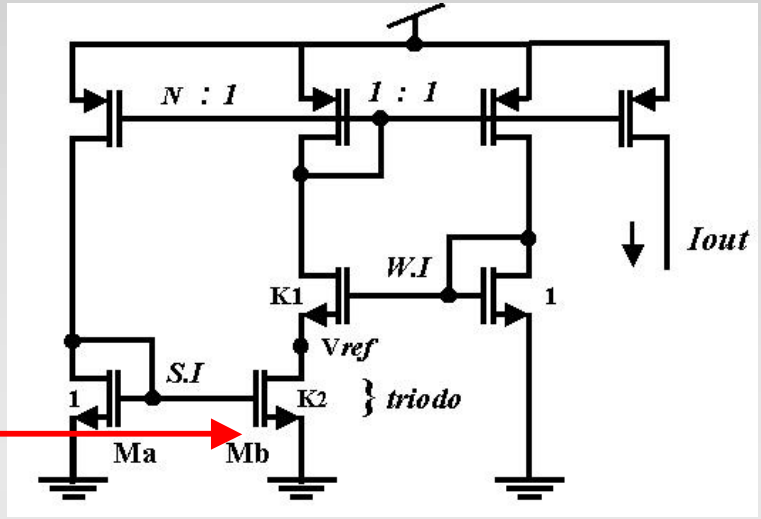


V_{SB}=0 & saturation



3. Self-biased current references





[Vittoz ,1977]

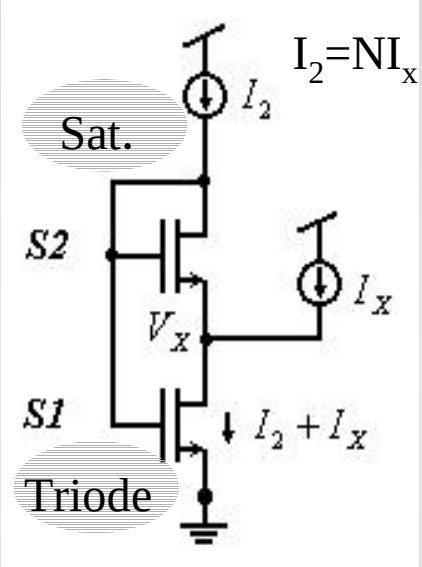
- $I_{ref} = (\phi_t / R).\ln K$
- I_{ref}=0.6nA(6nA)
- $\phi_t . \ln K$ =60mV→R=100(10)MΩ
- Efficiency =33%

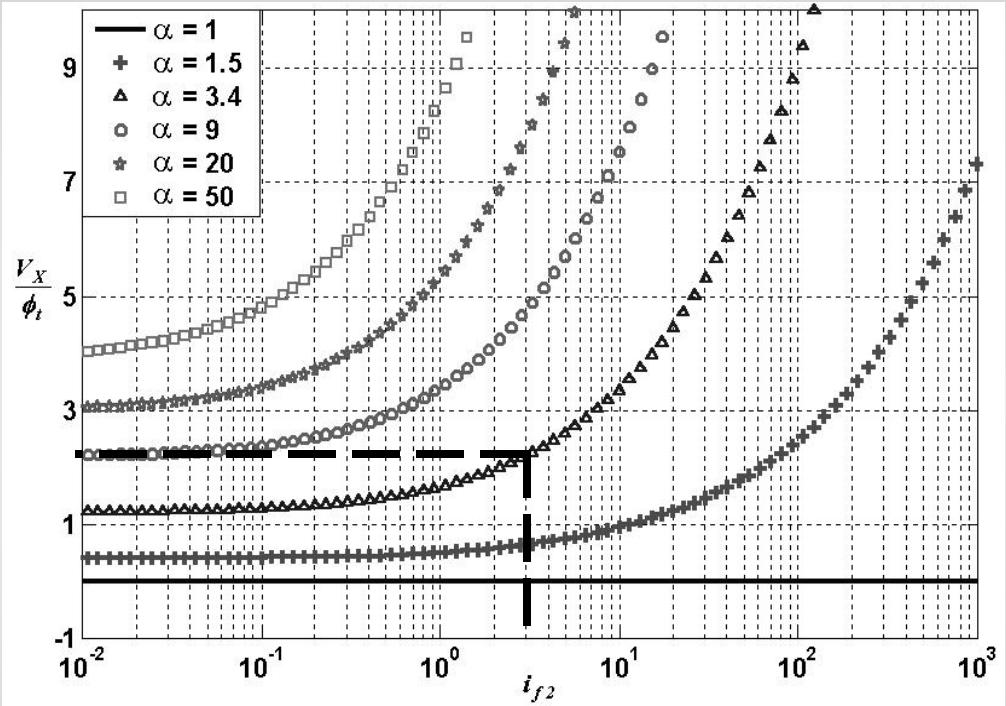
[Oguey ,1996]

- S.I. ($M_{a,b}$) not appropriate for LV
- NK_2>1 (M.I) and NK_2>4 (S.I)
- $I_{ref} \propto \mu C'_{ox}\, n\phi_t^2$
- Efficiency =14% for N=4

4. Proposed self-biased current reference

SCM (Self-Cascode MOSFET)



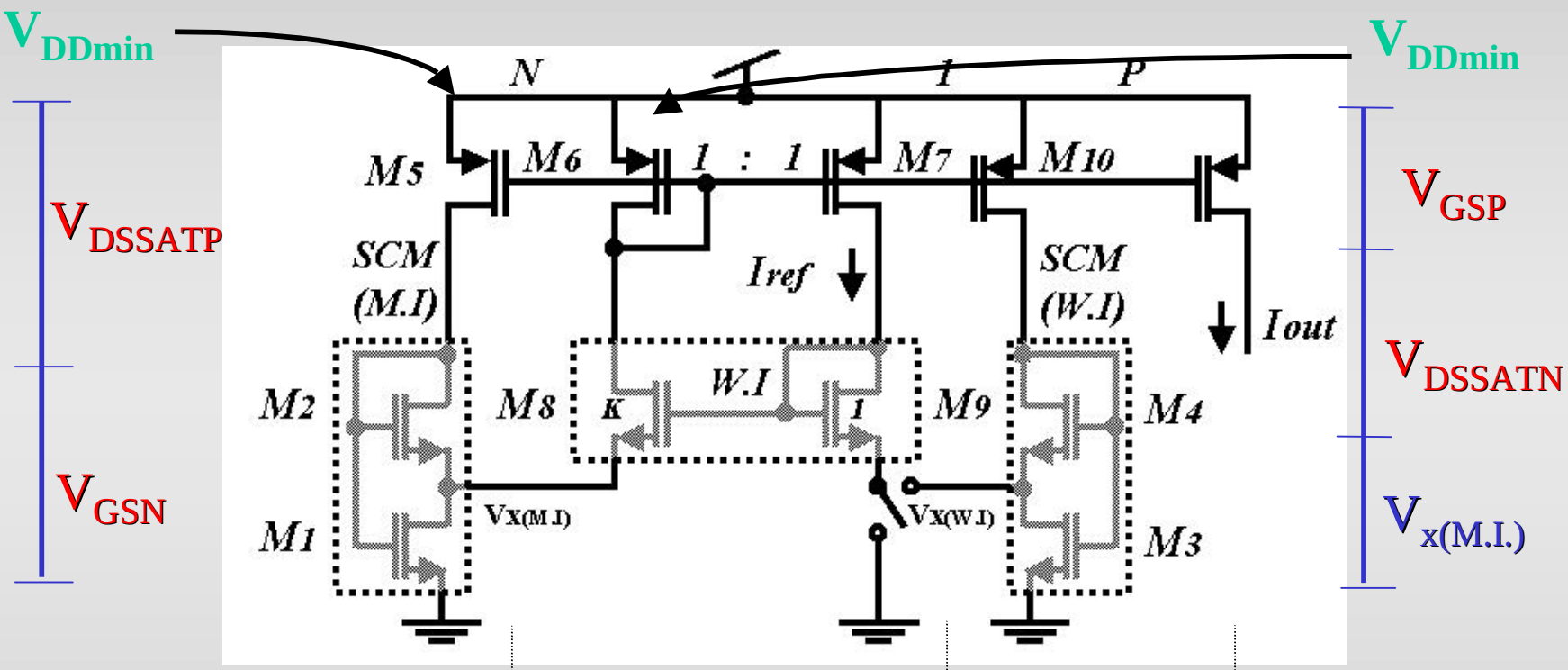


- W.I $\rightarrow V_X = \phi_t \ln\alpha$ - PTAT
- M.I, S.I $\rightarrow V_X = f(i_f, \alpha)$

$$\alpha = \left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right]$$

There is an OP stable for α(W.I) > α(M.I) >1

4. Proposed self-biased current reference



SCM (M.I.)

$\alpha(M.I) > 1$

voltage following current mirror

PTAT voltage

$\alpha(W.I) >> 1$

4. Proposed self-biased current reference

Design

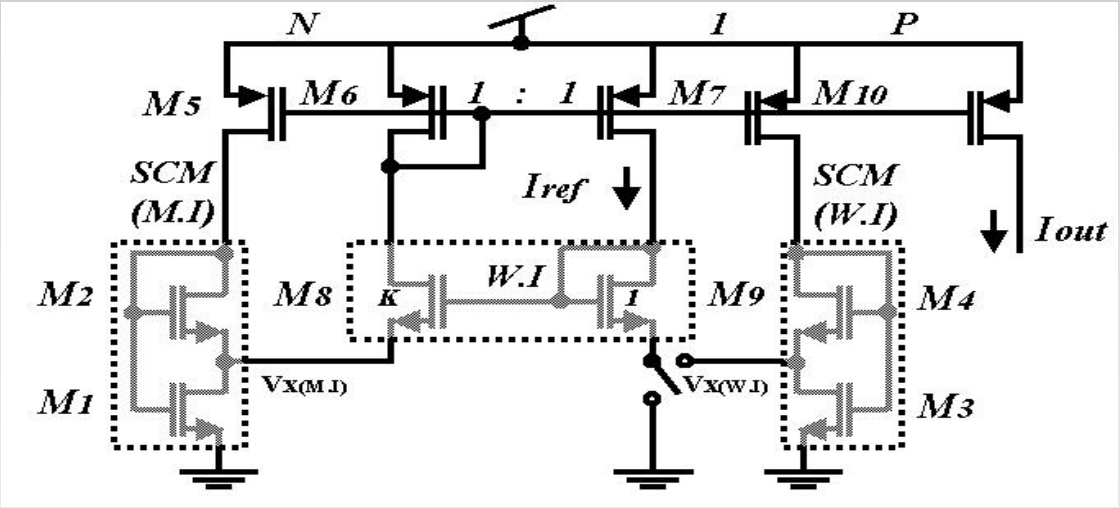
- I_{ref}=400pA, V_{DDmin}=1.2V (Possible?)
- V_X<100mV, e.g., α(W.I)=9 results in V_X=57mV
- i_{f2}=3 - w.i. not allowed →current very sensitive to V_X
  - s.i. operation increases V_{GSN} & V_{DDmin}
- V_X=57mV, N=1 and i_{f2}=3 results in α (M.I)= 3.4 < α(W.I)
- For the P-mirrors i_f<1 → V_{DSSATP}=100mV

5. Results

Parameter	Simple topology K=9, N=1		Symmetric topology, K=1 N=1		*Unit*
Technology	AMIS 1.5µm		0.35µm	1.5µm	
	Simulation *	Experiment	Experiment	Experiment	
V_{DDmin}	1.1	1.1	1.05	1.1	V
Power (at 1.1V)	1.5	1.5	2.0	2.0	nW
V_{ref} sensitivity to V_{DD}	0.9	1.6	0.85	1.3	%/V
V_{ref} sensitivity to T	+0.32	*X*	*X*	*X*	%/ºC
I_{ref} sensitivity to V_{DD}	4.7	6.2	4.0	6.0	%/V
I_{ref} sensitivity to T	+0.047	0.3	0.32	0.3	%/ºC
Efficiency (Iref/Itotal)	25	25	20	20	%

*** Simulation run with BSIM3 parameters provided by MOSIS**

5. Results



TRANSISTOR SIZES FOR THE SYMMETRIC TOPOLOGY IN TSMC 0.35µm

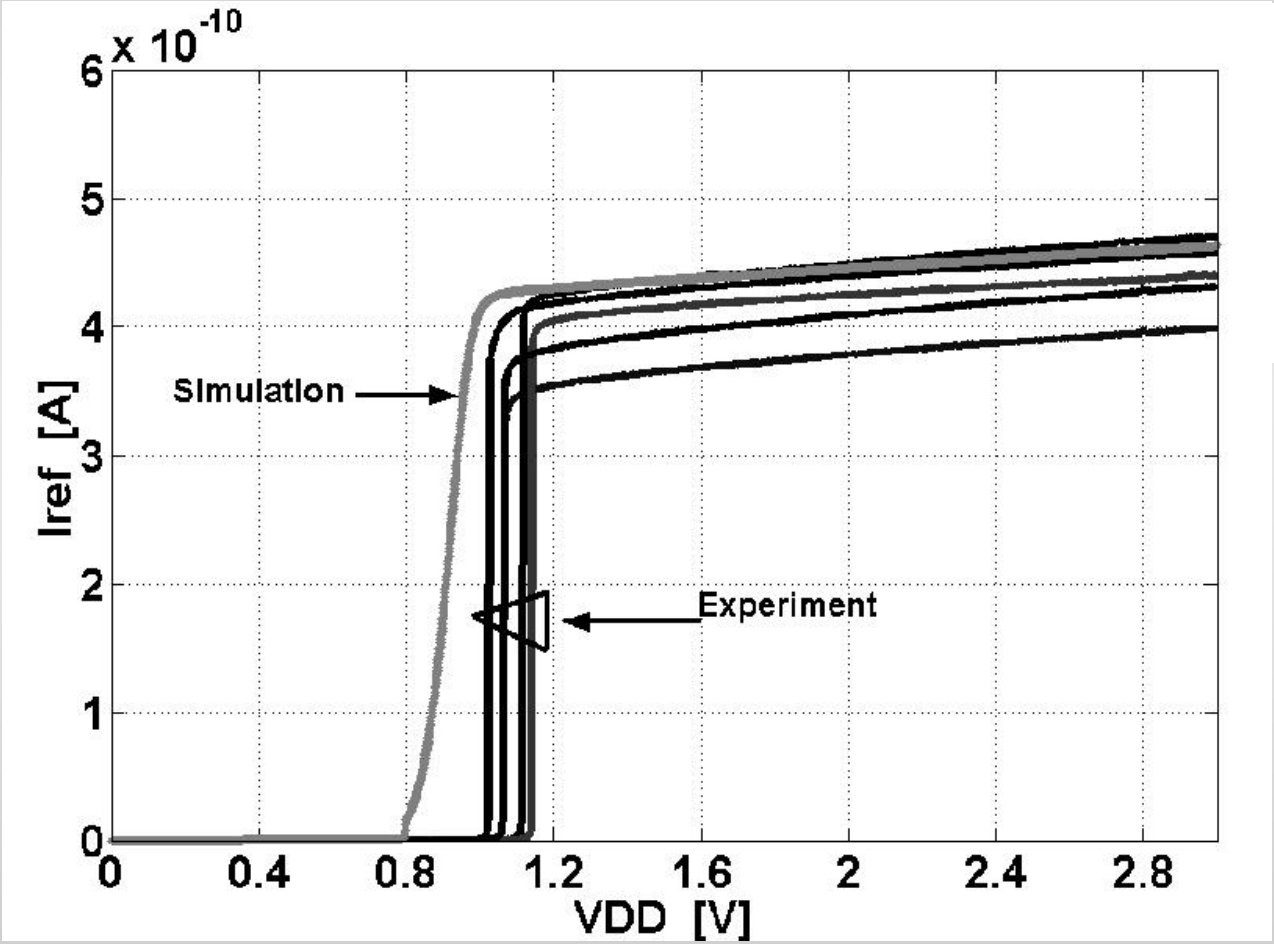
Transistor	W [µm]	L [µm]	i_f
M_1	2	18x60*	10.2
M_2	2	15x60*	3
M_3	10	6	0.008
M_4	4x10	6	0.001
$M_{5\text{-}7,\,10}$ &	4	10	0.04
$M_{8\text{-}9}$ &	10	6	0.004

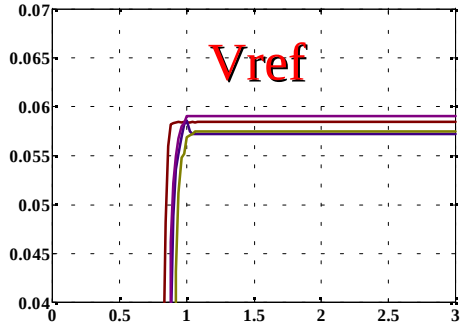
&Trapezoidal transistors. Dimensions of transistor connected to the source are W and L while the one connected to the drain is sized 8W and L.

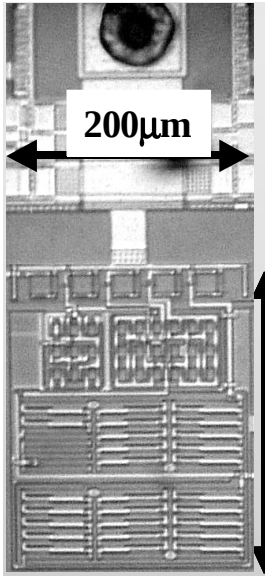
* Series association of 18 (15) transistors having W=2µm and L=60µm.

5. Results

Experimental (1.5um)



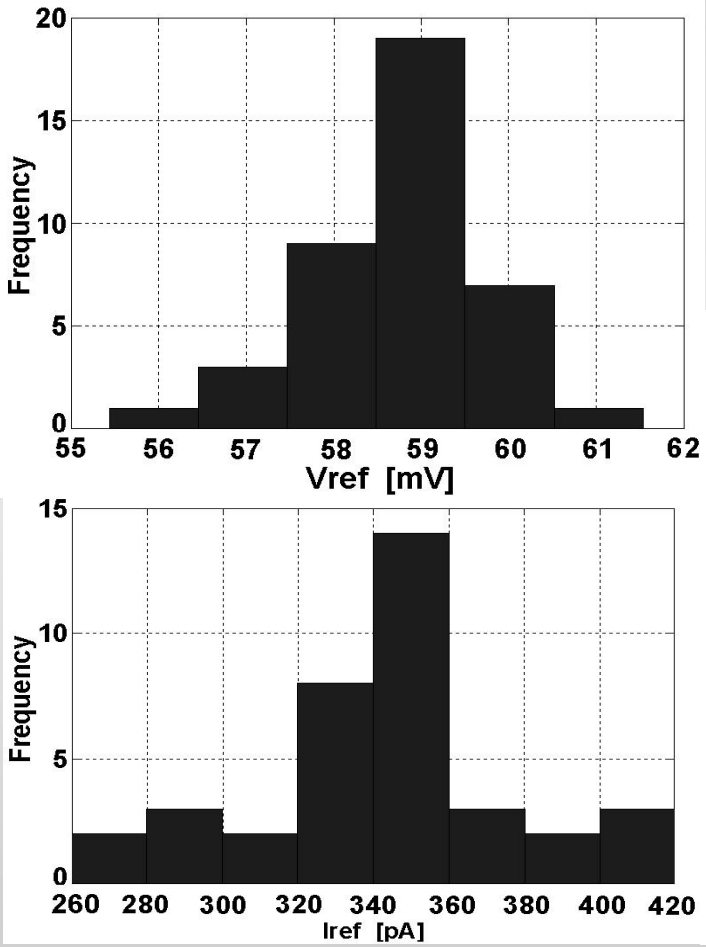




Micrograph

5. Results

Experimental (0.35um)



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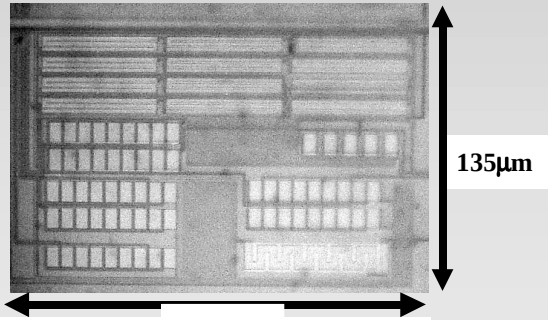

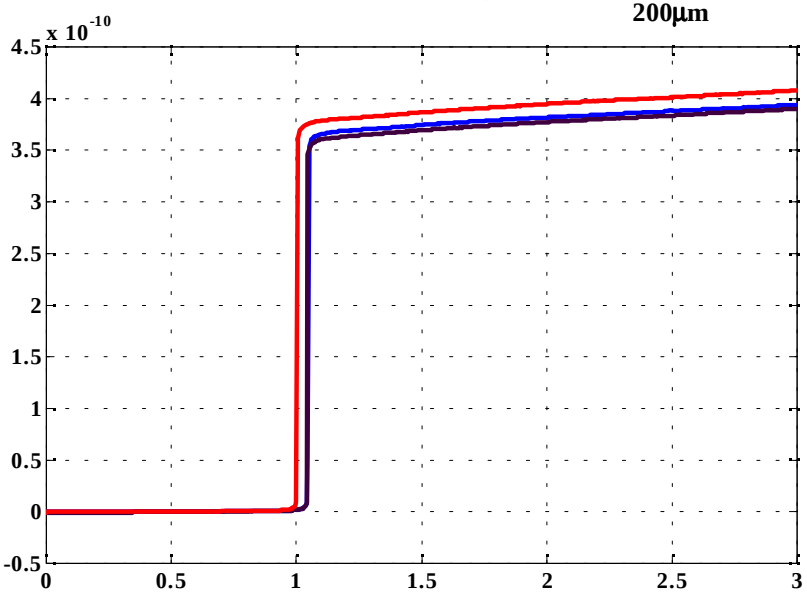

6. Summary and conclusions

- Successful generation of current references of the order of 400 pA in AMIS 1.5μm & TSMC 0.35μm;
- The consumption of the core cell is $4*I_{ref}$ or $3*I_{ref}$;
- Experimental results demonstrated the design correctness;
- Circuit operates from 1.1 V in 1.5 μm technology and potentially operates from 0.7 V in 0.18 μm technology;
- Performance of the self-biased current reference is better than other SBCS reported so far.

Acknowledgments

We are specially indebted to MOSIS for providing us access to silicon