Tunable CMOS Pseudo-Resistors for Resistances of Hundreds of GΩ

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***Abstract*— This paper presents the design of tunable CMOS pseudo-resistors aimed at achieving large and predictable resistance values. Instrumental to the proposed pseudo-resistor is the design of current sources of extremely low currents and transistors operating in subthreshold. The effects of the leakage currents of reverse-biased pn-junctions on the pseudo-resistor resistance are also evaluated. The proposed pseudo-resistor circuit was validated while in use as part of a filter integrated in a 180 nm CMOS process. Pseudo-resistors with resistances between 180 GΩ and 700 GΩ were employed to obtain low-frequency poles of a band-pass filter adjustable from 0.6 Hz to 2 Hz.**

***Index Terms*— Pseudo-resistor, CMOS design, subthreshold design, high resistance, high time constant, bio-signal amplifier.**

I. Introduction

In BIOMEDICAL applications, biopotentials sensed by electrode sensors are essential for diagnostic tests using techniques such as electrocardiography and electroencephalography [1]. Biopotential signals generally present amplitudes as low as tens of microvolts and frequencies in the sub-hertz to hertz range. To comply with such strict specifications, custom integrated filters are designed to pick up extremely low potentials at very low frequencies, which are often obscured by interfering out-of-band signals [2], [3]. Thus, filters for biomedical applications are required to achieve high time constants and high gain.

For continuous-time filtering, the active-RC (resistor-capacitor), active-MOSFETC and transconductance-C (capacitor) are commonly employed. For low-frequency applications, the popular active-RC technique is prohibitive since it requires large integrated resistors and/or capacitors, which need an excessively large silicon area [4]. Also, active-RC filters often produce inaccurate time constants owing to process variations. A straightforward alternative to the active-RC filters is the substitution of MOSFETs operating in the linear region for the resistors. In such a case, the MOSFETs are generally called pseudo-resistors. When biased in weak inversion, pseudo-resistors can give rise to extremely large channel resistances. Pseudo-resistors along with integrated capacitors can achieve the exceptionally large time constants required for very-low-frequency applications, but, as we shall see, they require the deployment of extremely low bias currents.

The transconductance-C technique with extremely low transconductances, coupled with integrated capacitors, is also a common choice to obtain very-low-frequency filters. Achieving the transconductances in the range of tens of pS to units of nS required for low-frequency filters is a difficult challenge that also involves the generation of extremely low currents, typically in the range of tens of pA to units of nA and/or current division [5], [6].

The challenges confronted when designing large time constants for either transconductance-C or MOSFET-C filters are similar, since both techniques require the generation of extremely low bias currents, typically in the pA range, combined with high-attenuation current mirrors. We will focus on the design of pseudo-resistors of exceedingly high resistance for application in MOSFET-C filters, but most of the strategies presented in this article can also be used to design ultra-low transconductances.

Herein, we propose the design of pseudo-resistors in the range of hundreds of GΩ while considering the leakage through the reverse-biased pn-junctions, which degrades the performance of the pseudo-resistors.

This paper is organized as follows. Section II explains the basics of the proposed pseudo-resistor, along with strategies to design very-high-value resistances. Section III presents the design of the pseudo-resistor cell together with its bias circuit. Section IV describes the application of the pseudo-resistor in a low-frequency filter and the effect of the leakage currents of the parasitic diodes on the DC input voltage of the filter. Section V reports the experimental results for both the integrated pseudo-resistor and the filter prototype. Section VI summarizes the main results of the paper.

II. Pseudo-Resistor

The use of transistors as resistive devices, also called pseudo-resistors, is a common practice in analog circuit design for cases in which integrated resistors are not suitable. Resistors compatible with CMOS technologies are available, but their small sheet resistance generally precludes their use for resistances higher than a few tens of MΩ. As an example, the sheet resistance of non-silicided polysilicon, which

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provides one of the highest resistivities in CMOS technologies, is typically less than 1 kΩ per square. Therefore, the use of non-silicided polysilicon for GΩ resistance values would require a prohibitively large silicon area. Alternatively, transistors offer the possibility of achieving resistance values of the order of TΩ [7]. In particular, the operation of transistors in the triode region allows them to emulate resistors whose values can be tuned through a bias circuit. Transistors, however, have their own disadvantages, such as the leakage currents through pn-junctions and a non-linearity in the channel resistance with the applied voltage [8]. Some of the drawbacks can be mitigated through ingenious circuit modifications, for example, by connecting multiple transistors in series to limit the nonlinearity of each transistor, as explained in [2], or using bias circuits that compensate the temperature dependence of the channel resistance [9].

The main driving force behind this study was the confidence that a predictable high value resistance of a pseudo-resistor could be achieved if the bias current is almost process-insensitive and has an extremely low value. The low sensitivity of the resistance to the process is attained in our design through a bias current defined by a fundamental parameter of the PMOS transistor, namely the sheet specific current (I_{SH}), which is almost independent of process variations.

The basic cell of the proposed floating pseudo-resistor, first presented in [2], is shown in Fig. 1. It is composed of a current source I_{BIAS} that is converted into a ground-referenced voltage (V_{REF}) by means of the PMOS transistor $\mathrm{P_{REF}}$. The voltage follower $\mathrm{N_{D1}}$-$\mathrm{N_{D2}}$ converts the ground-referenced voltage into a floating voltage reference.

If the pseudo-resistor operates in the subthreshold region, as is the case in this study, (1) describes the resistance value [2], [9] achieved with the topology shown in Fig. 1.

$$R_{PR}|_{V_{AB}=0} = \frac{2\phi_t}{I_{BIAS}} \frac{S_{P_{REF}}}{S_{PR}} \quad (1)$$

where ϕ_t is the thermal voltage, while $S_{P_{REF}}$ and S_{PR} are the aspect ratios W/L of the transistors $\mathrm{P_{REF}}$ and PR, respectively. From (1), we can see that two design strategies are available for achieving a high value of R_{PR}. First, the bias current must be made exceedingly small; this can be achieved through the design of an extremely low current reference and/or through down-mirroring strategies. Secondly, the ratio between the aspect ratios of $S_{P_{REF}}$ and S_{PR} must be large.

A benefit of the architecture in Fig. 1 would be a negligibly small temperature coefficient of the pseudo-resistor if the bias current were proportional-to-absolute temperature (PTAT) [9], as can be inferred from (1). However, to generate a PTAT current source, in the work described in [9], the authors made use of an external resistance. Instead, in this research, we used a self-biased current source (SBCS) that generates a bias current (I_{BIAS}) proportional to the PMOS sheet specific current (I_{SH}), which is a technology factor proportional to the oxide capacitance, mobility, slope factor and the square of the absolute temperature (see [10] for details). I_{SH} is slightly dependent on the gate voltage. For some technologies, I_{SH} is close to a PTAT current.

Given that matching between the devices that compose the pseudo-resistor (PR), the transistor ($\mathrm{P_{REF}}$) of the floating voltage reference and those of the core of the current source is fundamental in this design, all PMOS transistors have equal dimensions [11] to keep the same electrical parameters for all transistors. The aspect ratios required for the design were adjusted by means of the number of transistors connected in parallel and/or in series [12]. To increase the resistance and to improve its linearity, pseudo-resistors biased through different voltage followers ($\mathrm{N_{D1}}$-$\mathrm{N_{D2}}$ in Fig. 1) were connected in series [9], [13]. Note that a single current source (I_{BIAS}) and a single reference transistor ($\mathrm{P_{REF}}$) are employed to bias all the segments of the pseudo-resistor. Also, there is no need to provide each segment of the pseudo-resistor with separate I_{BIAS} and $\mathrm{P_{REF}}$, as in [9], since the floating voltage V_{REF} is the same for all segments.

Fig. 1. Schematic diagram of the pseudo-resistor and the bias circuit composed of a current source and a floating voltage reference.

Important limitations of pseudo-resistors arise due to parasitic effects, namely the DC leakage and the capacitance of reverse-biased pn-junctions, as well as the distributed capacitance of the transistor channel. As seen in Fig. 2, two separate N-wells give rise to two reverse-biased pn-junctions between the pseudo-resistor terminals and the P-type substrate. The parasitic well diode can pose a tough challenge for the design of extremely high resistance values, since the reverse junction current (orange path in Fig. 2(a)) can be a significant fraction of the channel current (represented as a blue - I_A - or red - I_B - path in Fig. 2(b)). Multiple pseudo-resistor cells connected in series will multiply the effects of the pn-junctions. Note that the contribution of the leakage current through the

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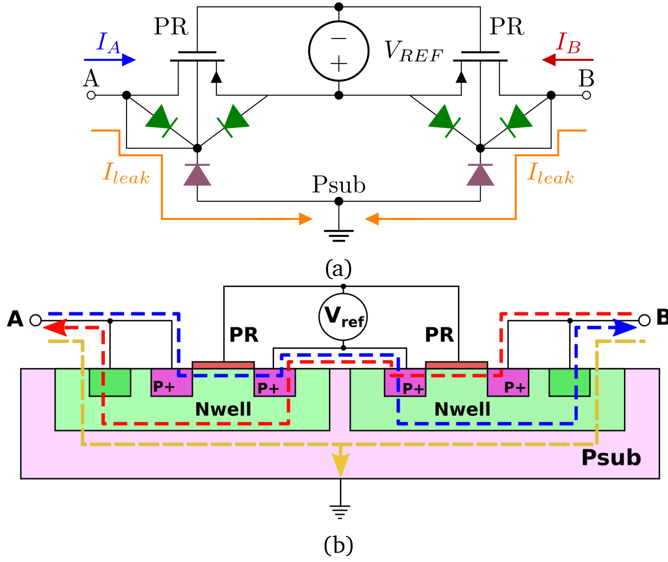

Fig. 2. (a) Schematic diagram of the floating pseudo-resistor and (b) view of the current paths in the pseudo-resistor structure where blue represents the current path when $V_{AB} > 0$, red is the current path when $V_{AB} < 0$; and the leakage current through the N-well is shown in orange.

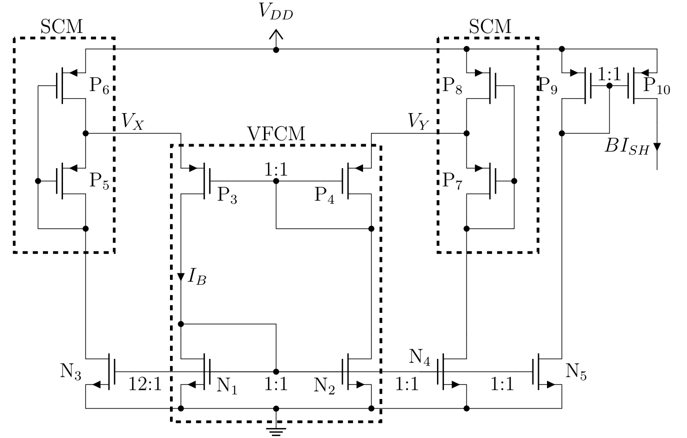

Fig. 3. Specific current generator.

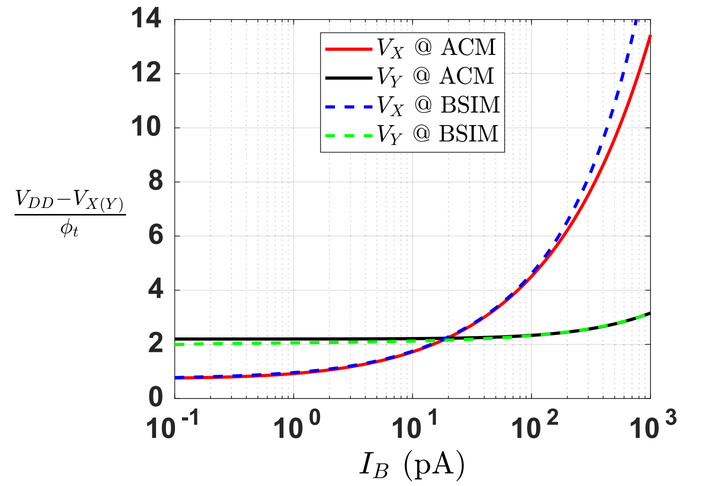

Fig. 4. Internal voltages of the SCMs as functions of the bias current @ I_{SH} = 38 nA, $S_5 = 1 \times 0.5$ μm/98 $\times$ 14 μm, $S_6 = 1 \times 0.5$ μm/98 $\times$ 14 μm, $S_7 = 2 \times 0.5$ μm/2 $\times$ 14 μm, $S_8 = 1\times$ 0.5 μm/4 $\times$ 14 μm.

P+/N-well junctions to the degradation of the *I-V* characteristic of the pseudo-resistor is negligible because it is in parallel with the conductive channel of the transistors. The current through the P+/N-well junction is much smaller than that through the transistor channel, even for the highest temperature used in our experiment.

III. Circuit Design

The main goal for the design of the pseudo-resistor of Fig 1 is the achievement of tunable high resistance values that are stable throughout variations in both the technology process and the temperature. Bearing in mind this goal, we explain how we designed the first stage of the pseudo-resistor, namely the SBCS, the current of which is a scaled version of the sheet specific current I_{SH} of PMOS transistors. The following stage of the pseudo-resistor is composed of a PMOS transistor, which converts the bias current into voltage V_{REF}, followed by a pair of identical NMOS transistors that converts the grounded-referenced V_{REF} into a floating voltage for biasing the pseudo-resistor itself. Lastly, we provide some details on the transistors that compose the pseudo-resistor.

In this research we chose PMOS transistors as the basic elements of the SBCS and the pseudo-resistors, while NMOS transistors were used for either current mirrors or voltage followers. In this setup, the resistance of the pseudo-resistor is a function of a single PMOS parameter, namely the sheet specific current (I_{SH}), and scaling factors, which are determined by the aspect ratios of the PMOS transistors and the gains of the current mirrors.

A. Self-Biased Current Source

The design of the SBCS is based on the distinct nonlinear *I-V* characteristics of two self-cascode MOSFETs (SCMs) coupled by either an operational amplifier [14]–[16], a voltage-following current mirror (VFCM) [17] or a coupling block containing two stacked transistors, each one copied from each of the two SCMs [18]. In every case, the output current of the current source is proportional to I_{SH}.

The design of the SBCS shown in Fig. 3 is based on the methodology presented in [17]. The SBCS is composed of SCMs P_5-P_6 and P_7-P_8, a VFCM with matched transistor pairs P_3-P_4 and N_1-N_2, and NMOS current mirrors. The *V-I* characteristics of the SCMs are shown in Fig. 4, using either the equations of the ACM model or simulation with the BSIM model. Note that the current pulled by transistor N_3 is $12I_B$. Since the two SCMs operate at the same intermediate voltage V_X, the operating point of the SBCS is that at which the two *V-I* curves intersect. The intersection pair is given approximately by (I_B = 20 pA, $(V_{DD} - V_X)/\phi_t$ = 2.23).

For the 180 nm CMOS technology of this design, the sheet specific current for the PMOS transistor is I_{SH} = 38 nA. To bias the pseudo-resistor, the output current selected for the SBCS was 20 pA and all p-channel transistors of the SBCS were of the same size (W = 0.5 μm, L = 14 μm). Parallel and/or series associations of equally sized transistors were employed to set the aspect ratios of the equivalent transistors [11], [12].

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The design equations of the SBCS are based on the ACM model [10], [19], which is summarized in the equations below for the PMOS transistor.

$$I_D = I_S\left(i_f - i_r\right) \quad I_S = S I_{SH} \qquad (2)$$
$$S = \frac{W}{L} \quad I_{SH} = \mu C_{ox} n \frac{\phi_t^2}{2}$$

where the symbols refer to I_D - drain current, I_S - specific current, I_{SH} - sheet specific current, $i_{f(r)}$ - forward (reverse) inversion coefficient, S - aspect ratio, W - channel width, L - channel length, μ - mobility, C_{ox} - oxide capacitance/unit area, n - slope factor, and ϕ_t - thermal voltage. It initially appears that I_{SH} is proportional to the square of the absolute temperature. However, since the mobility is a decreasing function of the temperature (see, for example, page 189 of [20]), the dependence of I_{SH} is almost PTAT. The forward and reverse inversion coefficients are functions of the terminal voltages referenced to the substrate, as given by the unified current control model (UICM)

$$\frac{V_{GB} - V_T}{n} - V_{SB(DB)} = \pm\phi_t F\left(i_{f(r)}\right) \qquad (3)$$
$$F\left(i_{f(r)}\right) = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right)$$

where V_T is the threshold voltage. The $+$ and $-$ signs in (3) apply to NMOS and PMOS transistors, respectively. Note that, in the UICM equation, the forward (reverse) inversion coefficient is dependent only on the gate and source (drain) voltages. For a saturated transistor, the inequality $i_f \gg i_r$ usually holds.

The following equalities of the inversion coefficients hold for the SCMs of the circuit in Fig. 3

$$i_{r8} = i_{f7} \quad i_{r6} = i_{f5} \qquad (4)$$

Since transistors P_5 and P_7 operate in the saturation region, $i_{f5} \gg i_{r5}$ and $i_{f7} \gg i_{r7}$.

As in [17], we have chosen one of the SCMs (P_7-P_8) to operate in subthreshold, while the other (P_5-P_6) operates in moderate inversion. Since the pair (P_7-P_8) operates in subthreshold, we have $i_{f7(8)} \ll 1$. Applying (3) to P_7-P_8 along with (4) yields

$$\frac{V_{DD} - V_Y}{\phi_t} \cong \ln\left(1 + 2\frac{S_7}{S_8}\right) = \ln(1 + 2 \times 4) = 2.2 \qquad (5)$$

We selected $S_7/S_8 = 4$ for a drain-to-source voltage of around 56 mV for P_6. This choice of S_7/S_8 is because the source-to-drain voltage of P_8 should be around halfway between 0 V and the saturation voltage (approximately 100 mV) of a transistor operating in weak inversion. Even though the design space for the SBCS is huge [14], [16], this choice of S_7/S_8 results in a good trade-off between silicon area and precision, as shown in references [14], [16].

The choice of the parameters for the SCM (P_5-P_6) requires that this pair operates with moderate inversion coefficients ($100 > i_f \gg 1$). The reason for this choice is twofold: (i) if the inversion coefficient is close to or less than unity, the resulting current will be highly dependent on mismatch; and (ii) high inversion coefficient values will lead to a large silicon area. Therefore, our goal is to operate P_5 with an inversion level within the range of 10-30. For the SCM (P_5-P_6) we have:

$$12 I_B = I_{S5} i_{f5} \quad (12 + 1) I_B = I_{S6}\left(i_{f6} - i_{f5}\right) \qquad (6)$$

Using (3) for both i_{f5} and i_{f6} we find that:

$$\frac{V_{DD} - V_X}{\phi_t} = F\left(i_{f5}\left[1 + \frac{S_5}{S_6}\left(1 + \frac{1}{12}\right)\right]\right) - F\left(i_{f5}\right)$$
$$= F\left(\frac{25}{12} i_{f5}\right) - F\left(i_{f5}\right) \qquad (7)$$

where $i_{f5} = \frac{12 I_B}{I_{SH} S_5}$ and $i_{f6} = \frac{25}{12} i_{f5}$ since we chose $S_5 = S_6$.

Since the VFCM is composed of identical PMOS and NMOS pairs, $V_X = V_Y$. Now, equating (5) and (7) we find that $i_{f5} \cong 17.3$, which results in $1/S_5 \cong 2740$ for the intended current $I_B = 20$ pA, with $I_{SH} = 38$ nA. Since the dimensions of the PMOS transistor are $W = 0.5$ μm and $L = 14$ μm, 98 series-connected transistors are required for the calculated value of S_5. The choice of a current equal to I_B through transistor P_5 for the value of $i_{f5} \cong 17.3$ would lead to 12×98 series-connected transistors, instead of the 98 series-connected required for a current equal to $12 I_B$. Although this choice causes a higher power consumption it has the advantage of less silicon area.

To design a SBCS that generates the extremely low currents needed for biasing the pseudo-resistors, we must consider two limiting factors. Firstly, transistors have leakage mechanisms that hinder their operation with currents of the order of fA [21], [22] without incurring significant errors. Secondly, the current provided by the SBCS needs to be mirrored and distributed throughout the circuit. Thus, the input transistors of the mirrors must operate in the saturation region while connected as diodes, which is only possible if the inversion coefficient is such that the drain-to-source voltage is, at least, 100 mV [10], [19]. In our design of the SBCS, both the output current of 20 pA and the transistors aspect ratios were chosen to keep the diode-connected transistors in saturation.

The time response and programmability of the simulated current source are plotted in Fig. 5. The output current can be selected as 20 pA, 10 pA, 6.7 pA or 5 pA by selectively enabling down-mirroring. The current source is programmed by means of a current mirror in which the input is composed of 4 transistors identical to the output transistor. A gain of 1, 1/2, 1/3 or 1/4 is selected through the parallel connection of 1, 2, 3 or 4 transistors, respectively, at the input. A start-up circuit allows the bias current to be reached within 250 ms. The technology used has a sheet specific current deviation σ/μ of 2.5% over the process variations.

B. Floating Voltage Reference

The floating voltage reference circuit shown in Fig. 6, which was introduced in [2], operates as follows. The diode-connected P_{REF} converts the bias current I_{BIAS} into a ground-referenced voltage (V_{REF}), which, in turn, is converted into a current by the action of N_{D1}. The current through N_{D2}, which is the same as that through N_{D1}, is converted back into the floating voltage V_{REF}. For the proper operation of the floating voltage reference, N_{D1} must be kept in the saturation region; therefore, the gate voltage of N_{D2}, which is equal to

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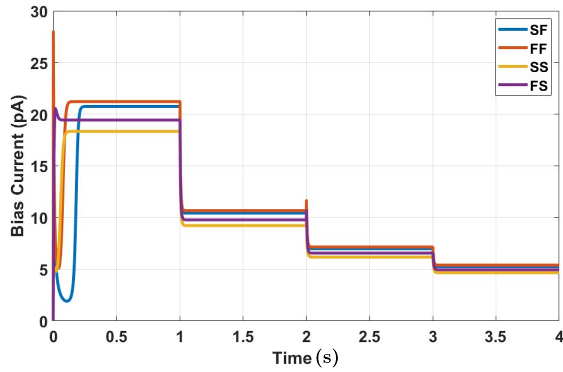

Fig. 5. Simulated time response and programmability of the SBCS for the technology corners.

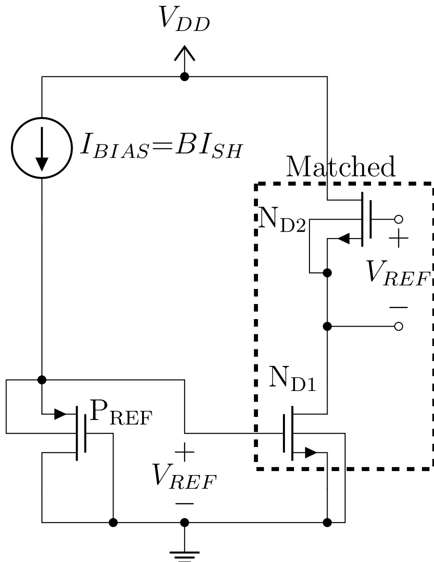

Fig. 6. Floating voltage reference: improved source follower based on matched deep N-well NMOS transistors.

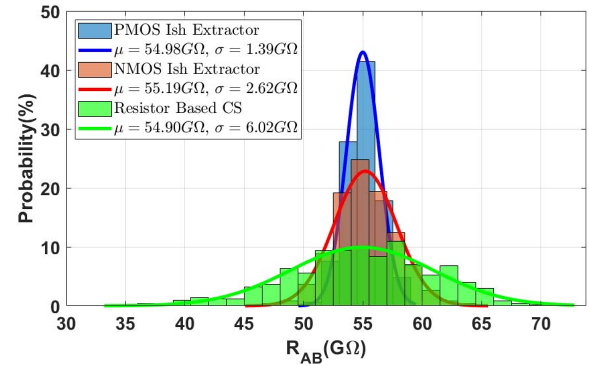

Fig. 7. Process variation and mismatch effects on the resistances of pseudo-resistors biased by either a PMOS-based or an NMOS-based sheet specific current extractor, or a resistor-based current source.

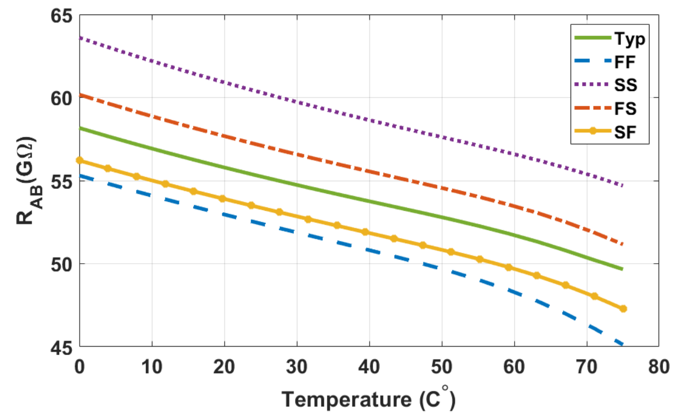

Fig. 8. Temperature dependence of the resistance of the proposed pseudo-resistor for the typical and corner parameters of the technology.

the common mode voltage across the pseudo-resistor, cannot be lower than V_{REF} plus the saturation voltage of N_{D1}. The simulated values of V_{REF} are 120 mV for $I_{BIAS} = 5$ pA and 160 mV for $I_{BIAS} = 20$ pA. Since N_{D1} operates in subthreshold, its saturation voltage is around 100 mV. Therefore, the gate voltage cannot be lower than 260 mV for $I_{BIAS} = 20$ pA.

C. Proposed Pseudo-Resistor

Since the bias current of the pseudo-resistor is proportional to the sheet specific current of the PMOS transistor, the resistance of the pseudo-resistor is independent of parameters other than those of the PMOS transistor, namely the sheet specific current I_{SH}. Note that voltage V_{REF} contains a *signature* of the PMOS transistor, since the bias current BI_{SH} is generated from a PMOS network. The remaining parameters in (1) are dependent on the aspect ratios only.

To compare the influence of the device employed for the current source on the pseudo-resistor, we simulated three designs. The first current source generates a current which is proportional to I_{SH} of a PMOS transistor of the same type as that of the pseudo-resistor. In the second generator, the current is proportional to I_{SH} of an NMOS transistor, while in the third case the current source is generated by means of a PTAT voltage across a poly-silicon resistance equal to 5.36 MΩ. Fig. 7 shows how the resistance of the pseudo-resistor is affected in each case by process and mismatch variations. Note that the σ/μ value of the proposed I_{SH} of the PMOS extractor is smaller than those of the resistor-based and NMOS-based current sources.

Fig. 8 shows the resistance of the pseudo-resistor, biased with a current proportional to the I_{SH} of a PMOS transistor, as a function of the temperature for the technology corners. This dependence is inherited from the sheet specific current, which is almost PTAT, but it includes the influence of parasitic diodes.

The ac characteristics of 10 series-connected segments of the pseudo-resistor for four values of the bias current are shown in Fig. 9. The pseudo-resistor behaves as an RC distributed network with an equivalent parasitic capacitance of the order of 40 fF distributed along the channel.

The noise of the pseudo-resistor is due to both its own generated noise and that induced by the floating voltage source V_{REF}. The V_{REF} noise, in turn, originates from the bias current that is transferred to the floating source, along with the noise introduced by P_{REF}, N_{D1} and N_{D2}.

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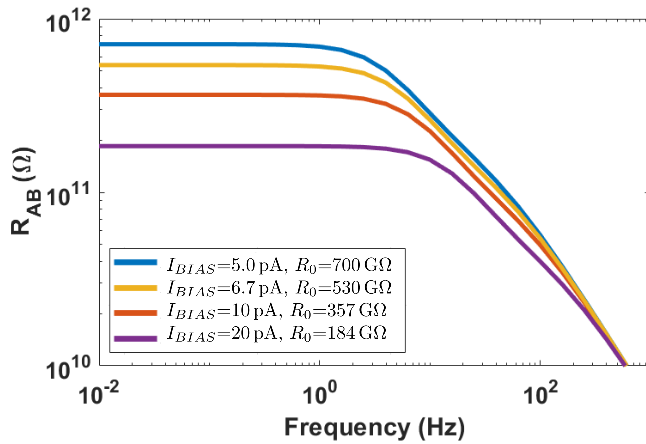

Fig. 9. Simulated AC characteristics of the programmable resistance at 27 °C.

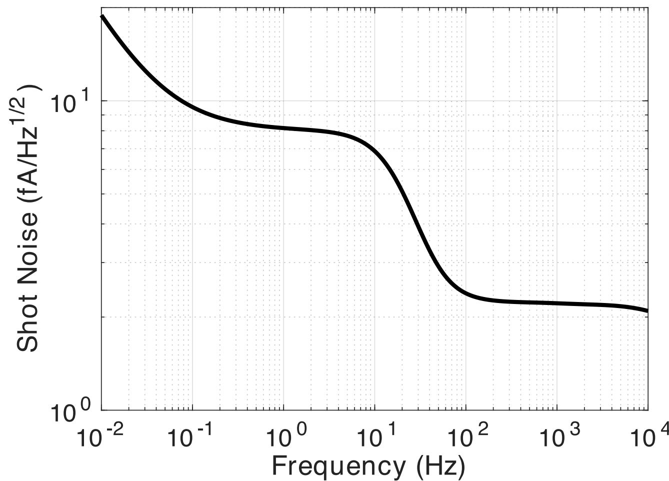

Fig. 10. Square root of the PSD of the current source @ $I_{BIAS} = 20$ pA.

Let us first present the noise components of the bias current. Its power spectral density (PSD) is the resultant of the combination of both the shot noise and the 1/*f* noise of the individual transistors that compose the current source, shaped by their transfer functions to the output. The PSD of the shot noise is given by the well-known formula

$$\frac{\overline{i^2}}{\Delta f} = 2qI_{BIAS} \tag{8}$$

where q is the electronic charge and Δf is the bandwidth in hertz over which the noise is measured.

For the nominal current $I_{BIAS} = 20$ pA, the shot noise is around 2.5 fA/Hz$^{1/2}$.

Fig. 10 is the simulated PSD of the current source for the nominal current of 20 pA. The shape of the curve is a result of the combination of the contribution of 1/*f* noise and shot noise of the transistors that compose the current source and their respective transfer functions to the output of the current source.

The PSD of the pseudo-resistor is shown in Fig. 11. The noise that comes from the floating source is removed when the differential voltage applied to the pseudo-resistor is equal to zero. In this case, the PSD of the noise current is given by the Nyquist-Johnson expression seen in (9).

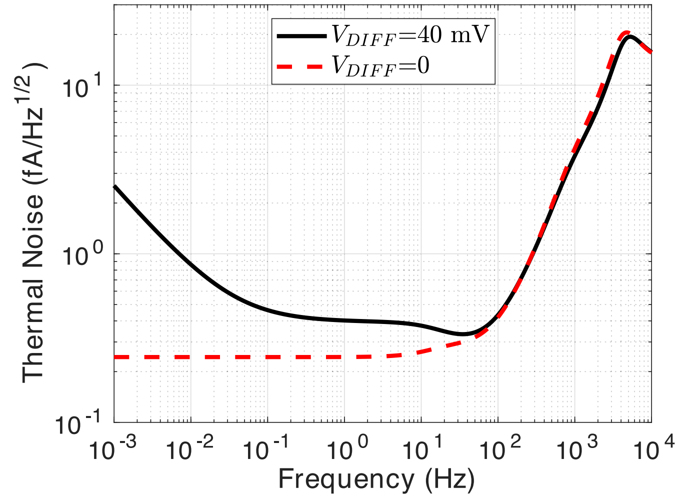

Fig. 11. Square root of the PSD of the three-segment pseudo-resistor for a bias current of 20 pA (nominal resistance equal to 61 GΩ).

TABLE I

COMPARISON OF PSEUDO-RESISTORS FROM DIFFERENT DESIGNS

	[9]	[8]	[23]	This study
Resistance [GΩ]	1	20	70	700
Process σ/μ [%]	3.6	25.5	30	2.53
Area [μm^2]	16 000	17 700	17 000	16 500
Technology	SOI 0.18 μm	0.35 μm	0.35 μm	0.18 μm

$$\frac{\overline{i^2}}{\Delta f} = 4kT\,\mathrm{Re}\{Y_{PR}\} \tag{9}$$

where k is the Boltzmann constant and Re$\{Y_{PR}\}$ is the real part of the pseudo-resistor admittance which, for low frequencies, is equal to $1/R_{PR}$.

When the voltage difference across the pseudo-resistor terminals is not zero, the noise from the floating voltage is transferred to the pseudo-resistor. Additionally, due to a non-zero dc current, a 1/*f* noise of the pseudo-resistor itself is added to its PSD. The resulting PSDs of the pseudo-resistor for differential voltages equal to zero and 40 mV, on top of a common-mode voltage of 0.9 V, are shown in Fig. 11.

Table I shows a comparison of different designs where pseudo-resistors were used to achieve high-value resistances. The methodology developed in this research to design pseudo-resistors is especially useful for the achievement of predictable and adjustable resistances of the order of hundreds of GΩ.

Table II summarizes the design of the proposed pseudo-resistor along with the forward inversion coefficient of each transistor. Note that all transistors of the same kind, N or P, are identical. To obtain the aspect ratios required for the design, we made use of series and/or parallel associations of unit transistors.

One of the most severe problems that can affect the characteristics of pseudo-resistors is the leakage current (I_{leak}) that flows through the pn-junction formed between the P-substrate and the N-well, as shown in Fig. 2. Measurements of the leakage current are plotted in Fig. 12 for a one-stage pseudo-resistor. Since two N-wells are used for a single pseudo-resistor, the leakage current that flows through each N-well is one half of the current in Fig. 12. Since the leakage current

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TABLE II
PSEUDO-RESISTOR DESIGN

Pseudo-resistor (Fig. 1)					
Dev.	Paral.	Series	W [µm]	L [µm]	i_f
PR	1	2	0.5	14	1 m-4 m
Floating voltage reference (Fig. 1)					
Dev.	Paral.	Series	W [µm]	L [µm]	i_f
$N_{D1(2)}$	2	4	0.5	8	70 m
P_{REF}	4	1	0.5	14	1 m-4 m
Self-biased current source (Fig. 3)					
Dev.	Paral.	Series	W [µm]	L [µm]	i_f
P_3	1	6	0.5	14	88 m
P_4	1	6	0.5	14	88 m
P_5	1	98	0.5	14	17
P_6	1	98	0.5	14	36
P_7	2	2	0.5	14	15 m
P_8	1	4	0.5	14	117 m
P_9	1	4	0.5	14	5 m
P_{10}	1	4	0.5	14	5 m
N_1	1	6	0.5	19	6 m
N_2	1	6	0.5	19	6 m
N_3	12	6	0.5	19	6 m
N_4	1	6	0.5	19	6 m
N_5	1	6	0.5	19	6 m

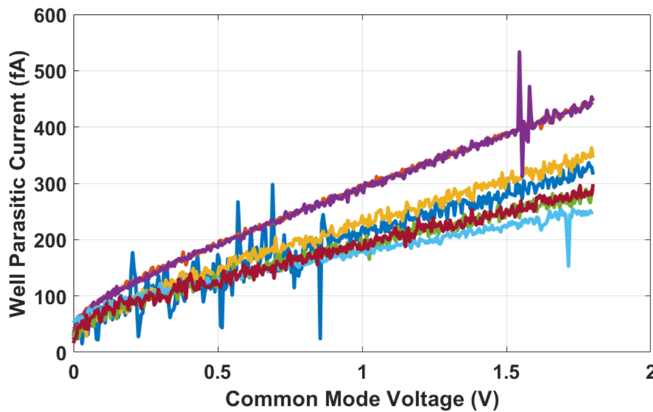

Fig. 12. Measured leakage current ($2I_{leak}$) through two P-sub/N-well (23 μm × 8 μm) junctions against the common-mode voltage of the pseudo-resistor for 5 chips.

is a function of the common-mode voltage, it contributes not only as a DC current at the pseudo-resistor terminals, but also decreases the value of the resistance.

The variation in the leakage current through the N-well/P-sub junction with changes in temperature is shown in Fig. 13. Both the dc leakage and the conductance of the junction have a strong dependence on the temperature. Thus, these two factors are mainly responsible for the degradation of the pseudo-resistor resistance at high temperatures, as will be shown in the Section on the measurements.

IV. FILTER DESIGN

The filter in Fig. 14, which is specifically intended for processing bio-signals, was proposed first in [24] and further tested in [25]. This filter can handle large common-mode voltages of the input signal. The filter presents a low-frequency pole defined by (10), where it is clearly seen how the resistance R_{PR} of the pseudo-resistor can be used to control the

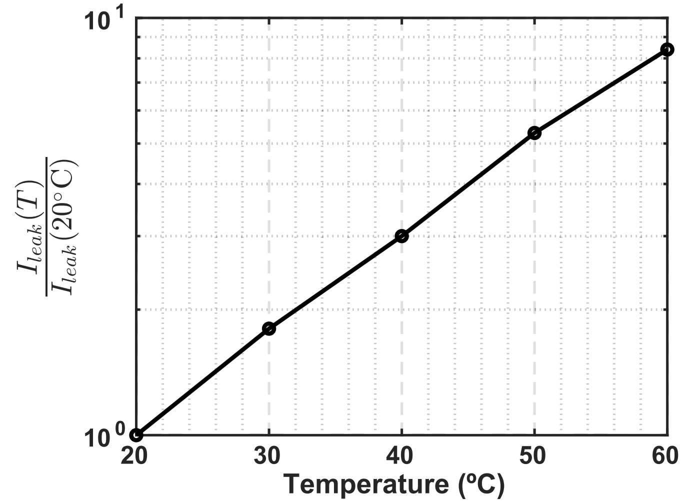

Fig. 13. Normalized leakage current through the N-well/P-sub vs temperature.

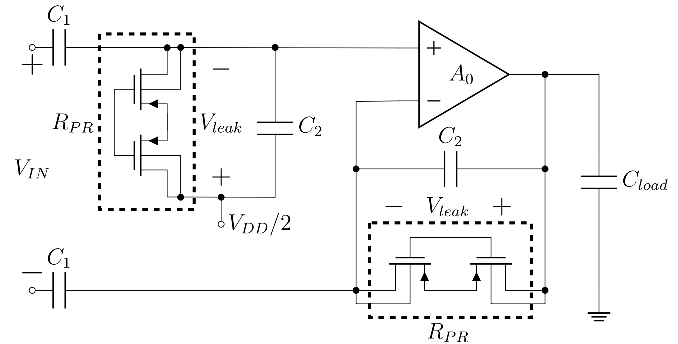

Fig. 14. Band-pass filter with pseudo-resistors.

low-frequency pole.

$$f_{p1} = \frac{1}{2\pi C_2 R_{PR}} \frac{1}{1 + \frac{C_1/C_2}{A}} \tag{10}$$

Here, A is the amplifier gain. The filter designed in this work uses a symmetrical amplifier that we had at hand with a gain A of around 48 dB and a 7 kHz bandwidth that covers the expected signal band (from 1 Hz to 1 kHz). The ratio $C_1/C_2 = 20\,\text{pF}/0.2\,\text{pF}$ would lead to a filter gain of 40 dB in the pass band for an infinite gain amplifier. However, as a consequence of the low amplifier gain (48 dB), the filter gain in the pass band is attenuated by a factor of around 3 dB, which can be calculated from the filter gain G in the pass band, given by

$$G = \frac{C_1}{C_2} \frac{A}{1 + A + C_1/C_2} \tag{11}$$

According to (10), the dominant pole of the filter is expected to be around 0.63 Hz for $R_{PR} = 700\,\text{G}\Omega$.

The leakage currents through the identical pseudo-resistors of Fig. 14 give rise to a DC common-mode input voltage at the operational amplifier input equal to $V_{DD}/2 - V_{leak}$. Here, V_{leak} is the DC voltage generated across the pseudo-resistor terminals due to the leakage through the reverse-biased P-sub/N-well junctions. The value of the voltage drop across the pseudo-resistor was calculated using the schematic

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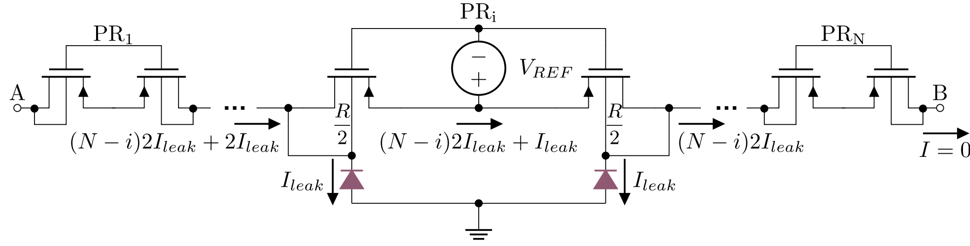


Fig. 15. Schematic used for the calculation of V_{leak} in the pseudo-resistor composed of N series-connected elements.

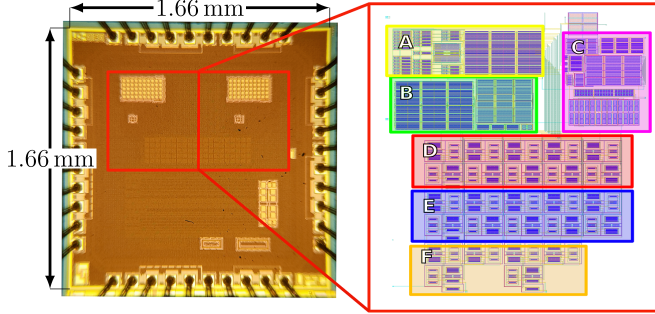


Fig. 16. Micrograph of the chip: A) mirrors and down-mirroring control, B) specific current extractor, C) filter amplifier, D) filter feedback pseudo-resistor, E) filter input pseudo-resistor and F) debug pseudo-resistors.

diagram of the pseudo-resistor composed of N elements, as shown in Fig. 15. Note that terminal B is connected to an input of the operational amplifier; thus, the current flowing out of B is equal to zero. The voltage drop across the ith element PR_i of the pseudo-resistor is given by

$$V_{PRi} = R(N-i)2I_{leak} + RI_{leak} \tag{12}$$

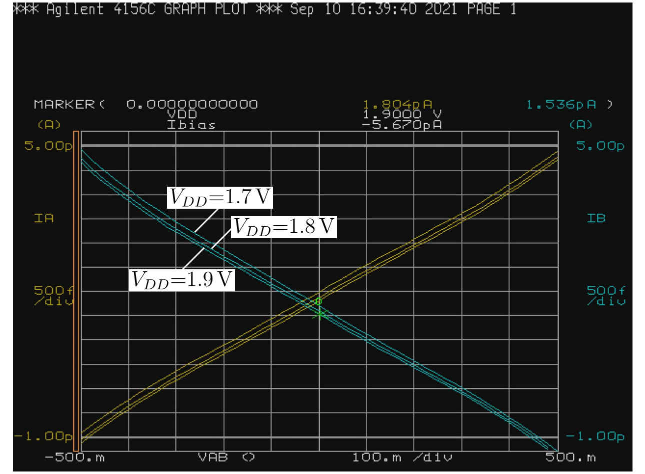
where N is the number of series-connected pseudo-resistor cells, R is the resistance of each cell, and I_{leak} is the leakage current of each well of the pseudo-resistor, which is assumed to be a constant for the derivation of $V_{leak} = V_{AB}$. In fact, the leakage current is dependent on the common mode voltage, as can be seen in Fig. 12, but due to its linearity, its average value is appropriate for first-order calculations. Overall, the distributed flow of the leakage currents through the highly resistive transistor channels gives rise to a DC voltage given by

$$V_{AB} = \sum_{i=1}^{N} R\left(N-i+\frac{1}{2}\right)2I_{leak} = RI_{leak}N^2 \tag{13}$$

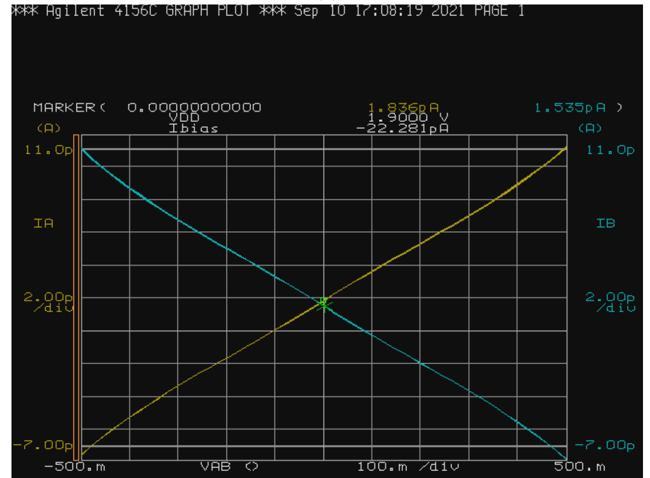
If we were to use the design proposed in this work with $N = 10$, $I_{leak} = 84\,\text{fA}$ for well dimensions of 23 μm by 8 μm, and R equal to either 18 GΩ or 70 GΩ, the value of V_{leak} would be either 150 mV or 600 mV, respectively. It should be noted that, for $V_{leak} = 600\,\text{mV}$, which corresponds to a common-mode input voltage of 0.3 V, the operational amplifier performs appropriately.

V. Measurements

The test prototype for the pseudo-resistors is shown in Fig. 16. Two debug pseudo-resistors, with three series-connected elements each, were made accessible to directly characterize their resistance and leakage currents. For bias currents of 20 pA and 5 pA the expected values of the resistances are 61 GΩ and 244 GΩ, respectively, at 300 K. The simulation for the nominal current of 20 pA at 300 K indicated a resistance value of 55 GΩ for the typical parameters of the technology, as shown in Fig. 8.



(a)



(b)

Fig. 17. *I-V* characteristics of the debug pseudo-resistor measured at SMU_1 (yellow line) and SMU_2 (cyan line) for bias currents of (a) 5 pA and (b) 20 pA at $V_{DD} = 1.7$, 1.8 and 1.9 V.

The *I-V* characteristics of the 3-element pseudo-resistor are shown in Fig. 17 for bias currents of 5 pA and 20 pA, at $V_{DD} = 1.7$, 1.8 and 1.9 V. Offset currents of less than 2 pA present in both characteristics are due to the leakage currents through the reverse-biased P+/N-well junctions. As can be noted, the sensitivity of the resistance to V_{DD} variations is very

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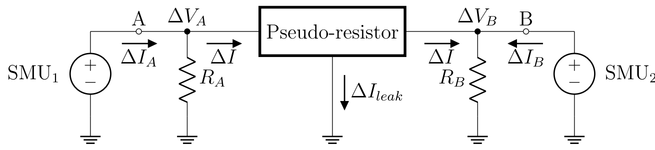

Fig. 18. Setup for measuring the resistance of the pseudo-resistor. R_A and R_B represent the leakage in the measurement setup.

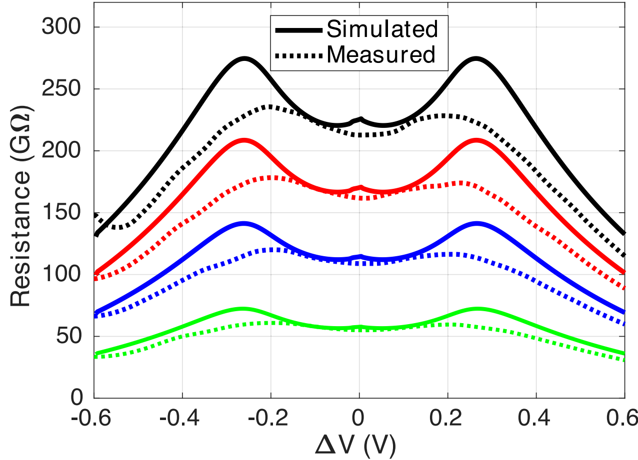

Fig. 19. Resistance of a debug pseudo-resistor. Solid lines represent simulation results, dotted lines represent measurements.

small. The power consumption for each 3-element pseudo-resistor is around 1 nW.

The setup for measuring the small-signal resistance of the pseudo-resistor is shown in Fig. 18. The measurements were taken for a common-mode voltage of $V_{DD}/2 = 0.9$ V and a differential DC voltage designated as ΔV. Voltage variations of 5 mV of opposite signs were then applied to the pseudo-resistor terminals and the resulting current variations in the source measure units (SMUs) were measured. The SMUs of an Agilent 4156C semiconductor parameter analyzer were used for the sources and measurements. The leakage in the measurement setup was removed for the calculation of the effective resistance. Since the leakage I_{leak} through the diodes is a linear function of the voltage over the operating range of the pseudo-resistor, keeping a constant common-mode voltage ($V_{DD}/2$) at the terminals of the pseudo-resistor ensures that I_{leak} is constant ($\Delta I_{leak} = 0$). Therefore, using the schematic of Fig. 18, we can write

$$\Delta I_A = \frac{\Delta V_A}{R_A} + \Delta I, \quad \Delta I_B = \frac{\Delta V_B}{R_B} - \Delta I \tag{14}$$

Using (14) in (15) yields

$$\frac{1}{R_{PR}} = \frac{\Delta I}{\Delta V} = \frac{\Delta I_A - \Delta I_B}{2\Delta V} - \left(\frac{1}{R_A} + \frac{1}{R_B}\right) \tag{15}$$

Measurements of the small-signal resistance of the debug pseudo-resistors are shown in Fig. 19. The curves show that the 3-element pseudo-resistor is (almost) linear for a voltage difference of around 200 mV between its terminals. Due to the extremely high level of noise in the measurements, a smoothing function was employed to generate the experimental curves shown in Fig. 19. The small discrepancy between the simulated curves and the measured curves in Fig. 19 in the regions close to the peaks is due to the relatively large voltage step (10 mV) used for the measurement of the small-signal resistance. This step magnitude does not allow the accurate measurement of abrupt variations of the resistance.

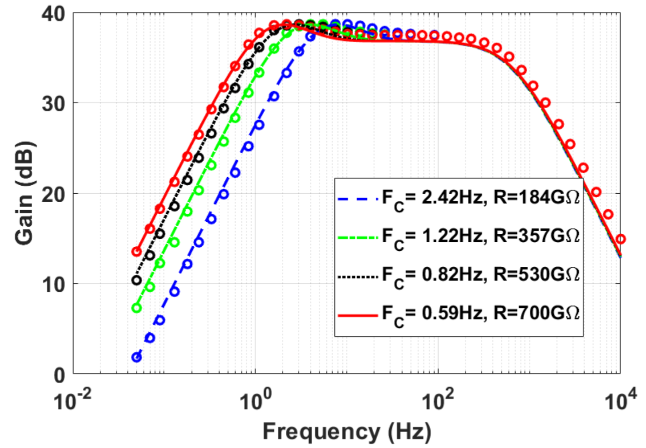

Fig. 20. Filter frequency response modulated by the pseudo-resistor: (-) lines are simulation results and (o) open circles are measurements from the test chip.

A filter prototype was designed to remove the influence of the leakage in the measurement setup on the measured resistance of the pseudo-resistor under test. When in operation, the filter prototype dissipates around 0.4 μW at 1.8 V. The designed filter uses two pseudo-resistors, each of them with ten series-connected elements. For the nominal bias currents of 20, 10, 6.7 and 5 pA, the calculated values of the filter resistances are 203, 407, 611 and 815 GΩ, respectively, at 300 K. Once the dominant pole f_{p1} has been measured and the remaining parameters in (10) are known, the value of R_{PR} can be readily determined. Measuring the value of R_{PR} by means of the filter frequency response has the advantage of avoiding errors introduced by the apparatus used for the direct measurement of the resistance. On the other hand, indirectly measuring the value of R_{PR} through the filter frequency response leads to errors due to (i) the inaccuracy of (10) and (ii) the error in evaluating the parameters of (10). Note that (10) does not take into account the distributed RC nature of the pseudo-resistor, which can be seen in Fig. 9.

Fig. 20 shows the results for the band-pass filter of Fig. 14 for a differential input signal and it can be observed that the experimental and simulation results show very close agreement. This is to be expected since, for a fixed temperature, the value of the pseudo-resistor resistance is a function of the bias current only, which, in turn, is dependent solely on the sheet specific current of the PMOS transistor, which is almost insensitive to process fluctuations.

Using (1) to obtain an estimate of the resistance gives values of 203, 407, 611 and 815 GΩ, which differ from the measurements by less than 15%. This is mainly because the bias current I_{BIAS} is higher than its expected value, which decreases the resistance. I_{BIAS} is an increasing function of the temperature in accordance with the interpolation function of the form aT^m. Based on the data in Fig. 21(a) the value of m is 1.2. The temperature coefficient of the current source is around 2,500 to 5,000 ppm/°C in the range 10 °C to 60 °C.

The distributed capacitance of the pseudo-resistor also affects the dominant pole frequency f_{p1} and, consequently,

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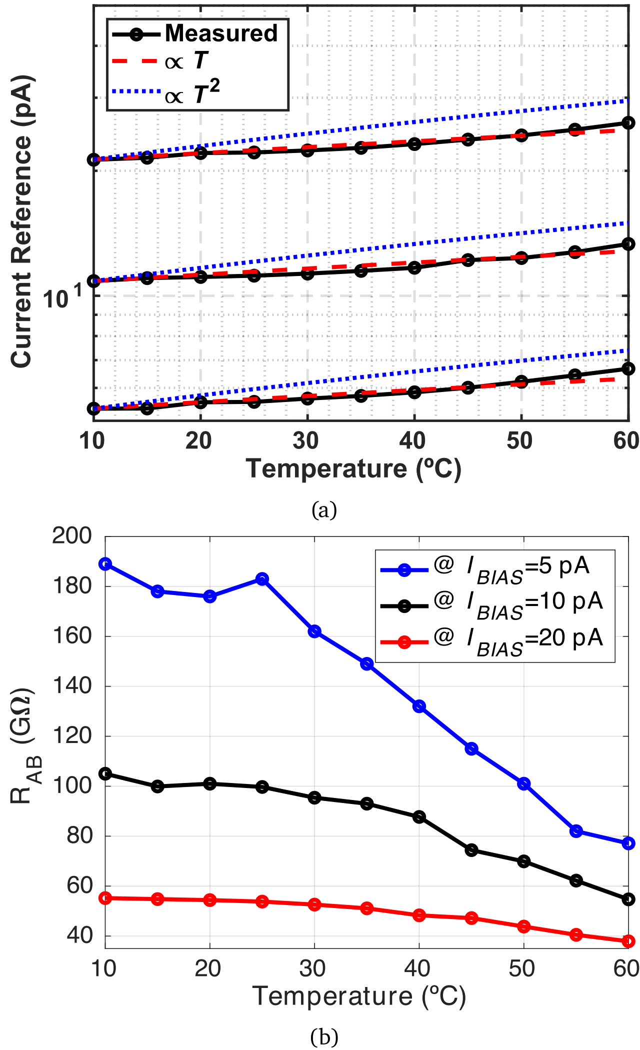

Fig. 21. (a) Current reference and (b) resistance of the debug pseudo-resistor vs temperature. The dashed lines in (a) represent terms proportional to T and to T squared.

the value of R_{PR} calculated with (10). The small peak in the frequency response of the filter is a consequence of the distributed RC nature of the pseudo-resistor.

The simulated and measured (small-signal) results for the CMRR in the pass band are around 78 dB. For the evaluation of the effect of a large common-mode signal on the response of the filter with a low cutoff frequency of 2.42 Hz, we measured the maximum common-mode voltage that could be applied without incurring a significant (visual) distortion. The filter was able to output a visually undistorted sine wave of 700 mV-peak, 298 Hz, for a common-mode input of 400 mV-peak sinusoidal signal of 100 Hz.

Further testing involved checking the dependence of both the bias current and the pseudo-resistor resistance on the temperature, which was controlled in a Tenney thermal chamber. The experimental results shown in Fig. 21 confirm that the reference current is approximately proportional to the absolute temperature. The application of (1) along with the bias current of Fig. 21 would result in resistances slightly decreasing with temperature. However, the measured resistance decreases much more rapidly with temperature than the expected results

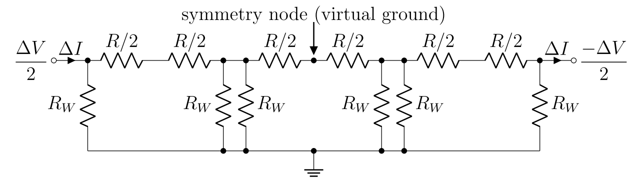

Fig. 22. Low-frequency equivalent circuit of the 3-element pseudo-resistor with the inclusion of the conductance of the N-well/P-sub junctions.

based on (1). The main cause of the discrepancy between the experimental and simulation results is the conductance of the N-well/P-sub junction in Fig. 12, which is poorly modeled in the simulator. The conductance of the N-well/P-sub junction in Fig. 12 leads to a decrease in the resistance, which is more pronounced for high temperatures. In fact, for higher temperatures, the increasing conductance of the reverse-biased P-sub/N-well junctions decreases the value of the pseudo-resistor resistance. For our realization of the pseudo-resistor, the temperature coefficient of the 3-element pseudo-resistor for a nominal bias current of 20 pA is within the range of 2,200 to 14,000 ppm/ °C for 10 °C to 60 °C.

The low-frequency model of the pseudo-resistor shown in Fig. 22 helps to explain the decrease in the differential resistance of the pseudo-resistor due to the conductance of the N-well/P-sub junction. The resistance of the 3-element pseudo-resistor, in accordance with Fig. 22, is given by

$$R_{PR} = 2\left[R_W // R\left(\frac{3R_W + 2R}{2(R + R_W)}\right)\right] \cong 2R_W // 3R\left(1 - \frac{1}{3}\frac{R}{R_W}\right) \tag{16}$$

where R_W is the AC equivalent resistance of the N-well/P-sub junction. Note that R_W is a decreasing function of the temperature. The approximation in (16) holds, since $R_W \gg R$. R_W values of around 1,700 GΩ and 200 GΩ at 20 °C and 60 °C, respectively, were measured for the 3-element pseudo-resistor. The value of R_W is independent of the value of the resistance per element (R) of the pseudo-resistor; thus, the effect of R_W is more pronounced for the highest pseudo-resistor resistance.

VI. Summary

This study demonstrates how the selection of appropriate bias circuits and technology parameters in the pseudo-resistor design can greatly lower the sensitivity to process and temperature variations, increase predictability and allow extremely high resistance values of up to hundreds of GΩ to be obtained. In our analysis we have included a problem often ignored in the design of extremely high resistances, namely the leakage current of reverse-biased pn-junctions. This leakage frequently introduces considerable errors for resistances over 50 GΩ, as observed from the measurement results for the debug pseudo-resistors. One of the main challenges in the design of pseudo-resistors with a low sensitivity to the temperature is to reduce the leakage through the N-well/P-sub junction or to devise a modified pseudo-resistor without the well/substrate junction.

A band-pass integrated filter using the designed pseudo-resistor demonstrated the tunability of the low-frequency pole

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between 0.59 Hz and 2.42 Hz. We expect that the results reported herein will be useful in the design of the extremely-low-frequency filters required for bio-signal acquisition.

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REFERENCES

[1] Clinical Neurophysiology Society, "Guideline 10: Guidelines for writing clinical evoked potential reports," *J. Clin. Neurophysiol.*, vol. 23, no. 2, pp. 180–183, Apr. 2006.

[2] D. Djekic, M. Ortmanns, G. Fantner, and J. Anders, "A tunable, robust pseudo-resistor with enhanced linearity for scanning ion-conductance microscopy," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 842–845.

[3] V. Chaturvedi and B. Amrutur, "An area-efficient noise-adaptive neural amplifier in 130 nm CMOS technology," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 4, pp. 536–545, Dec. 2011.

[4] Y. Papananos, T. Georgantas, and Y. Tsividis, "Design considerations and implementation of very low frequency continuous-time CMOS monolithic filters," *IEE Proc.-Circuits, Devices Syst.*, vol. 144, no. 2, pp. 68–74, Apr. 1997.

[5] J. Pérez-Bailón, A. Márquez, B. Calvo, N. Medrano, and M. Sanz-Pascual, "A 1V-1.75μW Gm-C low pass filter for bio-sensing applications," in *Proc. IEEE 9th Latin Amer. Symp. Circuits Syst. (LASCAS)*, Feb. 2018, pp. 1–4.

[6] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "Nanowatt, sub-nS OTAs, with sub-10-mV input offset, using series-parallel current mirrors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sep. 2006.

[7] K. Sharma, A. Pathania, R. Pandey, J. Madan, and R. Sharma, "MOS based pseudo-resistors exhibiting tera ohms of incremental resistance for biomedical applications: Analysis and proof of concept," *Integration*, vol. 76, pp. 25–39, Jan. 2021.

[8] E. Guglielmi *et al.*, "High-value tunable pseudo-resistors design," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2094–2105, Aug. 2020.

[9] D. Djekic, G. Fantner, K. Lips, M. Ortmanns, and J. Anders, "A 0.1% THD, 1-MΩ to 1-GΩ tunable, temperature-compensated transimpedance amplifier using a multi-element pseudo-resistor," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1913–1923, Apr. 2018.

[10] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, 1st ed. New York, NY, USA: Cambridge Univ. Press, 2010.

[11] R. Sanchotene Silva, L. Pereira Luiz, M. Cherem Schneider, and C. Galup-Montoro, "A test chip for characterization of the series association of MOSFETs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 8, pp. 1967–1971, Aug. 2019.

[12] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FET's for high gain and high frequency applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1094–1101, Sep. 1994.

[13] A. Tajalli, Y. Leblebici, and E. Brauer, "Implementing ultra-high-value floating tunable CMOS resistors," *Electron. Lett.*, vol. 44, no. 5, pp. 349–350, Feb. 2008.

[14] E. Bolzan, E. B. Storck, M. C. Schneider, and C. Galup-Montoro, "Design and testing of a CMOS self-biased current source," in *Proc. 26th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2019, pp. 382–385.

[15] C. Zamarreno-Ramos, T. Serrano-Gotarredona, and B. Linares-Barranco, "OTA-C oscillator with low frequency variations for on-chip clock generation in serial LVDS-AER links," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2009, pp. 2657–2660.

[16] A. F. O. Hurtado, "Design methodology of a modular CMOS ultra-low power self-biased current source," M.S. thesis, Dept. Elect. Electron. Eng., Univ. Federal de Santa Catarina, Florianópolis, Brazil, 2017. [Online]. Available: https://www.lci.ufsc.br/pdf/Dissertacao%20-%20Andres%20Fernando%20Ordonez%20Hurtado.pdf

[17] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, "A 2-nW 1.1-V self-biased current reference in CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 2, pp. 61–65, Feb. 2005.

[18] P. Heim, S. Schultz, and M. A. Jabri, "Technology-independent biasing technique for CMOS analog micropower implementation of neural networks," in *Proc. 4th IEEE Int. Workshop Cellular Neural Netw. Appl.*, Apr. 1995, pp. 9–12.

[19] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[20] Y. Tsividis, *Operation Modeling MOS Transistor*, 2nd ed. New York, NY, USA: McGraw-Hill, 1999.

[21] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.

[22] A. C. de Oliveira, D. Cordova, H. Klimach, and S. Bampi, "Picowatt, 0.45-0.6 V self-biased subthreshold CMOS voltage reference," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 12, pp. 3036–3046, Dec. 2017.

[23] R. Puddu *et al.*, "A precision pseudo resistor bias scheme for the design of very large time constant filters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 762–766, Jul. 2017.

[24] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[25] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad, and A. M. Sodagar, "Analysis and design of tunable amplifiers for implantable neural recording applications," *IEEE J. Emerg. Sel. Topics Circuits Syst*, vol. 1, no. 4, pp. 546–556, Dec. 2011.

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