Design of a Temperature-Compensated Voltage Reference based on the MOSFET Threshold Voltage

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ABSTRACT

In this paper, the analysis and design of a temperature-compensated reference based on the MOSFET threshold voltage is presented. The circuit, which core is a specific current generator, explores the temperature behaviour of the gate-bulk voltage of an NMOS transistor. The transistor is chosen to operate in a region where a PTAT voltage compensates the CTAT characteristic of the threshold voltage. The design is validated through simulation results in different standard CMOS processes. For a low power 0.18 μm CMOS process, the voltage reference is 0.912 V and the current reference is 78.68 nA. The temperature coefficient of the voltage reference is 36 ppm/℃ in the range from -20 to 80 ℃. The line sensitivity is 775 ppm/V for a supply voltage range of 1.1 - 1.8 V, and the power supply rejection ratio (PSRR) is -55 dB at 1 kHz. The power dissipation is 346 nW at room temperature. The chip area is 0.0084 mm^2.

Categories and Subject Descriptors

B.7.0 [**Integrated Circuits**]: General—*advanced.*

General Terms

Design.

Keywords

CMOS, voltage-current reference, analog design, compact model, low-power low-voltage.

1. INTRODUCTION

Voltage and current references are some of the most important buildings blocks in integrated circuits. Their use covers operational amplifiers, comparators, A/D and D/A converters. Traditionally, bandgap references are widely used in integrated circuits [3, 11, 17]. Depending on the particular topology the output voltage is around 1.2 to 1.3 V, which is close to the theoretical bandgap voltage of silicon at 0 K. Taking advantage of the parasitic bipolar transistors present in CMOS standard technology this kind of circuit was adapted to the CMOS process. However, the advance of the technology and the search for ultra low power circuits results in a reduction of the supply voltage to sub-1V operation, thus reducing the applicability of the bandgap references. One approach to obtain a bandgap reference with sub-1-V operation is presented in [2]. Its drawback is the necessity of resistors of several hundred megohms to achieve low-power operation.

In the last years, the focus of the reference circuits is pointing to the CTAT (complementary to absolute temperature) behaviour of the MOSFET threshold voltage [7]. A great number of papers were published following this new direction [1, 6, 9, 12, 15]. However, none of these papers use compact model equations, confining the design to the MOSFET operating in either weak or strong inversion, thus, hindering designers from finding the best trade-off between power consumption and circuit area. This work explores compact model equations using the inversion coefficient to help the design of temperature-compensated references. A simple design procedure, applied to the design of a low-power, low-voltage reference in two different CMOS standard technologies is presented. Our circuit uses the resistor-less specific current generator described in [4] to generate a voltage reference.

This paper is organized as follows: after the introduction, a review of a compact MOSFET model is presented in Section 2. Then, in Section 3, the operating principle and the equations for temperature compensation is shown. Section 4 is dedicated to develop the circuit configuration and design. Simulation results are presented in Section 5 and finally, in Section 6 some final remarks are elaborated.

2. MOSFET MODEL

According to the all-region MOSFET model, the drain current of a long channel transistor can be split into the symmetric forward (I_F) and reverse (I_R) components, which are dependent on the transistor sheet specific current (I_{SQ}), aspect ratio ($S = W/L$), and forward (i_f) and reverse (i_r) inversion levels.

$$I_D = I_F - I_R = I_{SQ}\, S\, (i_f - i_r) \tag{1a}$$

$$I_{SQ} = \mu\, C'_{ox}\, n\, \frac{\phi_t^2}{2} \tag{1b}$$

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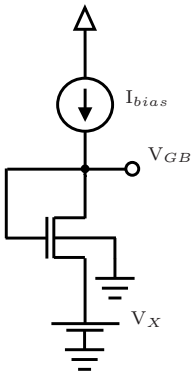

Figure 1: NMOS transistor in diode connection.

The sheet specific current (I_{SQ}) is a technological parameter described by the mobility (μ), the gate-oxide capacitance/area (C'_{ox}), the slope factor (n) and the thermal voltage (ϕ_t). The relationship between the inversion levels and the terminals voltages is the UICM equation given by

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{i_{f(r)} + 1} - 2 + \ln(\sqrt{i_{f(r)} + 1} - 1) \quad (2a)$$

$$\frac{V_P - V_{S(D)}}{\phi_t} = F\left(i_{f(r)}\right) \quad (2b)$$

where V_P is the transistor pinch-off voltage. In (2a), all the voltages are referenced to the bulk.

When the transistor is saturated, the reverse current is negligible with respect to the forward current and the drain current is almost independent of the drain voltage, i.e.

$$I_D \simeq I_{SQ}\, S\, i_f \quad (3)$$

In minimum saturation drain-source voltage (V_{DSsat}) can be approximated by

$$V_{DSsat} \simeq \phi_t \left(\sqrt{i_f + 1} + 3\right) \quad (4)$$

More details regarding (1)-(4) can be found in [8, 14].

3. OPERATION PRINCIPLE

The voltage reference is an NMOS transistor connected as a diode, biased by a current source I_{bias}, with its source terminal connected to a voltage source V_X, as illustrated in Fig. 1. This structure was used in different works [12, 15] to generate a temperature compensated voltage reference. They explore the fact that the gate-bulk voltage (V_{GB}) has complementary dependences on the threshold voltage (V_{TH}) and on the drain current. While the threshold voltage has a CTAT behaviour, the increasing current gives a PTAT (proportional to absolute temperature) behaviour to V_{GS}. We take advantage of the MOSFET compact model equations to describe the design of this kind of temperature compensated voltage reference, using the transistor inversion level as a design variable to compensate the threshold voltage dependence on the temperature.

Considering the NMOS transistor operating in saturation, the I-V characteristic for all operating regions of a long channel device can be obtained from (2b),

$$V_P - V_X = \phi_t F(i_f) \quad (5)$$

At this point, two linear approximation are made to obtain simple equations for the reference voltage and its dependence on the temperature. The first one, is the linear approximation of the pinch-off voltage around $V_{GB} \simeq V_{TH}$ giving by,

$$V_P \simeq \frac{V_{GB} - V_{TH}}{n} \quad (6)$$

where n is the slope factor [8].

The second linear approximation is about the dependence of the transistor's threshold voltage on the temperature, which is considered to decrease linearly, represented by,

$$V_{TH} = V_{TH0} - \kappa_T\, T \quad (7)$$

where V_{TH0} is the extrapolated threshold voltage at T = 0 K and κ_T is the temperature coefficient for V_{TH}. For a first hand-made calculation κ_T can be inferred from the BSIM3V3 model parameter κ_{T1} [16].

Applying (6) and (7) in (5), the reference voltage (V_{REF}) can be expressed as,

$$V_{REF} = V_{GB} = V_{TH0} - \kappa_T T + n\left[V_X + \phi_t F(i_f)\right] \quad (8)$$

In [6] the V_X voltage is set to zero, but we can set this node to a voltage with a PTAT characteristic, allowing the temperature compensation with lower values of inversion level as shown in [12, 15]. This can be achieved if V_X is proportional to ϕ_t ($V_X = \beta\,\phi_t$). Considering V_X with a PTAT characteristic, expression (8) can be modified to

$$V_{REF} = V_{TH0} - \kappa_T T + n\phi_t\left[\beta + F(i_f)\right] \quad (9)$$

In order to have a temperature compensated voltage reference, the following condition must be satisfied:

$$\frac{\partial V_{REF}}{\partial T} = 0 \quad (10)$$

From (9), it is easy to demostrate that this condition is obtained when the CTAT term $\kappa_T T$ equals the PTAT term $n\phi_t\left[\beta + F(i_f)\right]$, inferring the existence of a i_f value which cancel the temperature dependence of V_{REF}.

$$F(i_f) = -\left(\frac{\kappa_T T}{n\phi_t} + \beta\right) = -\left(\frac{\kappa_T q}{n k_B} + \beta\right) \quad (11)$$

The design challenge is to produce a constant inversion level over the operating temperature range to get a continuous compensation. To achieve this behaviour let us analyze the definition of the inversion level and its temperature dependence. According to (1a) the forward inversion level of a saturated MOSFET depends on the drain current (I_D), the sheet specific current (I_{SQ}) and the aspect ratio ($S = W/L$). Neglecting variations of the aspect ratio and the slope factor (n) with the temperature, to get an inversion level independent from temperature variations, the drain current must be proportional to the specific current.

4. CIRCUIT CONFIGURATION

The schematic of the voltage reference circuit, illustrated in Fig. 2, is the self-biased current source (SBCS) presented in [4], which generates a current proportional to the specific current. The cores of the SBCS are the self-cascode MOSFET circuit (SCM - transistors M_1, M_2) and the cascode voltage follower current mirror circuit (CVFCM - transistors

Table 1: Transistor Sizes for the 0.18-μm and 0.50-μm CMOS voltage reference.

Process	0.5-μm CMOS	0.18-μm CMOS
Transistor	Value (W / L)	
M_1	3 μm / 40 μm = (3 μm / 20 μm) $\times$ 1/2	3.5μm / 60 μm = (3.5 μm / 20 μm) $\times$ 1/3
M_2	3 μm / 100 μm = (3 μm / 20 μm) $\times$ 1/5	3.5 μm / 80 μm = (3.5 μm / 20 μm) $\times$ 1/4
M_3	720 μm / 2 μm = (30 μm / 2 μm) $\times$ 24	480 μm / 2 μm = (20 μm / 2 μm) $\times$ 24
M_4	60 μm / 2 μm = (30 μm / 2 μm) $\times$ 2	40 μm / 2 μm = (20 μm / 2 μm) $\times$ 2
M_5-M_6	20 μm / 20 μm = (20 μm / 20 μm) $\times$ 1	20 μm / 20 μm = (20 μm / 20 μm) $\times$ 1
M_7-M_8	50 μm / 20 μm = (10 μm / 20 μm) $\times$ 5	20 μm / 20 μm = (20 μm / 20 μm) $\times$ 1
M_9	100 μm / 20 μm = (10 μm / 20 μm) $\times$ 10	40 μm / 20 μm = (20 μm / 20 μm) $\times$ 2

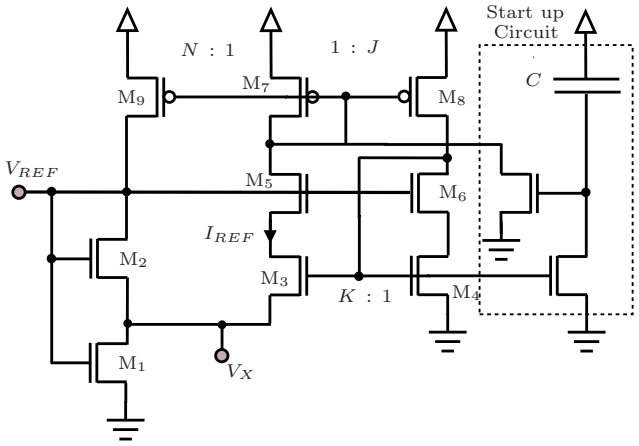

Figure 2: Schematic of the proposed voltage reference circuit.

M_3, M_4, M_5, M_6, M_7, and M_8). Transistor M_9 acts as a current source to bias the SCM. The bulks of the NMOS transistors are connected to ground, while those of the PMOS transistors to V_{DD}. The reference voltage is obtained from $V_{GB}(= V_{REF})$ of the SCM. M_2 is designed to operate at an inversion level (i_f) that compensates the CTAT behaviour of the threshold voltage (V_{TH}), according to (11).

4.1 Circuit Design

CMOS standard technologies 0.50-μm and 0.18-μm were employed for the design of the voltage references, as in Fig. 2. The threshold voltage and specific current were extracted using the methodology described in [8], obtaining 0.858 V and 0.623 V for V_{TH} and 63 nA and 107 nA for I_{SQ}, for the 0.50-μm and 0.18-μm technologies respectively. All the design equations are described in [4]. The operating point of the SBSC circuit is established when the SCM and CVFCM have the same V_X voltage, which depends on the ratio of currents determined by the current mirrors. The reference current (I_{REF}) generated for both SBCS was set to 80 nA. In our design the CVFCM is operating in weak inversion. The value of V_X was set to $3\phi_t$. Applying (11) for $V_X = 3\phi_t$ ($\beta = 3$), $n = 1.2$ and the κ_T of the technologies ($\kappa_{T\,0.50\mu m}$ = 1.528 mV/K - $\kappa_{T\,0.18\mu m}$ = 0.907 mV/K), the inversion levels were 120 and 30 for the 0.50μm and 0.18μm technologies, respectively. With the values of the inversion levels and N, we could calculate the aspect ratio of transistors M_1 and M_2. N was set to 2 with the aim of reducing the area of the SCM. Transistor areas were chosen greater than 60 μm^2 to reduce mismatch effects, with a channel length of at least 2 μm. Some adjustments had to be done with the aid of the simulator for the determination of final transistor dimensions. The main reasons for this fine tuning are: approximation (6), valid for inversion levels around $i_f = 3$, and the uncertainty in the n value and its shift with temperature, which has an important impact on the determination of i_f when (11) is applied. Table 1 gives transistor widths (W) and lengths (L).

4.2 Minimum Supply Voltage

The minimum supply voltage (V_{DDmin}) is determined by the constraints imposed by the two leftmost branches in Fig. 2, which can be written as

$$V_{DDmin} > \max\{|V_{DSsat,M_9}| + V_{REF}, \\ |V_{GS,M_7}| + V_{DSsat,M_5} + V_{DSsat,M_3} + V_X\} \quad (12a)$$

where the saturation voltages of M_3, M_5 and M_9 are lower than 125 mV since all transistors operate with $0.5 < i_f < 2$. The right branch is not in the critical path for the minimum power supply determination because transistor M_4 is set to weak inversion whereas M_1 is set to strong inversion, imposing the relationship $V_{GS,M_1} > V_{GS,M_4}$. V_X was chosen equal to $3\phi_t$ and M_7 has the same inversion level as M_9 ($i_f \simeq 1$); therefore, the voltage $V_{GS,M_7} \simeq V_{TH,P}$. With the last design considerations expression (12a) can be approximated by (12b).

$$V_{DDmin} > \max\{V_{REF} + 125\,\text{mV}, |V_{TH,P}| + 350\,\text{mV}\} \quad (12b)$$

Although (12b) is a rough approximation, it is very useful for predicting the minimum supply voltage required to turn on the current reference circuit.

5. SIMULATION RESULTS

The designed reference circuits are validated with Cadence ® simulations, using BSIM3V3 model provided by the foundries. DC and AC simulations were run to extract the nominal current and voltage reference values, the temperature coefficient (TC), the line sensitivity (LS), and the power supply rejection ratio (PSRR). Figure 3 shows the

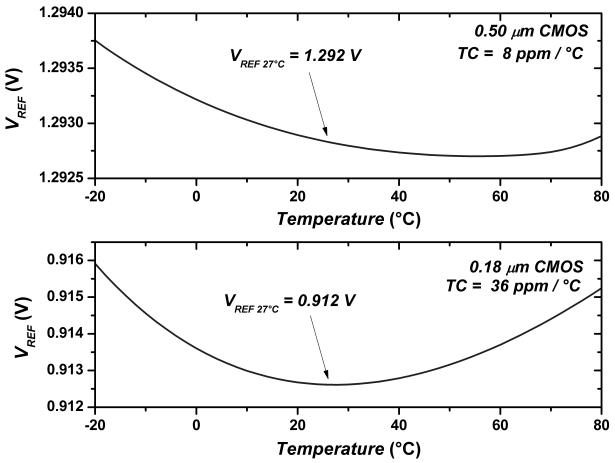

Figure 3: Simulated output voltage (V_{REF}) as a function of the temperature. The voltage reference is 0.912 V for the 0.18-μm and 1.292 V for the 0.50-μm CMOS technology respectively.

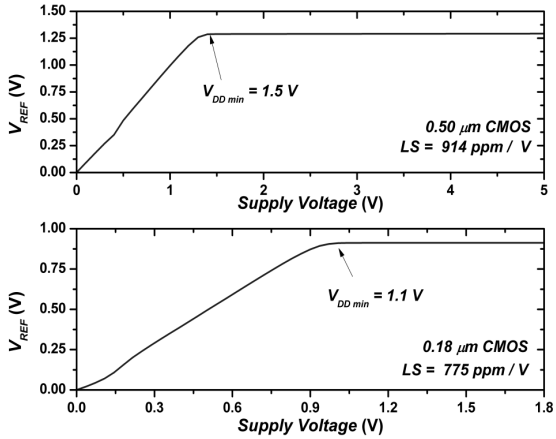

Figure 4: Simulated output voltage (V_{REF}) at room temperature as a function of power supply. The minimum supply voltage is 1.1 V for the 0.18-μm and 1.5 V for the 0.50-μm CMOS technology respectively.

Table 2: Simulated Performance of the designed low-power CMOS voltage reference.

Process	0.50-μm CMOS	0.18-μm CMOS
Temp. range	–20 - 80 ℃	–20 - 80 ℃
V_{DD}	1.5 - 5 V	1.1 - 1.8 V
$\overline{V_{REF}}$	1.292 V	0.912 V
$\overline{I_{REF}}$	79.05 nA	78.68 nA
Power	465 nW (@1.5 V)	346 nW (@1.1 V)
	Room temp.	Room temp.
TC (V_{REF})	8 ppm/℃	36 ppm/℃
LS (V_{REF})	912 ppm/V	775 ppm/V
LS (I_{REF})	0.44 %/V	1.35 %/V
PSRR	-59 dB (@100 Hz)	-72 dB (@100 Hz)
	-49 dB (@1 kHz)	-55 dB (@1 kHz)
Chip area	0.027 mm^2	0.0084 mm^2

simulated reference voltage as a function of the temperature in the range from -20 to 80 ℃. The nominal reference voltage was 1.292 mV for the 0.50-μm and 912.5 mV for the 0.18-μm CMOS technologies. The calculated temperature coefficients were very small 8 ppm/℃ and 36 ppm/℃, respectively. The nominal reference current was 79.05 nA for the 0.50-μm and 78.68 nA for the 0.18-μm CMOS reference, both very close to the design value of 80 nA. Figure 4 exhibits the simulated reference voltage at room temperature as a function of the supply voltage. The minimum supply voltages were 1.4 V for the 0.50-μm and 1.1 V for the 0.18-μm CMOS technologies, obtaining a line sensitivity of 914 ppm/V and 775 ppm/V, respectively. All results are sumarized in Table 2.

Table 3: Corner Simulations Results.

Process	0.50-μm CMOS		0.18-μm CMOS	
	V_{REF}	TC	V_{REF}	TC
Typ[a]	1.292 V	8 ppm/℃	0.912 V	36 ppm/℃
WCS[b]	1.371 V	19 ppm/℃	0.947 V	37 ppm/℃
WCP[c]	1.217 V	36 ppm/℃	0.881 V	38 ppm/℃

[a] Typical Model Parameters.
[b] Worst Case Speed Model Parameters.
[c] Worst Case Power Model Parameters.

To study the dependence of the circuit outputs on process variations, corners and Monte Carlo simulations were performed. For the Monte Carlo analysis, mismatch and process variations were assumed, using a Gaussian distributions for the statistical parameters determination considering a 6σ range. Table 3 presents the corners simulations results, showing a great dispersion of the V_{REF} value due to process variations. However, the V_{REF} thermal coefficient did not present significant variation, explained by the fact that both the threshold voltage thermal coefficient and the inversion level have low dependence on process variations.

Monte Carlo simulations, depicted in Fig. 5 and Fig. 6, show a standard deviation of 34 mV and 10 mV, presenting a variation coefficient (σ/μ) of 2.6 % and 1.1 %, for the 0.50-μm CMOS and 0.18-μm CMOS respectively.

6. CONCLUSIONS

To validate the procedure, two different CMOS standard technologies were used to design current-voltage references. The simulation results agreed very well with theory; moreover, a great reduction in area was achieved comparing with published work [5, 6, 10, 13, 15]. Variations in both the reference voltage/current and in the temperature coefficient due to process variation were evaluated through Monte Carlo

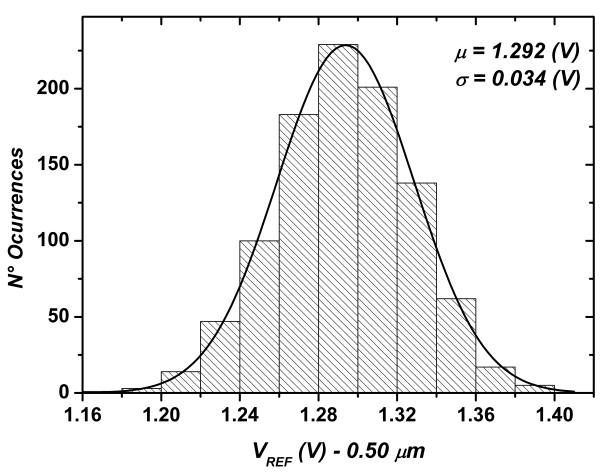

Figure 5: Distribution of the voltage reference obtained from Monte Carlo simulations for the 0.50-μm circuit (1000 runs).

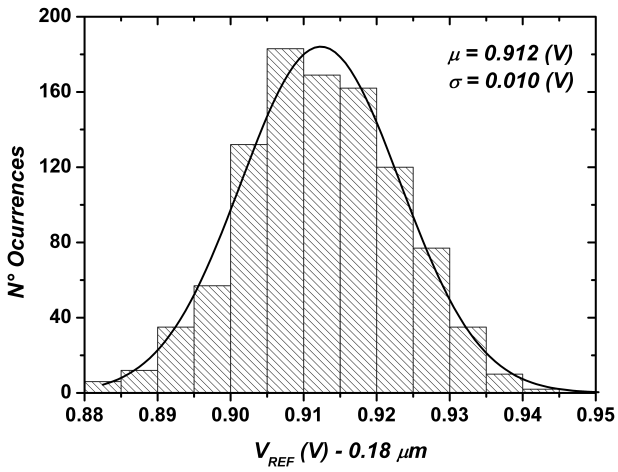

Figure 6: Distribution of the voltage reference obtained from Monte Carlo simulations for the 0.18-μm circuit (1000 runs).

simulations, which showed a small deviation of the temperature coefficient in the tested technologies. Variations in the reference value could be corrected through a trimming approach.

7. ACKNOWLEDGMENTS

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