DIRECT DETERMINATION OF THRESHOLD CONDITION IN DG-MOSFETS FROM THE g_m/I_D CURVE

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ABSTRACT

In this work we apply the current-based threshold voltage definition (equality between the drift and diffusion components of drain current) to intrinsic symmetric double-gate MOSFETs. We show that the half maximum point of the g_m/I_D (transconductance-to-current ratio) curve in the linear region corresponds exactly to the condition $I_{Ddrift} = I_{Ddiff}$ when mobility variation is neglected. Numerical simulations show that the threshold voltages determined from the g_m/I_D curve and from the $I_{Ddrift} = I_{Ddiff}$ condition differ by about $\phi_t/2$ (one half of the thermal voltage) when considering realistic mobility variations. Simulation results show that the threshold voltages determined with the g_m/I_D procedure are close to those obtained with the $Y (= I_D/\sqrt{g_m})$ function method for a considerable range of silicon film thicknesses, channel lengths, and temperature values. The current-based procedure has also been successfully applied experimentally to a FinFET over a wide temperature range.

Keywords: DG-MOSFET, Parameter Extraction, Threshold Voltage.

1. INTRODUCTION

Double-Gate (DG) MOSFETs with undoped body have been proposed for nanometer size CMOS [1-2]. Due to the improved electrostatic control of the channel charges, DG transistors present nearly ideal subthreshold slope of 60mV/decade at room temperature and reduced short-channel effects. Additionally, the fluctuations in characteristics due to random discrete dopants are avoided. Even if the threshold voltage is the main parameter to model the on-off transition in MOSFETs, there is no consensus about its definition for intrinsic channel devices [3].

Several definitions have been proposed for the threshold voltage of undoped MOSFETs [3], most of them failing to provide simultaneously a physical meaning, unambiguity in the extraction methodology, and a proper description of the dependence on the silicon and insulator thicknesses. In this paper we show that the current-based definition of threshold voltage (equality between the drift and diffusion components of drain current), previously introduced and applied to conventional bulk MOSFETs [4-7], is very appropriate for undoped symmetric double-gate MOSFETs.

The difficulty in determining the threshold voltage is due to the fact that no critical point can be directly identified in the current voltage characteristic as the turn on or threshold point. Although there are two clearly different conduction regimes for the MOSFET, the exponential (weak inversion) and the approximately linear/quadratic (strong inversion) regimes, the transition between them is very gradual, corresponding to two orders of magnitude of variation in the current [8]. The threshold voltage is somewhere in this transition region, its precise location depending on the adopted definition.

To obtain a directly observable point (e.g., a minimum of a curve) associated with the threshold condition, derivatives of the current-voltage characteristic must be calculated. A method using a first logarithmic derivative only, the g_m/I_D (transconductance-to-current ratio) method, has been proposed [5, 6, 9] and has been shown to be consistent with the thermal charge density definition ($-C'_{ox}\phi_t$, see Appendix A) of the threshold voltage [4-6].

In this study, we apply the current-based definition of threshold to undoped body symmetric DG-MOSFETs (Section 2), show examples of the g_m/I_D procedure for extracting the threshold voltage of undoped body symmetric DG-MOSFETs (Section 3), and compare this extraction procedure to others (Section 4).

2. CURRENT-BASED DEFINITION OF THRESHOLD

The weak inversion current in MOSFET is essentially due to the carrier diffusion, whereas the strong inversion current is mostly due to the carrier drift.

At some point in the transition region between weak and strong inversion, the drift and diffusion components of the current are equal. Taking this point as the threshold is very appropriate [4].

In order to obtain general results we will use the Pao-Sah model of the MOSFET which includes both the drift and diffusion transport mechanisms, and gives an exact model of the long-channel MOSFET. In the Pao-Sah model [10], the drain current in an n-channel MOSFET is

$$I_D = I_{Ddrift} + I_{Ddiff} = -\alpha\mu W Q_e' \frac{dV_C}{dy} \tag{1}$$

where μ is the electron mobility, Q_e' is (one half of) the mobile charge density in single-gate (symmetric double-gate) devices, W is the channel width and V_C is the channel voltage (quasi-Fermi potential of electrons). The factor α is equal to 1 for a conventional planar MOSFET and is equal to 2 for a symmetric DG-MOSFET (Fig. 1).

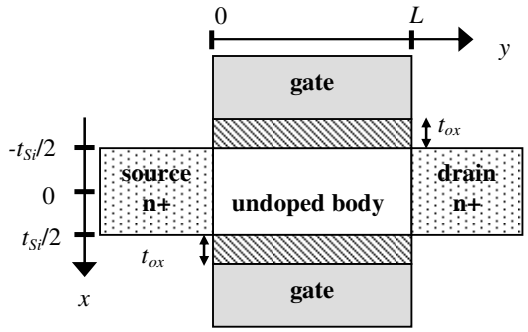

Figure 1 – Schematic diagram of an N-channel intrinsic symmetric DG MOSFET.

The diffusion component of the current is

$$I_{Ddiff} = \alpha\mu W \phi_t \frac{dQ_e'}{dy} \tag{2}$$

Using (1) and (2), the condition I_{Ddrift}=I_{Ddiff} is fulfilled if

$$-\alpha\mu W Q_e' \frac{dV_C}{dy} = 2\alpha\mu W \phi_t \frac{dQ_e'}{dy} \tag{3.a}$$

which can be rewritten as

$$\frac{\partial Q_e'}{\partial V_C}\frac{1}{Q_e'} = -\frac{1}{2\phi_t} \tag{3.b}$$

Since the channel charge is controlled by the difference between the gate (V_G) and the channel voltages (see Appendix A), $\partial Q_e'/\partial V_C = -\partial Q_e'/\partial V_G$, and, thus, (3.b) is equivalent to

$$\frac{\partial Q_e'}{\partial V_G}\frac{1}{Q_e'} = \frac{1}{2\phi_t} \tag{4}$$

for an intrinsic symmetric double-gate MOSFET.

In the linear region ($V_{DS} \leq 2\phi_t$), the Pao-Sah integral expression of the drain current in conventional planar ($\alpha = 1$) or symmetric DG-MOSFET ($\alpha = 2$) reduces to:

$$I_D = \alpha\mu\frac{W}{L}Q_e'(V_G, V_S)V_{DS} \tag{5}$$

where V_S and V_{DS} are the source and drain-to-source voltages, respectively.

Thus the transconductance-to-current ratio is given by:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_G} = \frac{\partial \ln \mu}{\partial V_G} + \frac{\partial \ln Q_e'(V_G, V_S)}{\partial V_G} \tag{6}$$

where g_m is the gate transconductance.

In weak and in the low moderate inversion regions the carrier charge density varies (quasi) exponentially with the gate voltage. Since the mobility dependence on the gate voltage is much lower than the charge dependence we can write

$$\frac{g_m}{I_D} = \frac{\partial Q_e'(V_G, V_S)}{\partial V_G} \frac{1}{Q_e'} \tag{7}$$

for the weak and the low moderate inversion regions.

Since the double-gate MOSFET has an ideal subthreshold slope (see Appendix A) the maximum value of g_m/I_D in the linear region is $1/\phi_t$. According to (3.b) and (7), the condition $I_{Ddrift}=I_{Ddiff}$ in the linear region is equivalent to:

$$\frac{g_m}{I_D} \cong \frac{1}{2\phi_t} \tag{8}$$

Therefore, the current-based definition of threshold voltage is related to an unambiguous feature of the I-V characteristic in the linear region: a drop of 50 % in g_m/I_D relative to its maximum value. The gate voltage at this point corresponds to the (equilibrium) threshold voltage.

3. g_m/I_D EXTRACTION PROCEDURE OF THRESHOLD VOLTAGE

The test device should be connected as shown in Fig. 2, where $V_S = 0$ and V_D is very small ($2\phi_t$ or below). In Fig. 2, the g_m/I_D versus V_G characteristic has been obtained through three-dimensional numerical simulation [13], for a 0.3 μm-long N-channel double-gate device with oxide thickness t_{ox} = 2 nm, silicon film thickness t_{Si} = 20 nm, p-

type light doping concentration of $1x10^{15}$ cm^{-3}, silicon film height H_{Si}=60 nm, gate metal work function of 4.7 eV, drain and source diffusion lengths of 0.15 μm, donor concentration at source and drain $N_D = 5x10^{20}$ cm^{-3} and considering the mobility dependence with the horizontal and vertical electric fields. We have adopted $V_S = 0$ and $V_{DS} = 50$ mV (and $T = 300$ K). Condition (8) is represented by the circle.

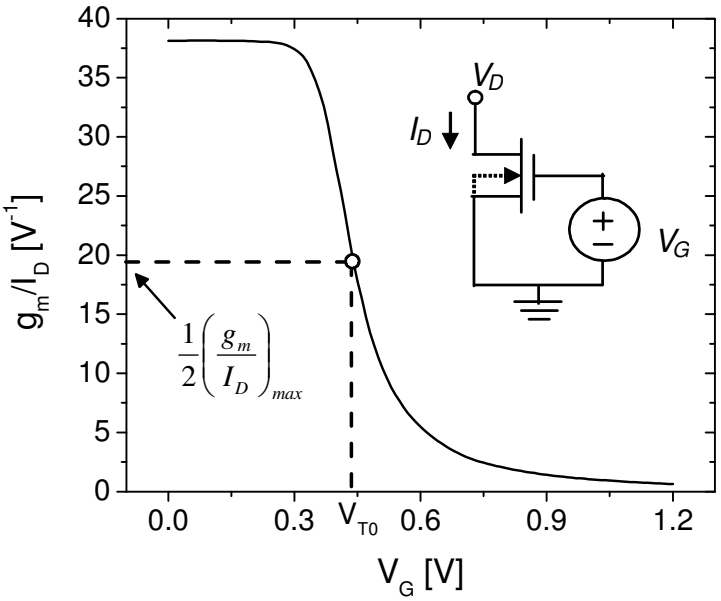

Figure 2 – Simulated transconductance-to-current ratio for $V_{DS} = 50$ mV and $V_S = 0$. V_{T0} is the value of V_G for $g_m/I_D=0.5(g_m/I_D)_{max}$. $t_{ox} = 2$ nm, $t_{Si} = 20$ nm, $L = 0.3$ μm.

To demonstrate the application of the proposed definition for the threshold voltage extraction Fig. 3 presents the integral of the drift and diffusion current components as a function of the gate voltage for devices with the same parameters than that of Fig. 2, with the exception of L = 1 μm and t_{Si} of 10 nm and 40 nm.

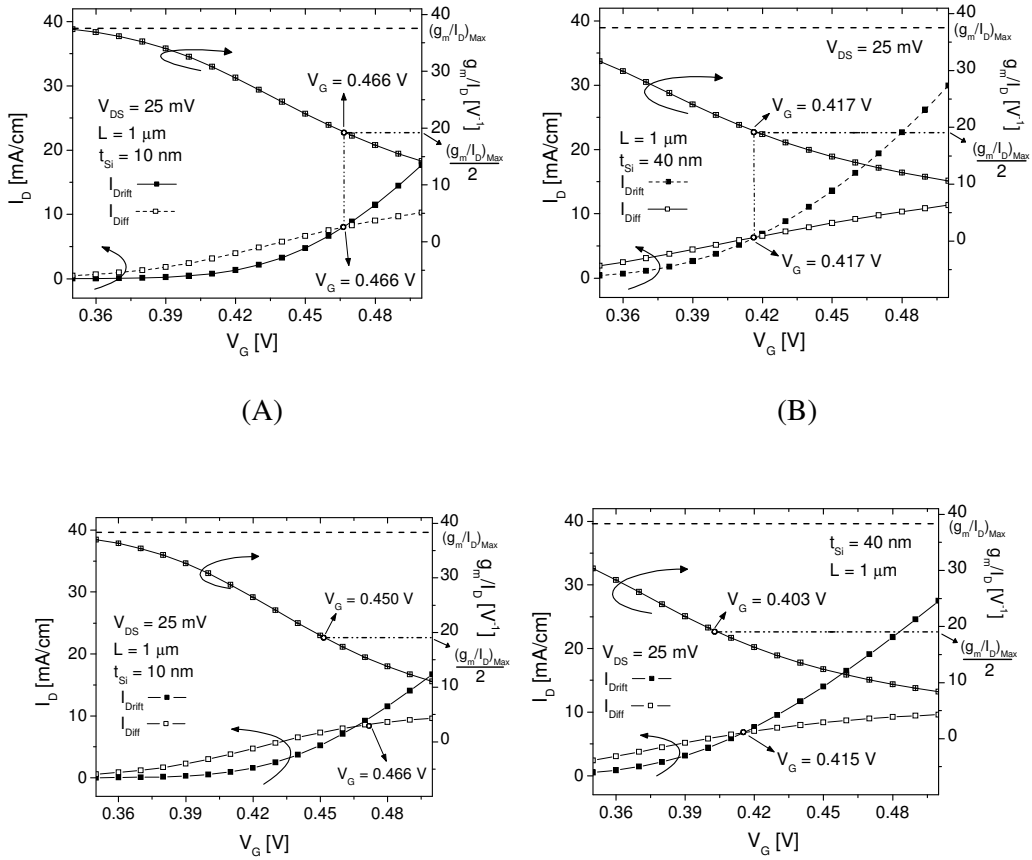

Figure 3 – Curve of the drift and diffusion components of the drain current (left Y-axis) and g_m/I_D (right Y-axis) *vs.* the gate voltage, comparing the threshold condition when g_m/I_D ratio drops to the half of its maximum value and when I_{Ddrift}=I_{Ddiff} considering a constant mobility (A, B) and the mobility degradation due to the vertical and lateral electric fields (C, D) for devices with t_{Si} = 10 nm and 40 nm, respectively.

For the device with t_{Si} = 10 nm the influence of quantum mechanics has been accounted for. Also, in the same figure, the extracted g_m/I_D characteristic is shown. In Fig. 3A and B the mobility degradation with the electric field has been neglected and in Fig. 3C and D the mobility degradation caused by both horizontal and vertical electric

fields has been included.

When mobility is assumed to be constant, the equality between I_{Ddrift} and I_{Ddiff} perfectly matches the g_m/I_D procedure for threshold voltage definition. On the other hand, if the mobility degradation is considered in the simulation, a small diference between the equality of both current components and the g_m/I_D procedure can be observed. This difference reaches 16 mV for t_{Si} = 10 nm and increases as t_{Si} is reduced.

The difference between the definitions of the threshold voltage from (i) the equality between the diffusion and drift currents (equation (4)) and (ii) the transconductance-to-current ratio (equation (6)) can be explained as follows. In definition (i), the measurement of the threshold voltage depends only on how the channel charge is dependent on the gate voltage, being independent on how mobility varies with the transversal electric field (see equation (4)). On the other hand, in definition (ii) one can see that the measurement of the threshold voltage is dependent not only on the charge variation with the gate voltage but also on the mobility dependence on the transversal field.

One typical feature of narrow (or thin) undoped DG MOSFETs is the occurrence of volume inversion [14] for low electron charge density. For gate voltages above the threshold voltage, the flow of carriers is more pronounced close to the interface between the silicon and insulator while for gate voltages below threshold, the flow of carriers tends to be more homogeneous across the semiconductor film. As a result of the volumetric conduction, the mobility for low carrier concentration is higher than that for the case of surface conduction [14]. This variation in the carrier mobility is the main responsible for the slight discrepancy between the definitions of the threshold voltage based on equation (4) and equation (6).

In Fig. 4, the current-based threshold voltage is compared with other definitions from the literature, namely the charge-based criterion described in [11] (reviewed in [12]), the condition $\partial Q_e'/\partial \phi_S = C_{ox}'$ [2] and the crossover from one type of surface potential behavior to another [12].

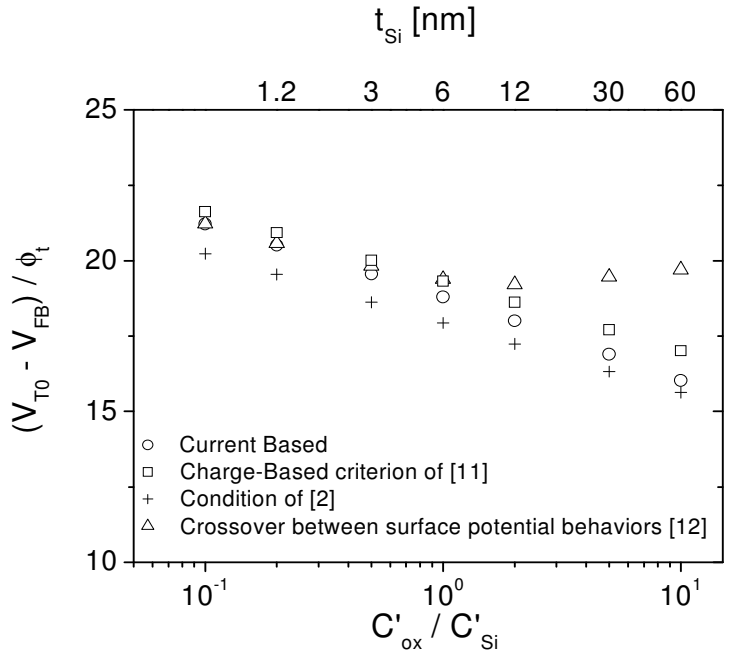

Figure 4 – Threshold voltage of intrinsic symmetric DG MOSFET, calculated from: current-based (circles); charge-based criterion of [11] (squares); condition of [2] (crosses); crossover between surface potential behaviors (triangles) [12]. t_{ox} = 2 nm.

According to the charge-based criterion, the threshold voltage is the value of the gate voltage for which the mobile charge density vanishes as extrapolated from strong inversion [11]. The condition $\partial Q_e'/\partial \phi_S = C_{ox}'$ for threshold definition is based on a capacitive model that locates V_T in moderate inversion [2]. According to the definition based on the crossover from one type of surface potential behavior to another, the

threshold voltage is the value of V_G for which the derivatives of ϕ_S and $-Q'_e/C'_{ox}$ with respect to V_G are equal to each other, and thus to 1/2 [12].

The three definitions agree very well except for thick silicon films where the crossover criterion is less sensitive to the ratio between oxide and silicon capacitances.

4. COMPARISON BETWEEN V_T EXTRACTION PROCEDURES

In this Section the proposed g_m/I_D extraction procedure, the second difference of the logarithm (SDL) method [12] and the *Y* function method [15-16] are compared as applied to symmetric double-gate MOSFETs with lightly doped body. The SDL method is a well-known procedure to determine the (approximate) threshold voltage and has as the major drawback the need to calculate the usually extremely noisy second-order derivative of the current. The *Y* function method, in which the linear region of the curve $Y = I_D/\sqrt{g_m}$ vs. V_G is extrapolated to the *x* axis, has the advantage of removing the series resistance effect.

Our procedure also minimizes the effect of series resistances since they are much lower than the transistor channel resistance in weak and in the lower moderate inversion regions. In effect, the minimum channel sheet resistance in our procedure is $1/(\mu n C'_{ox} \phi_t)$, which is of the order of tens of kilo-ohms, even for advanced technologies.

Fig. 5 compares the threshold voltage determined through the SDL, g_m/I_D and *Y* function procedures applied to simulated characteristics with variable silicon film thickness. The threshold voltage calculated using expressions (A6) (with ϕ_{ST} and Q'_{eT} calculated from (A2.b) and (A2.c), respectively, using the value of β_T determined using (A5)) is also exhibited. The simulation was carried out for intrinsic symmetric n-

channel double-gate devices with L = 90 nm and silicon film thicknesses (t_{Si}) of 5, 10, 15, 20, 30 and 40 nm, and V_{DS} = 50 mV. For the devices with t_{Si} smaller than 20 nm the influence of quantum mechanics has been accounted for.

As expected, the definition of the threshold voltage V_{T0} proposed here and the g_m/I_D extraction procedure show very good matching. The g_m/I_D methodology has also exhibited an excellent agreement with the Y function method. On the other hand, the threshold voltage determined by the extremum of the second derivative deviates with respect to the other two determinations by less than $1.5\phi_t$.

The results shown in Fig. 6 were obtained through the g_m/I_D, SDL and Y function procedures applied to simulated current characteristics in order to investigate how short-channel effects affect the values of the threshold voltage. We have adopted the same parameters as in the previous simulation, but with constant t_{Si} (20 nm) and L = 0.05, 0.06, 0.08, 0.1, 0.13, 0.15, 0.2, 0.3, and 0.5 μm. It can be noted that the deviation in the extracted threshold voltage values, from one method to the other, remains below 1.5 ϕ_t, even for the shortest length.

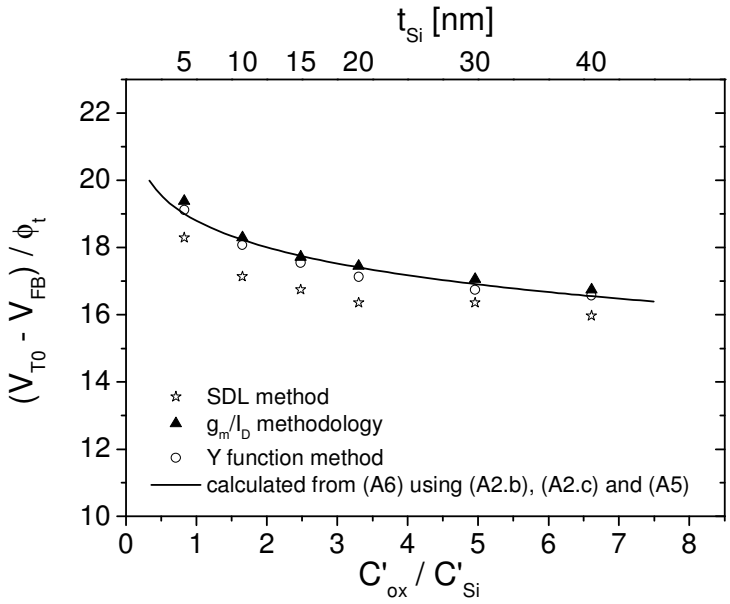

Figure 5 – Threshold voltage of intrinsic symmetric DG MOSFET (t_{ox}= 2 nm, L = 90 nm) *vs*. silicon film thicknesses: calculated from (A6) using (A2.b), (A2.c), and (A5) (solid line); extracted from simulated data using: g_m/I_D methodology (triangles); maximum of second derivative method (stars) and Y function method (circles).

The results of Fig. 6 show that the threshold voltage degradation due to short-channel effects due to channel length reduction is similarly obtained from both extraction procedures ensuring that the proposed g_m/I_D methodology is similarly affected by the reduction in channel length.

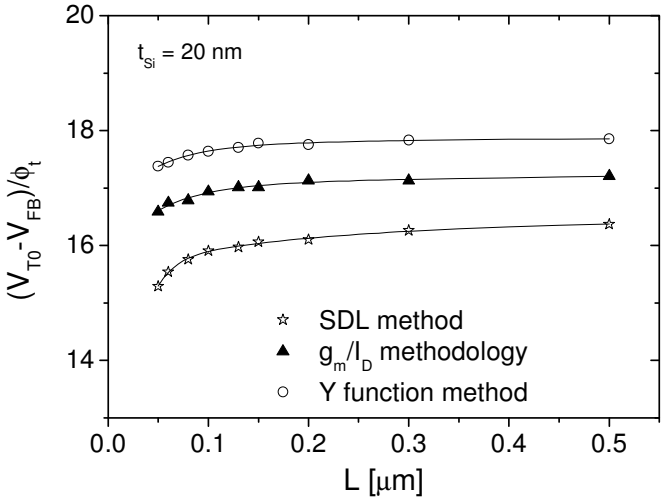

Figure 6 – Threshold voltage of intrinsic symmetric DG MOSFET (t_{ox} = 2 nm, t_{Si} = 20 nm) *vs*. channel length, extracted from simulated data using: g_m/I_D methodology; maximum of second derivative method and *Y* function method.

Numerical three-dimensional simulations at different temperatures, from 100 K to 400 K, have been performed for triple-gate FinFETs with L = 90 nm and t_{Si} = 20 nm. In

these 3D simulations, analytical models accounting for mobility dependence with horizontal and vertical electric fields, bandgap narrowing and incomplete carrier ionization have been included in the simulation files. Fig. 7 presents the threshold voltage values extracted from these simulation data at V_{DS} = 50 mV, using the g_m/I_D, SDL and Y function methods.

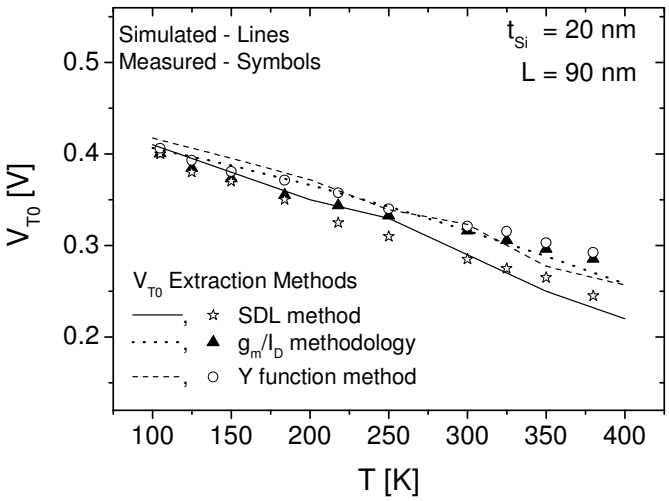

Figure 7 – Threshold voltage of intrinsic symmetric DG MOSFET *vs*. temperature extracted from simulated and measured data with V_{DS} = 50 mV, t_{Si} = *20* nm and t_{ox} = 2 nm, using: g_m/I_D methodology , maximum of second derivative and *Y* function methods.

Measurements for a similar range of temperature have been accomplished [17] for a FinFET with L = 90 nm, t_{ox} = 2 nm and t_{Si} = 20 nm. The V_{T0} values extracted from these experimental data through the g_m/I_D, SDL and Y function methods are also exhibited in Fig.7. From the results of Fig. 7 it is clear that the SDL method overestimates the threshold voltage variation with temperature, especially at higher

temperatures, while the g_m/I_D methodology agrees with the Y function method.

In [18], the variation of threshold voltage with temperature is investigated according to an analytical model presented in [2]. Applying this analysis to the simulated devices, the V_{T0} rate of variation with T is equal to -0.49 mV/K for t_{Si} = 20 nm and is equal to -0.57 mV/K for t_{Si} = 50 nm. These values agree very well with those obtained using the threshold voltage extracted through the g_m/I_D method: dV_{T0}/dT = -0.49 mV/K for t_{Si} = 20 nm and dV_{T0}/dT = -0.56 mV/K for t_{Si} = 50 nm. On the other hand, the values obtained using the SDL method are dV_{T0}/dT = -0.62 mV/K and dV_{T0}/dT = -0.66 mV/K, for t_{Si} = 20 nm and t_{Si} = 50 nm, respectively. For the Y function method the dV_{T0}/dT variation are -0.51 mV/K and -0.56 mV/K for the devices with 20 nm and 50 nm of silicon thickness, respectively, which are very close to the values of the g_m/I_D method. Therefore, the threshold voltage given by the g_m/I_D extraction procedure behaves with temperature in closer agreement with the analytical model of [2] and with the V_{T0} obtained through the Y function method. From ref. [18], it is also worth noting that even for a triple gate device (t_{Si} = 50 nm) the proposed charge-based definition works in good agreement with the tridimensional simulations in the studied temperature range differently from the SDL method.

5. CONCLUSIONS

A current-based definition of threshold, derived from the equality between the drift and diffusion components of drain current, has been extended to symmetric DG-MOSFETs with undoped body. The threshold voltage is extracted from the g_m/I_D curve in the linear region, being minimally affected by short channel effects as well as by

mobility degradation due to transversal field. The g_m/I_D extraction method agrees with the SDL method, which, however, is not associated to a physical based definition and suffers from the resulting noise of second-order derivative determination. The threshold voltage extraction using the g_m/I_D procedure also present a very good agreement with the its extraction following the Y function method ensuring a negligible influence of the series resistance.

APPENDIX A

Neglecting the hole charge for an undoped or lightly doped n-channel MOSFET, the voltage balance equation is

$$Q_e' = -C_{ox}'\left(V_G - V_{FB} - \phi_S\right) \tag{A1}$$

where Q_e' is one half of the mobile charge density in symmetric double-gate devices, V_G the gate voltage, V_{FB} the flat-band voltage, ϕ_S the surface potential, $C_{ox}' = \varepsilon_{ox}/t_{ox}$ the oxide capacitance per unit area, ε_{ox} is the oxide electrical permittivity and t_{ox} the gate oxide thickness.

The solution of the Poisson-Boltzmann equation in the case of an intrinsic symmetric n-channel DG-MOSFET (Fig.1) [19-20] leads to

$$\phi(x,y) = V_C(y) - 2\phi_t \ln\left[\frac{t_{Si}}{4\beta L_{Di}}\cos\left(2\beta\frac{x}{t_{Si}}\right)\right] \tag{A2.a}$$

$$\phi_S(y) = V_C(y) - 2\phi_t \ln\left[\frac{t_{Si}}{4\beta L_{Di}}\cos(\beta)\right] \tag{A2.b}$$

$$Q'_e = -4C'_{Si}\phi_t \beta \tan\beta \tag{A2.c}$$

$$\frac{V_G - V_{FB} - V_C}{2\phi_t} - \ln\left(\frac{4L_{Di}}{t_{Si}}\right) = \ln\left(\frac{\beta}{\cos\beta}\right) + 2\frac{C'_{Si}}{C'_{ox}}\beta\tan\beta \tag{A2.d}$$

where $\phi_S(y) = \phi(x,y)$ for $x = \pm t_{Si}/2$, t_{Si} is the silicon film thickness, ϕ_t is the thermal voltage and V_C is the channel voltage (quasi-Fermi potential of electrons). $C'_{Si} = \varepsilon_{Si}/t_{Si}$ and $L_{Di} = \sqrt{\varepsilon_{Si}\phi_t/(2qn_i)}$ are the silicon-film capacitance per unit area and the intrinsic Debye length, respectively. L_{Di} is of the order of 100 μm at room temperature.

The auxiliary variable β is directly associated with the carrier charge density, as shown in (A2.c).

Differentiating (A2.c) with respect to V_G gives

$$\frac{\partial Q'_e}{\partial V_G} = -4C'_{Si}\phi_t\left(\tan\beta + \beta + \beta\tan^2\beta\right)\frac{\partial\beta}{\partial V_G} \tag{A3}$$

From (A2.d) (for $V_C = 0$) we can find the derivative in the right-hand side of (A3), which allows us to write

$$\frac{\partial Q'_e}{\partial V_G}\frac{1}{Q'_e} = \frac{\left(\tan\beta + \beta + \beta\tan^2\beta\right)/(2\phi_t\tan\beta)}{\left[1 + \beta\tan\beta + \frac{2C'_{Si}}{C'_{ox}}\left(\beta\tan\beta + \beta^2\tan^2\beta + \beta^2\right)\right]} \tag{A4}$$

As Q'_e (and β) approaches 0, it follows from (A4) that $\frac{\partial Q'_e}{\partial V_G}\frac{1}{Q'_e}$ approaches $1/\phi_t$, thus, the inversion charge density has an ideal subthreshold slope.

Equating (A4) and (4) we find that the value of β according to the *current-based definition of threshold* is the solution (β_T) of

$$\tan\beta_T\left(\tan\beta_T + \beta_T + \beta_T \tan^2\beta_T\right) = \frac{C'_{ox}}{2C'_{Si}} \tag{A5}$$

Therefore, the threshold voltage in equilibrium is given by

$$V_{T0} = V_{FB} + \phi_{ST} - Q'_{eT}/C'_{ox} \tag{A6}$$

where Q'_{eT} and ϕ_{ST} are the mobile charge density and the surface potential at threshold, respectively, calculated from (A2.c) and (A2.b) for $V_C = 0$, respectively, with $\beta = \beta_T$, calculated according to (A5).

Fig. A1 shows the mobile charge density for which drift equals diffusion versus the ratio C'_{ox}/C'_{Si}, calculated from (A2.c) and (A5). It can be noted that half the carrier charge density inside the silicon film at threshold approaches the thermal charge ($-C'_{ox}\phi_t$) for very thin silicon films. This limit is easily determined from (A5) considering the limit at which β_T approaches zero.

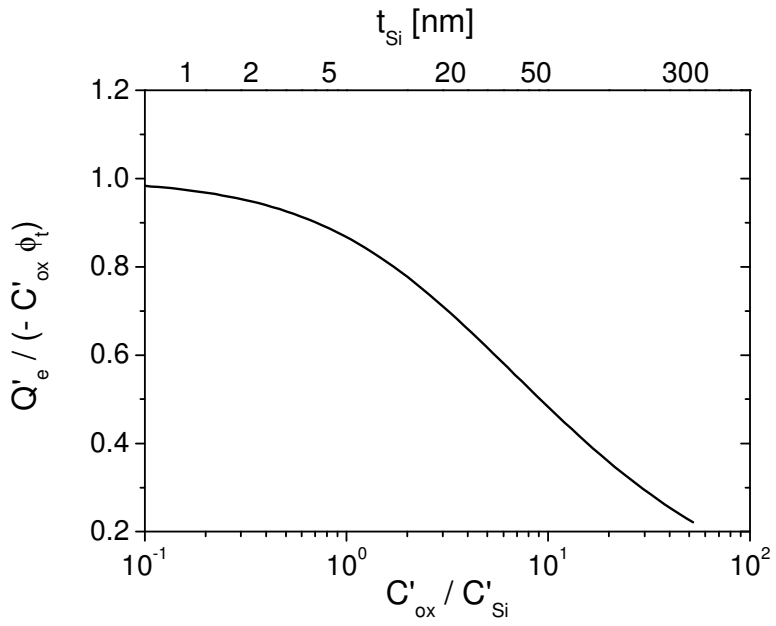

Figure A1 – One half of the normalized threshold mobile charge of the intrinsic symmetric dual gate MOSFET. t_{ox} = 2 nm.

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Figures Captions

Figure 1 – Schematic diagram of an N-channel intrinsic symmetric DG MOSFET.

Figure 2 – Simulated transconductance-to-current ratio for V_{DS} = 50 mV and V_S = 0. V_{T0} is the value of V_G for $g_m/I_D=0.5(g_m/I_D)_{max}$. t_{ox} = 2 nm, t_{Si} = 20 nm, L = 0.3 μm.

Figure 3 – Curve of the drift and diffusion components of the drain current (left Y-axis) and g_m/I_D (right Y-axis) *vs.* the gate voltage, comparing the threshold condition when g_m/I_D ratio drops to the half of its maximum value and when $I_{Ddrift}=I_{Ddiff}$ considering a constant mobility (A, B) and the mobility degradation due to the vertical and lateral electric fields (C, D) for devices with t_{Si} = 10 nm and 40 nm, respectively.

Figure 4 – Threshold voltage of intrinsic symmetric DG MOSFET, calculated from: current-based (circles); charge-based criterion of [11] (squares); condition of [2] (crosses); crossover between surface potential behaviors (triangles) [12]. t_{ox} = 2 nm.

Figure 5 – Threshold voltage of intrinsic symmetric DG MOSFET (t_{ox}= 2 nm, L = 90 nm) *vs*. silicon film thicknesses: calculated from (A6) using (A2.b), (A2.c), and (A5) (solid line); extracted from simulated data using: g_m/I_D methodology (triangles); maximum of second derivative method (stars) and Y function method (circles).

Figure 6 – Threshold voltage of intrinsic symmetric DG MOSFET (t_{ox} = 2 nm, t_{Si} = 20 nm) *vs*. channel length, extracted from simulated data using: g_m/I_D methodology ; maximum of second derivative method and *Y* function method.

Figure 7 – Threshold voltage of intrinsic symmetric DG MOSFET *vs*. temperature extracted from simulated and measured data with V_{DS} = 50 mV, t_{Si} = *20* nm and t_{ox} = 2 nm, using: g_m/I_D methodology , maximum of second derivative and *Y* function methods. The devices present channel lengths of 90 nm.

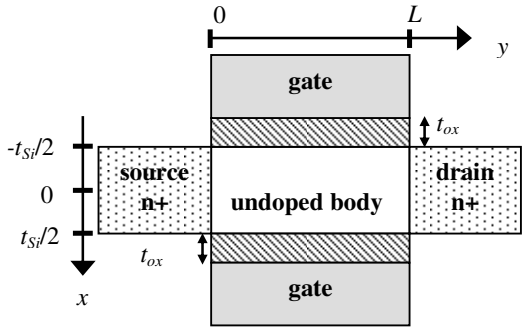

Figure 1

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

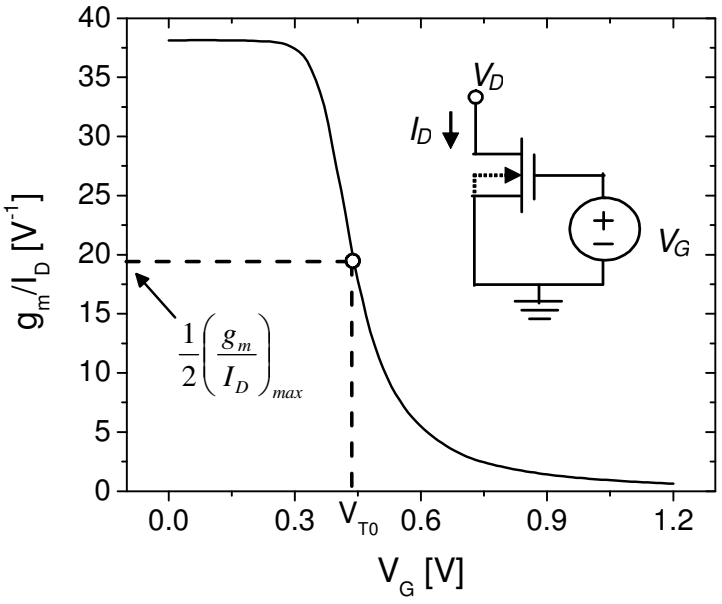

Figure 2

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

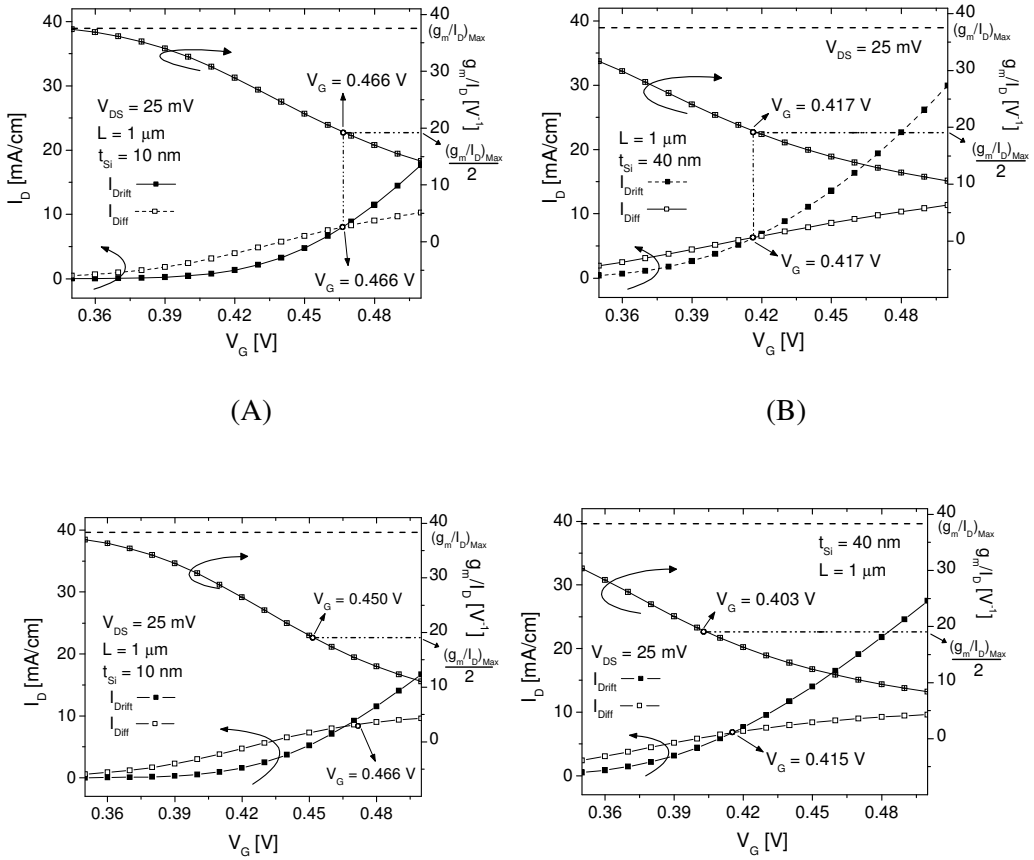

Figure 3

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

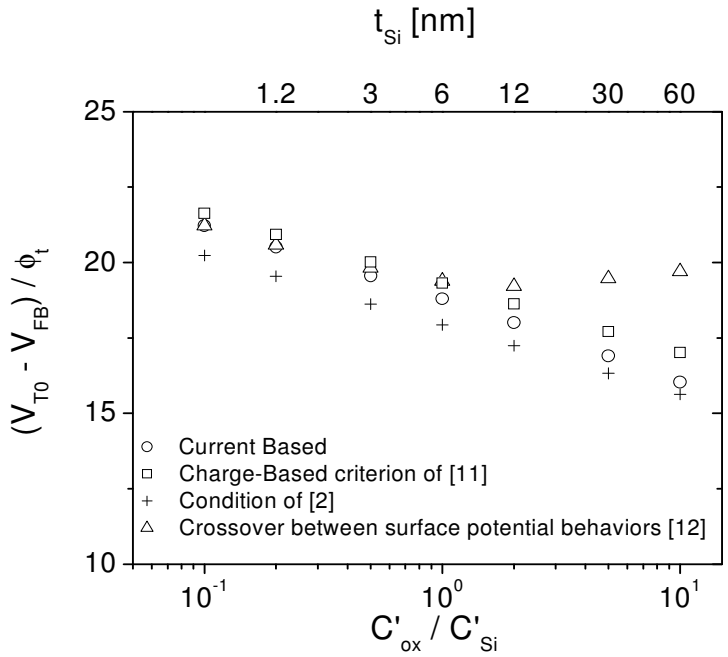

Figure 4

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

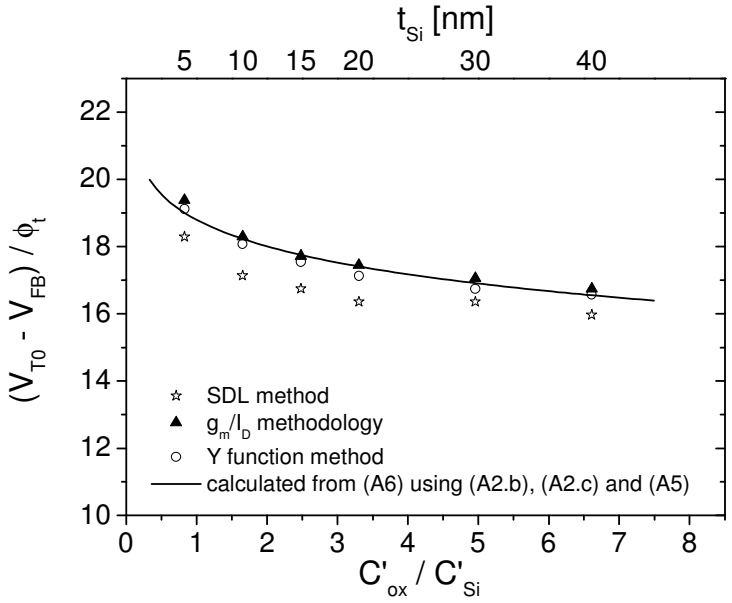

Figure 5

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

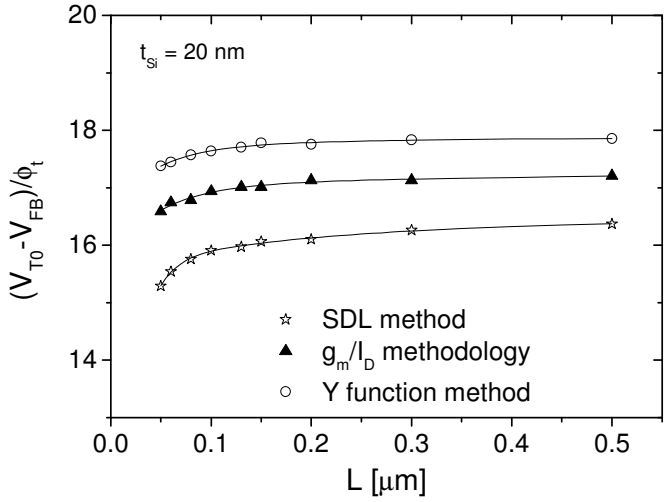

Figure 6

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

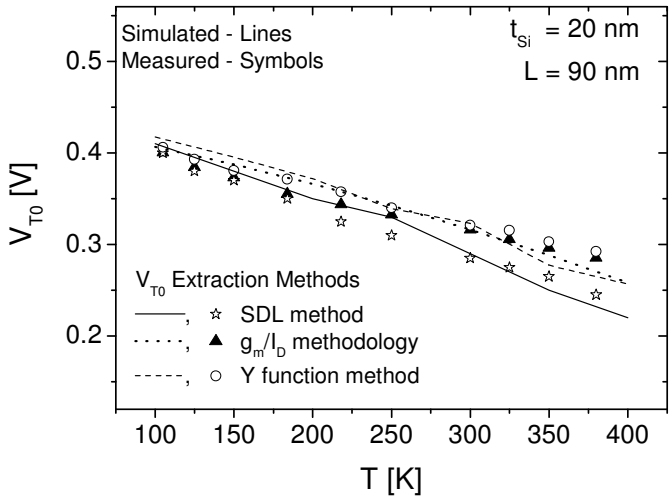

Figure 7

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"

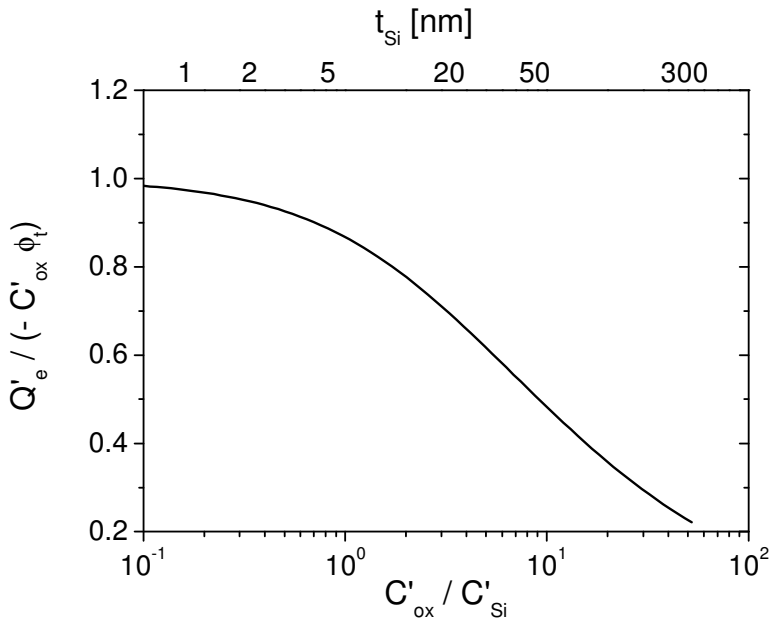

Figure A1

Ana Isabela Araújo Cunha *et al.*, "Direct Determination of Threshold Condition in DG-MOSFETS from the g_m/I_D Curve"