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CRYSTAL OSCILLATOR FOR LOW-VOLTAGE APPLICATIONS

Trabalho de Conclusão de Curso submetido ao Departamento de Engenharia Elétrica e Eletrônica da Universidade Federal de Santa Catarina para a obtenção do título de Bacharel em Engenharia Eletrônica
Orientador: Prof. Dr. Márcio Cherem Schneider

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Este Trabalho foi julgado adequado para obtenção do Título de Bacharel em Engenharia Eletrônica e aprovado em sua forma final pela Banca Examinadora

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To my parents and my sister, who always encouraged and gave me strength throughout this journey.

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Finally, I thank my parents Sheila and Antonio for their care, their emotional support and understanding; for being my safe haven even when I was miles away.

Success is not final, failure is not fatal: it is the courage to continue that counts.

Winston Churchill

RESUMO

Em virtude do recorrente aumento de aplicações para IoT (Internet das Coisas), que exige dispositivos autossuficientes, este trabalho de conclusão de curso propõe o projeto de um circuito integrado de baixa tensão que, combinado a um cristal de quartzo, forma um oscilador, o qual é um bloco importante em sistemas digitais e de comunicação. Esse circuito opera com 100mV de tensão de alimentação, compatível com o uso de dispositivos de colheita de energia, visto que esses dispositivos geram tensões de dezenas a centenas de milivolts. Por operar em baixa tensão, o consumo de potência do circuito diminui. Este trabalho apresenta a teoria, medições práticas usando componentes discretos e o projeto do circuito integrado, em conjunto com simulações de esquemático e *layout*, que permitem verificar o comportamento do circuito integrado e suas condições de operação.

Palavras-chave: Oscilador a cristal. Operação em baixa tensão. Tecnologia CMOS.

ABSTRACT

Given the increase of IoT applications, which requires autonomous devices, this final year project proposes the design of a low-voltage integrated circuit that, combined with a quartz-crystal, forms an oscillator, an important block in digital and communication systems. The circuit operates with 100 mV of supply voltage, which is compatible with the use of energy harvesting devices, since these devices provide from tens to hundreds of millivolts. By operating at low-voltages, the circuit's power consumption is reduced. This work presents the theory, measurements using discrete components and the design of the integrated circuit of a Pierce oscillator along with schematic and layout simulations, which allows to verify and predict the behavior of the integrated circuit.

Keywords: Crystal oscillator. Low-voltage. CMOS technology.

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LIST OF ABBREVIATIONS AND ACRONYMS

CMOS – Complementary Metal Oxide Semiconductor
EDA – Electronic Design Automation
GPS – Global Positioning System
IoT – Internet of Things
MOSIS – Metal Oxide Semiconductor Implementation Service
NMOS – N-channel Metal Oxide Semiconductor
PMOS – P-channel Metal Oxide Semiconductor
RF – Radio Frequency
RTC – Real Time Clock
SMD – Surface Mount Device
WSN – Wireless Sensor Networks
XO – Crystal oscillator

LIST OF SYMBOLS

C_0 – Shunt capacitance of crystal model
C_1: capacitor connected to the inverter input
C_2: capacitor connected to the inverter output
$C_{1,2}$: when $C_1 = C_2$
C_{in} – parasitic capacitance at inverter input
C_{out} – parasitic capacitance at inverter output
C_L – Load capacitance
C_m – Motional capacitance of crystal model
C_{stray} – total parasitic capacitance in the circuit
f_0 – nominal frequency of operation
f_a – anti-resonance frequency
f_r – resonance frequency
f_L – frequency of operation due to added load
gm – transconductance of transistor
gm_{crit} –critical transconductance for oscillation
gm_N – transconductance of NMOS transistor
gm_P – transconductance of PMOS transistor I_D – drain current
L_m – Motional inductance of crystal model
L_{min} – minimum channel length of transistor
L_n – Channel length of NMOS transistor
L_p – Channel length of PMOS transistor
$L_{n,p}$ – Channel length when $L_n = L_p$
M: number of multipliers of transistor cells
n – slope factor
Q – Quality factor
Q_{xtal} – Quality factor of crystal
R_F – feedback resistor between input and output of inverter
R_m – Motional resistance of crystal model
R_N – Negative resistance
R_S – resistor prevent overdrive of crystal in circuit
V_{DD} – supply voltage
W_n – Width of NMOS transistor
W_p – Width of PMOS transistor
Z_0 – Impedance of shunt capacitance
Z_C – impedance viewed by the motional impedance Z_m
Z_m – Motional impedance
Z_x – Crystal total impedance
ϕ_t – thermic voltage
ω – angular frequency

SUMMARY

1 INTRODUCTION

"*Si le Temps peut être observé, il peut aussi être fabriqué*", Musée du Temps, Besançon, France. If time can be observed, it can be fabricated.

Using mechanical devices, the first watchmakers built an artificial clock, based on the count of small regular time intervals. From this initial rhythm, from this first base of time, they managed to calculate the passage of hours. A sound signal from a bell or a visual indication given by a needle allowed the passing of time to be materialized.

In the 15th century, explorers traveled through the seas and oceans in search of new lands and treasures. They could determine the latitude by using a sextant and observing the position of the sun or the stars.

However, they had trouble determining the longitude, because to do so, they required a sextant and a clock synchronized with the time from the port of departure, which would be of a known longitude. Then, the difference between the time from the clock and the midday sun allowed them to calculate their longitude while at sea. [1]

Unfortunately, the clocks were not sufficiently precise to keep the time in accordance with the point of depart throughout their journey, which led to many disasters. The Englishman, John Harrison, was the first to propose a sufficiently precise chronometer that allowed longitude calculation, which was a great advance in maritime navigation [1].

Since then, the timekeeping industry has done nothing but evolved, from the use of mechanical resonators, such as the diapason, in conjunction with an electric system, to the use of atomic clocks in the Global Positioning System (GPS). Timekeeping is an important part of mankind and it is crucial in the current era of information, that requires precise timing to manage the flow of information, in a way that it is reliable, robust and inexpensive [1].

Since the second half of the 20th century, the utilization of quartz has revolutionized the measurement of time and allowed to gain considerable precision. The crystal oscillator industry is based on the principle of piezoelectricity, a specific property of quartz and other mineral crystals, discovered in France by the brothers Pierre and Jacques Curie in 1880. Once this material is submitted to an electric current it begins to vibrate in a regular way. The frequency of such regular movement can be used as an electronic time base. This stable frequency enables to obtain superior precision in comparison to the mechanical devices used thus far. Figure 1.1 presents quartz crystal resonators used in the 1960's; at that time, they were not miniaturized for everyday use.

Figure 1.1 – Quartz crystal resonators from 1960's. Picture taken at the Musée du Temps in Besançon, France.

The quartz crystal oscillators are essential elements for radio, radar, television, computers and smartphones. Their use in large scale was possible because of the advancement in transistor technology.

In fact, the progress in the field of electronics enabled the miniaturization of devices while increasing their processing power [2]. It allowed the emergence of the Internet of Things (IoT) concept, which describes a structure in which all physical everyday objects are connected to the internet without need of human interaction [3]. To construct an IoT network the devices must be autonomous and durable [3], capable of harvesting energy from the environment to supply their needs and ensure operation. Hence the research on energy harvesting devices, such as RF sources and thermoelectric generators that provided voltage of tens of millivolts, and photovoltaic cells which generate voltages of hundreds of millivolts.

To ensure electronics systems can operate with such low-voltage supplies, the research and development of low-voltage circuits are paramount. However, before trying to make major systems operate with low-voltage, the basic blocks need to operate successfully with such supplies first.

The oscillator is a fundamental block in electronic circuits, especially when it comes to timekeeping and control of systems, which is why this project aims at the design of a 100 mV Pierce oscillator, a common crystal oscillator topology [4]. Nowadays, its use has been explored in IoT applications, which demand timing accuracy to start or synchronize Wireless Sensor Networks (WSN) [5].

1.1 STATE OF THE ART

It can be found, in literature, many current researches regarding the matter of low-power crystal oscillators. For instance, in [6], the authors propose a crystal oscillator circuit that operates with supply voltage below 1.0 V and power consumption of 5.58 nW. However, they used two power supplies and a large silicon area of 0.3 mm^2 to implement the design.

In [7], a self-charged crystal oscillator is proposed. This technique reduced the power consumption to 1.89 nW and employed a supply voltage of 150 mV. However, the 28nm technology used is too expensive.

The work presented in [5] is similar to the one, proposed here. It implements a Pierce oscillator that operates with 300 mV of supply voltage. In [5] the proposed technique combined with operation in the sub-threshold region provided an average power consumption of 1.5 nW.

The oscillators in [6], [7] and [5] operate with 32.768 kHz crystals. Table 1.1 presents the summarized comparison of these low-power crystal oscillator designs.

Table 1.1 – Comparison of low-power crystal oscillators found in literature

	[6]	[7]	[5]
Frequency	32 kHz	32 kHz	32 kHz
Area (mm^2)	0.3	0.03	0.0625
Power consumption (nW)	5.58	1.89 @ 0.15V V_{DD}	1.5 @ 0.3 V V_{DD}
Supply voltage V_{DD} (V)	0.92 – 1.8	0.15 – 0.5	0.3 – 0.9
Technology	180 nm	28 nm	130 nm

1.2 OBJECTIVE

The main objective of this project is to design the integrated circuit that drives the crystal resonator in an oscillator block. This circuit should allow oscillation to start and be sustained using a low-voltage supply of 100 mV. To facilitate operation at low-voltage, the oscillator will employ a 32.768 kHz crystal resonator.

This frequency is typical of Real-Time Clocks (RTC) and wristwatches, because the number of oscillations is convenient for the associated digital electronic circuit. A digital chip divider can easily divide 32768 by 2^{15}, resulting in one cycle or pulse per second [1].

1.3 METHODOLOGY

This document introduces a bit of oscillator's theory by presenting two approaches used for oscillator analysis. It presents the resonator's electric model and equations that describe its behavior, as well as the circuit analysis for the Pierce oscillator used in this project.

The oscillator was assembled with discrete components and transistors from the chip 4007, to evaluate the practical impact of component values in the required supply voltage for oscillation to start. The measurements were performed with available equipment in the Integrated Circuits Laboratory [8], where the project development took place. Power supplies such as E3630A from HP and Tektronix oscilloscopes such as TDS3032B and MSO 5204 are a few of the instruments used.

To integrate the circuit, this project was developed using the CMOS 180 nm technology from TSMC and the Cadence Virtuoso Design Environment, an EDA software from Cadence that allows a more thorough analysis and design of integrated circuits. It enables to create circuit schematics, design the layout and perform simple electric simulations, as well as simulations that consider the parasitic RC extraction post-layout, which provides more helpful and reliable results to evaluate the circuit performance and operation throughout the project's development.

The 32.768 kHz crystals employed are part numbers AB38T [9] and ABS07W [10] from Abracon.

2 THEORETICAL FOUNDATION

2.1 THEORY OF OSCILLATORS

Oscillators are electronic circuits which generate their own periodic signal. There are two main types of oscillators: the relaxation and the harmonic oscillators.

The relaxation oscillators have their frequency defined by an RC product, which represents the time constant of alternately charging and discharging the capacitor, an energy storage element. Usually they produce square or triangular waveforms.

The oscillator in this project is a harmonic oscillator. This type of oscillator provides a tuned frequency by the use of an LC tank. It can provide stable nearly sinusoidal waveforms with low phase noise. And, for that reason, they are widely used in RF and digital systems.

There are two ways to perform circuit analysis of such oscillators, one is by using the positive feedback loop approach and the other is to use the negative resistance approach. Depending on the circuit topology one approach may be more suitable than the other.

2.1.1 Positive feedback loop

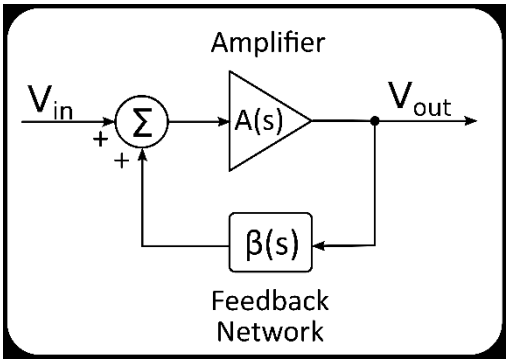

Figure 2.1 – Positive feedback loop analysis

The positive feedback loop analysis consists of viewing the oscillator as a linear feedback system composed of two blocks: the amplifier and the feedback network. Suppose the amplifier has transfer function A(s) and the feedback network has transfer function β(s). When both are connected in a feedback loop, as shown in Figure 2.1, it is possible to derive T(s) in (2.1). [11]

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s)}{1 - A(s)\beta(s)} \quad (2.1)$$

From (2.1), by replacing $s = j\omega$, the following conditions of oscillation are obtained.

$$|A(j\omega)\beta(j\omega)| \geq 1 \quad (2.2)$$

$$\angle A(j\omega)\beta(j\omega) = 2\pi N \quad (2.3)$$

Where N is an integer number. Equations (2.2) and (2.3) constitute the Barkhausen criteria, which states oscillation occurs, when the magnitude of the open loop gain A(s)β(s) is greater than or equal to 1 (2.2) and the phase-shift must be 0° or an integer multiple of 360° (2.3). [11]

2.1.2 Negative resistance

An ideal electronic oscillator is composed of two reactive components: an inductor and a capacitor (Figure 2.2a). It is also known as LC tank, tuned circuit or resonant circuit. It's a circuit in which energy is stored and it flows back and forth between capacitor and inductor in its own resonance frequency. In an ideal LC tank, no energy is lost.

However, in the real world, an LC circuit is in fact a resonator (Figure 2.2b), which is simply the component that defines the frequency of an actual oscillator. A resonator cannot oscillate by its own, because real reactive components have resistance associated with them due to physical construction, which means there's energy loss, hence, the oscillation will not be sustained unless energy is added to the circuit.

The negative resistance approach views the oscillator as two one-port components: a lossy resonator and an active circuit that cancels the loss [12]. It consists on cancelling the effect of the resonator's positive resistance with a circuit that provides a negative resistance sufficient to allow oscillation to start and be sustained (Figure 2.2c). The term negative resistance is, in fact, a misnomer of the "negative transresistance", defined by the ratio between a given voltage variation (ΔV) and the induced current variation (ΔI) [13], which can be positive or negative. It can be generated using active devices such as linear amplifiers [14].

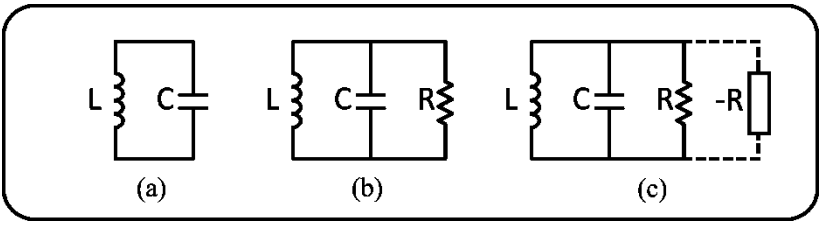

Figure 2.2 - (a) Circuit of an ideal LC oscillator; (b) Example of a resonator circuit; (c) Negative resistance approach proposes to use an active circuit to provide the negative resistance, that cancels the loss effects from the resonator.

2.2 CRYSTAL OSCILLATOR

To better understand and design crystal oscillators, one must understand the crystal resonator itself and its equivalent electric model, as presented in the following section.

2.2.1 The crystal resonator

Quartz crystals are composed of silicon dioxide and they can be cut in a certain way to provide a specific frequency. The quartz crystal presents several interesting properties that allow their use in the most diversified fields. They have low acoustic loss, good thermal and chemical stability, and they are piezoelectric devices.

The piezoelectricity is the property that permits the use of crystals in oscillators. It can be defined as the capability to generate electrical voltage (or current) in response to mechanical vibrations. The piezoelectric effect consists of an electromechanical linear interaction between mechanical and coulombic forces in crystalline materials.

The piezoelectric effect can be direct, when an electric charge is generated by applying a mechanical force; or indirect, when a mechanical tension is generated by applying an electric field. For instance, in a quartz crystal, if a voltage pulse is applied on its terminals, this voltage generates a mechanical vibration which generates an oscillating electric voltage.

The crystal tends to vibrate at its own resonance frequency, determined by its physical characteristics, which makes it a good mechanical resonator with a high-quality factor. The quality factor (Q) can be evaluated as the ratio of the energy stored in the oscillating resonator to the energy dissipated per cycle (2.4).

$$Q = 2\pi f_0 \frac{\text{Stored energy}}{\text{Dissipated energy}} \tag{2.4}$$

Due to its piezoelectric characteristic, the quartz crystal mechanical vibrations can be represented by a series RLC circuit, in which the resistor R_m represents the mechanical losses, L_m represents the mass and C_m a spring [15]. The crystal's equivalent electrical model consists on a mechanical or motional branch, i.e., the series RLC circuit, in parallel with a shunt capacitance C_0, which represents the physical capacitance formed by both the parallel plate capacitance of the electrode metallization and the stray package capacitance [15].

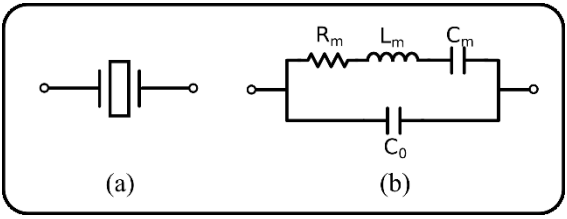

Figure 2.3 - Crystal's (a) symbol and (b) equivalent electrical model

From this model, it is possible to determine the crystal's equivalent impedance Z_x (2.8), given by (2.7) the parallel association of the motional branch impedance Z_m (2.5) and the shunt capacitance impedance Z_0 (2.6).

$$Z_m(j\omega) = \frac{1 - \omega^2 L_m C_m + j\omega R_m C_m}{j\omega C_m} \tag{2.5}$$

$$Z_0(j\omega) = \frac{1}{j\omega C_0} \tag{2.6}$$

$$Z_x(j\omega) = Z_m(j\omega) || Z_0(j\omega) = \frac{Z_m(j\omega) Z_0(j\omega)}{Z_m(j\omega) + Z_0(j\omega)} \tag{2.7}$$

$$Z_x(j\omega) = \frac{-\omega R_m C_m + j(1 - \omega^2 L_m C_m)}{\omega^3 L_m C_m C_0 - \omega(C_0 + C_m) + j\omega R_m C_m C_0} \tag{2.8}$$

If the resonator presented $R_m = 0$, then the impedance Z_x would be zero when $1 - \omega^2 L_m C_m = 0$, which yields the resonant frequency f_r (2.9) due to the series motional branch.

Also, Z_x would tend to infinity when the denominator equals zero, that is, when $\omega^3 L_m C_m C_0 - \omega(C_0 + C_m) = 0$, hence, $\omega^3 L_m C_m C_0 = \omega(C_0 + C_m)$. This gives the anti-resonance frequency f_a (2.10). [16]

$$f_r = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{2.9}$$

$$f_a = f_r \sqrt{1 + \frac{C_m}{C_0}} \tag{2.10}$$

Since $R_m \neq 0$, f_r is the point of minimum impedance, whereas f_a is the maximum impedance point. These points can be easily identified in the impedance magnitude and phase plots like the ones presented in Figures 2.4 and 2.5. The impedance magnitude of a crystal is given by (2.11) and the phase by (2.12). Both expressions are plotted in Figures 2.4 and 2.5, respectively.

$$|Z_x(j\omega)| = \sqrt{\Re\{Z_x(j\omega)\}^2 + \Im\{Z_x(j\omega)\}^2} \tag{2.11}$$

$$\angle Z_x(j\omega) = \tan^{-1}\frac{\Im\{Z_x\}}{\Re\{Z_x\}} \tag{2.12}$$

In both plots, it is possible to identify both resonant and anti-resonant frequencies. For instance, the minimum impedance occurs at the same frequency f_r where there's a pronounced shift in phase. As for the maximum impedance, it occurs at f_a along with the second phase shift.

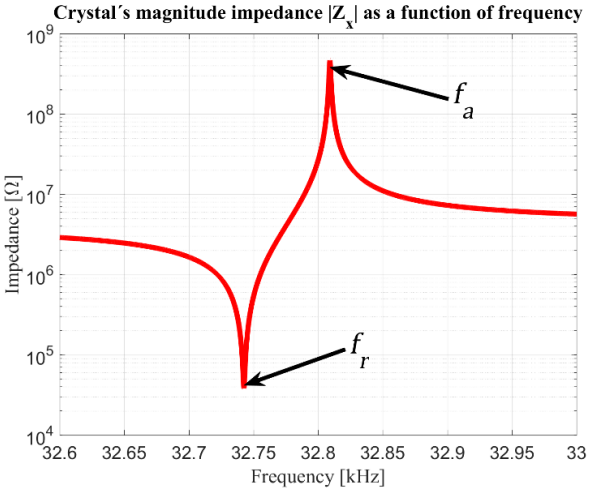

Figure 2.4 - Crystal's impedance magnitude determined using equations (2.8) and (2.11), considering the equivalent electric model from the ABS07W resonator.

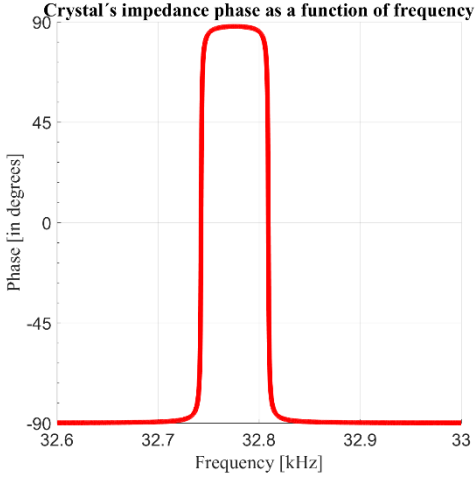

Figure 2.5 - Crystal's impedance phase determined using equations (2.8) and (2.12), considering the equivalent electric model of the ABS07W resonator.

These frequencies are usually very close due to the crystal's high-Q given by (2.13), and, usually, when inserted in a circuit, the crystal will operate in a frequency between f_r and f_a. In this region the equivalent

circuit resembles an inductive impedance [17] with a quality factor given by:

$$Q_{xtal} = \frac{\omega L_m}{R_m} \tag{2.13}$$

In a crystal datasheet, instead of finding the values for the model's motional branch components, it is customary to find the values of C_0 and the ratio C_0/C_m. These values are useful to calculate the crystal's pulling when a load capacitance C_L is connected to the crystal. Because the insertion of this capacitance changes the reactance, the frequency changes as well. The pulling is given by (2.14), where f_L is the frequency of oscillation due to the added load. [18]

$$\frac{f_L - f_r}{f_r} = \frac{C_m}{2(C_0 + C_L)} \tag{2.14}$$

Depending on how the capacitive load is connected to the resonator, the oscillator will operate in the series or parallel mode with a frequency f_L given by (2.15). [13]

$$f_L = f_r \left(1 + \frac{C_m}{2(C_0 + C_L)}\right) \tag{2.15}$$

Equation (2.15) is valid for either parallel or series load capacitance added to the crystal, the difference being that, when a series load is added, the circuit will operate at the point of minimum impedance; while in the case of a parallel load capacitance, the circuit will operate at the maximum impedance point. This is illustrated in Figures 2.6 and 2.7. In Figure 2.6, the arrows indicate the point of oscillation when a load is added. The frequency of oscillation was shifted to the same value; however, the impedance is minimum for a series load and maximum for a parallel load.

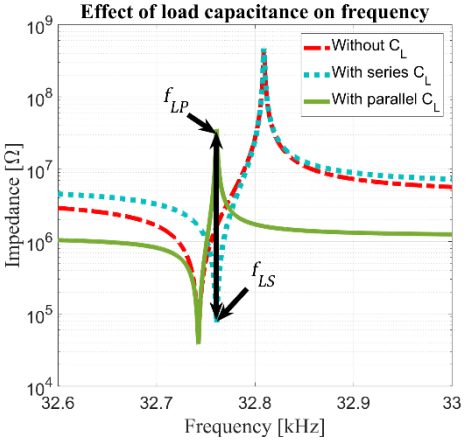

Figure 2.6 - Crystal's impedance magnitude considering the equivalent electric model from the ABS07W resonator associated with C_L in series (dotted-blue line) and parallel (solid-green line). The impedance of the crystal without a capacitive load (dashed-red line) serves as reference to observe which frequency, f_r or f_a, shifts.

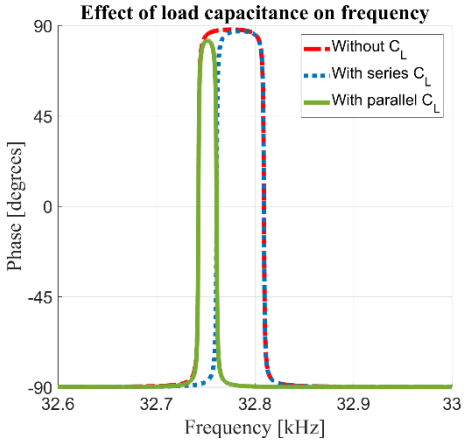

Figure 2.7 – Crystal's impedance phase considering the ABS07W resonator model associated with C_L in series (dotted-blue line) and parallel (solid-green line). The phase of the crystal without a capacitive load (dashed-red line) serves as reference to observe the original frequency at which the phase shifted.

Usually for crystals designed to operate in parallel mode, the manufacturer specifies the value of load capacitance that allows oscillation at the nominal frequency of datasheet. If the load capacitance

is greater than the specified one, the oscillation should occur at a lower frequency, so to move the frequency of operation to a higher frequency, closer to the expected one, the overall capacitance at the crystal's ends must be reduced.

2.2.1.1 The resonators chosen for this project

To simulate the Pierce oscillator and to plot Figures 2.4-2.7, the crystal electrical model was used. The values used in the model were found in the datasheet [9] [10] and in additional documents from the manufacturer Abracon [19]. The crystal models are based on the AB38T and ABS07W crystals (Figure 2.8). Their motional values and shunt capacitance, as well as a few important electrical characteristics are shown in Table 2.1.

Table 2.1 - Electrical model and electrical characteristics of quartz crystals AB38T and ABS07W

Crystals	**AB38T (tuned fork)**	**ABS07W (SMD)**
Electrical model		
Motional capacitance C_m	3.69 fF	4.68 fF
Motional Inductance L_m	6.39 kH	5.048 kH
Motional resistance R_m	22.9 kΩ	38.2 kΩ
Shunt capacitance C_0	1.82 pF	1.15 pF
Important electrical characteristics from datasheet		
Load capacitance C_L	12.5 pF	3 pF
Typical Drive Level	1 µW	0.1 µW
Typical Quality Factor Q	9 000	13 000

The drive level is the only characteristic from Table 2.1 not mentioned thus far. Its value represents the amount of drive the crystal can handle without affecting its operation. Basically, it is how much voltage and current can be applied to the crystal terminals. If the drive level is exceeded the resonator might age faster, lowering its frequency stability, or it might even break, because of the piezoelectric characteristic [20]. If the voltage or current through the crystal is too high, it is the same as applying a very strong mechanical force, which can cause a fracture in the crystal resonator.

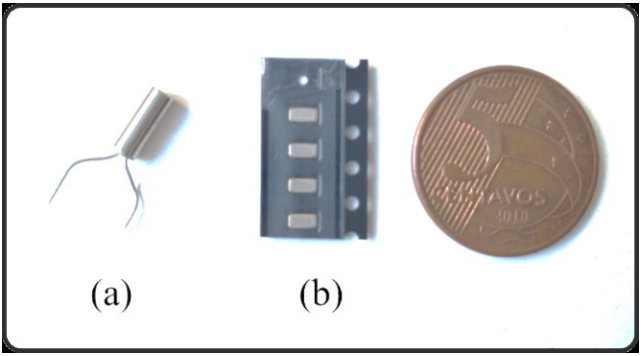

Figure 2.8- In comparison with a coin of R$0.05, (a) the AB38T tuned-fork crystal; and (b) four SMD crystal of model ABS07W.

2.2.2 The Pierce oscillator

The Pierce oscillator is one of the most common crystal oscillator topologies used [13]. One of its advantages is the capability to generate oscillation at a specific frequency using few components.

In [21], Vittoz analyzes the Pierce oscillator using an NMOS transistor as the active device (Figure 2.9). The analysis is performed for operation at the crystals' fundamental frequency.

Using the negative resistance approach, Vittoz considers the crystal's motional impedance Z_m and the equivalent impedance Z_C, which encompasses all the green shaded area in Figure 2.9. The condition of oscillation is given by (2.16), which, as a first approximation, can be estimated as a negative resistance R_N (2.17), meaning the negative resistance from Z_C must compensate the crystal's positive resistance R_m.

$$Z_C + Z_m = 0 \tag{2.16}$$

$$\Re\{Z_C\} = R_N = -R_m \tag{2.17}$$

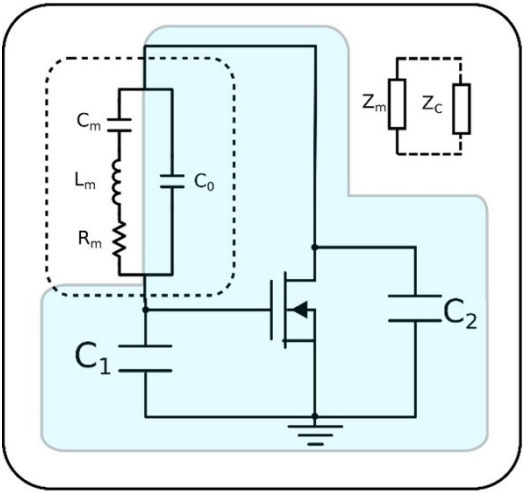

Figure 2.9 - Pierce oscillator with NMOS transistor as the active device that provides negative resistance. The negative resistance approach in this model includes C_0, from the crystal model, in the impedance Z_C. At the top right, the equivalent impedance association of Z_m with Z_C illustrates the principle of the negative resistance approach, presented in Figure 2.2c.

Using the motional impedance expression, the negative resistance can be found to be (2.18), where *gm* is given by (2.19) because the transistor operates in weak inversion. In (2.20) I_D is the transistor drain current, n is the slope factor and ϕ_t is the thermal voltage [22].

$$R_N = -\frac{g_m C_1 C_2}{(g_m C_0)^2 + \omega^2 (C_1 C_2 + C_2 C_0 + C_0 C_1)^2} \tag{2.18}$$

$$g_m = \frac{I_D}{n\phi_t} \tag{2.19}$$

From a handful of calculations, Vittoz [21] determines the critical transconductance g_{mcrit} that allows oscillation to occur, given by (2.20). However, in [16] it is said that it is common practice to design a circuit with g_m greater than 5 times g_{mcrit}, to ensure that oscillation will start.

$$g_{m_{crit}} = 4R_m \left(1 + \frac{C_0}{C_L}\right)^2 (2\pi f_0)^2 (C_0 + C_L)^2 \tag{2.20}$$

The analysis performed by Vittoz [21] can be extended for use with a CMOS inverter (Figure 2.10) as the active device, in which the transconductance is given by both PMOS and NMOS transistor's transconductances g_{mP} and g_{mN}, respectively [22].

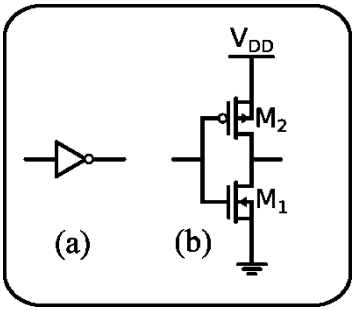

Figure 2.10 - CMOS inverter (a) symbol and (b) schematic. M_1 is the NMOS transistor and M_2 the PMOS transistor.

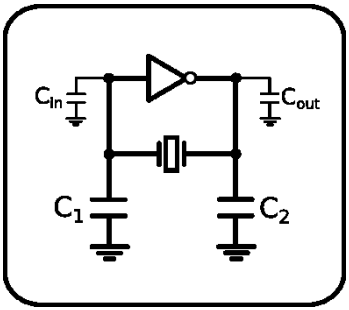

Figure 2.11 - CMOS Pierce oscillator, including stray capacitances, represented by C_{in} and C_{out}.

The Pierce using an inverter is shown in Figure 2.11, where C_{in} and C_{out} represent the stray, or parasitic, capacitances due to the interconnections between devices and the intrinsic transistors' capacitances.

To determine the values of C_1 and C_2 to use in accordance with the load capacitance specified in the crystal's datasheet, expression (2.21) is used.

$$C_L = \frac{C_1 C_2}{C_1 + C_2} + C_{stray} \tag{2.21}$$

3 THE PIERCE OSCILLATOR WITH DISCRETE COMPONENTS

The Pierce oscillator was assembled with discrete components and transistors from the chip 4007, primarily, following the schematic presented in Figure 3.1a. Tests using different component values were performed to evaluate the practical impact of such components in the required supply voltage (V_{DD}) for the start-up of oscillation.

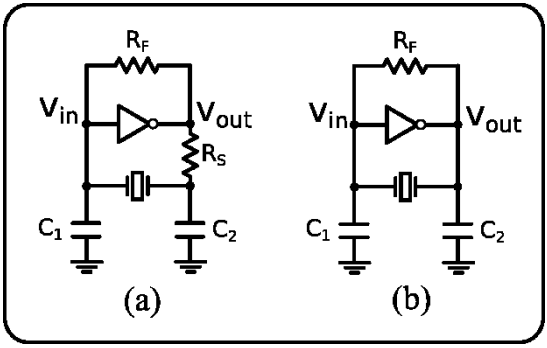

Figure 3.1 – Schematic of a Pierce oscillator (a) with resistor R_S and (b) with a short circuit between crystal and the inverter output.

In the theoretical analysis, the feedback resistor R_F is not accounted for, as a mean of simplification. However, if not added in a real design, the circuit will not oscillate, because the feedback resistor biases the CMOS inverter, ensuring its operation as a linear amplifier.

The crystal selected for the experiment is the model AB38T [9] from Abracon, because it was the only 32.768 kHz tuned-fork crystal with a datasheet available for purchase in the national market at the time. The tuned fork crystal is easier to place in a circuit board than a crystal with SMD packaging (like the ABS07W resonator).

The first assembly consisted on following the recommendation [20] of inserting a resistor R_S between the crystal terminal and the inverter output, as shown in Figure 3.1a. This resistor is supposed to prevent exceeding the crystal drive level mentioned in section 2.2. The component values used in such configuration were $R_S = 330k\Omega$ and $R_F = 10\ M\Omega$. The capacitors $C_1 = C_2$ were altered to see their effect.

The minimum supply voltage that allowed oscillation to build up was 2.83 V, using $C_{1,2} = 1$ pF (Table 3.1). After oscillation has started up, the circuit sustained oscillation with minimum V_{DD} of 2.4V. In Figure 3.2,

the waveform is diminishing, almost resembling a sinusoidal waveform as V_{DD} decreases.

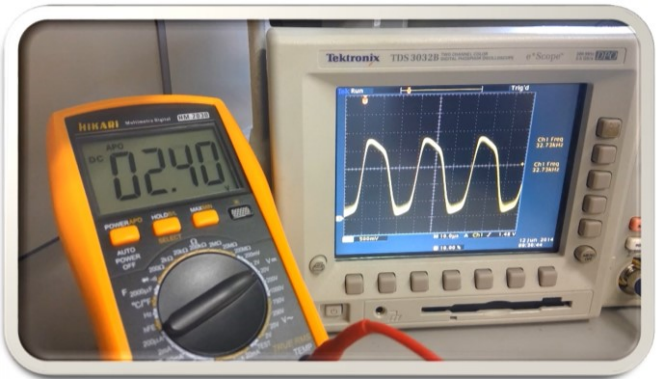

Figure 3.2 - XO output waveform using the minimum supply voltage that sustained oscillation

To reduce the supply voltage required for oscillation, the oscillator was assembled without R_S, which was replaced by a short circuit, as shown in Figure 3.1b; also, R_F was increased. With these changes, oscillation started up from 1.86 V of supply voltage, C_1=C_2 = 6.8 pF and R_F = 25 MΩ. This result is shown in Figure 3.3. In addition, the minimum voltage to sustain oscillation was 1.25 V, very close to the threshold voltages of the CMOS transistors from 4007, which are around ±1.2 ~ 1.5V.

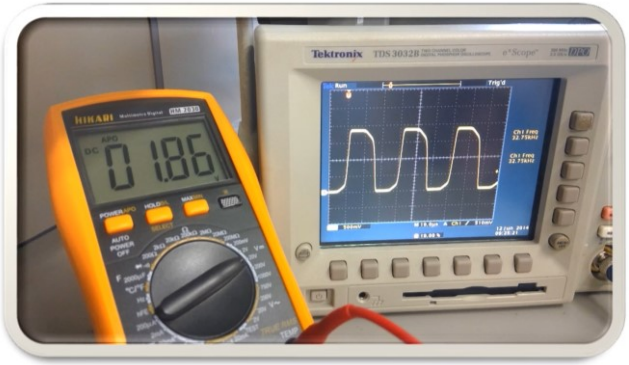

Figure 3.3 - Photo taken of the XO output waveform using the minimum supply voltage that allowed oscillation to start up.

Such measurements were performed more than once and on different days. Table 3.1 presents a summary of the typical results obtained using different combinations of components. The result shown in Figure 3.3 is the one that required the lowest voltage to start up oscillations.

Table 3.1 – Summary of results obtained from changing the components in the Pierce circuit. O.B.U stands for the supply voltage that enabled Oscillation to Build Up; S.O. stands for the minimum supply voltage that Sustains Oscillation.

R_F		**10 MΩ (with R_S)**		**25 MΩ**		**50 MΩ**	
V_{DD} (V)		**O.B.U**	**S.O**	**O.B.U**	**S.O**	**O.B.U**	**S.O**
$C_{1,2}$ (pF)	**22**	3.10	2.40	2.28	1.25	2.27	1.26
	15	2.99	2.25	2.14	1.25	2.19	1.22
	10	2.97	2.15	2.12	1.25	2.20	1.18
	6.8	2.96	2.01	2.08	1.25	2.17	1.22
	2.2	2.88	1.85	2.08	1.25	2.20	1.56
	1	2.83	1.82	2.07	1.25	2.08	1.23

From this experiment, it has been shown that increasing R_F to 50MΩ did not have much impact as reducing the load capacitance or increasing R_F from 10 MΩ to 25 MΩ after removing R_S from the circuit.

The voltage for which oscillation builds up is different than the supply voltage for which oscillation is sustained, because to start-up oscillators the loop gain must be greater than 1, and afterwards, to sustain a stable oscillation the gain must be equal to 1.

In this case, when oscillation starts, the output voltage is almost a square waveform, i.e., the output amplitude saturates at V_{DD} because the open loop gain remains greater than 1 after oscillation started. As V_{DD} decreases so does the inverter's transconductance. The observed almost sinusoidal waveform in Figure 3.3 demonstrates that the gain is reaching unity. When oscillation fades or fails to start, it means the amplifier's transconductance is not enough to compensate the resonator's mechanical losses, i.e., the loop gain is lower than 1.

4 THE INTEGRATED CIRCUIT DESIGN

To implement and simulate the Pierce oscillator, the crystal electrical model (presented in section 2.2) was used to create the resonator components for simulations.

The CMOS inverter, (Figure 2.10) to be used as a linear amplifier in the Pierce oscillator, requires, first, the determination of a few of the technology transistors' characteristics that are important when selecting and sizing the devices.

The available PMOS and NMOS transistors are standard and medium-vt on the 180 nm technology from TSMC. The threshold voltage of both types of transistors was determined by means of the *gm/I_D* method [23], and it was found that medium-vt transistors have lower threshold voltage (around 300 mV) than the standard ones (around 450 mV); thus, the medium-vt transistors are used in the inverter's design.

It can be seen, from Figure 4.1, that the threshold voltage decreases with the increase of channel's length, but, for a preliminary analysis, the CMOS inverter was designed with L_p=L_n, using the minimum channel length (L_{min}) for NMOS medium-vt transistors, which is 0.3 µm (PMOS medium-vt transistors have L_{min} = 0.25 µm, which prevents using L_p=L_n).

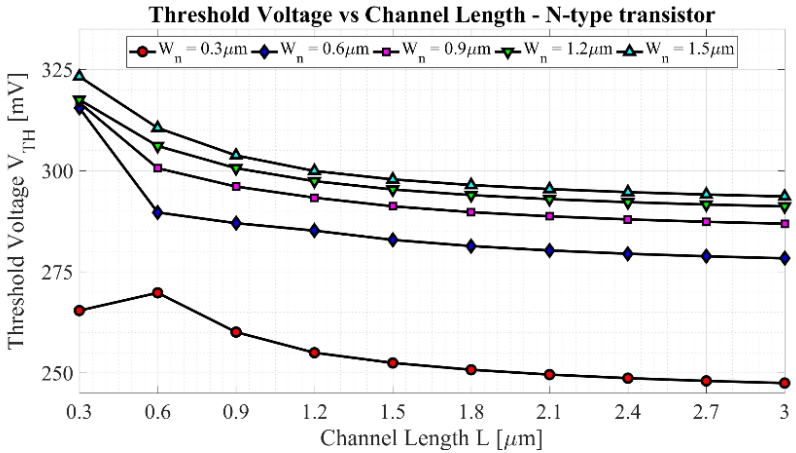

Figure 4.1 - Threshold voltage vs channel length of a medium-vt NMOS transistor

To determine the DC bias point of the CMOS inverter with a supply voltage V_{DD} of 100 mV, a DC simulation was performed to evaluate the transfer function V_{out} x V_{in} considering a fixed width W_n of

0.6 µm and a parametric variation in W_p, as shown in Figure 4.2. The gain is maximum at the bias point $V_{out} = V_{in} = V_{DD}/2$ (red marker in Figure 4.2), which, in this case, occurs when W_p is 0.6 µm. However, due to a preliminary misunderstanding, the inverter was firstly designed with $W_p = 2W_n = 1.2\mu m$, which shifts the mean value in oscillation to a few millivolts above $V_{DD}/2$. In a later design, presented in section 4.2, $W_p = W_n = 0.6$ µm.

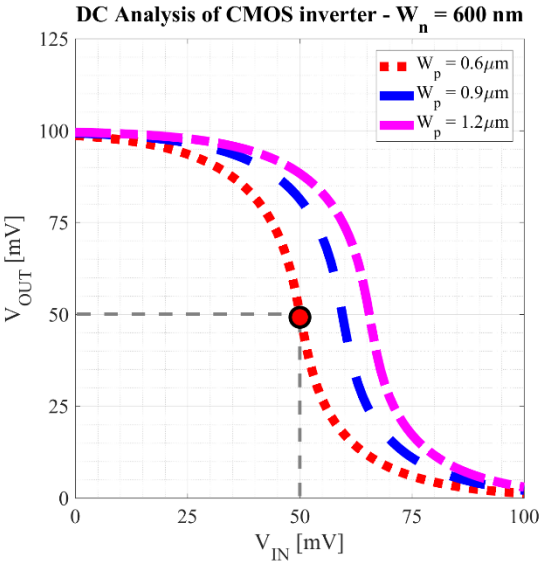

Figure 4.2 - Transfer function of CMOS inverter to determine DC bias point with $W_n = 0.6$ µm

The design is proposed for use with the ABS07W crystal, because this resonator specifies a smaller load capacitance than AB38T (Table 2.1), which means it can work with lower voltages, as seen from the practical experiment.

However, before beginning the design for 100 mV of supply voltage considering the ABS07W, a few simulations and iteration of values were performed to determine if the testbench for simulation was working properly.

4.1 THE 1ST DESIGN

Since the resonator employed in the practical experiment was, in fact, the AB38T, the first simulations considered its model and the component values from those tests. The CMOS 180 nm technology used allows operation to a maximum of 1.8V. The circuit simulated is the same from Figure 3.1b.

The first simulation was conducted with 1.0 V of supply voltage, which is 10 times greater than the proposed operation voltage for this project. This simulation also included load capacitors $C_{1,2}$ of 22pF and R_F of 20 MΩ. The CMOS inverter presents $L_{n,p}$ = 0.3 µm, W_n=0.6 µm and W_p = 1.2 µm.

With these values, oscillation occurred for supply voltages within the range of 325 mV to 1.0 V. Voltages greater than 1.0V were not simulated because the objective is to start oscillation with much lower voltages.

To reduce the supply voltage, transistors were associated in parallel, thus increasing the number of multipliers M (thus far, equal to 1) and, consequently, increasing the transistors' strength to drive the crystal. Still using the AB38T model, the oscillation was possible at 100 mV with $M_{n,p}$ = 30.

Now, changing to the ABS07W crystal model, different combinations of $C_{1,2}$, M and R_F were simulated. A few of the tested combinations are presented in Table 4.1.

Table 4.1 – Tested combinations for oscillation with V_{DD} = 100 mV using ABS07W model

$C_{1,2}$ (pF)	M	R_F (MΩ)	Peak-to-peak voltage (mV_{pp})	Minimum to maximum values
4	8	20	71	23 to 94 mV
	10	20	79	18 to 97 mV
	12	20	82	15 to 97 mV
	20	20	82	15 to 97 mV
	12	25	89	11 to 100 mV

The highest peak-to-peak amplitude of oscillation achieved, based on the tested combinations, was of 0.9V_{DD}, using $C_{1,2}$ = 4 pF, R_F = 25MΩ, M = 12 and the transistors' dimensions $L_{n,p}$ = 0.3 µm, W_n=0.6 µm and W_p equal to 1.2 µm. Thus, these were the values used for the upcoming simulations.

4.1.1 Simulation results using ideal capacitors and resistor

The simulations performed are for transient analysis, this kind of simulation allows analysis of the circuit behavior in the time domain; therefore, it is possible to observe and measure the start-up time and evaluate the generated waveforms, that is, if oscillation does occur.

The simulations were performed for different V_{DD} to see how the circuit handles voltage variations at voltages below 300 mV. The tested supply voltages were 70 mV, 80 mV, 100 mV, 200 mV, 250 mV and 300mV. Table 4.4 summarizes the obtained results and Figure 4.3 accommodates the obtained output waveforms, as a general view.

Table 4.2 - The designed circuit oscillation for different V_{DD}. The X suggests oscillation failed to start and the tick implies oscillation was successful

V_{DD} (mV)	70	80	100	200	250	300
Oscillation starts	X	✓	✓	✓	✓	X

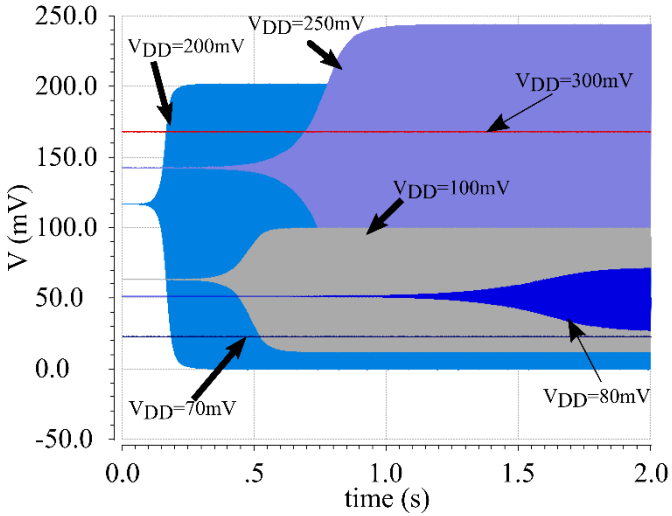

Figure 4.3 - Simulation result for different supply voltages. With this image is it possible to observe the cases for which oscillation starts, as well as estimate the time to reach steady-state. The arrows point to the waveforms of the respective applied supply voltage.

Figure 4.3 shows that oscillation successfully starts and is sustained for supply voltages from 80 mV to 250 mV. However, only for 200 mV the output presents full voltage swing (ground to V_{DD}). At 80 mV the minimum value is even higher than the one of 11 mV, observed for V_{DD} = 100mV (Table 4.1). The difference in start-up time is, also, very pronounced; while at 200 mV, it takes around 250 ms to reach steady state, at 100mV it takes 500ms; with supply voltages of 80mV and 250 mV, the circuit takes even longer time to stabilize oscillation, requiring more than 1.5 s when V_{DD} = 80mV.

The start-up failed at 70 mV because the inverter wasn't strong enough to drive the crystal, while, at 300 mV, oscillation did not occur because, by increasing the voltage supply, the loop gain decreased due to the increase of energy loss of the resonator, preventing a gain greater than 1, a condition required for oscillation.

Since the specified circuit operation is for 100 mV, further details (such as zooming in the waveforms) will be provided regarding oscillation at V_{DD} = 100 mV, preventing a set of similar images that are not so relevant in the context of this work.

4.1.2 Simulation results using resistor and capacitors from the 0.18µm CMOS technology

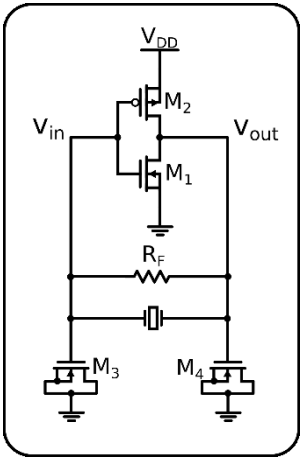

Figure 4.4 - Schematic of 1st design

The 4 pF capacitors were built from medium-vt NMOS transistors, by connecting both drain and source to substrate (transistors M_3 and M_4

in Figure 4.4). The capacitance of 4 pF was determined for a transistor with L_n = W_n = 10 µm and M = 21. From the technology library, the resistor with the highest available resistance per square (1037 Ω/square) to use as the feedback resistor R_F was chosen. To obtain 25 MΩ, its dimensions were calculated as segment width = 1 µm, segment length = 100 µm and number of segments = 231.

Figure 4.5 shows the resultant waveforms for both input and output nodes using only components from the 180 nm technology. In general, the amplitudes have not suffered significant changes in comparison with the obtained results using ideal components. The only difference is that the simulation took longer to be completed.

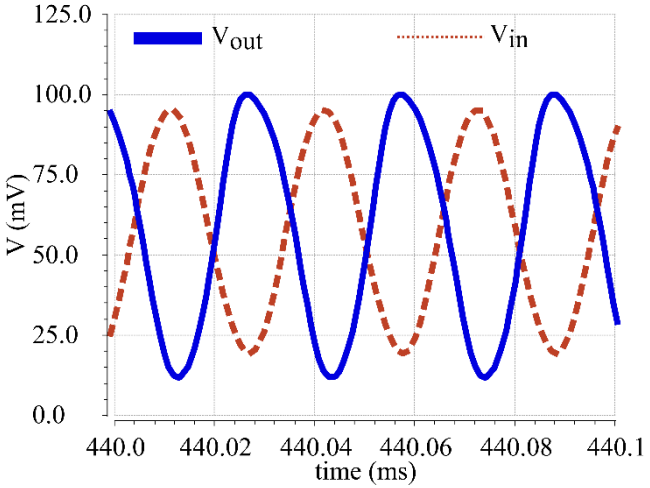

Figure 4.5 - Simulation result @ V_{DD} = 100 mV using components from 180 nm technology. The inverter input is in dot-red and the inverter output in solid-blue.

From the simulation waveforms, by using expressions inherent to the simulator, it was possible to determine the average consumed power, the frequency of oscillation and the minimum, maximum and mean output values of amplitude. For this design, the results are shown in Table 4.3.

Table 4.3 - Parameters calculated from simulation

Frequency	32.769 kHz
Average power consumption	829.7 pW
Peak-to-peak amplitude	88.19 mV
Minimum output value	11.87 mV
Maximum output value	100.06 mV
Mean output value	57.77 mV

4.1.3 Post-layout simulation results

In the previous section it was seen that the circuit behaves as expected using components available on the chosen CMOS technology, therefore, once the layout was created, the parasitic RC extraction was performed.

Simulating with the extracted layout showed that oscillation still occurred, but the trough of oscillation increased from 11 mV to about 40 mV, as shown in Figure 4.6. On the other hand, the peak of oscillation decreased from 100 mV to 95 mV.

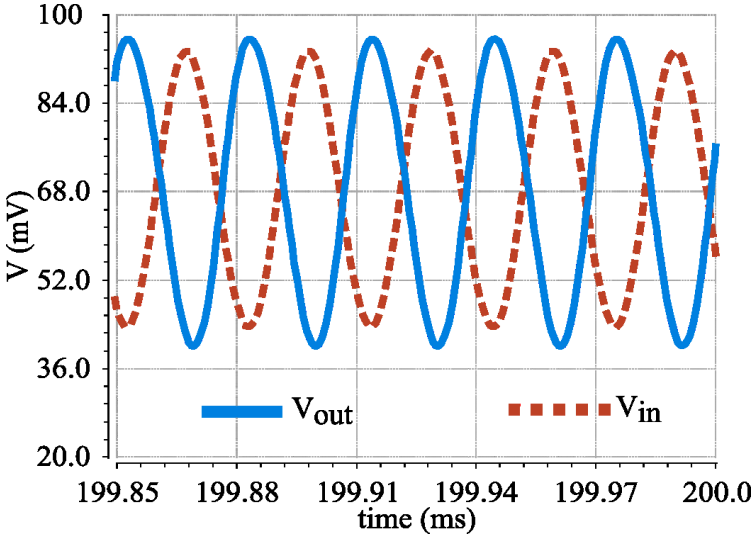

Figure 4.6 – Post-Layout simulation result @ V_{DD} = 100 mV using extracted RC parasitic layout. The inverter input is in dot-red and the inverter output in solid-blue.

One hypothesis for why this happened is that the NMOS transistor wasn't strong or fast enough to let the oscillation drop to a lower value. Hoping to increase the NMOS strength and speed, its area was increased by doubling M_n; another layout was created [the one shown in Annex A] and the parasitic RC extracted again.

However, increasing M_n did not have any noticeable effect in the trough of oscillation. Despite such loss in the peak-to-peak amplitude, this layout was sent to MOSIS for fabrication in the hope of performing chip measurements before the conclusion of this project. Unfortunately, the chip sent in March for fabrication did not arrive in time, thus preventing us to measure the oscillator.

The parameters presented in Table 4.3 were also determined in the post-layout simulation and are shown, along with the layout area, in Table 4.4. In comparison with the simulation before the RC parasitic extraction, the post-layout average power consumption has increased from 830 pW to 1.123 nW.

Table 4.4 - Parameters calculated from post-layout simulation

Frequency	32.768 kHz
Average power consumption	1.124 nW
Area	291.42 µm x 141.56 µm = 0.04 mm^2
Peak-to-peak amplitude	55.94 mV
Minimum output value	39.87 mV
Maximum output value	95.81 mV
Mean output value	57.77 mV

4.2 THE 2ND DESIGN

As it was seen, after the parasitic RC extraction, the circuit still managed to operate with 100 mV of supply, but with only 60% of the expected peak-to-peak amplitude voltage at the output.

Perhaps it was not enough to double the area of the NMOS transistor, because the 25 MΩ resistor used was too large in terms of area, hence, in the RC extraction, too many parasitic capacitances were added to the circuit and these capacitances ended up holding the voltage at 40 mV. Instead of increasing even more the NMOS transistor's strength and speed to pull down the voltage to zero, another design is proposed.

In this second design, no resistors have been used. To replace the resistor from technology, a standard PMOS transistor in the triode region [22] was sized and biased to provide a resistance around 25 MΩ.

The standard PMOS provided more resistance per area than a medium-vt PMOS transistor or any (standard and medium-vt) NMOS transistor. In the triode region, the transistor is similar to a resistance [24]. The longer is the channel length, the smaller the flow of holes from source to drain, i.e. the resistance increases with channel length.

For the PMOS transistor to operate as a resistor, the gate was connected to ground, the bulk connected to V_{DD} and the source and drain terminals are connected to the points where the resistor was replaced. Note that in the Pierce oscillator shown, the transistor operates with a DC drain-to-source voltage equal to zero; thus, it operates in the triode region. In this design's schematic (Figure 4.7), M_5 is the triode region transistor.

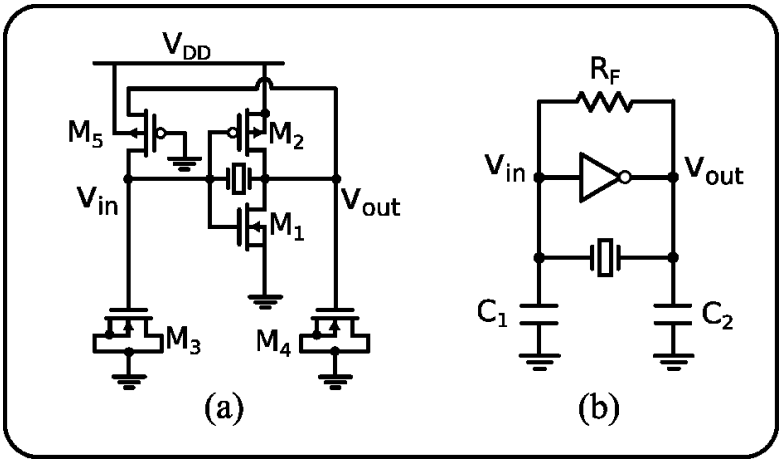

Figure 4.7 - (a) Schematic used for the proposed design at transistor level and (b) symbolic Pierce oscillator schematic.

Figure 4.7a presents the transistor level schematic of the oscillator proposed for the design, related to the symbolic Pierce schematic in Figure 4.7b. The inverter consists of transistors M_1 and M_2, while transistors M_3 and M_4 emulate load capacitors C_1 and C_2, respectively. Finally, M5 plays the role of the feedback resistor R_F.

In this second design, the inverter transistors were sized with equal length ($L_n = L_p$) and width ($W_n = W_p$), to operate at the DC bias point around $V_{DD}/2$, as shown in Figure 4.1. In addition, it was verified that standard NMOS transistors present greater capacitance per area than medium-vt transistors; hence, the dimensions were recalculated, reducing the number of multipliers and, consequently, the layout area. Table 4.5 presents the transistors' dimensions used in this design.

Table 4.5 - Dimensions used in the transistors from Figure 4.7a

Transistor	Type	W (µm)	L (µm)	M
M_1	Medium-vt NMOS	0.6	0.3	12
M_2	Medium-vt PMOS	0.6	0.3	12
M_3	Standard NMOS	10	10	16
M_4	Standard NMOS	10	10	16
M_5	Standard PMOS	0.4	10	1

4.2.1 Simulation results before layout

By running the transient analysis, the start-up time is around 650ms. The resulting waveforms are presented in Figures 4.8 and 4.9.

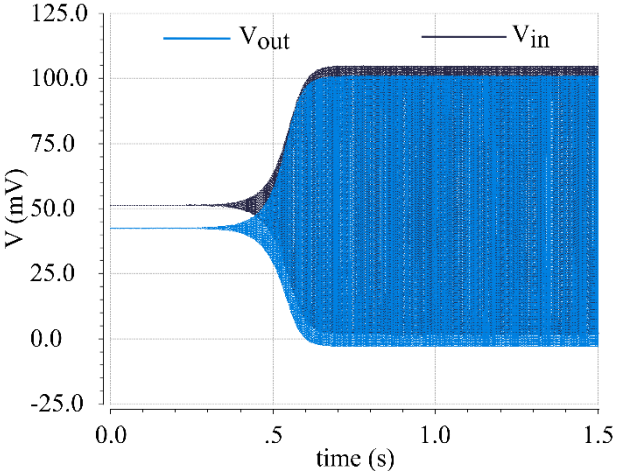

Figure 4.8 - Result from transient analysis simulation of the oscillator schematic. In blue, the inverter output and in black the inverter input.

The use of a triode region PMOS transistor, instead of the resistor from technology, provided a better output voltage swing, from, approximately, zero to V_{DD}.

Taking a closer look at the generated waveforms (Figure 4.9), the result is a nearly sinusoidal wave, as expected. The circuit is oscillating at the frequency of 32.768 kHz and the average power consumption has decreased, in comparison with the previous design. The results are presented in Table 4.6.

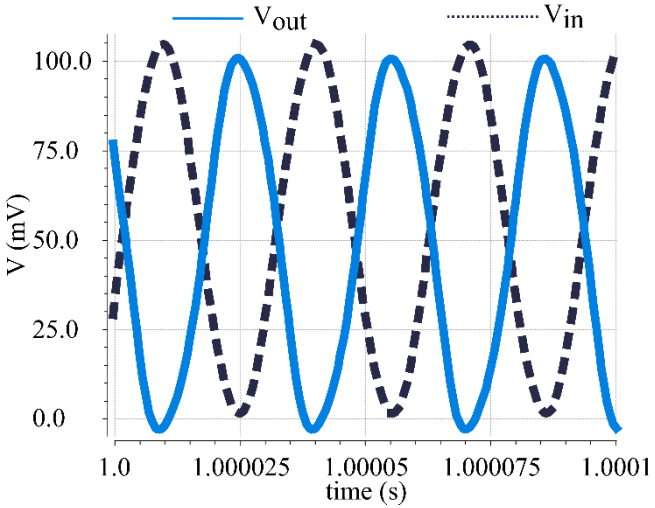

Figure 4.9 - Zoom of the simulation result of Figure 4.8.

Table 4.6 – Simulation results before layout

Frequency	32.768 kHz
Average power consumption	556.43 pW
Peak-to-peak amplitude	104.74 mV
Minimum output value	-3.22 mV
Maximum output value	101.52 mV
Mean output value	47.28 mV

4.2.2 Post-layout simulation results

The layout of this design is presented in Annex B. It occupies a smaller area than the layout of the previous design (Annex A), now having the capacitors as the responsible for most of the occupied area instead of the resistor. Again, the parasitic RC extraction was performed.

Figure 4.10 presents the simulated waveform using the extracted layout. It shows that oscillation occurs, and the minimum and maximum output values are, approximately, ground and V_{DD}, respectively.

The values of area, average power consumption, frequency, maximum, minimum and mean output values calculated in the post-layout simulation are shown in Table 4.7.

Table 4.7 – Post-layout simulation results

Frequency	32.769 kHz
Average power consumption	565.58 pW
Area	100.845 µm x 44.6 µm = 0.0045 mm^2
Peak-to-peak amplitude	104.39 mV
Minimum output value	-3.17 mV
Maximum output value	101.22 mV
Mean output value	48.20 mV

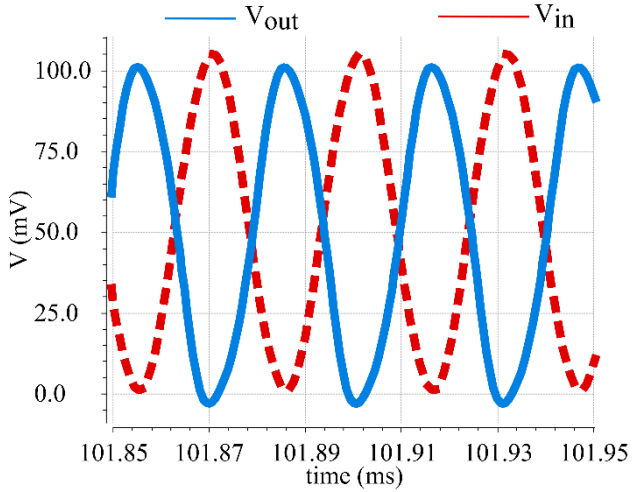

Figure 4.10 - Post-layout simulation result @ V_{DD} = 100 mV using extracted RC parasitic layout. The inverter input is in dot-red and the inverter output in solid-blue.

4.2.3 Corners and Monte Carlo simulations

To verify the circuit operation in the extreme cases of process variation, transient simulations of corners were performed. The corners evaluated are TT (Typical), FF (fast-fast), SF (slow-Fast), FS (fast-Slow) and SS (slow-slow). Table 4.8 summarizes the results for frequency of oscillation. Although the maximum variation in frequency was less than 7 Hz, oscillation failed to be sustained for the FS and SF corners.

Table 4.8 - Result of corners simulations

Corner	Frequency (kHz)
TT	32.76804
FF	32.76787
FS	32.76138 (oscillation not sustained)
SF	32.76778 (oscillation not sustained)
SS	32.76775

The Monte Carlo simulation was performed to verify how sensitive the frequency of oscillation is to process variations. The histogram, presented in Figure 4.11, shows that most samples developed the expected frequency of 32.768 kHz. The simulation used 50 samples, with σ = 0.17402 Hz and μ = 32.768 kHz.

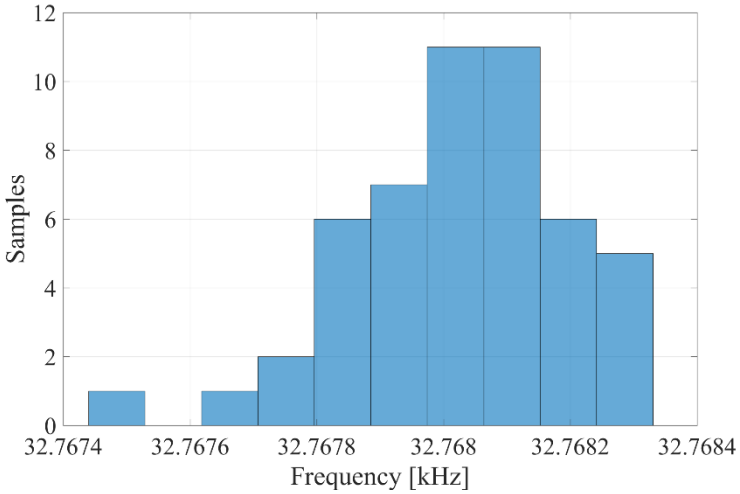

Figure 4.11 - Histogram obtained from Monte Carlo simulation

In addition to these simulations, the temperature was varied from -10 to 60 degrees Celsius to see how frequency shifts with the change in temperature. The obtained results are shown in Figure 4.12. With -10 ºC the circuit sustained oscillation, but with 10 mVpp, i.e., 10% of the expected peak-to-peak voltage.

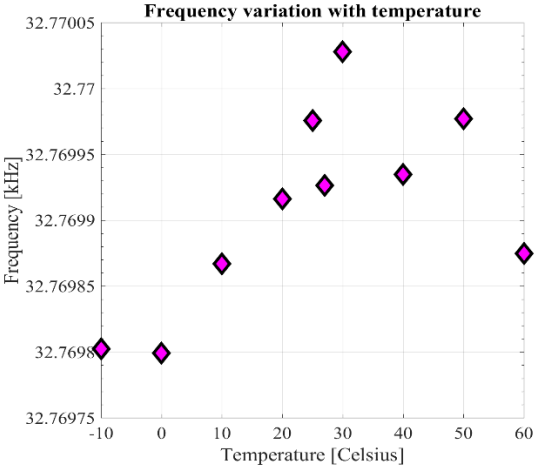

Figure 4.12 - Frequency dependency on temperature obtained from simulation

5 FINAL CONSIDERATIONS

Table 5.1 presents the summarized results, obtained from post-layout simulations, for the designs described in this work, in comparison with the state-of-the-art designs of crystal oscillators presented in section 1.1.

Table 5.1- Comparison of results of both designs from this work with the state of the art

	This work		**[6]**	**[7]**	**[5]**
	1st	**2nd**			
Frequency (kHz)	32	32	32	32	32
Area (mm^2)	0.04	0.0045	0.3	0.03	0.0625
Power consumption (nW)	1.124	0.5656	5.58	1.89	1.5
Supply voltage V_{DD} (V)	0.1	0.1	0.92–1.8	0.15	0.3
Technology (nm)	180	180	180	28	130

Both designs developed in this work operate with 100 mV of supply voltage, as it was the project's main objective. From Table 5.1, the second design here developed (the one that incorporates only transistors) presented smaller layout area than the first one with resistor from the technology. This area was also smaller than the state of the art [6], [7] and [5], being almost 10 times smaller than the oscillator from [7] that uses a 28 nm technology.

The same is valid for the average power consumption, which, although the first design consumed almost as much as the state of the art designs, the second design demonstrated an improvement in power consumption, requiring 10 times less power than the work presented in [6] that also uses a 180 nm CMOS technology and 3 times less power than the one required in [5], that uses a 130 nm technology.

The objective of operation at 100 mV supply voltage was achieved and helped reduce the average power consumption. To reduce the overall area was not part of the proposed objectives, but it is a welcome result, which leaves more room on the chip to implement more circuits. The circuits were tested for lower supply voltages, such as 80 mV. The first design managed to oscillate, despite its amplitude loss. The second design with $W_n = W_p$, however, did not manage to sustain oscillation at 80 mV, having its range of supply voltage of operation from 100 mV to 250 mV. But, with a bit more of optimization it is possible to successfully obtain

oscillation at lower voltages. For instance, it was tested although not shown, that if the ratio C_2/C_1 is increased, the loop gain increases and oscillation for 70 mV and 300 mV happened to be possible in the first circuit designed.

The developed project seems promising based on the simulations' results. However, it leaves plenty of room for improvement in future work.

5.1 FUTURE WORK

Despite promising results, it is still required to perform chip measurements to validate the first design. To do same with the second circuit, it must, first, be sent to fabrication.

Regarding the design, other inverter topologies could be explored, like using the Schmitt Trigger inverter as a linear amplifier [25], aiming to reduce even more the supply voltage of operation. In addition, in future work, the oscillation start-up time should be considered, because to make it advantageous to use this circuit in a real system, oscillation shouldn't take such a long time (half a second) to reach steady state.

Another important aspect to consider in oscillators is the phase noise and jitter measurements. A low-power oscillator might have the phase noise deteriorated, requiring a low-power design that predicts it and prevents such deterioration.

Besides maintaining a reasonable phase noise for crystal oscillators, it is necessary to investigate how to properly perform these measurements in the laboratory, since, due to the crystal high-Q, their bandwidth is too narrow, requiring high bandwidth resolutions to perform reliable measurements. Unfortunately, the available laboratory instruments do not present such resolution; hence, other techniques to perform these measurements will have to be explored.

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ANNEX A – LAYOUT OF 1ST CIRCUIT DESIGN

Below, the layout for the first circuit design is presented: arrows indicate the overall width and height dimensions; the colored boxes relate the component with its respective layout cell. To recall, M_1 and M_2 form the CMOS inverter, M_3 and M_4 are MOS capacitors and R_F is the resistor from technology, which occupies most of the layout area.

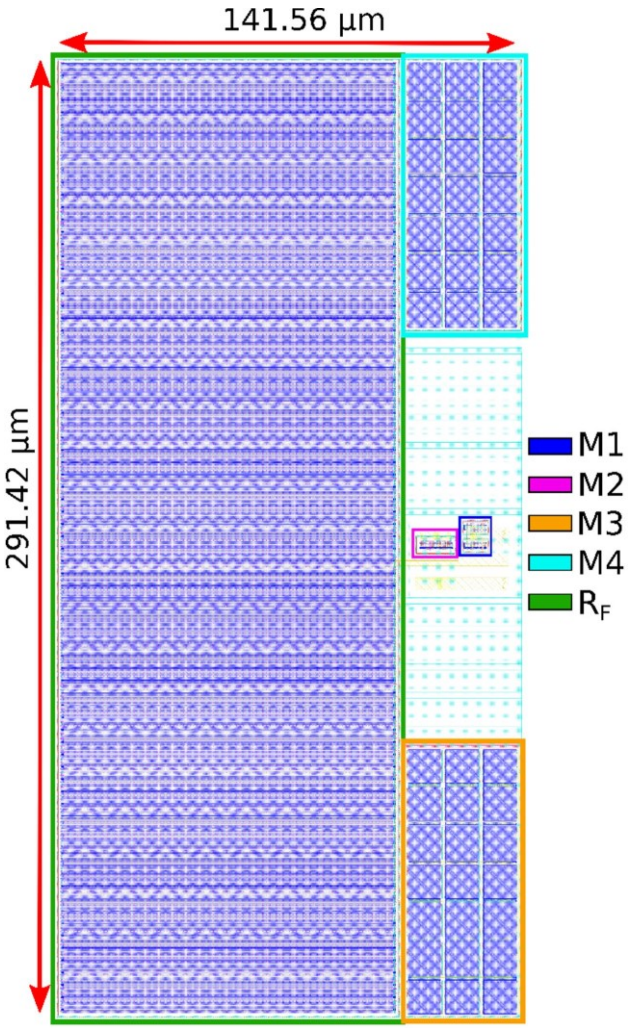

Figure A.1 - Layout of first circuit design

ANNEX B – LAYOUT OF 2ST CIRCUIT DESIGN

Below, the layout for the second circuit design is presented: arrows indicate the overall width and height dimensions; the colored boxes relate the component with its respective layout cell. To recall, M_1 and M_2 form the CMOS inverter, M_3 and M_4 are MOS capacitors and M_5 substitutes the resistor from technology, hence, this layout has smaller area.

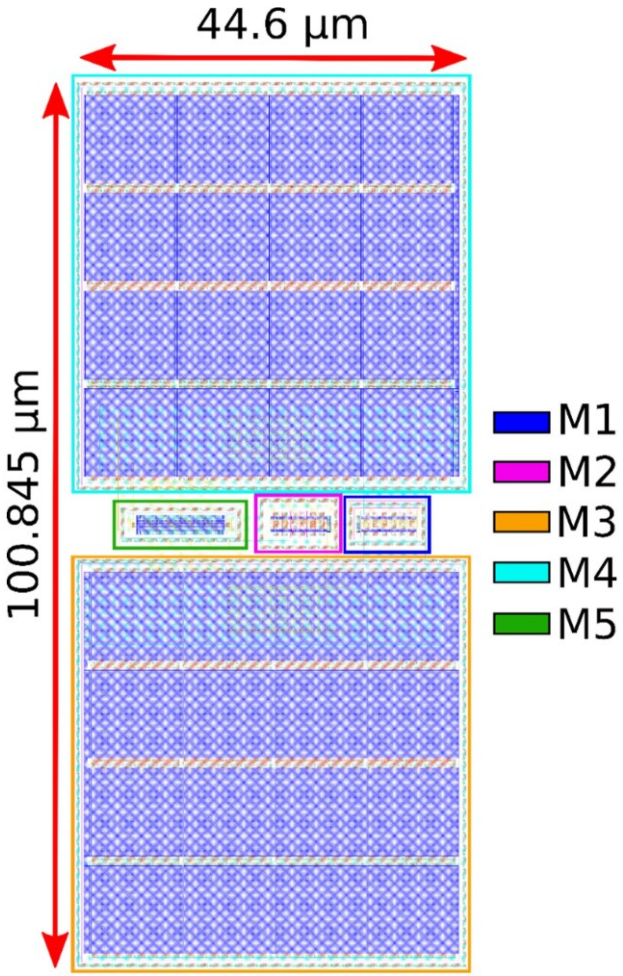

Figure B.1 – Layout of second circuit design