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ISFETs in standard CMOS technology: design and test

Florianópolis

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Orientador: Prof. Dr. Carlos Galup-Montoro.

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ISFETs in standard CMOS technology: design and test

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Florianópolis, 2022.

Este trabalho é dedicado à minha mãe, Gislaine Wrege, e à memória de meu pai, João Alberto Wrege.

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RESUMO

Transistores de efeito de campo sensível a íons (ISFETs) são sensores de íons baseados em transistores de efeito de campo metal-óxido-semicondutor (MOSFETs) e são aplicados em diversas áreas, incluindo detecção de vírus e sequenciamento de DNA. ISFETs implementados em tecnologia CMOS (*complementary metal-oxide semiconductor*) padrão adotam a típica passivação de Si_3N_4 como camada sensitiva e se beneficiam de alto níveis de integração sem a necessidade de etapas de pós-fabricação. Porém, esta implementação é associada a não-idealidades, como offsets aleatórios na tensão de limiar devido a cargas presas na passivação, que necessitam de maior compreensão e caracterização. Para a análise de parâmetros elétricos sem os efeitos eletroquímicos das medições convencionais, esta tese propõe um teste a seco, no qual uma fina camada de metal substitui a solução e o eletrodo de referência. A estrutura do sensor foi analisada e foi desenvolvido um modelo físico para ISFETs em contato com líquidos e com metais. Esta tese apresenta o projeto de dois chips-teste projetados no software Virtuoso® e enviados para fabricação em tecnologias CMOS comerciais de 0.18- e 0.35-µm. ISFETs fabricados na tecnologia de 0.18 µm foram encapsulados com uma câmara de epoxy, metalizados com uma camada de ouro e caracterizados. Resultados de testes a seco, analisados com o modelo físico, mostraram que n-ISFETs e p-ISFETs tiveram, em média, offsets devido a cargas presas similares quando estão no mesmo chip, e uma larga variação entre chips. A dispersão da tensão de limiar medida com o teste a seco está de acordo com as dispersões reportadas na literatura para testes com líquidos. Sensibilidades ao pH medidas de um n-ISFET e de um p-ISFET presentes em chips não-metalizados produzidos no processo de 0.18 µm foram próximas ao valor previsto pelo modelo simulado no MATLAB® (~45 mV/pH). Esta tese também propõe uma topologia de circuito que permite leituras diferenciais e não-diferenciais e apresenta a análise do circuito e simulações. A caracterização de ISFETs fabricados mostrou que o teste a seco pode ser útil como uma ferramenta complementar ao teste com líquidos para análises de ISFETs. A fabricação dos chips foi custeada pela empresa Chipus Microeletrônica S.A. O encapsulamento, a metalização e o teste com líquidos foram concedidos pelo Itt Chip/UNISINOS, LAMATE/UFSC e Laboratório de Prototipagem/FIOCRUZ-PR, respectivamente.

Palavras-chave: ISFET. Sensor de pH. Modelagem do ISFET. Caracterização elétrica. Teste a seco.

RESUMO EXPANDIDO

Introdução

Transistor de efeito de campo sensível a íons (ISFET) é um micro sensor baseado em transistor de efeito de campo metal-óxido-semicondutor (MOSFET) e é capaz de medir concentrações iônicas, geralmente pH. O ISFET vem sendo usado em diversas áreas, incluindo análise de alimentos [1], mapeamento iônico [2], detecção de bactérias [3] e de vírus [4], sequenciamento de DNA [5] e detecção de estágios iniciais de câncer [6]. O conceito de ISFET surgiu em 1970 [7] mas somente em 1999 foi proposta uma técnica para implementar ISFETs em tecnologia CMOS (*complementary metal-oxide semiconductor*) padrão [8]. Apesar do crescente uso dos ISFET em diversas áreas e dos benefícios em se usar o processo CMOS padrão, a implementação destes sensores apresenta certas não-idealidades. Algumas destas não-idealidades possuem valores imprevisíveis, como as cargas presas na passivação, e necessitam de uma melhor compreensão e caracterização. Frente a isso, esta tese foca no projeto, modelagem e medição de ISFETs fabricados em tecnologia CMOS padrão. Este trabalho aborda os desafios gerados pelas não-idealidades e propõe um teste a seco, no qual a solução e o eletrodo de referência são substituídos por uma fina camada de metal. Desta forma, o teste a seco permite a medição de parâmetros elétricos do sensor, tais como atenuação capacitiva e cargas presas na passivação, sem as interferências eletroquímicas dos testes convencionais. Este teste é proposto como uma ferramenta complementar ao teste com líquidos na análise de ISFETs. Um modelo físico é proposto tanto para ISFETs em contato com líquidos como em contato com metais. Além disso, uma topologia de circuito para leituras diferencias e não-diferenciais também é apresentada neste trabalho.

Objetivos

ISFET são comumente caracterizados utilizando líquidos (geralmente com pH 7) e um eletrodo de referência (geralmente Ag/AgCl) cujas características eletroquímicas afetam na medição. Além da sensibilidade ao pH, outros parâmetros elétricos dos ISFETs precisam ser caracterizados para se desenvolver um projeto apropriado. Desta forma, esta tese propõe um teste a seco para uma caracterização puramente elétrica de parâmetros dos ISFETs, sem influências eletroquímicas. Neste teste, a solução e o eletrodo são substituídos por uma fina camada de metal. O teste a seco remove efeitos degradantes das medições convencionais, tais como as correntes de fuga do eletrodo de referência que afetam a deriva temporal [9] e a degradação da camada de passivação causada por longos períodos de contato com o liquido [10]. A estrutura do ISFET em contato com líquidos e com a camada de metal é analisada e é proposto um modelo físico para as condições liquidas e metalizadas. O modelo é utilizado juntamente com as medidas para a análise dos sensores projetados durante esta tese e fabricados em tecnologia CMOS comercial. Além disso, este trabalho propõe o projeto de um chip teste CMOS optimizado para medidas diferenciais e apresenta uma topologia de circuito que permite tanto medidas diferenciais quanto não-diferenciais.

Metodologia

Esta tese apresenta o projeto de dois chips enviados para fabricação em tecnologias CMOS comerciais. Ambos os chips foram projetados na ferramenta Virtuoso® e tiveram suas fabricações custeadas pela empresa Chipus Microeletrônica S.A (Florianópolis/SC, site: [11]). O primeiro chip foi projetado em 2018 e fabricado em tecnologia CMOS 0.18 µm (Malaysia). Este chip possui matrizes de 15 n-ISFETs e 15 p-ISFETs e foi encapsulado em DIP40 com uma câmara de epoxy com dimensões aproximadas de 1 mm de diâmetro e 0.5 mm de altura, a qual cobriu *pads* e *wire bonding*, deixando exposta somente a área dos sensores. Esta câmara foi desenvolvida e aplicada pelo ITT Chip (São Leopoldo/RS, site: [12]). O segundo chip foi enviado para fabricação em 2021 em uma tecnologia CMOS 0.35 µm. Este chip

contém matrizes de 8 n-ISFETs e 8 p-ISFETs distribuídas para facilitar a aplicação de duas micro câmaras sobre o chip, para se realizar medidas diferenciais. O teste a seco, proposto neste trabalho, foi realizado através da deposição de uma camada de ouro sobre o chip fabricado na tecnologia de 0.18 μm, utilizando-se a técnica de DC *sputtering*. O procedimento de metalização foi realizado no laboratório LAMATE/UFSC, sob coordenação do Prof. Dr. Carlos Rambo. A sensibilidade ao pH foi medida depositando-se buffers de pH 4, 7 e 9 sobre chips não metalizados da tecnologia de 0.18 μm e polarizados com um eletrodo padrão Ag/AgCl. Os testes com líquidos foram realizados no laboratório Friocruz/PR, sobre coordenação do Dr. Lucas Blanes. As simulações do modelo e dos circuitos foram realizadas nos programas computacionais MATLAB®, LTSPICE® e Virtuoso® e o projeto da PCB para testes com líquidos no programa Proteus®.

Resultados e Discussão
Os ISFETs fabricados no processo de 0.18 μm foram caracterizados em bancada. Resultados da caracterização a seco de quatro chips metalizados foram analisados e comparados com o modelo desenvolvidas nesta tese. Mediu-se os parâmetros elétricos de cerca de 100 ISFETs, incluindo tipos n- e p-. Utilizando-se o modelo proposto e o teste a seco, estimou-se as cargas presas na passivação, que são responsáveis por grandes variações na tensão de limiar dos dispositivos. Em resumo, n-ISFETs e p-ISFETs do mesmo die apresentaram, em média, offsets similares, porém apresentaram grandes variações entre chips. A dispersão da tensão de limiar medida com o teste a seco está de acordo com as dispersões reportadas na literatura para testes com líquidos. As sensibilidades ao pH medidas de um n-ISFET e de um p-ISFET de chips não-metalizados foram próximas ao valor previsto pelo modelo teórico (cerca de 45 mV/pH). A topologia de um circuito para medidas diferenciais e não diferenciais foi proposta e simulada. Resultados de simulação estão de acordo com a análise teórica, e a topologia permitiria a compensação de certas não-idealidades do sensor.

Considerações Finais
Este trabalho mostrou a possibilidade de se utilizar um teste a seco para a determinação de parâmetros puramente elétricos dos ISFETs sem influências eletroquímicas da solução e do eletrodo de referência. A modelagem do ISFET metalizado permitiu a estimativa de cargas presas na passivação. Trabalhos futuros podem aprimorar a técnica de metalização para aplica-la em dispositivos não-encapsulados, permitindo uma caracterização mais barata e mais rápida. O teste a seco pode ser usado para uma análise separada das contribuições químicas e elétricas de efeitos como ruido e temperatura nas características dos ISFETs. Durante os testes com líquidos, percebeu-se a necessidade de se aplicar uma técnica de limpeza mais robusta para a reutilização dos chips, devido a instabilidades após algumas horas de teste. A câmara de epoxy poderia ser aprimorada para permitir a aplicação de duas câmaras sobre um chip, o que permitiria realizar medidas diferenciais entre ISFETs do mesmo chip. Com uma análise mais profunda dos parâmetros, os sensores poderão ser aplicados na análise de amostras biológicas e serem integrados juntamente com o circuito de leitura e com um pseu-eletrodo para formar um sistema portátil, adequado para aplicações *lab-on-a-chip*.

Palavras-chave: ISFET. Sensor de pH. Modelagem do ISFET. Caracterização elétrica. Teste a seco.

ABSTRACT

Ion-sensitive field-effect transistors (ISFETs) are ion sensors based on metal-oxide-semiconductor field-effect transistors (MOSFETs) and are used in various applications, including virus detection and DNA sequencing. ISFETs implemented using standard complementary metal-oxide semiconductor (CMOS) technology adopt the inherent Si_3N_4 passivation as the sensing layer and benefit from high integration levels with no need for post-processing steps. However, this implementation is associated with nonidealities, such as random offsets in the threshold voltage due to charges trapped in the passivation, that still need better understanding and characterization. For the analysis of electrical parameters without the electrochemical effect from conventional measurements, this thesis proposes a dry test wherein a thin metal film replaces the solution and reference electrode. The sensor structure was analyzed, and a physical model of ISFETs in contact with electrolytes and metals was developed. This thesis presents the project of two test chips designed using the software Virtuoso® and sent for fabrication in 0.18- and 0.35-µm commercial CMOS technologies. ISFETs fabricated using the 0.18 µm technology were packaged with an epoxy chamber, metallized with a gold film and characterized. Dry test measurements, conducted using the physical model, showed that n-ISFETs and p-ISFETs had, on average, similar intra-die offsets due to trapped charges and high die-to-die variations. The dispersion of threshold voltage measured using the dry test was in accordance with the dispersions reported in the literature for wet tests. The measured pH sensitivities of an n-ISFET and a p-ISFET from non-metalized chips produced in the 0.18 µm process were close to the value predicted by the model simulated in MATLAB® (~45 mV/pH). This thesis also proposes a circuit topology that allows both differential and single-ended measurements and presents the circuit analysis and simulation. The characterization of the fabricated ISFETs showed that the dry test could be useful as a complementary tool to the wet test for ISFET analysis. The fabrication of the chips was funded by Chipus Microeletrônica S.A. The packaging, metallization, and wet measurements were supported by Itt Chip/UNISINOS, LAMATE/UFSC and Laboratório de Prototipagem/FIOCRUZ-PR, respectively.

Keywords: ISFET. pH sensor. ISFET modelling. Electrical characterization. Dry testing.

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ABBREVIATIONS

ACM - Advanced Compact MOSFET

BSIM - Berkeley Short-Channel Insulated gate field-effect transistor Model

CDS - Correlated double sampling

CMOS – Complementary Metal Oxide Semiconductor

CVCC - Constant-Voltage, Constant-Current

DIL - Dual in line

DNA – deoxyribonucleic acid

FPN - Fixed-pattern noise

GCS - Gouy-Chapman-Stern

HV – High Voltage

ISFET - Ion Sensitive Field Effect Transistor

IUPAC - International Union of Pure and Applied Chemistry

MOSFET - Metal Oxide Semiconductor Field Effect Transistor

n-ISFET – n-channel ISFET

n-MOSFET – n-channel MOSFET

OHP - Outer Helmholtz plane

PCB - Printed circuit board

PCR - Polymerase chain reaction

PDK - Process design kit

pH - Concentration of hydrogen ions in a substance

pH_{pzc} - pH at which the oxide surface is electrically neutral (point of zero charge)

p-ISFET – p-channel ISFET

p-MOSFET – p-channel MOSFET

qRE - Quasi Reference Electrode

REFET – Reference FET

RNA – Ribonucleic acid

SHE – Standard Hydrogen Electrode

SPICE - Simulation Program with Integrated Circuits Emphasis

TSMC - Taiwan Semiconductor Manufacturing Company

UICM - Unified current-control model

USG - Undoped Silicate Glass

SYMBOLS

A_{mos} - Gate area

A_{pass} - Top metal area

C - Electrolyte concentration in mol/m³

C'_{eq} – Series equivalent of C'_G and C'_H

C'_G – Gouy-Chapman capacitance per unit area

C'_H – Helmholtz capacitance per unit area

C'_{ox} - Oxide capacitance per unit area

C_b - Depletion capacitance

C_d – Differential capacitance

C_{eff} - Equivalent series capacitance of C_{ox} and C_{pass}:

C_{ox} – Oxide capacitance

C_{pass} – Passivation capacitance

C_{SiN} – Si_3N_4 layer capacitance

C_{USG} –USG layer capacitance

E_{ref} – Absolute electrode potential

g_m – Transconductance

H_b - Ion concentration in the solution

H_s - Proton concentration in the insulator surface

I_D – Drain current

i_f – Forward inversion level

i_r – Reverse inversion level

I_S – Specific (normalization) current of the MOSFET

I_{SISF} – Specific current of the ISFET in contact with electrolytes

I_{SISF_met} – Specific current of the metal-gate ISFET

K_- - Negative dissociation constant of the passivation

k -Boltzmann constant

K_+ - Positive dissociation constant of the passivation

K_n - Amine sites dissociation constants of the passivation layer

L - Transistor length

n^0 - Concentration of ions in the bulk solution

Na - Avogadro's constant

n_{ISF} – Slope factor of the ISFET in contact with electrolytes

n_{ISF_met} – Slope factor of the metal-gate ISFET

n_{mos} – MOSFET slope factor

N_{nit} - Primary amine sites per area

N_{sil} - Number of silanol (SiH_3OH) sites per area

q – Electron charge

Q_b - Charge trapped at the silicon

Q_{ox} – Charge at the interface oxide/semiconductor

Q_{pass} – Charge at the passivation layer

T – Absolute temperature

t_{ox} – Gate oxide thickness

t_{pass} - Passivation thickness

V_{BIAS} – Bias voltage

V_{chem} – Potentials due to electrochemical contributions

V_D – Drain voltage

V_{DD} – Positive supply voltage

V_{DS} – Drain-source voltage

V_{DSsat} - Saturation voltage between drain and source terminals

$V_{FB,ISF}$ – ISFET flat-band voltage

V_{GB} – Gate-Bulk voltage

V_{GS} – Gate-source voltage

V_O – Output voltage

V_P – Pinch-off voltage

V_{REF} - Reference electrode voltage

V_S – Source voltage

V_{SS} – Negative supply voltage

V_{tc} - Offset in threshold voltage due to trapped charges

V_{TISF} – Threshold voltage of the ISFET in contact with electrolytes

V_{TISF_met} – Threshold voltage of the metal-gate ISFET

V_{Tmos} – MOSFET threshold voltage

W – Transistor width

x_2 - OHP distance from electrode

X_{sol} - Potential due to dipoles in the insulator interface

z - Magnitude of the ionic charge

α – ISFETs sensitivity parameter

α_{att} – Capacitive attenuation constant

β_{int} – Intrinsic buffer capacity

γ - MOSFET body-effect factor

γ_{chem} – Sum of electrochemical potentials

ε_0 - Permittivity of free space

ε_r - Relative dielectric constant of the medium

ε_{rox} - Relative dielectric constant of the gate oxide

ε_{rpass} - Relative dielectric constant of the passivation

ε_s – Permittivity of silicon

κ_T – Technological depended constant of ISFET threshold voltage

μ - Carrier mobility

ρ – Charge density

σ_d - Charge density at the diffuse layer

σ_{mos} – Charge density at the semiconductor

σ_o - Charge density at electrolyte/insulator interface

ϕ_2 - Potential in the OHP

ϕ_{Au} - Work function per electron charge of gold

ϕ_{eo} - Electrolyte/insulator interface potential

ϕ_f - Fermi potential

ϕ_{lj} - Liquid junction potential between electrode and solution

ϕ_{met} - Work function per electron charge of aluminum

ϕ_{poly} - Work function per electron charge of the polysilicon gate

ϕ_s – Semiconductor surface potential

ϕ_{sc} - Work function per electron charge of the semiconductor

ϕ_t – Thermal voltage

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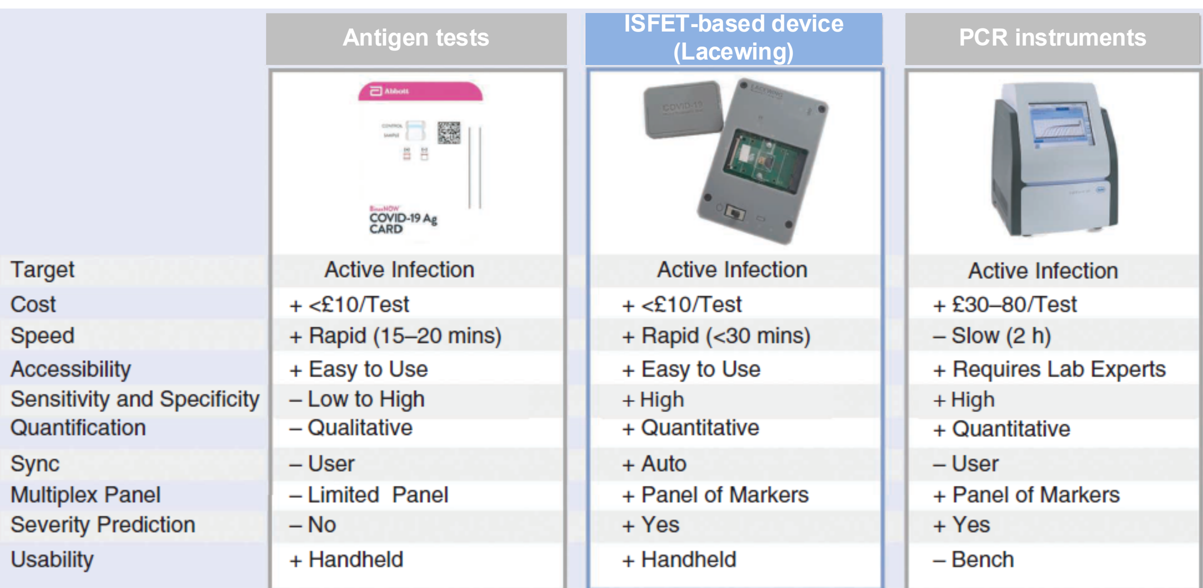
1 INTRODUCTION

The ion-sensitive field-effect transistor (ISFET) is a microsensor based on the metal oxide semiconductor field-effect transistor (MOSFET) capable of measuring the ionic concentration of a solution, such as pH. The ISFET has been used in different fields, including food analysis [1], ion imaging [2], detection of bacteria [3] and viruses [4], DNA sequencing [5] and early detection of DNA methylation for cancer screening [6]. As Figure 1 shows, an ISFET-based handheld device for detection of infectious diseases (called Lacewing [13]) can be portable and cheap as an antigen test and precise as a PCR instrument.



	Antigen tests	ISFET-based device (Lacewing)	PCR instruments
Target	Active Infection	Active Infection	Active Infection
Cost	+ <£10/Test	+ <£10/Test	+ £30–80/Test
Speed	+ Rapid (15–20 mins)	+ Rapid (<30 mins)	– Slow (2 h)
Accessibility	+ Easy to Use	+ Easy to Use	+ Requires Lab Experts
Sensitivity and Specificity	– Low to High	+ High	+ High
Quantification	– Qualitative	+ Quantitative	+ Quantitative
Sync	– User	+ Auto	– User
Multiplex Panel	– Limited Panel	+ Panel of Markers	+ Panel of Markers
Severity Prediction	– No	+ Yes	+ Yes
Usability	+ Handheld	+ Handheld	– Bench

Figure 1 – Comparation of an ISFET-based handheld device, antigen tests and PCR instruments for detection of infectious diseases [13].

In 1970, Bergveld introduced the basic idea behind ISFET [7]. During the early years of research, additional fabrication steps were required to convert the MOSFETs into ion-sensitive sensors. In 1999, almost three decades after the advent of ISFETs, Bausells proposed a technique to implement ISFETs in standard complementary metal-oxide semiconductor (CMOS) technology, without additional fabrication steps [8]. The extended-gate technique is used to connect the transistor gate to the top metal, which is in contact with the passivation layer, usually Si_3N_4, as shown in Figure 2a. The extended-gate technique eliminated the post-processing steps required in the early fabrication methods, reduced fabrication costs and time, and expanded the sensor application to lab-on-chip platforms, allowing the integration of

high-density arrays with more than 1000 sensors per chip [14], with small dimensions, mass production at low cost, and the coexistence of the sensor, readout, and bias circuitry on the same chip.

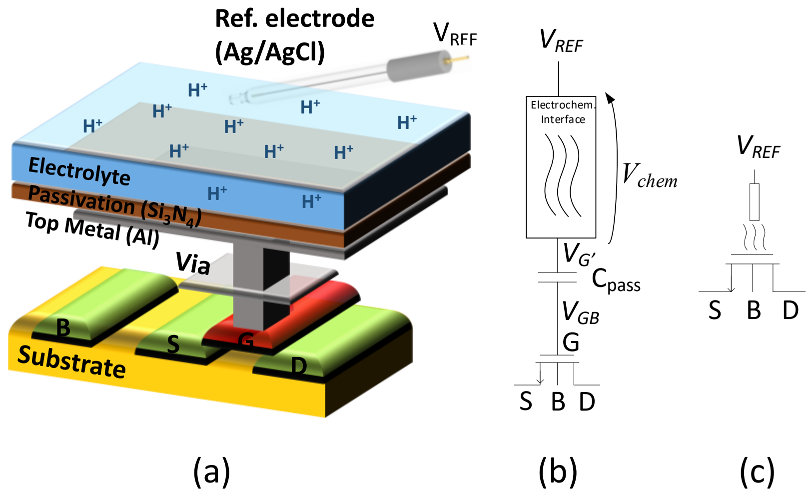


Figure 2 – (a) Illustration of the ISFET cross-section in standard CMOS technology. (b) Simplified ISFET capacitive model (adapted from [15]). (c) The ISFET symbol (*B*, *S*, *D*, and *G* are the bulk, source, drain and floating gate terminals, respectively.).

In the extended-gate technique, the floating-gate terminal is covered with a passivation layer, which is in contact with a solution polarized by a reference electrode (usually Ag/AgCl). Consequently, the ISFET threshold voltage changes according to the ion concentration of the solution. Theoretically, a maximum sensitivity of $2.3\phi_t$ (59 mV/pH at 25°C) is expected [16], where ϕ_t is the thermal voltage. The sensitivity depends on the material used as the sensing membrane. Practical results are lower than this value, mainly because of imperfections in the material used as the sensing membrane [1]. The deposition of selective polymer membranes above the passivation layer allows the detection of different ionic species, such as sodium and potassium, rather than pH [17].

Despite the increasing use of ISFETs in different areas and the benefits of using a standard CMOS process, the implementation of these sensors presents some non-ideal behavior. Some nonidealities have unpredictable values, such as trapped charge offsets, and need to be better understood and characterized.

This PhD thesis focuses on the design, modelling, and measurement techniques of ISFETs in commercial CMOS technologies. This work addresses some of the ISFET non-ideality challenges by proposing a dry test in which a thin metal film replaces the solution and

reference electrode. The dry test allows measurement of electrical parameters, such as threshold voltage, capacitive attenuation, and estimation of trapped charges, without electrochemical influences. This test is supposed to be a complementary tool for ISFET analysis, given that the conventional wet test is still required for full sensor characterization. For better device design and analysis of measurements, this research proposes a model for ISFETs in contact with electrolytes and with a metal layer, presenting mathematical expressions for the main electrical parameters. A circuit topology aimed at single-ended and differential measurements is also presented.

1.1 THESIS OBJECTIVES

1.1.1 General Objectives

ISFETs are commonly characterized by a wet setup, using solutions (usually with pH 7) and a reference electrode (usually Ag/AgCl), whose chemical characteristics affect measurements. In addition to ion sensitivity, other important ISFET parameters must be characterized for an appropriate design, such as the slope factor, threshold voltage dispersion, capacitive attenuation, and specific current. However, some of the above-mentioned parameter's values are difficult to predict, such as the threshold voltage, which is affected by fluctuations of trapped charges in the passivation layer.

Therefore, to characterize the electrical parameters of ISFETs without electrochemical interaction, this thesis proposes a dry test in which a metal film replaces the reference electrode and solution. The proposed dry test removes some deleterious effects from measurements, such as the leakage current of the reference electrode, which affects the output temporal drift [9] and the passivation degradation due to the long-term contact with the solution [10]. The dry test is supposed to be a complementary tool to the wet test for ISFET analysis and characterization.

This thesis analysis the ISFET structure in contact with electrolytes and with a metal layer and proposes a physical model for both wet and dry conditions. The physical model is used together with the measured results for the analysis of the sensors designed in this thesis and fabricated using a commercial CMOS technology.

A CMOS test chip optimized for differential measurements is proposed, considering the benefits of this type of measurement, such as the reduction of common-mode effects and

the possibility of using compact quasi-reference electrodes for portable applications. This thesis also proposes a circuit topology that allows for both single-ended and differential measurements.

1.1.2 Specific Objectives

The specific objectives of this thesis are:

1. Propose a dry test for the measurement of the electrical parameters of ISFETs without electrochemical effects from conventional wet measurements.
2. Characterize ISFETs implemented in standard CMOS technology through a conventional wet test and the proposed dry test.
3. Model the main ISFET electrical parameters for wet and dry tests.
4. Design a chip optimized for differential measurements and suitable for the implementation of two chambers on the chip.
5. Propose a topology for a readout circuit capable of addressing the main ISFET nonidealities.

1.2 THESIS STRUCTURE

The remainder of this paper is organized as follows: Section 2 presents a literature review. In Section 3, an ISFETs model for the conventional wet test is presented. Section 4 presents details of the designed chips. The methodology and modelling of the dry test are presented in Section 5. A readout topology that allows for both differential and single-ended measurements is proposed in Section 6. The measurement results are presented in Section 7, and the conclusions and future work are presented in Section 8. Complementary materials are presented in the appendices.

2 LITERATURE REVIEW

This chapter summarizes the main nonidealities of ISFETs fabricated using standard CMOS technology and presents some techniques to reduce the effects of these nonidealities and some readout circuit architectures.

2.1 ISFET NONIDIEALITIES

2.1.1 Trapped charges

Charges are trapped in the floating gate and passivation layer of the ISFET owing to the fabrication process. These charges induce random offsets in the threshold voltage, causing large mismatches between the devices (Figure 3a). For example, threshold voltages ranging from -14 V to +8 V have been reported for ISFETs implemented using 0.35 µm CMOS technology [18]. The removal of the top layers from the passivation showed that charges are trapped mainly at the interface of the layers [19].

To reduce the effects of trapped charges, different techniques have been proposed: exposure of the sensor to ultraviolet (UV) radiation for a prolonged time to remove trapped charges [20], hot-electron injection using a high source-drain voltage [21], and electron tunneling through a high voltage coupled to the floating gate by a capacitor [22]. In addition, linear and interdigitated structures present different threshold voltages [8].

2.1.2 Temporal Drift

The threshold voltage of ISFETs suffers from a temporal drift that is influenced by different factors, including the electrolyte pH, sensitive membrane material, device dimensions, and leakage in the reference electrode [10], [9]. This effect is illustrated in Figure 3b and is more relevant for long-term measurements. Drifts between 1.5 and 8.5 mV/h have been reported [18]. To reduce the drift effects, differential sensing between an ISFET and a non-pH-sensitive FET (REFET), an ISFET/ISFET pair, or ISFET/MOSFET can be used [23], [24], [25]. Software processing that implements a mathematical model to reduce its effects on data processing was also used [26].

2.1.3 Capacitive attenuation

Using standard CMOS technology, the ISFET floating gate voltage, which corresponds to the MOSFET gate voltage (V_{GB}), is attenuated with respect to the reference electrode (V_{REF}) as shown in Figure 3a, owing to the capacitive division formed by the passivation layers (usually Si_3N_4/SiO_2) and MOSFET capacitances. This can be concluded from eq. (1) [10]:

$$V_{GB} = V_{G'} \frac{C_{pass}}{C_{pass} + \left(C_{ox}C_b\right) / \left(C_{ox} + C_b\right)} = \alpha_{att} V_{G'} \quad (1)$$

where $V_{G'}$ corresponds to $V_{REF} - V_{chem}$ in Figure 2b, C_b, C_{pass}, C_{ox} are the depletion, passivation, and gate oxide capacitances, respectively, and α_{att} is the capacitive attenuation constant. A complete analysis of the ISFET structure is presented in this thesis.

Capacitor mismatches cause variations in the attenuation factor of ISFETs in an array, affecting, for example, the gain of the sensors [27]. The passivation layer can be modified to reduce the attenuation factor and/or the mismatch. For example, Xu *et al.* [28] exposed the top metal layer of an ISFET letting a natural Al_2O_3 oxidation layer with a thickness of 5 nm grow. Architectures that automatically compensate for the gain of each sensor [27] or are more robust to the attenuation factor [29] are also used.

2.1.4 Temperature effects

The effects of temperature in ISFETs are comparable to those in MOSFETs, but with the additional influence of the electrolyte, reference electrode, and sensitivity membrane. This nonideality is shown in Figure 3c. The influence of temperature is comparable with a variation of 1 pH for each 7 K variation at room temperature [10]. These effects can be reduced by using differential measurements.

2.1.5 Noise

This nonideality reduces sensor resolution. ISFETs present both chemical and MOSFET noise (Figure 3d) [18]. The excess 1/f noise can be reduced by averaging sensors in an array [30], [31].

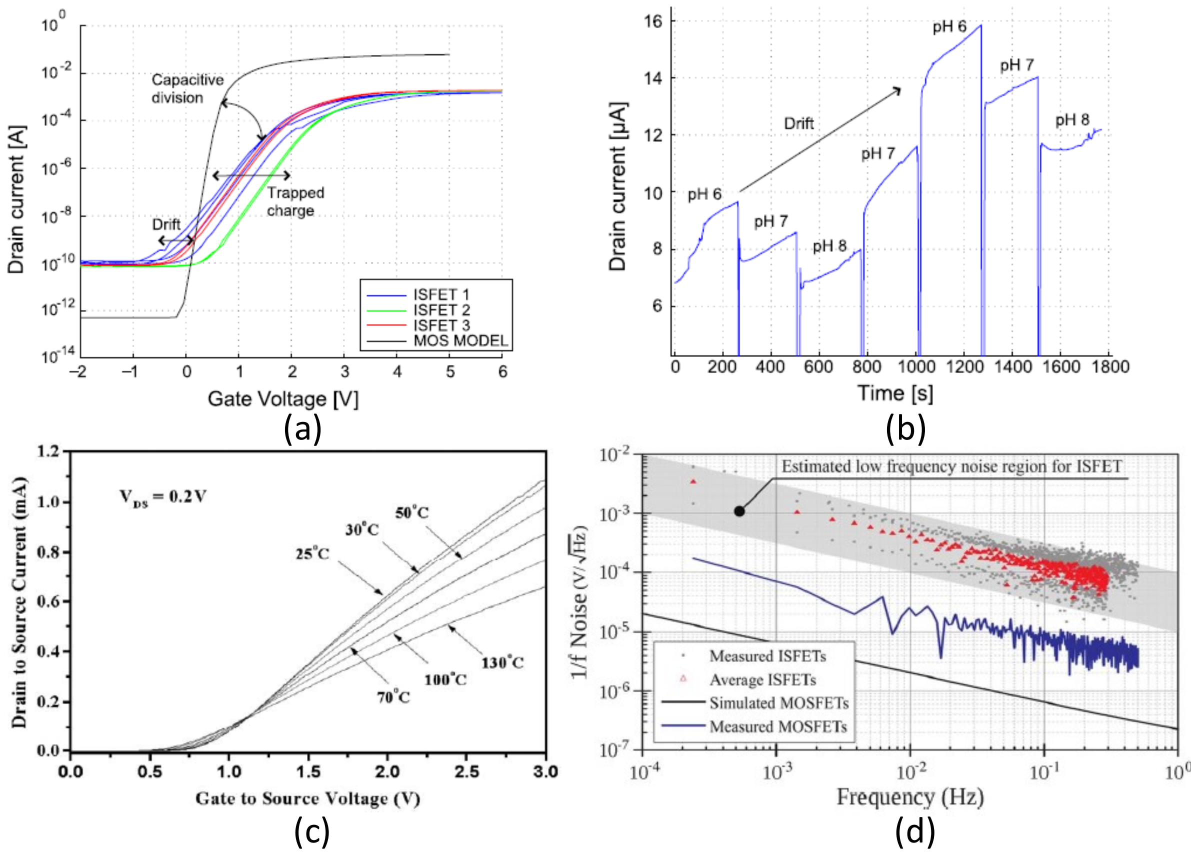


Figure 3 - Main ISFET nonidealities: (a) trapped charges offset and capacitive attenuation, (b) temporal drift, (c) temperature effect, and (d) noise [10], [18].

2.2 ISFETS READOUT

The ISFET readout circuit provides appropriate voltages and/or currents to ensure that the sensor works with optimized electrical characteristics (such as low power consumption), resulting in an electrical output that varies with the pH (such as voltage, current, and frequency of a signal). The readout circuit can be implemented using discrete components (off-chip) or can be integrated into the same chip as the sensor, resulting in a more compact and usually low-power device. The readout can also be performed using a single-ended method, in which a single sensor is used, or a differential method, in which two sensors, or a combination of a sensor with other device, are used to reduce common-mode signals (reducing effects of temperature and temporal output drift [10]).

The readout circuit must address the nonidealities of the sensor and be optimized for the intended application. For example, for long-term tests (of the order of tens of minutes [4], [32]), the temporal drift of the ISFET output voltage may be critical. There are also high-

frequency applications, such as the use of ISFETs as ion image sensors, with sample rates higher than thousand frames per second [33], in which the readout circuit must work at the desired sample rate. Simple and small-area readout circuits may be preferred for dense arrays composed of thousands of ISFETs [10]. Detection of small pH variations (such as 0.045 pH caused by Escherichia coli bacteria in food safety screening [34]) requires a low-noise implementation. The readout circuit must also address large variations in the threshold voltage between sensors in the same or different dies caused by trapped charges.

Therefore, readout circuits for ISFETs implement different topologies. The following sections will present more details about the reference electrode, an important component in the readout of ISFETs, and some of the integrated circuit topologies used in the literature for both single and differential measurements.

2.2.1 Reference electrode

The reference electrode polarizes the solution in contact with the ISFET. Therefore, this element affects the performance of the ISFET, influencing linearity, sensitivity, and noise [35].

For an ideal electrode, the voltage between the electrode and solution does not vary with the solution composition, owing to the electrochemical equilibrium maintained with the solution [36]. Other desirable characteristics of an ideal electrode are reproducibility, chemical and thermodynamic reversibility, low-temperature coefficient, low hysteresis, and easy preparation and handling [37]. Electrodes made of silver-silver chloride (Ag/AgCl) and calomel (Hg_2Cl_2) are commonly used [38].

2.2.1.1 Ag/AgCl electrode

Many ISFET applications use an Ag/AgCl reference electrode. This electrode is composed of an Ag wire covered with AgCl immersed in a saturated inner filling solution containing Cl^- (such as KCl) inside a glass tube with a porous membrane separating it from the test solution [35], as illustrated in Figure 4.

The potential of the Ag/AgCl electrode, relative to the standard hydrogen electrode (SHE), is 0.19 V [5]. At 25°C, the absolute potential of SHE is (4.44 ± 0.02) V [39].

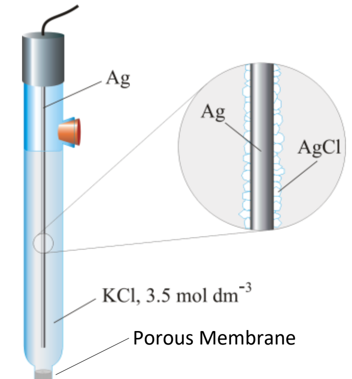


Figure 4 - Ag/AgCl reference electrode [40].

Despite its good electrochemical characteristics, due to its large dimensions, the standard Ag/AgCl electrode is difficult to implement in small volumes, on the order of tens of microliters, or in portable devices. For example, common commercial electrode models have tip diameters of 12 mm and lengths greater than 10 cm [41]. This diameter is close to the cavity width of the chip package used in this study, resulting in a tight fit. As a result, an appropriate standard electrode model must be selected based on the chip chamber dimensions and sample volume, for example.

Smaller alternatives to the standard Ag/AgCl electrode include microfabricated reference electrodes, which have complex construction and a short lifetime [35]. Another option is to use a quasi-reference electrode (qRE).

2.2.1.2 Quasi-reference electrodes

Quasi-reference electrodes are composed of a metal pad or wire in direct contact with the test solution. Figure 5 shows an example of an on-chip Au qRE implemented in a TSCM 0.35 µm technology post-processed with gold [42].

Despite its simplicity and compactness, qRE does not provide a stable potential, presenting variations in the electrode/solution potential according to the solution composition. Therefore, qRE is usually implemented in differential measurements [36], [43]. For example, Scaff [37] compared the pH response of ISFETs using an Ag/AgCl standard electrode and quasi-reference electrodes composed of Pt, Ag, and Au wires. According to measurements, the Au qRE presented the most linear response among the tested quasi-reference electrodes (close to Ag/AgCl linearity), but resulted in a lower pH sensitivity (approximately 34 mV/pH) than the standard Ag/AgCl electrode (approximately 50 mV/pH) [37].

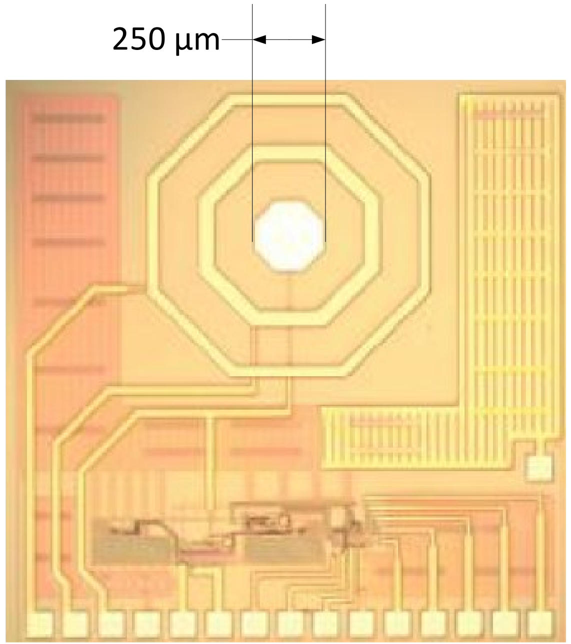


Figure 5 - A built-in Au qRE [42].

2.2.2 Single-ended readout

2.2.2.1 Source follower

The source follower is a commonly used technique (Figure 6a), in which the source voltage is read while the drain current (I_D) and other terminal potentials are kept constant, resulting in changes in the source voltage according to threshold voltage variations with pH [33], [44], [45], [46]. Despite its simplicity, which is suitable for large arrays, the device can alternate between saturation and linear operation because the drain-source voltage (V_{DS}) is not constant [47].

2.2.2.2 Source and drain follower

Other technique used is the source and drain follower, also known as *Constant-Voltage and Constant-Current* (CVCC) (Figure 6b) [20, 33, 48]. In this case, the ISFET is polarized with a constant I_D and constant V_{DS}, so the device does not change the region of operation. The changes in the pH can be read in the source voltage.

2.2.2.3 Current mode

In the current-mode readout, the ISFET drain current I_D is read while the terminals have a constant voltage (Figure 6c). Thus, pH variations are translated into variations in the current I_D. This method benefits from the easier operations in current than in voltage, such as averaging and better compatibility with weak inversion operations [10].

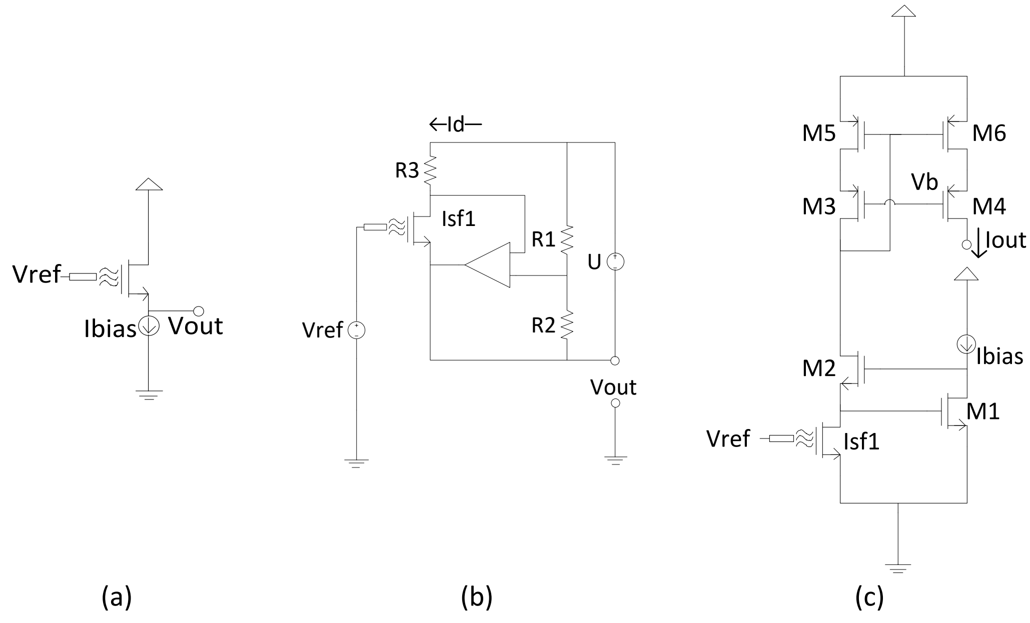


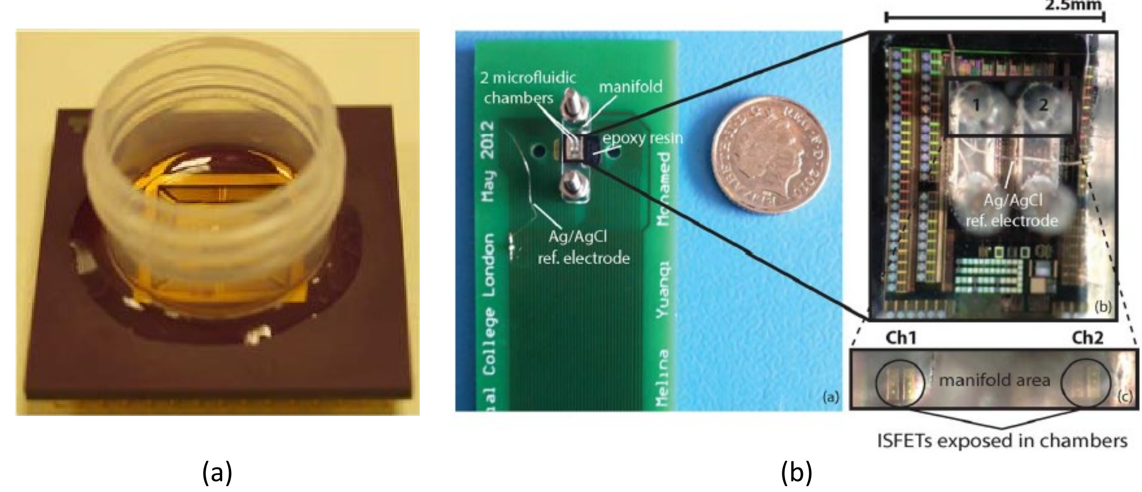
Figure 6 – Single-ended readout circuits: (a) source follower [44], (b) CVCC [1], and (c) current mode [30].

2.2.2.4 Other techniques

Other readout techniques are being developed based on the circuits mentioned in previous sections. For example, there is an active pixel sensor (APS) that originates from image sensors and topologies that convert pH to other domains, such as time or frequency (in order to increase the signal-to-noise ratio) [10]. It is important to mention the benefits of polarizing ISFETs near the threshold or subthreshold voltage, given that in this case, the g_m/I_D ratio is increased and the capacitance due to inverted channel charges is reduced [28].

2.2.3 Differential readout

As mentioned previously, differential measurements can compensate for several nonidealities, such as temperature effects and temporal drift, and allow the use of quasi-reference electrodes. This method can be applied between an ISFET and a non-pH-sensitive FET (called REFET), or an ISFET/ISFET pair, or ISFET/MOSFET [23], [24], [25]. Despite the benefits, differential sensing implementing two ISFETs requires two chambers (one chamber for each ISFET), which are more difficult to implement than the one chamber used in single-ended measurements (Figure 7). When two chambers are used, each ISFET measures different solutions: one is the reference solution (usually pH 7), and the other is the solution in which the pH must be monitored. Another challenge with differential measurements is threshold voltage mismatch between devices [10].



(a) (b)

Figure 7 - Example of chambers for (a) single-ended [31], and (b) differential measurements [23].

2.2.3.1 ISFET-REFET pair

Milgrew *et al.* [49] implemented a pair of ISFET/REFET polarized with a quasi-reference electrode (Figure 8a). The output is the difference between the drain voltages of the devices as obtained using an instrumentation amplifier.

2.2.3.2 ISFET-ISFET Chemical Gilbert Cell

Figure 8b shows a circuit that operates under differential currents. In this case, an ISFET/ISFET pair was implemented in a Gilbert cell, in which the output current is the difference between the drain current of each ISFET [23].

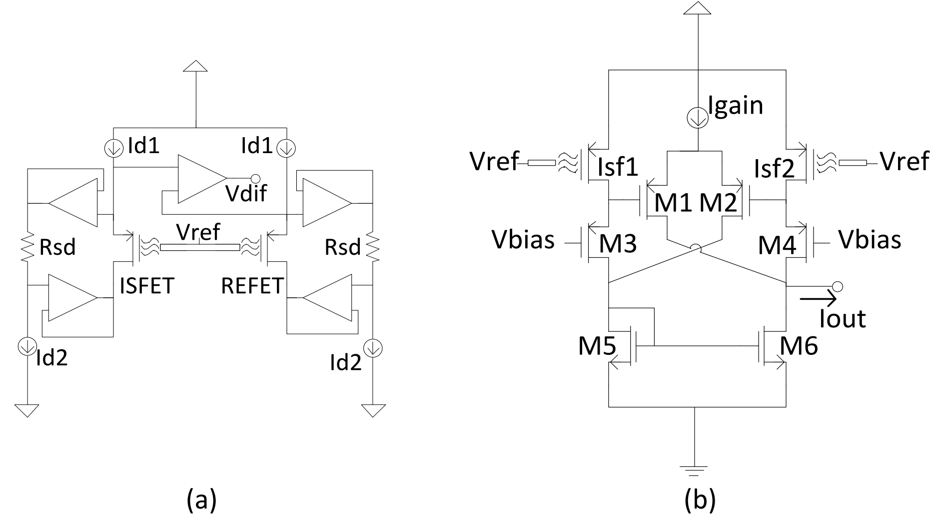


Figure 8 - Differential measurements: (a) voltage [49], and (b) current mode [23].

2.3 SUMMARY OF COMPENSATION TECHNIQUES

The techniques applied to overcome ISFET nonidealities can be distinguished into two categories: sensor/device adaptation, in which compensation methods are applied to the sensor, and system-level compensation, in which the output signal is processed to compensate for the nonidealities [10].

Table 1 summarizes the main device- and system-level compensation techniques used to overcome trapped charge offsets, temporal drift, capacitive attenuation, temperature, and noise of ISFETs implemented in commercial technologies. Procedures to improve the sensor performance by modifying the passivation layer, such as the removal of the passivation top layers [19] or the replacement of the passivation layer with other materials [28], are not shown. Further details are discussed in [10].

Table 1 - Compensation techniques for ISFETs in commercial technologies (adapted from [10])

		Method.	Description.	Advantages.	Disadvantages.
Trapped Charge	Device	UV exposure	Exposure to UV for hours.	No need of extra circuits.	Post-processing technique.
		Programmable-Gate (PG) ISFET	A capacitor is added to the floating gate (FG) of ISFET with a bias voltage.	Allows calibration algorithms or feedback to the FG.	Reduction on sensor sensitivity. Extra circuit components. External bias voltage or lookup table. Phases of operation increase the complexity.
		Hot-electron injection	Removal of electrons from the FG using large $V_{DS.}$	No need of extra circuits.	Requires high voltage. It is unidirectional.
		Bidirectional electron tunnelling	Addition or removal of electrons from the FG.	Lower current levels than hot-electron injection. Allows to inject or remove electrons.	Uses high voltages. Leakage current. Slow compensation process.
		Reset switch on the FG	Switch at the FG for offset reset.	Simple circuit.	Leakage current reduces the measurement time.
		Source voltage compensation	Modulation of the ISFET source voltage.	No need to access the FG. No need of extra components or post-processing.	Limited compensation range. Specific to certain topologies.
		Technology with high quality dielectric [43]	Controlled fabrication applying anneals in a hafnium dielectric.	No need to access the FG. No need of extra circuits.	Requires a specific commercial process, not commonly available (ex. TSMC SOI 180 nm).
	System	Baseline frame calibration	Subtraction of the mean of a number of baseline frames before measure the output.	Elimination of Fixed-pattern noise (FPN).	Averaging is computational and requires software processing. Post-readout compensation.
		Correlated Double Sampling (CDS)	Typical CDS amplifier readout.	On-chip implementation.	Uses a high frequency clock. Post-readout compensation.
Drift	Device	Offset calibration	Reset to the FG or PG-ISFET.	Simple implementation. Direct feedback to the FG.	Leakage current.
		Cycling of electric fields	Drift reset with an on-chip ring oscillator driving $V_{REF.}$	On-chip implementation.	Oscillation of V_{REF} can be restraining.
	System	Differential measurement	Subtract the output from a REFET or an ISFET in a ref. solution.	Eliminates common-mode voltages.	Requires 2 sensors. The 2 ISFETs must have same behavior.
		External signal processing	Based on sampling and differentiating of the output voltage.	Robustness.	Off-chip data processing. Assumes a negligible drift compared to pH changes.
		Correlated Double Sampling (CDS)	Uses an OPAMP with switched-capacitor feedback.	On-chip implementation.	Needs a clock period higher than the drift time. Post-readout compensation.

		Method.	Description.	Advantages.	Disadvantages.
Capacitive divider	Device	Capacitive feedback with CVCC [29]	A CVCC readout with feedback to the FG bypasses the capacitive division.	On-chip implementation.	Feedback to the FG.
	System	Automatic Gain Control [50], [27]	The system compensates gain mismatches that are continuously measured with a high frequency and small amplitude signal superimposed to the ref. electrode.	Real-time compensation. On-chip implementation.	Requires a superimposed signal in the electrode. Extra circuits.
Temperature	Device	Biasing at the athermal point	Dynamic ISFET biasing using an algorithm.	Suitable for nonlinear temperature compensation.	Computational technique. Off-chip implementation. Based on mathematical assumptions.
		Periodic gate reset	Reset the FG to a ref. voltage.	Simple technique.	Leakage current limits the measurement time.
	System	Temperature coefficient cancellation	Add a CTAT voltage to the output.	Simple implementation.	Temperature dependence is not well known and also varies with pH.
		On-chip temperature regulation	Chip designed with temperature sensors and heaters.	Allows applications like on-chip PCR. Robustness due to closed-loop.	Needs spreading of heaters. Not an ISFET compensation method.
		Differential measurement	Subtract the output from a REFET or an ISFET in a ref. solution.	Eliminates common-mode voltages.	Requires 2 sensors. The 2 ISFETs must have same behavior.
Noise	Device	Reset pixel	Periodic reset (structure based on Active Pixel Sensors – APS - architecture).	Flicker noise attenuation due to fast reset. Shot noise reduction.	Possible time effects. Requires high frequency clocks.
	System	Averaging array	Lowers the uncorrelated noise floor by averaging.	Robust for large arrays.	Non efficient for 1/f noise.
		CDS	Attenuates 1/f noise.	On-chip implementation.	Non efficient for white noise. Requires a high frequency clock.

* This table shows only additional references from the ones presented in [10]. For a complete list of references, please refer to [10].

3 ISFET MODELLING

To describe the relationship between the voltages and currents in the ISFET terminals, the site-binding and Gouy-Chapman-Stern (GCS) theories are combined with a transistor model. This thesis uses the advanced compact MOSFET (ACM) model, which is valid in all regions of operation [51], [52]. This chapter describes a model developed for ISFETs in contact with electrolytes, presenting expressions for the main electrical parameters, such as the threshold voltage, slope factor, and specific current.

3.1 CURRENT-VOLTAGE RELATIONSHIP IN THE ISFET TERMINALS

The ACM was extended to the ISFET in a previous paper [53]. According to ACM, the drain current I_D is given in terms of the forward and reverse inversion levels (i_f and i_r, respectively) by [52]:

$$I_D = I_S(i_f - i_r) \tag{2}$$

with I_S being the normalization current, also known as specific current. For a MOSFET, I_S is given by [52]:

$$I_S = \mu C'_{ox} n_{mos} \frac{\phi_t^2}{2} \frac{W}{L} \tag{3}$$

where μ is the carrier mobility, C'_{ox} is the oxide capacitance per unit area, n_{mos} is the MOSFET slope factor, ϕ_t is the thermal voltage (approximately 26 mV at room temperature), W is the transistor width, and L is the transistor length. The terminal voltages are related to the forward and reverse inversion levels according to the following expression, denominated unified current-control model (UICM) [52]:

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \tag{4}$$

where V_S and V_D are the source and drain voltages, respectively, and V_P is the pinch-off voltage [52]:

$$V_P = \frac{V_{GB} - V_{Tmos}}{n_{mos}} \quad (5)$$

where V_{GB} is the gate voltage and V_{Tmos} is the MOSFET threshold voltage.

In the case of the ISFET, eq. (5) can be written as:

$$V_P = \frac{V_{REF} - V_{TISF}}{n_{ISF}} \quad (6)$$

where V_{TISF} and n_{ISF} are the threshold voltage and slope factor of the ISFET, which will be derived in the next subsections. The combination of eqs. (2) and (4) gives the transconductance-to-current ratio (g_m/I_D), where g_m can be either dI_D/dV_G for the MOSFET or dI_D/dV_{REF} for the ISFET.

$$\frac{g_m}{I_D} = \frac{1}{n\phi_t} \frac{2}{\sqrt{1+i_f} + \sqrt{1+i_r}} \quad (7)$$

In eq. (7), n can be either n_{mos} or n_{ISF}. In the next sections, the three main design parameters of the ACM model (threshold voltage, slope factor and specific current) will be derived for the ISFET in contact with electrolytes.

3.2 THRESHOLD VOLTAGE

Threshold voltage is an important electrical parameter for the implementation of devices, such as MOSFETs and ISFETs, in circuit design. Most of the expressions for the ISFET threshold voltage currently presented in the literature are still based on the classical ISFET structure, which differs from the structure implemented in standard CMOS processes that is commonly applied nowadays, as shown in Figure 9. Despite the large and random variations in ISFET threshold voltages due to the fabrication process, an accurate expression can be relevant for better device implementation and for a better understanding of the device nonidealities.

In this section, an expression for ISFETs in standard CMOS technology is proposed and compared with the expressions presented in the literature.

3.2.1 The ISFET Flat-Band Voltage

Figure 2 illustrates an ISFET implemented in standard CMOS technology using the extended gate technique. This technique involves connecting the MOSFET gate, which is left floating, to the top metal that is in contact with the passivation layer, typically silicon nitride (Si_3N_4).

In MOSFETs, the flat-band voltage is the gate bulk voltage that counterbalances the effects of the contact potential and oxide charges [52]. The same concept can be extended to ISFETs by considering the effects of electrochemical potentials, as performed for the classical ISFET structure in [54] and [55]. However, the classical ISFET structure (Figure 9a) differs from that of the ISFET implemented in standard CMOS technology (Figure 9b).

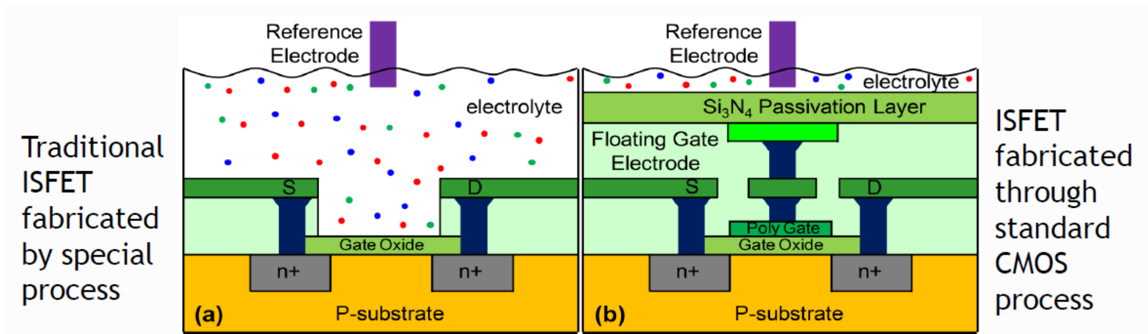


Figure 9 - ISFET fabrication: (a) with post-processing, (b) in standard CMOS process [56].

Comparing both implementations, in standard CMOS technology, the passivation layer forms an additional capacitance in the ISFET structure (C_{pass}), where charges are trapped owing to the fabrication process (Q_{pass}), creating an offset in the ISFET threshold voltage. Furthermore, poly-silicon is connected to the top metal layer (usually Al) of the technology, creating a contact potential [57]. Considering these characteristics, and based on the expression for the classical structure presented in [54] and [55], the flat-band voltage of the ISFET implemented in standard CMOS technology is given by:

$$V_{FB,ISF} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{sc} - (\phi_{met} - \phi_{poly}) - \frac{Q_o}{C_{eff}} - \frac{Q_{pass}}{C_{pass}} \qquad (8)$$

where E_{ref} is the absolute reference electrode potential, ϕ_{lj} is the liquid junction potential between the electrode and solution, ϕ_{eo} is the electrolyte/insulator interface potential (varies with the solution pH), X_{sol} is the potential due to dipoles in the insulator interface, C_{eff} is the effective series capacitance of oxide (C_{ox}) and passivation (C_{pass}) capacitances, Q_o is the

equivalent charge at the interface oxide semiconductor, ϕ_{poly}, ϕ_{sc} and ϕ_{met} are the work functions per electron charge of the polysilicon gate, semiconductor, and aluminum, respectively. The semiconductor work function for n(p)-channel devices ($\phi_{sc_{N(P)}}$) is given by:

$$\phi_{sc_{N(P)}} = \left[\chi + \frac{E_g}{2q} + \phi_t \ln\left(\frac{N_{a(d)}}{n_i} \right) \right] = \left[\chi + \frac{E_g}{2q} + \phi_F \right] \quad (9)$$

where χ is the semiconductor electron affinity per electron charge, E_g is the silicon bandgap, q is the electron charge (1.6×10^{-19} C), $N_{a(d)}$ is the p(n)-type substrate doping, ϕ_F the Fermi potential, and n_i is the intrinsic carrier concentration in silicon [58]. The values for previously cited parameters are listed in Table 2 (p. 56).

An Ag/AgCl reference electrode is typically used in ISFETs. Its absolute potential is given by [59]:

$$E_{ref} = E_{abs}(H^+ \mid H_2) + E_{rel}(Ag \mid AgCl) \quad (10)$$

where $E_{abs}(H^+|H_2)$ is the standard hydrogen electrode (SHE) absolute potential and $E_{rel}(Ag|AgCl)$ is the potential of the Ag/AgCl reference electrode relative to the SHE. Considering the values listed in Table 2, results in $E_{ref} = 4.63V$.

3.2.1.1 The electrolyte/insulator interface potential ϕ_{eo}

The electrolyte/insulator interface potential ϕ_{eo} changes according to the electrolyte pH. It can be obtained from the Gouy-Chapman-Stern (GCS) double-layer model and site-binding theories. The condition for charge neutrality in the ISFET structure results in [60]:

$$\sigma_d + \sigma_o + \sigma_{mos} = 0 \quad (11)$$

where σ_d, σ_o, and σ_{mos} are the charge densities at the diffuse layer, electrolyte/insulator interface, and semiconductor, respectively. Considering σ_{mos} to be constant with pH and much smaller than σ_d and σ_o, the relationship between σ_o and σ_d can be approximated as [60]:

$$\sigma_d = -\sigma_o = -C'_{eq}\,\phi_{eo} \quad (12)$$

where C'_{eq} is the total capacitance per unit area in the double layer interface.

The charge density σ_o can be obtained using the site-binding theory, which describes the equilibrium between the SiOH sites and H^+ ions in solution. According to this theory, σ_o is given by [61]:

$$\sigma_{\mathrm{o}} = \left(\frac{H_s^2 - K_- K_+}{H_s^2 + K_+ H_s + K_- K_+} \right) q N_{sil} + \left(\frac{H_s}{H_s + K_n} \right) q N_{nit} \qquad (13)$$

where N_{sil} is the number of silanol (SiH_3OH) sites per area, N_{nit} is the number of primary amine sites per area, K_+, K_- and K_n are the positive, negative, and amine site dissociation constants of the passivation layer, respectively [61]**.** H_s is the proton concentration on the insulator surface, which is related to the ion concentration in the solution (H_b) using the Boltzmann equation [61]:

$$H_s = H_b \exp\left(-\phi_{eo} / \phi_t \right) \qquad (14)$$

The electrolyte pH is given by $-log_{10}(H_b)$. The parameters used for the Si_3N_4 are listed in Table 2 (p. 56).

The charge density σ_d and capacitance C'_{eq} are obtained using GCS theory. This model considers the charges in two layers: the Helmholtz layer, where charges are close to the insulator surface; the potential varies linearly, extending up to a boundary in the outer Helmholtz plane (OHP); and the Gouy-Chapman layer with diffuse charges following the Boltzmann distribution [38].

The following equations from GCS model are valid for symmetrical electrolytes, also known as z:z electrolytes. Symmetrical electrolytes present one cationic and one anionic species with charge magnitude z, $|z^+| = |z^-| = z$ (for example NaCl, is 1:1) [38], [62].

The charge density σ_d is calculated as [38]:

$$\sigma_{\mathrm{d}} = -\sqrt{8 \mathrm{kTn}^0 \varepsilon_r \varepsilon_0} \sinh\left(z\phi_2 / (2\phi_t) \right) \qquad (15)$$

where ε_0 is the permittivity of free space (8.85×10^{-12} F/m), ε_r is the relative dielectric constant of the medium, k is the Boltzmann's constant (1.38×10^{-23} J/K), T is the absolute temperature, ϕ_2 is the potential of the OHP (eq. (17)) and n^0 is the concentration of ions in the bulk solution (m^{-3}). The parameter n^0 can be expressed in terms of the electrolyte concentration C (mol/L)

through $n^0 = NaC$, where Na is Avogadro's constant (6.02×10^{23} mol^{-1}) and considering that 1 mol/L = 10^3 mol/m^3.

The capacitance C'_{eq} in this model is given by [38]:

$$\frac{1}{C'_{eq}} = \frac{x_2}{\varepsilon_r \varepsilon_0} + \frac{1}{\sqrt{2\varepsilon_r \varepsilon_0 z^2 q^2 n^0 / (kT)} \cosh\left(z\phi_2/(2\phi_t)\right)} = \frac{1}{C'_H} + \frac{1}{C'_G} \qquad (16)$$

where x_2 is the OHP distance from the electrode. C'_{eq} is the effective series capacitance of a linear capacitance (C'_H) and a non-linear capacitance (C'_G), denoted the Helmholtz and Gouy-Chapman capacitances per unit area, respectively. The ε_r and x_2 values are listed in Table 2 (p. 56). More details about the GCS theory are presented in [38].

With the expressions presented, potentials ϕ_{eo} and ϕ_2 can be obtained using the following equations:

$$\begin{cases} \phi_{eo} = \dfrac{\sigma_o}{C'_{eq}} \\ \phi_2 = \phi_{eo} + \dfrac{\sigma_d}{C'_H} \end{cases} \qquad (17)$$

The assumption that σ_{mos} is invariant with respect to pH and much smaller than σ_d and σ_o used in eq (12) allows the separation of ISFET modeling into an *electrochemical stage* (electrolyte/insulator interface) and an *electronic stage* (MOSFET), originating a behavioral macro model [60]. This model can be easily implemented in commercial simulation tools such as SPICE by connecting a block that models the electrochemical characteristics and potentials to a built-in MOSFET block [60], [63]. On the other hand, physical-chemical models, such as those implemented in BIOSPICE, consider σ_{mos} in the charge neutrality condition, resulting in a more complete model with an equation system that fully characterizes the sensor behavior [61], [64]. However, to implement these physical-chemical models in software such as SPICE, a more complex set of equations is needed as well as a deep knowledge of the codes and language used in the simulation program [60], [61], [65]. Because the comparison between the macro model, physical-chemical model, and practical measurements resulted in good agreement [60], the present work implements the macro model aiming at better compatibility with commercial tools.

3.2.1.2 A simplified expression for ϕ_{eo}

Equation (18) presents a simpler and more intuitive expression for ϕ_{eo} obtained from the variation of ϕ_{eo} with the electrolyte pH ($d\phi_{eo}/dpH = -2.3\phi_t\alpha$) [16], [1]:

$$\phi_{eo} = 2.3\phi_t\alpha(pH_{pzc} - pH) \tag{18}$$

where pH_{pzc} is the pH at which the oxide surface is electrically neutral (point of zero charge) and depends on the material used as sensing membrane (see Table 2 on p. 56 for Si_3N_4). The term α is a dimensionless sensitivity parameter that varies between 0 and 1, given by [16]:

$$\alpha = \frac{1}{(2.3\phi_t C'_{eq} / q\beta_{\text{int}}) + 1} \tag{19}$$

where β_{int} denotes the intrinsic buffer capacity of the surface. It quantifies the ability of the oxide surface to deliver or take up protons [1] and is derived from $d\sigma_o/dpH_S = -q\beta_{int}$ [16]. Therefore, by considering σ_o from eq. (13), results in:

$$\beta_{int} = 2.3N_{sil}H_S\left(\frac{K_+H_S{}^2 + 4K_+K_-H_S + K_+^2K_-}{(H_S{}^2 + K_+H_S + K_-K_+)^2}\right) + 2.3N_{nit}H_S\left(\frac{K_n}{(H_S + K_n)^2}\right) \tag{20}$$

The first definition of β_{int} was presented by Van Hal *et al* [16], who considered only the first term of σ_o in eq. (13), which is related to the silanol sites, N_{sil}. Compared with the definition of [16], β_{int} presented in eq. (20) includes the second term, which is a function of the primary ammine sites, N_{nit}. As will be discussed later in the text, using the Si_3N_4 parameters in Table 2, this second term is not as relevant for β_{int} as the first term.

A unit value of α results in a maximum theoretical sensitivity of 59 mV/pH at 27°C. The practical results of the pH sensitivity are usually below 59 mV/pH. For example, different studies have reported sensitivities between 20 and 47 mV/pH for ISFETs implemented in standard CMOS technologies using a Si_3N_4 passivation layer [53], corresponding to α between 0.339 and 0.797.

For more practicality, and given the different pH sensitivities, probably due to variations in material properties, reported for ISFETs implemented in standard CMOS processes instead of using eq. (19), α is typically estimated by considering the reduction in the measured pH sensitivity from the ideal 59 mV/pH [66]. For example, α = 0.715 modeled a

sensitivity of 42.6 mV/pH in [67], and values of α close to 0.9, 0.75 and 0.95 are considered for TiO_2, SiO_2 and Ta_2O_5 layers, respectively [66].

Figure 10a shows the results of a MATLAB® simulation implementing the complete and simplified expression of ϕ_{eo}, given in eqs. (17) and (18), respectively. Equation (17) was simulated with the Si_3N_4 parameters shown in Table 2, resulting in an average sensitivity of 45 mV/pH and a pH_{pzc} of 7.5 (pH at ϕ_{eo} = 0 V). Equation (18) was simulated with the mentioned sensitivity of 45 mV/pH (=$2.3\phi_t\alpha$) and pH_{pzc} of 7.5. It is possible to see that the expressions are in agreement. The ϕ_{eo} curves are also in accordance with the simulation results from [68] and [60].

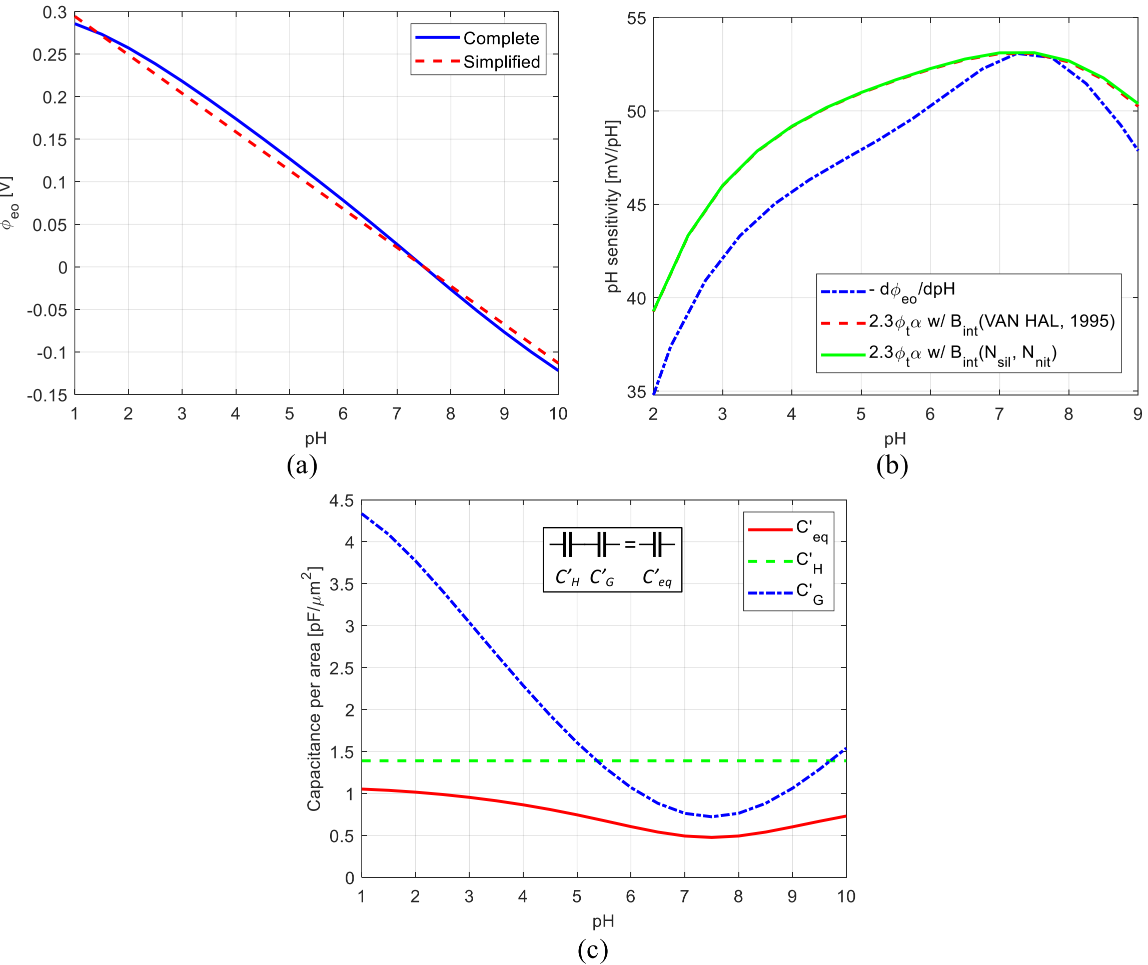


Figure 10 - Simulations of (a) ϕ_{eo} using the complete and the simplified expressions, (b) pH sensitivity simulated with - $d\phi_{eo}/dpH$, and with β_{int} from [16] and from eq. (20), and (c) electrochemical capacitances as a function of pH.

Figure 10b shows a comparison of the pH sensitivity obtained with - $d\phi_{eo}/dpH$ using the ϕ_{eo} curve defined by eq. (17) with the pH sensitivity obtained as $2.3\phi_t\alpha$, where α is given

in eq. (19) using β_{int} presented in [16] and β_{int} from eq. (20). As shown in the figure, the sensitivity with the β_{int} from eq. (20) is approximately the same as that with β_{int} from [16], indicating that the second term in eq. (20) is not so relevant to the pH sensitivity of the Si_3N_4 passivation layer. In addition, as expected, the $2.3\phi_t\alpha$ simulation is in close agreement with -$d\phi_{eo}/dpH$.

Figure 10c shows the values of C'_H, C'_G, and C'_{eq}, with pH simulated using a MATLAB® implementation of eq. (16), and the parameters in Table 2. As expected, C'_H did not change with pH, and C'_{eq} corresponded to the equivalent capacitance of C'_H and C'_G in series. The MATLAB® algorithms are on APPENDIX A – MATLAB algorithm.

3.2.1.3 Estimation of the pH sensitivity at $pH = pH_{pzc}$

Simple equations that do not require sophisticated methods of solution can be an important tool for first-order analysis, especially for hand-designed applications. Considering the equations presented in the previous subsection, it is possible to obtain the pH sensitivity for a specific material in contact with a solution at a pH close to pH_{pzc} without the need to solve an equation system or to find a numerical solution.

Considering $pH = pH_{pzc}$ in eq. (18) results in $\phi_{eo} = 0$ V. In this case, from eqs. (12) and (17), $\sigma_d = -\sigma_o = 0$, resulting in $\phi_2 = 0$ V. This corresponds to $H_s = H_b = 10^{-pHpzc}$ according to eq. (14). Thus, from eq. (20), β_{int} at the point of zero charge is given by:

$$\beta_{int_pzc} = 2.3N_{sil}10^{-pH_{pzc}}\left(\frac{K_+10^{-2pH_{pzc}} + 4K_+K_-10^{-pH_{pzc}} + K_+^2K_-}{(10^{-2pH_{pzc}} + K_+10^{-pH_{pzc}} + K_-K_+)^2}\right) + 2.3N_{nit}10^{-pH_{pzc}}\left(\frac{K_n}{(10^{-pH_{pzc}} + K_n)^2}\right) \quad (21)$$

Considering C'_G for $\phi_2 << 2\phi_t$, as presented in [60], C'_{eq} at the point of zero charge becomes:

$$\frac{1}{C'_{eq_pzc}} = \frac{x_2}{\varepsilon_r\varepsilon_0} + \frac{1}{\sqrt{8\varepsilon_r\varepsilon_0 z^2 n^0 kT}/(2\phi_t)} \quad (22)$$

In summary, considering the characteristics of a material, such as K_+, K_-, K_n, pH_{pzc}, N_{sil} and N_{nit}, it is possible to estimate α at $pH = pH_{pzc}$ by substituting eqs. (21) and (22) into (19). This can be a useful procedure for first-order estimation of the pH sensitivity of a material. Note that practical measurements and the average sensitivity for a large range of pH values can differ from the sensitivity at pH_{pzc}, as shown in Figure 10b.

For example, using the Si_3N_4 parameters from Table 2 and pH_{pzc} = 7.5, results in $\beta_{int_pzc} = 1.55 \times 10^{18}$ *groups/m²*, $C'_{eq_pzc} = 0.47\ pF/\mu m^2$ and $2.3\phi_t\alpha = 53\ mV/pH$, which is very close to the sensitivity and C'_{eq} at pH = 7.5 shown in Figure 10b and Figure 10c, respectively,.

3.2.2 The ISFET threshold voltage formulation

In the following paragraphs, an expression for threshold voltage for an n-channel ISFET (V_{TISF_N}) is derived and then extended to the p-channel ISFET (V_{TISF_P}). The ISFET threshold voltage can be defined as for the MOSFET [57], considering that at the threshold condition, a voltage V_{REF} must be applied to the ISFET reference electrode, such that the surface potential ϕ_S at the semiconductor equals $2\phi_F$. At this surface potential, the semiconductor charge is equal to $-\gamma C_{ox}\sqrt{2\phi_F}$. Thus, assuming a flat-band voltage equal to zero, V_{REF} is given by:

$$\frac{C_{pass}C_{ox}}{C_{pass}+C_{ox}}\left(V_{REF}-2\phi_F\right)=\gamma C_{ox}\sqrt{2\phi_F} \qquad (23)$$

Considering the flat-band voltage $V_{FB,ISF}$, the ISFET threshold voltage is given by:

$$V_{TISF_N}=V_{FB,ISF}+2\phi_F+\frac{\gamma C_{ox}\sqrt{2\phi_F}}{C_{eff}} \qquad (24)$$

Substituting $V_{FB,ISF}$:

$$V_{TISF_N}=(E_{ref}+\phi_{lj})-(\phi_{eo}-\chi_{sol})-\phi_{sc}-(\phi_{met}-\phi_{poly})-\frac{Q_o}{C_{eff}}-\frac{Q_{pass}}{C_{pass}}+2\phi_F+\frac{\gamma C_{ox}\sqrt{2\phi_F}}{C_{eff}} \qquad (25)$$

This expression can be written as a function of the MOSFET threshold voltage (V_{Tmos}) as follows:

$$V_{TISF_N} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{sc} - (\phi_{met} - \phi_{poly}) - \frac{Q_{pass}}{C_{pass}} + 2\phi_F$$
$$+ \frac{C_{pass} + C_{ox}}{C_{pass}} \left(\underbrace{\gamma\sqrt{2\phi_F} - \frac{Q_o}{C_{ox}} + (2\phi_F + \phi_{poly} - \phi_{sc})}_{V_{Tmos}} - (2\phi_F + \phi_{poly} - \phi_{sc}) \right) \quad (26)$$

Resulting in:

$$V_{TISF_N} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{met} + \frac{C_{pass} + C_{ox}}{C_{pass}} V_{Tmos_N} - \frac{C_{ox}}{C_{pass}} (2\phi_F + \phi_{poly} - \phi_{sc}) - \frac{Q_{pass}}{C_{pass}} \quad (27)$$

By grouping terms and extending it to the p-channel device, the last expression can be written as:

$$V_{TISF_{N(P)}} = \left(\frac{C_{pass} + C_{ox}}{C_{pass}} \right) V_{Tmos_{N(P)}} + V_{chem} + V_{tc} - \kappa_{T_{N(P)}} \quad (28)$$

This expression models the effects of the capacitive divider from oxide and passivation capacitances on the MOSFET threshold voltage (first term), the contributions of chemical potentials due to the solution (second term: V_{chem}), the trapped charge offset (third term: V_{tc}), and a technologically dependent constant (fourth term: $-\kappa_{T_{N(P)}}$). The parameters are defined as follows:

$$V_{chem} = (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) = \gamma_{chem} - \phi_{eo} \quad (29)$$

$$V_{tc} = -\frac{Q_{pass}}{C_{pass}} \quad (30)$$

$$\kappa_{T_N} = \phi_{met} + \frac{C_{ox}}{C_{pass}} (\phi_{n^+ poly} - \phi_{sc_N} + 2|\phi_F|) \quad (31)$$

$$\kappa_{T_P} = \phi_{met} + \frac{C_{ox}}{C_{pass}} (\phi_{p^+ poly} - \phi_{sc_P} - 2|\phi_F|) \quad (32)$$

Table 3 (p. 57) presents the expressions for the ISFET threshold voltage from papers considering the classical structure (with post-processing) and the new structure (using standard CMOS technology). As can be concluded from eq. (5), an increase in the threshold voltage corresponds to a decrease in the MOSFET gate voltage (V_G). Therefore, some studies have reduced the electrochemical contribution V_{chem} from the MOSFET gate voltage instead of adding it to the MOSFET threshold voltage (as in [22]).

There are some differences between the expressions derived in this study and the expressions commonly used for ISFETs in standard CMOS (Table 3, p. 57). For example, there is a technological term κ_T, which is a function of the oxide and passivation capacitance, the work function of the top metal plate, polysilicon, and silicon, and the Fermi level potential. By comparing the obtained V_{chem} with the expression commonly used in ISFET modeling [45], the absence of ϕ_m can be observed, which in our expression is associated with the technological term κ_T .

Disregarding the effects of the passivation layer ($Q_{pass} = 0\ C$, $C_{pass} >> C_{ox}$) and of the potential contact between the top metal and polysilicon (ϕ_{met} - ϕ_{poly} = 0), expression (27) becomes:

$$V_{Tisf_{N(P)}} = V_{Tmos_{N(P)}} + (E_{ref} + \phi_{lj}) - (\phi_{eo} - \chi_{sol}) - \phi_{met} \quad (33)$$

This is in accordance with the expression for the threshold voltage for the classical ISFET structure presented in [59] and [61].

3.3 SLOPE FACTOR

The MOSFET slope factor is given by [52]:

$$n_{mos} = 1 + \frac{C_b}{C_{ox}} \quad (34)$$

Figure 11 shows the MOSFET and ISFET capacitive models. In the ISFET structure, the passivation capacitance (C_{pass}) is connected to the gate of the MOSFET resulting in a series connection between C_{ox} and C_{pass} and the Gouy-Chapman capacitance C_{eq} [69].

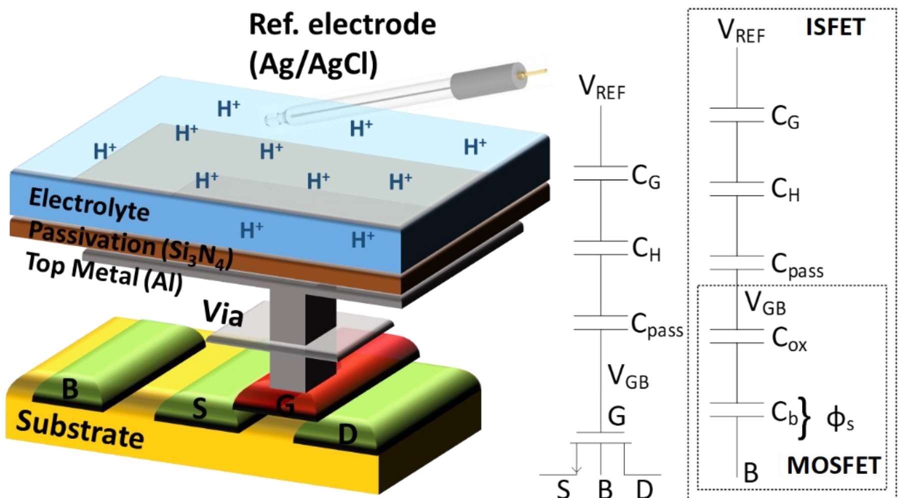


Figure 11 - Cross-section illustration, schematic showing the MOSFET and the capacitive model of an ISFET with electrolytes.

Common values for commercial CMOS-technology parameters, such as a SiO_2 gate oxide and Si_3N_4 passivation with relative dielectric constants of 3.9 and 7.5, respectively, a gate oxide thickness of 8 nm, and a passivation thickness of 1.1 µm result in C'_{ox} and C'_{pass} of 0.04 pF/µm² and 0.06 fF/µm², respectively, which are much lower than the simulated C'_{eq} in Figure 10c (close to 1 pF/µm²). Therefore, the Gouy-Chapman capacitances from the electrochemical interface can be neglected in the series connection, resulting in the following ISFET slope factor [69]:

$$n_{ISF} = 1 + \frac{C_b}{C_{eff}} \tag{35}$$

where C_{eff} is the equivalent series capacitance of C_{ox} and C_{pass}:

$$\frac{1}{C_{eff}} = \frac{1}{C_{ox}} + \frac{1}{C_{pass}} \tag{36}$$

The capacitances C_b, C_{pass}, C_{ox} are given, respectively, by:

$$C_b = (n_{mos} - 1)C_{ox} \tag{37}$$

$$C_{pass(ox)} = \frac{\varepsilon_{r_{pass(ox)}} \varepsilon_0 A_{pass(ox)}}{t_{pass(ox)}} \tag{38}$$

where $\varepsilon_{rpass(ox)}$ is the relative dielectric constant of the passivation (gate oxide) material, ε_0 is the vacuum dielectric constant (8.854×10^{-12} F/m), $A_{pass(ox)}$ is the top metal (gate oxide) area, and $t_{pass(ox)}$ is the thickness of the passivation (gate oxide).

It can be proved that the slope factor of MOSFETs and ISFETs is associated with capacitive attenuation according to:

$$n_{ISF} = \frac{n_{mos}}{\alpha_{att}} \tag{39}$$

From this equation, it is expected an increase in the slope factor of the ISFET compared to that of the MOSFET, due to the passivation capacitance.

3.4 SPECIFIC CURRENT

Equation (3) defines the MOSFET specific current (I_S), where $C'_{ox} = C_{ox}/(WL)$. Considering the ISFET structure and replacing n_{mos} for $n_{ISF} = n_{mos}/a_{tt}$, and C_{ox} for the equivalent series association between C_{ox} and C_{pass} from eq (3), results in the following ISFET specific current (I_{SISF}):

$$I_{SISF} = \mu \frac{C_{ox} C_{pass} / \left(C_{ox} + C_{pass}\right)}{(WL)} n_{ISF} \frac{\phi_t^2}{2} \frac{W}{L} \tag{40}$$

Writing this expression as a function of the MOSFET specific current (I_S):

$$I_{SISF} = I_S \frac{C_{pass} + \left(C_{ox} C_b\right) / \left(C_{ox} + C_b\right)}{C_{pass} + C_{ox}} \tag{41}$$

According to this expression, for $C_{pass} >> C_{ox}$ and/or $C_b >> C_{ox}$, the ISFET specific current is close to that of the MOSFET ($I_{SISF} \approx I_S$).

3.5 ISFET MODEL IN VIRTUOSO

Most circuits sent for fabrication are designed using specific EDA tools that support files from the process design kit (PDK) provided by the foundry. Aiming at projects using ISFETs, a model was developed for DC simulations using the Virtuoso®, a commercial software commonly used for integrated circuit projects.

The device symbol is shown in Figure 12. It consists of a non-modified MOSFET instance from the PDK, implemented in BSIM (Berkeley Short-Channel Insulated gate field-effect transistor Model), and a block connected to the gate terminal of the MOSFET.

This block, described in the Verilog-A language, models the potentials related to the electrode, passivation, and electrolyte, as well as the capacitive attenuation, implementing the ISFET threshold voltage expression proposed in this thesis. The user can define parameter values or use pre-defined values. More details, user-defined parameters and testbenches of the modelled device are on APPENDIX B - ISFET DC model implemented on Virtuoso.

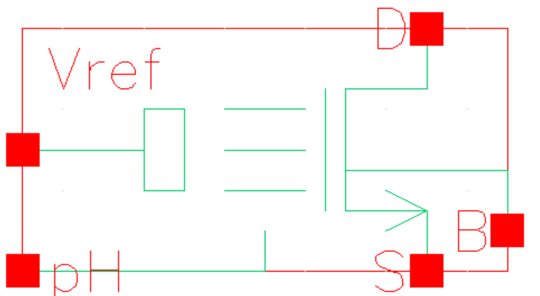


Figure 12 - n-ISFET symbol implemented on Cadence.

As an alternative to this model, it is possible to implement the ISFET parameters V_{TISF}, n_{ISF} and I_{SISF} derived in this thesis, directly into the compact transistor model based on the ACM, which is implemented in Verilog-A and presented in [70].

Table 2 - Electrochemical and MOS parameter values.

Material	Parameter	Value	Ref.
Electrolyte	ϕ_{lj}	1 mV	[60]
	X_{sol}	3 mV	[60]
MOS structure	χ	4.05 V (Si)	[58]
	E_g	1.12 eV	[58]
	n_i	10^{10} cm^{-3} at 25°C	[58]
	$\|\phi_F\|$	0.4 V *	
	ϕ_{Au}	5.1 V	[71]
	ϕ_{met}	4.28 V (Al)	[71]
	ϕ_{n+poly}	4.15 V **	[72], [73]
	ϕ_{p+poly}	5.27 V **	[72], [73]
Ref. electrode (Ag/AgCl)	$E_{abs}(H^+\|H_2)$	4.44 ± 0.02 V at 25°C	[39]
	$E_{rel}(Ag\|AgCl)$	0.19 V	[35]
Passivation Layer (Si_3N_4)	K_+	15.8 mol/L	[61]
	K_-	63.1×10^{-9} mol/L	[61]
	K_n	10^{-10} mol/L	[61]
	N_{sil}	3×10^{18} m^{-2}	[61]
	N_{nit}	2×10^{18} m^{-2}	[61]
	pH_{pzc}	≈ 7	[61]
GCS Model	ε_r	78.49 ***	[38]
	x_2	0.5 nm	[38]

* for a substrate doping of $Na = 9\times10^{16}$ cm^{-3}

** for heavily doped poly-Si gates.

*** for dilute aqueous solutions at 27°C.

Table 3 - ISFET threshold voltage expressions presented in different papers.

	Reference	V_{TISF} expression
Classical Structure	[1], [74]	$V_\mathrm{t} = E_\mathrm{ref} - \Psi + \chi^\mathrm{sol} - \frac{\Phi_\mathrm{Si}}{q} - \frac{Q_\mathrm{ox}+Q_\mathrm{ss}+Q_\mathrm{B}}{C_\mathrm{ox}} + 2\phi_\mathrm{f}$
	[67], [54], [59], [61], [65]	$V_\mathrm{th(ISFET)} = (E_\mathrm{ref}+\phi_\mathrm{lj}) - (\varphi_{eo}-\chi_{eo}) - \left[\frac{Q_\mathrm{tot}}{C_{ox}} - 2\phi_f + \frac{\phi_s}{q}\right] = V_\mathrm{th(MOS)} + V_\mathrm{chem}$ $V_\mathrm{chem} = (E_\mathrm{ref}+\phi_\mathrm{lj}) - (\varphi_{eo}-\chi_{eo}) - \frac{\phi_m}{q}$
Standard CMOS Technology	[10], [75], [32], [76], [77], [78], [79]	$\mathrm{V_{th(ISFET)}} = \mathrm{V_{th(MOSFET)}} + \gamma + \alpha \mathrm{S_N}\ \mathrm{pH}$ $V_{G'} = V_{ref} - V_{Chem} = V_{ref} - (\gamma + \alpha S_N pH)$ $V_G = V_{G'}\lfloor C_{mem}/(C_{mem}+C_g+C_p)\rfloor$
	[45]	$V_{chem} = \gamma + 2.3\alpha U_T pH$, $\gamma = E_{ref} + \chi_{sol} + \phi_{lj} - \frac{\phi_m}{q}$ $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{chem} - V_{TH})^2(1+\lambda V_{DS})$
	[63]	$V_{th-ISFET} = V_{th-MOSFET} + V_{chem}$, $V_{chem} = \gamma + 2.303\alpha U_T pH$
	[18]	$V_\mathrm{th-ISFET} = \underbrace{\frac{V_\mathrm{th-MOSFET} C_\mathrm{Tfg} C_\mathrm{TCp}}{C_\mathrm{chem} C_\mathrm{pass}}}_{\mathrm{MOSV_{th}\ contribution}} + \underbrace{\frac{(V_s C_\mathrm{Tfg} - \sum C_j V_j)\frac{C_\mathrm{TCp}}{C_\mathrm{pass}} - \sum C_i V_i}{C_\mathrm{chem}}}_{\text{Parasitic contribution}} - \underbrace{\frac{Q_\mathrm{TCfg}\frac{C_\mathrm{TCp}}{C_\mathrm{pass}} + Q_\mathrm{TCp}}{C_\mathrm{chem}}}_{\text{Trapped charge contribution}} + \underbrace{\kappa}_{\text{Chemical contribution}}.$
	[22]	$\mathrm{V_{chem}} = \gamma + 2.3\alpha \mathrm{N_s pH}$ (1) $\mathrm{V_{fg}} = \frac{(V_\mathrm{ref} - V_\mathrm{chem})*\mathrm{C_{pass}} + \mathrm{V_D C_{GD}} + \mathrm{V_S C_{GS}} + \mathrm{V_B C_{GB}} + \mathrm{V_{tun} C_{tun}}}{\mathrm{C_{tot}}}$ $I_{ds} = I_{d0}\frac{W}{L}e^{(V_{fg} - V_t/nU_T)}$
	[15]	$V'_G = V_G - V_{tc} - V_{chem}$, $V_{chem} = \gamma + 2.3aS_N pH$ $I_D = I_0 \exp\frac{V_{FG} - V_s}{nU_t}\left(1 - \exp\frac{-V_{DS}}{U_t}\right)$ $V_{FG} = \frac{V'_G C_{pass} + V_{CG} C_{CG} + V_S C_{GS} + V_D C_{GD}}{C_T}$
	This work	$V_{TISF_{N(P)}} = \left(\frac{C_{pass} + C_{ox}}{C_{pass}}\right) V_{Tmos_{N(P)}} + V_{chem} + V_{tc} - \kappa_{T_{N(P)}}$

4 THE DESIGNED CHIPS

This chapter describes the fabrication flow and presents details about the fabricated chips.

4.1 DESIGN-TO-SILICON FLOW

This thesis focuses on ISFETs implemented in standard CMOS technology. Figure 13 summarizes the main steps in the design and testing of the chips. The chip is designed with an electronic design automation (EDA) tool, such as Virtuoso®, following the design rules defined by the process design kit (PDK) (Figure 13a). A file with the chip layout is sent to the foundry, where various samples are fabricated on a silicon wafer. The fabrication process is performed in a cleanroom facility and involves several steps, such as lithography, oxidation, and ion implantation [80] (Figure 13b). Each sample, called die, is cut from the wafer, packaged, and electrically connected to the external pins of the package using the wire bonding technique (Figure 13c). The previous steps are standard for CMOS chips. For ISFETs, an extra step is needed in which a chamber is installed to allow electrolytes to be applied only above the ISFETs, covering other parts of the chip. Subsequently, the chip can be measured (Figure 13d).

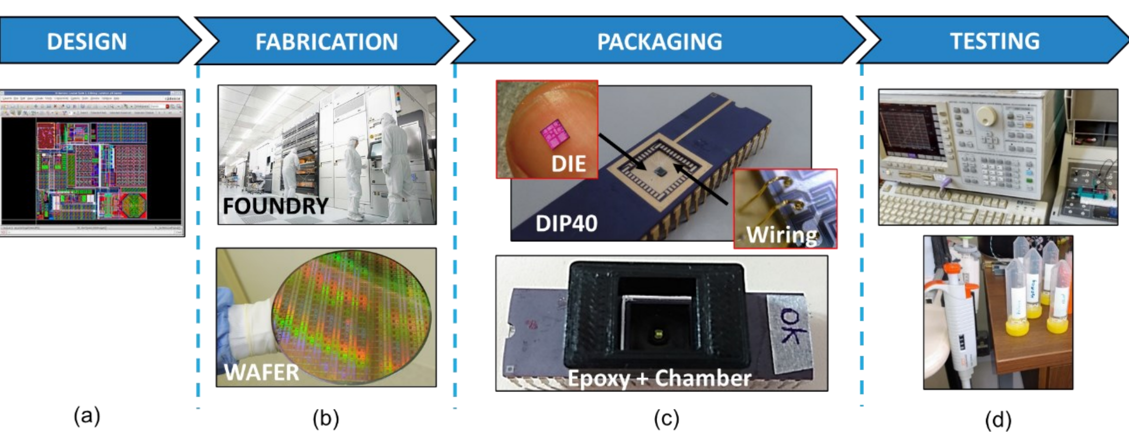


Figure 13 - Design and test flow of ISFET chips designed in this thesis.

Commercial CMOS technology allows for large-scale fabrication at a low price per chip. For the prototype, it is common to use a multi-project wafer (MPW) run, in which the foundry divides the fabrication costs and silicon area between groups, resulting in a lower prototype cost, a reduced number of dies (20–40 samples), and a higher price per chip

compared to a dedicated run. Once the chips are validated, they can be mass produced. In this case, the customer pays for the full wafer(s), which requires a large amount of money but results in thousands of samples, drastically reducing the price per chip (around $1.00 per square inch [81], [82]).

During this research, two chips were sent for fabrication: one chip using SilTerra D18V 0.18 μm technology, and another chip using OnSemi I3T25 0.35 μm technology. Both chips were designed in the software Virtuoso®. The fabrication costs of the chips were supported by Chipus Microeletrônica S.A (Florianópolis/SC, webpage: [11]). The following sections present the project details for both chips.

4.2 CHIP SILTERRA

4.2.1 Chip Design

This chip was produced in the SilTerra D18V 0.18 μm technology (Kulim/Malaysia). The chip consists of an array of 15 p-ISFETs, 15 n-ISFETs, 1 p-MOSFET, and 1 n-MOSFET. The ISFETs and MOSFETs employ thick oxide transistors (12.5 nm thickness, supporting V_{GS} of 5.5 V, mainly used for input/output pins) with a gate width (W) and length (L) of 9 μm and 1.8 μm, respectively, and a top metal area (A_{pass}) of 80 μm × 80 μm, which results in $A_{pass} = 395A_{mos}$ ($A_{mos} = W \times L$). The total area of the die was 2.28 mm × 2.28 mm with a sensing area of 871 μm × 420 μm at the die center. The available n-ISFETs and p-ISFETs of the array are identified as N01–N15 and P01–P15, respectively, in Figure 14c (the remaining devices are dummy elements). The pixel dimensions are shown in Figure 14d.

Figure 15 shows the electrical connections between the devices on the chip. The source terminals of the same type of ISFETs are connected to a pad, the bulk terminals are connected to another pad, and the drain terminals can be individually accessed. The reference MOSFETs have individual access to the gate, drain, and source terminals, whereas the bulk is connected to the ISFETs bulk. More details on the design of this chip can be found in [83]. The chip pin mapping is provided in APPENDIX C - Chip Silterra: pin mapping.

The SilTerra D18V technology has six metal layers and a passivation layer of silicon nitride (Si_3N_4) on top of undoped silicate glass (USG) with typical thicknesses of 500 nm (±11%) and 900 nm (±10%), respectively, and relative dielectric constants of 7.5 and 4.2, respectively. The MOSFET gate oxide capacitance (C_{ox}) is 44 fF, calculated using the relative

dielectric constant of 3.9 for silicon dioxide, a specified oxide thickness of 12.5 nm, and A_{mos}. The passivation capacitances of the Si_3N_4 (C_{SiN}) and USG (C_{USG}) layers for the previously specified A_{pass}, thickness, and dielectric constants are 849 fF and 264 fF, respectively. The total passivation capacitance (C_{pass}) is the series combination of the capacitances of the Si_3N_4 and USG layers: $C_{pass} = C_{SiN}C_{USG}/(C_{SiN} + C_{USG}) = 201 fF$.

4.2.2 Chip Packaging

The die was wire-bonded in a DIP40 (dual in-line package with 40 pins) with an open cavity (uncovered die), as shown in Figure 14a. To protect the pads and bonding wires, epoxy was applied to them only, leaving the top plates of the ISFETs uncovered (Figure 14b). This structure forms a chamber with a diameter of 1 mm and height of 0.5 mm, such that it is possible to apply different solutions or other materials. This chamber was developed by ITT Chip, Instituto Tecnológico de Semicondutores da Unisinos (São Leopoldo/RS), a specialized center for the packaging and testing of semiconductors and electronics (webpage: [12]).

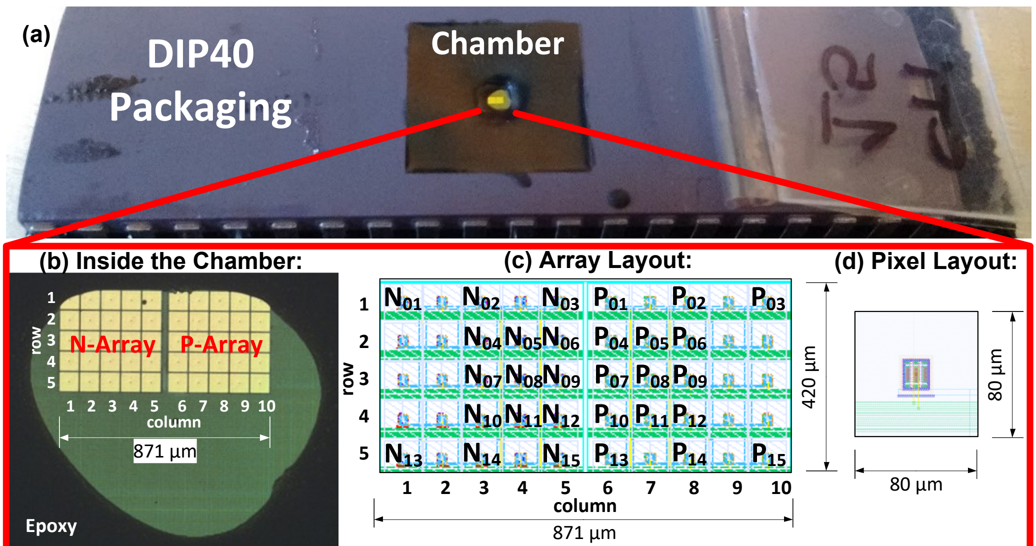
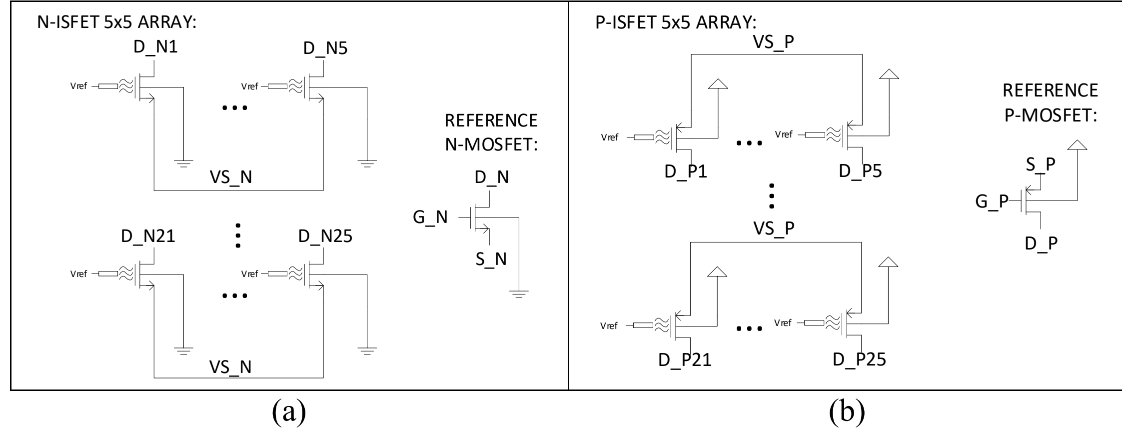


Figure 14 - Chip SilTerra: (a) the chip encapsulated in DIP40, (b) details of the epoxy chamber, (c) array layout with identification of devices, and (d) pixel layout.



(a) (b)

Figure 15 - Electrical connections of the (a) n-channel and (b) p-channel devices [83].

To check the integrity of the electrical connections after epoxy deposition, the devices were visually inspected using X-ray images provided by the ITT Chip (APPENDIX D - Chip Silterra: x-ray verification) and electrically tested by measuring the bulk/source and bulk/drain junctions of the ISFETs. Table 4 summarizes the fabrication steps and schedule performed in this round.

Table 4 - Chip SilTerra: fabrication schedule.

Step	Company name	Location	Period (Y-M)
Chip design	LCI	Florianópolis/SC	2018/03 - 2018/04
Dies fabrication	SilTerra	Kulim/Malaysia	2018/04 - 2018/08
DIP40 packaging	CTI	Campinas/SP	2018/11 - 2018/12
Epoxi chamber	ITT Chip	São Leopoldo/RS	2019/01 - 2019/07
Gold Metallization	LAMATE	Florianópolis/SC	2019/10 – 2019/11
Wet test	Lab de Prototipagem	Curitiba/PR	2020/09 – 2020/09

4.3 CHIP ONSEMI

4.3.1 Chip Design

In the chip described in the previous section, many ISFETs of the same type are placed too close to each other, which makes it difficult to implement a differential chamber setup. Considering this, the chip described in this section was developed to characterize n-ISFETs and p-ISFETs on ONSEMI I3T25 0.35 µm technology, allowing both single and differential measurements. The die has a total area of 2 mm × 2 mm and is composed by 8 n-ISFETs, 8 p-ISFETs, 1 n-MOSFET and 1 p-MOSFET (Figure 16a). The ISFETs and MOSFETs are connected as described for the SilTerra chip (Figure 15). This chip has 40 pads

with an area of 70 µm × 70 µm and a pitch of 150 µm. Because this die was shared with another project, there are other devices and internal pads that are not part of this research and will not be detailed in this document. PADs connectivity is detailed on APPENDIX E - Chip Onsemi: PADs connectivity.

The ISFETs are grouped into two arrays, each containing 4 n-ISFETs and 4 p-ISFETs, totaling a sensitive area of 150 µm × 260 µm per array (Figure 16b). The two arrays are spaced 500 µm apart to better accommodate the two chambers for differential measurements. Each pixel is composed of a MOSFET with gate dimensions of $W/L = 7\ \mu m/3.5\ \mu m$, a top metal area of 120 µm × 30 µm, and a minimum dimension aperture in the center above the MOSFET gate of 3 µm × 3 µm (Figure 16c).

The ONSEMI I3T25 technology has four metal layers and a Si_3N_4 passivation layer with a typical thickness of 1.1 µm (±10%). The n-channel and p-channel MOSFETs implemented in the n-channel and p-channel ISFET pixels have gate oxide thicknesses of 7.75 nm and 8.15 nm respectively, supporting V_{GS} close to 3.3 V. Considering the top metal area, the Si_3N_4 thickness, and a relative dielectric constant of 7.5, results in a passivation capacitance of 217 fF. The gate oxide capacitances for n-MOSFETs and p-MOSFETs are 109 fF and 103 fF, respectively, considering the previously mentioned gate oxide thickness and the silicon dioxide relative dielectric constant of 3.9. Table 5 summarizes the characteristics of the device implemented on this chip.

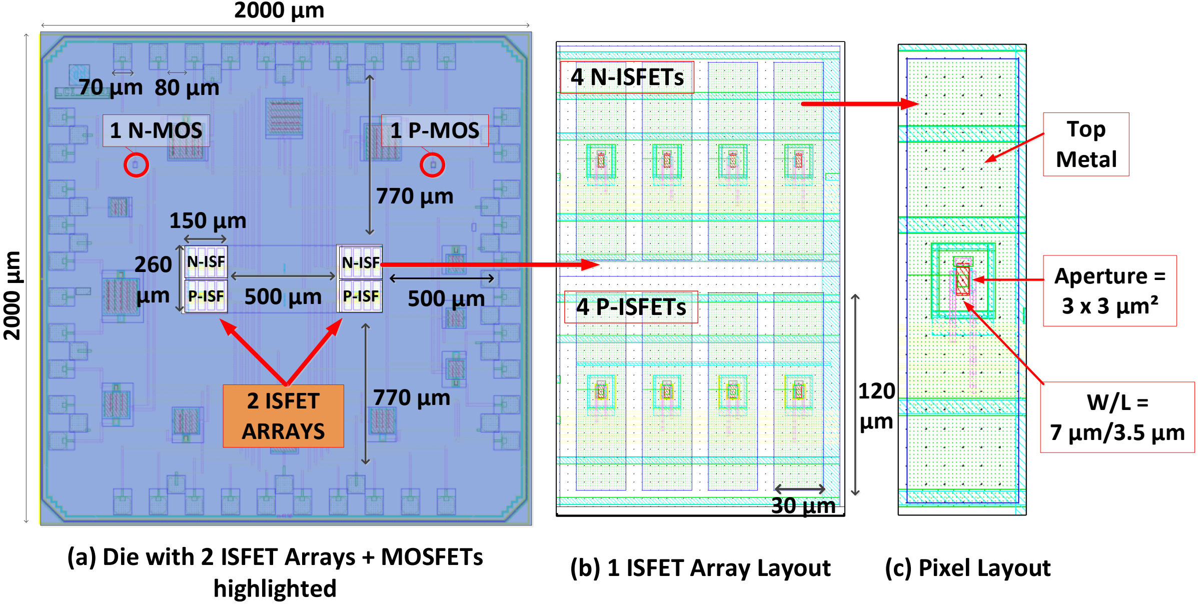


Figure 16 - Chip Onsemi: (a) die with 2 ISFETs arrays and MOSFETs highlighted, (b) array layout formed by 4 n-ISFETs and 4 p-ISFETs, and (c) pixel layout.

Table 5 - Chip Onsemi: simulated electrical characteristics (typical conditions).

Parameter	Value		Unity
	n-type	p-type	
MOSFET gate oxide thickness (t_{ox})	7.75	8.15	nm
MOSFET dimensions (W/L)	7 µm/3.5 µm	7 µm/3.5 µm	-
Maximum V_{GS} voltage (V_{GSmax})	3.3	3.3	V
MOSFET threshold voltage (Vt_{mos})	0.557	-0.552	V
MOSFET specific current (Is)	153	31.6	nA
MOSFET slope factor (n_{mos})	1.35	1.39	-
Passivation thickness	1.1	1.1	µm
ISFET top metal dimensions	120x30*	120x30*	µm²
MOSFET gate oxide capacitance (C_{ox})	109.11	103.76	fF
Passivation capacitance (C_{pass})	217.23	217.23	fF

*A rectangular ISFET was chosen because this technology limits the metal length to 30 µm. Other studies have used rectangular ISFETs: [23], [18].

4.3.2 Chip Packaging

The chip can be packaged with one chamber for single-ended measurements or two chambers for differential measurements. For example, Kalofonou and Toumazou [23] implemented two chambers with dimensions of 1 mm × 0.4 mm × 0.4 mm.

Figure 17a illustrates the proposed die with two chambers whose diameters are 300 µm each, while Figure 17b illustrates the die with one chamber with a diameter of 1 mm (as in the chamber implemented in our tape-out 1 by ITT Chip).

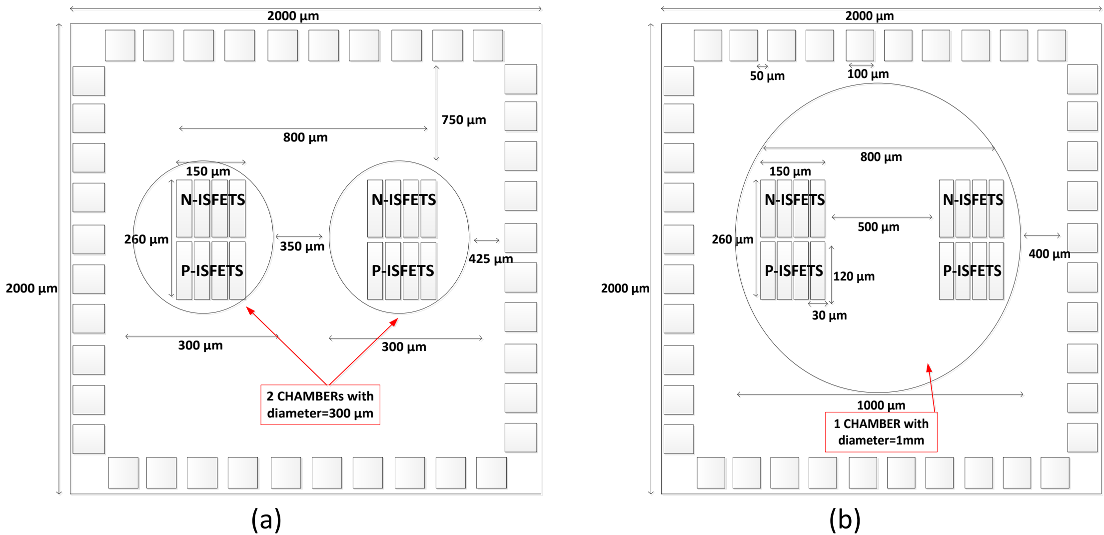


Figure 17 - Chip Onsemi: illustrations of the die with (a) 2 chambers for differential measurements, and (b) 1 chamber for single-ended measurements.

This project was sent for fabrication in April/2021 and suffered several delays during the fabrication process in the foundry, mostly due to the COVID-19 situation. Therefore, this chip could not be measured during this thesis.

5 A DRY TEST FOR ISFETS

As already mentioned, some ISFET nonidealities require better understanding and compensation techniques. To characterize the ISFET parameters without the electrochemical influences of wet measurements, this thesis proposes a dry test in which the solution and reference electrode are replaced with a metal film. This chapter describes the methods adopted to implement the proposed dry test as well as the modeling of the main electrical parameters of the metallized ISFET. The metallization process was implemented in the Chip Silterra 0.18 µm.

5.1 METAL LAYER DEPOSITION

To carry out the dry test proposed in this work, an Au layer was deposited on the chamber to provide electrical contact with the floating gates. Sputtering, a commonly technique used to deposit sensing films in ISFETs [84], was employed to form the thin film with neutral Au particles [85]. The metallization was performed in LAMATE/UFSC. Illustrations of the ISFET cross section with a metallization layer and the encapsulated chip are shown in Figure 18.

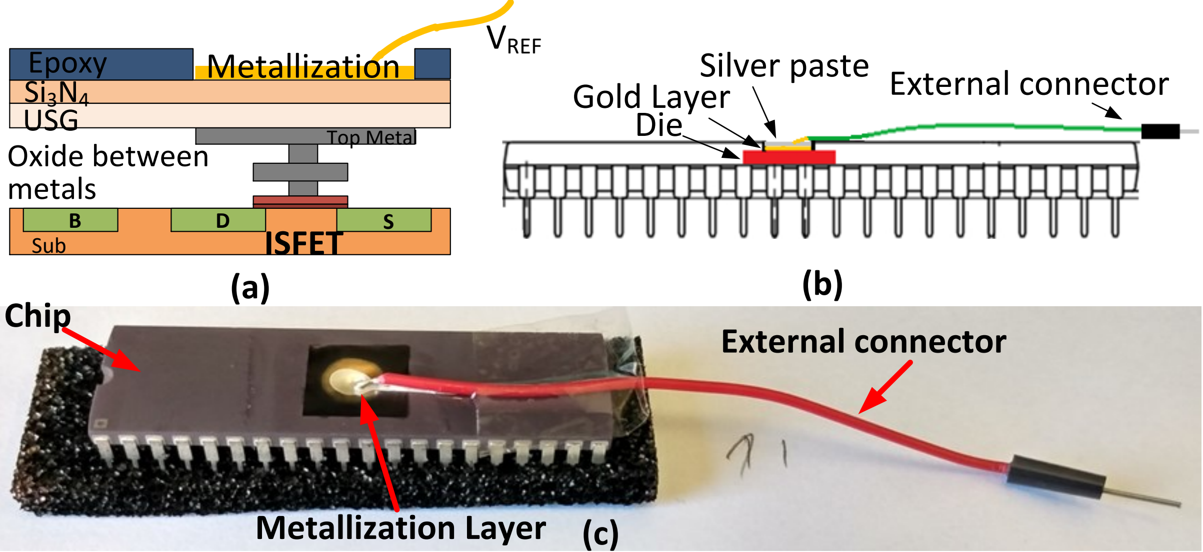
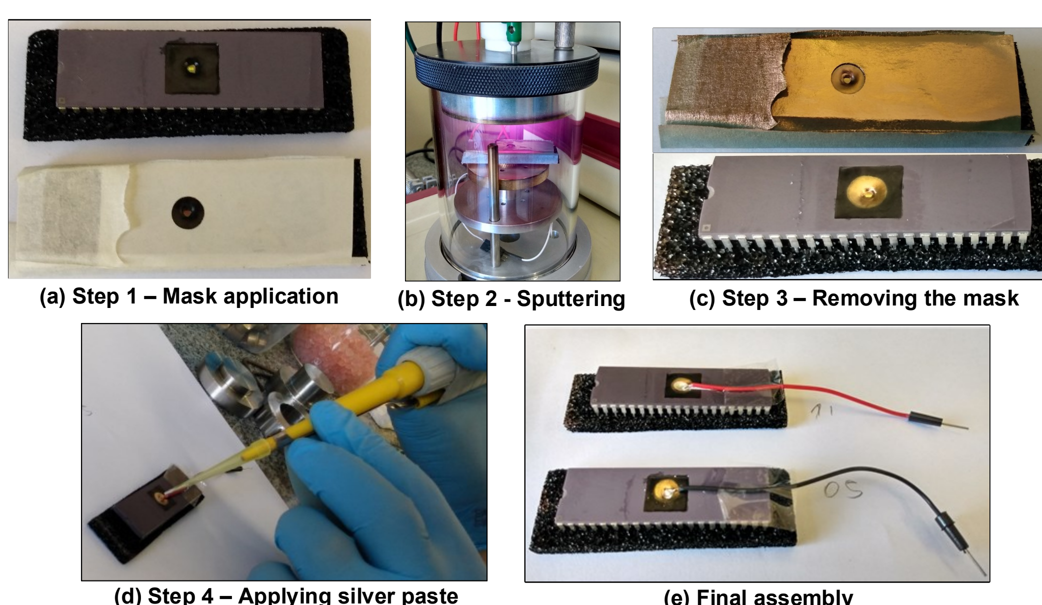


Figure 18 - (a) Cross-section of a metallized ISFET; (b) diagram of the die encapsulated in DIP40 package, and (c) encapsulated chip.

Figure 19 shows the main steps employed for the Au metallization of the chip. The Au DC sputtering was performed using an SPI-Module sputter coater with the parameters

listed in Table 6, giving rise to an estimated Au-layer thickness of 40 nm. More details of the metallization process are provided in APPENDIX F - Gold metallization with sputtering for dry test.



(a) Step 1 – Mask application (b) Step 2 - Sputtering (c) Step 3 – Removing the mask

(d) Step 4 – Applying silver paste (e) Final assembly

Figure 19 - Steps of the Au metallization process.

Table 6 - Deposition parameters for Au.

Parameter	Value
Sputter target	Au
Substrate temperature	25°C
Deposition time	120 s
Target to substrate distance	5 cm
Cathode voltage	-1000 V
Cathode current	20 mA

5.2 MODELLING OF METALLIZED ISFETS

Figure 20 shows an illustration of an ISFET with a metallization layer for its gate along with its capacitive model (ϕ_s is the surface potential). The metallized ISFET characteristics are modified with respect to those of the MOSFET due to the following factors. Firstly, the ISFET *dry-gate* is made of a gold layer, whereas polysilicon is used for the MOSFET gate. The different materials for the gates translate into different gate work functions (defined as the energy required to remove an electron from the Fermi level of the material to vacuum [86]), and consequently different flat-band voltages. Secondly, the ISFETs have a capacitive coupling between the external contact (V_{REF}) and the floating gate

terminal (V_{GB}); therefore, the voltage V_{GB} is attenuated with respect to V_{REF}. Thirdly, the connection of the polysilicon floating gate to the Al top metal generates a contact potential.

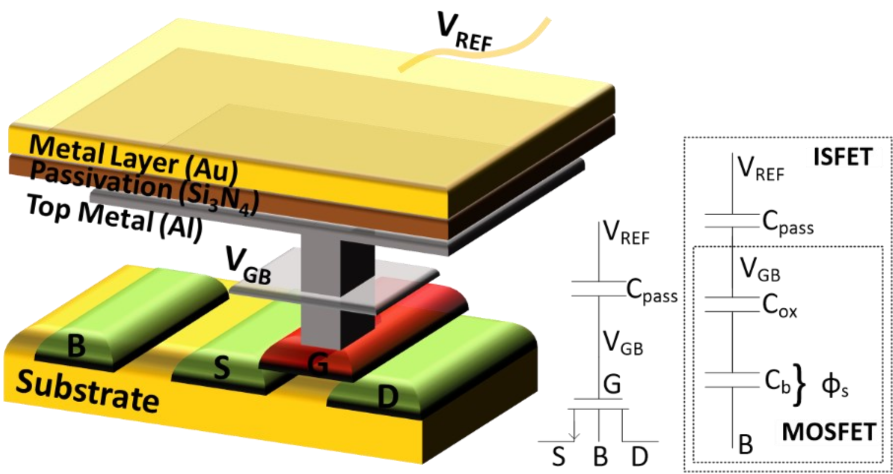


Figure 20 - Cross-section illustration, schematic showing MOSFET and the capacitive model of an ISFET with a metallization layer.

In the next sections, the three main design parameters of the ACM model (threshold voltage, slope factor and specific current) will be derived for the metallized ISFET.

5.2.1 Threshold voltage

The MOSFET threshold voltage (V_{Tmos}) is given [52] by:

$$V_{Tmos} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \tag{42}$$

where ϕ_F is the bulk Fermi potential and γ is the body-effect factor, which can be related to the slope factor as follows [52]:

$$\gamma = 2(n_{mos} - 1)\sqrt{2\phi_F} \tag{43}$$

V_{FB} is the flat band voltage given by:

$$V_{FB} = \phi_{MS} - \frac{Q_o}{C_{ox}} \tag{44}$$

Q_o is the equivalent charge at the oxide-semiconductor interface. ϕ_{MS}, designated as the contact potential [87], is the difference between the work functions per electron charge of the polysilicon gate (ϕ_{poly}) and semiconductor (ϕ_{sc}, eq. (9)) materials and is given by [87]:

$$\phi_{MS} = \phi_{poly} - \phi_{sc} = \phi_{poly} - \left[\chi + \frac{E_g}{2q} + \phi_t \ln\left(\frac{N_a}{n_i} \right) \right] \tag{45}$$

Common values for these parameters are listed in Table 2 (p. 56).

The ISFET threshold voltage is defined in a manner similar to that of the MOSFET, *i.e.,* at the threshold condition, the surface potential ϕ_S at the semiconductor equals $2\phi_F$, and the semiconductor charge is equal to $-\gamma C_{ox}\sqrt{2\phi_F}$. As in the MOSFET, a gate voltage equal to the flat-band voltage $V_{FB,ISF}$ is required to compensate for the difference in the work functions of the materials employed in the ISFET and charges Q_o and Q_{pass}, where Q_{pass} is the charge trapped at the interface between the passivation layer and top metal of the technology:

$$V_{FB,ISFmet} = \phi_{Au} - \phi_{sc} + \phi_{poly} - \phi_{met} - \frac{Q_o}{C_{eff}} - \frac{Q_{pass}}{C_{pass}} \tag{46}$$

where ϕ_{Au} and ϕ_{met} are, respectively, the work functions of gold (applied at the top of the passivation layer) and aluminum (the metal at the bottom of the passivation layer). The term Q_{pass}/C_{pass} represents the offset in the flat-band voltage due to the charges trapped at the passivation.

Assuming that the flat-band voltage is equal to zero, a voltage V_{REF} must be applied to the ISFET Au gate, such that the surface potential ϕ_S equals $2\phi_F$. At such a surface potential, the semiconductor charge is equal to $-\gamma C_{ox}\sqrt{2\phi_F}$; therefore, the value of V_{REF} is given by:

$$\frac{C_{pass}C_{ox}}{C_{pass} + C_{ox}}\left(V_{REF} - 2\phi_F\right) = \gamma C_{ox}\sqrt{2\phi_F} \tag{47}$$

Finally, superimposing the results from eqs. (46) and (47), we find that the threshold voltage of the *metal-gate* ISFET is:

$$V_{TISF_met} - 2\phi_F = \phi_{Au} - \phi_{met} + \phi_{poly} - \phi_{sc} + \frac{1}{C_{eff}}\left(-Q_o + \gamma C_{ox}\sqrt{2\phi_F}\right) - \frac{Q_{pass}}{C_{pass}} \quad (48)$$

Compared with the MOSFET threshold voltage, in the dry-gate ISFET, another contact potential between Au and Al (top metal) is included. The effects of both the oxide charge and the semiconductor charge are, in the ISFET case, coupled to the Au gate by means of C_{eff}, rather than C_{ox} as in the MOSFET. Equation (48) can be rewritten in terms of the MOSFET threshold voltage as:

$$V_{TISF_met} = \phi_{Au} - \phi_{met} + \frac{C_{pass} + C_{ox}}{C_{pass}} V_{Tmos} - \frac{C_{ox}}{C_{pass}}\left(2\phi_F + \phi_{poly} - \phi_{sc}\right) - \frac{Q_{pass}}{C_{pass}} \quad (49)$$

Equation (49) can be expressed as:

$$V_{TISF_met} = \phi_{Au} - \phi_{met} - \frac{Q_{pass}}{C_{pass}} + V_{Tmos} + \frac{\gamma C_{ox}\sqrt{2\phi_F} - Q_o}{C_{pass}} \quad (50)$$

The values for the work functions per electron charge for Au (ϕ_{Au}), aluminum (ϕ_{met}), and heavily doped n^+poly (ϕ_{n+poly}, for n-MOSFETs) and p^+poly (ϕ_{p+poly}, for p-MOSFETs) are listed on Table 2. Note that 1 V is equivalent to an energy of 1 eV (= 1.6×10^{-19} J) per elementary charge q [88].

A similarity between the proposed threshold voltage expression for *wet-gate* ISFETs in eq. (27) and the expression proposed for the *metal-gate* ISFET in eq. (49) may be noted. In the wet test expression, the potentials due to electrochemical elements replace the potential due to the metal employed as the gate contact in our dry experiment.

5.2.2 Slope factor

In the metallized ISFET, the passivation capacitance (C_{pass}) is connected to the gate of the MOSFET [69], resulting in C_{ox} and C_{pass} being connected in series (Figure 20). Substituting C_{ox} for the equivalent capacitance of the series association between C_{ox} and C_{pass} in the MOSFET slope factor expression given in eq. (34) results in the following metallized ISFET slope factor [69]:

$$n_{ISF_met} = 1 + \frac{C_b}{C_{eff}} \tag{51}$$

With C_{eff}, being the equivalent series capacitance of C_{ox} and C_{pass}:

$$\frac{1}{C_{eff}} = \frac{1}{C_{ox}} + \frac{1}{C_{pass}} \tag{52}$$

Therefore, the slope factor for a metallized ISFET is the same as the slope factor for wet tests, presented in eq. (35).

5.2.3 Specific current

Because the metallized ISFET and the wet-gate ISFET have the same slope factor and the same equivalent series association between C_{ox} and C_{pass}, the specific current of the metallized ISFET (I_{SISF_met}) is analogous to that presented in eq. (41):

$$I_{SISF_met} = I_S \frac{C_{pass} + \left(C_{ox}C_b\right)/\left(C_{ox} + C_b\right)}{C_{pass} + C_{ox}} \tag{53}$$

6 A DIFFERENTIAL/SINGLE-ENDED READOUT CIRCUIT

This chapter describes a proposal for a readout integrated circuit for ISFETs that allows both differential and single-end measurements using the same circuit and chip. The circuit compensates for the following ISFET nonidealities: common-mode variations, such as temporal drift, are compensated in a differential configuration using one ISFET in a buffer chamber (with constant pH) and the other ISFET in the reaction chamber (where the electrolyte to be analyzed is applied); intra-die variations in ISFETs threshold voltages are allowed by using the ISFET in the reaction chamber in a source-follower configuration operating in weak inversion, giving room to variations in threshold voltage between sensors in the same chip on the order of hundreds of mV; inter-die (die-to-die) threshold voltage variations are compensated by a feedback loop using an operational amplifier and the ISFET in the buffer chamber to generate an appropriate electrode voltage for both ISFETs; quasi-reference electrodes, such as a wire, can be used in the differential configuration, allowing a more compact application compared to the standard reference electrodes. In summary, using a supply voltage of 3.3 V, the proposed circuit can compensate for trapped charge offsets between chips with variations higher than 2 V and allow variations in the threshold voltage of ISFETs inside the chip on the order of hundreds of mV, while suppressing common-mode voltage variations in the differential configuration (such as temporal drift) and allowing the use of a quasi-reference electrode for compact applications. The simulations of the circuits were performed using the Virtuoso® software, implementing the PDK from ONSEMI 0.35 µm technology, an operational amplifier described in Verilog-A and the ISFET model developed in this work and detailed in APPENDIX B - ISFET DC model implemented on Virtuoso.

6.1 DIFFERENTIAL CIRCUIT

Figure 21 shows the proposed differential circuit.

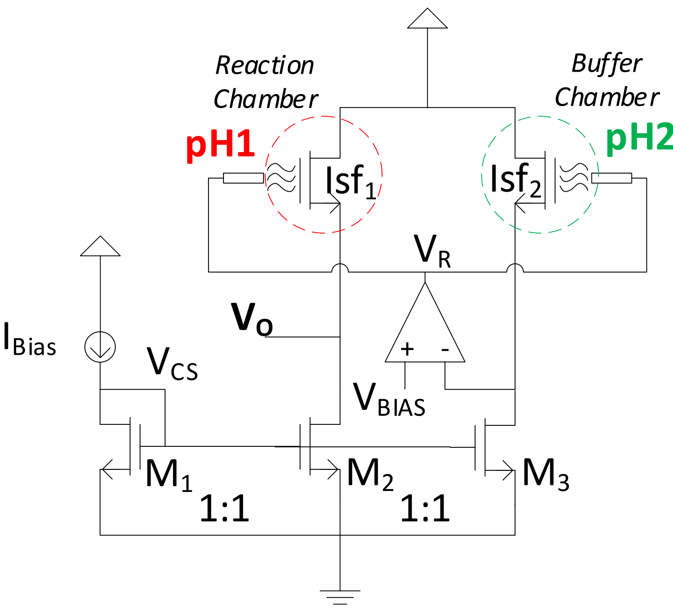


Figure 21 - Differential circuit (bulk terminals are connected to ground).

The differential configuration implements two ISFETs in different chambers: a buffer chamber (with a constant-pH solution) and a reaction chamber (where the solution to be analyzed is applied).

A quasi-reference electrode (qRE), such as an Au wire, biases both ISFETs of the pair. Each ISFET is in the source-follower configuration.

An operational amplifier (OPAMP) is used to compensate for inter-die threshold voltage variations and common-mode voltages, as described below. The OPAMP noninverting input is connected to a voltage V_{BIAS}. The inverting input is connected to the source of the ISFET with a constant pH (control-ISFET). The OPAMP output V_R is connected to the qRE, which polarizes both chambers. The loop is closed in the ISFET of the buffer chamber, and because of the virtual short circuit, the voltage in the non-inverting terminal will replicate to the inverting terminal of the OPAMP (the source terminal of the control-ISFET). Because the control-ISFET has a drain current determined by the current source (M3), the OPAMP compensates for any variations in the threshold voltage of the control-ISFET by applying a suitable reference electrode voltage.

Considering that common-mode variations (such as temporal drift) affect both ISFETs in a similar manner, any compensation in the gate of the control ISFET is reflected in the ISFET of the reaction chamber. Ideally, the output voltage (the source voltage of the ISFET in the reaction chamber) will only reflect variations in pH.

Chips with different trapped charge offsets (inter-die variations in threshold voltages) are compensated by the qRE potential provided by the OPAMP, respecting the output saturation levels of the OPAMP. The circuit can reflect the pH variation, neglecting common-mode voltages, even for hundreds of millivolts of mismatch in the threshold voltages of ISFETs in the same chip (respecting the saturation region of operation of the transistors).

6.1.1 DC analysis

In the proposed circuit, all bulk terminals are connected to the ground. Writing the UICM for ISFET1 present in the reaction chamber:

$$\frac{V_{REF}-V_{TISF1}}{n_{ISF1}}-V_{\mathrm{SB1}}=\phi_t\left[\sqrt{1+i_{f1}}-2+\ln\left(\sqrt{1+i_{f1}}-1\right)\right]=\phi_t f(i_{f1}) \quad (54)$$

The output voltage is the source voltage of ISFET1 ($V_O = V_{SB1}$), so this equation can be rewritten as:

$$V_{\mathrm{O}}=\frac{V_{REF}-V_{TISF1}}{n_{ISF1}}-\phi_t f(i_{f1}) \quad (55)$$

The UICM for the ISFET2 present in the buffer chamber can be written as:

$$\frac{V_{REF}-V_{TISF2}}{n_{ISF2}}-V_{SB2}=\phi_t\left[\sqrt{1+i_{f2}}-2+\ln\left(\sqrt{1+i_{f2}}-1\right)\right]=\phi_t f(i_{f2}) \quad (56)$$

From this equation, and considering $V_{SB2} = V_{BIAS}$ owing to the OPAMP virtual short circuit between its inputs, V_{REF} can be written as:

$$V_{REF} = n_{ISF2}\left(\phi_t f(i_{f2}) + V_{BIAS}\right) + V_{TISF2} \quad (57)$$

Substituting eq. (57) in eq. (55):

$$V_O = \frac{n_{ISF2}\left(\phi_t f(i_{f2}) + V_{BIAS}\right) + V_{TISF2} - V_{TISF1}}{n_{ISF1}} - \phi_t f(i_{f1}) \quad (58)$$

Considering that both ISFETs have similar slope factors ($n_{ISF1} = n_{ISF2} = n_{ISF}$) and inversion levels ($i_{f1} = i_{f2} = I_D/I_{SISF}$), results in:

$$V_O = V_{BIAS} + \frac{V_{TISF2} - V_{TISF1}}{n_{ISF}} \quad (59)$$

From this equation, we observe that the output voltage is a function of the voltage V_{BIAS} and the difference between the threshold voltages of the ISFETs in the buffer and reaction chambers. In this case, any common-mode variations in the threshold voltages of both ISFETs are canceled out, resulting in a differential output.

Because the pH in the buffer chamber is constant, $dV_{TISF2}/dpH = 0$. Therefore, the output pH sensitivity is given by:

$$\frac{dV_O}{dpH} = \frac{1}{n_{ISF1}}\frac{d\phi_{eo1}}{dpH} \quad (60)$$

According to this equation, the output pH sensitivity is attenuated by the ISFET slope factor.

Because the MOSFETs must operate in the saturation region and considering the ISFETs to be in the source-follower configuration, from eq. (57), V_{BIAS} must be in the following range:

$$V_{DSsat(M3)} < V_{BIAS} < \frac{V_{REF\max} - V_{TISF2}}{n_{ISF}} - \phi_t f(i_{f2}) \quad (61)$$

where V_{DSsat} is the saturation voltage between drain and source terminals given by:

$$V_{\text{DSsat}} \approx \phi_t \left[\sqrt{1+i_f} + 3 \right] \tag{62}$$

Devices in weak inversion reduce the minimum V_{DSat}, with a limit being $4\phi_t \approx 100$ mV, for $i_f << 1$. For matched ISFETs, the V_{BIAS} voltage appears in the source voltage of ISFET1 (V_O) at $pH = pH_{pzc}$. Therefore, considering the maximum ISFET pH sensitivity and half excursion in the pH range of 1 to 10 (56 mV/pH × 5pH) it is good to add (subtract) at least 250 mV to the minimum (maximum) V_{BIAS} owing to output voltage variations with pH.

The qRE voltage must be within the saturation levels of the OPAMP output voltage, which is typically hundreds of millivolts above 0 V and hundreds of millivolts below V_{DD}, corresponding to V_{REFmin} and V_{REFmax} respectively. Note that for the ISFET to be saturated, V_{BIAS} must also be lower than $V_{DD} - V_{DSsat(ISF)}$, resulting in $V_{BIAS} < V_{DD} - 0.1\ V$ in weak inversion. Therefore, this analysis considers only the OPAMP saturation limitation given in eq. (61), as it is dominant in this case.

Because the output voltage V_O is read at the source of ISFET1, this voltage must respect limits similar to those on V_{BIAS}:

$$V_{DSsat(M3)} < V_{\text{O}} < \frac{V_{REF\max} - V_{TISF1}}{n_{ISF1}} - \phi_t f(i_{f1}) \tag{63}$$

Using eq. (59) to write V_O as a function of the ISFET threshold voltage difference $\Delta V_{TISF} = V_{TISF2} - V_{TISF1}$, we obtain:

$$n_{ISF}(V_{DSsat(M3)} - V_{BIAS}) < \Delta V_{TISF} < V_{REF\max} - V_{TISF1} - \frac{\phi_t f(i_{f1}) + V_{BIAS}}{n_{ISF}} \tag{64}$$

This equation corresponds to the maximum variations in the threshold voltages of ISFETs on the same chip (intra-die) that this circuit supports.

Now, considering that both ISFETs have the same threshold voltage V_{TISF} and using eq. (57), the maximum variation of the threshold voltage between chips (inter-die) is defined by the OPAMP saturation levels V_{REFmin} and V_{REFmax}, according to:

$$V_{REF\min} - n_{ISF2}\left(\phi_t f(i_{f2}) + V_{BIAS}\right) < V_{TISF} < V_{REF\max} - n_{ISF2}\left(\phi_t f(i_{f2}) + V_{BIAS}\right) \quad (65)$$

Because the OPAMP saturation levels limit the circuit compensation of trapped charge offsets, higher compensation can be obtained using a high-voltage (HV) symmetrical OPAMP. This can be difficult to integrate into new technological nodes owing to the low supply voltage but can be implemented in discrete versions (off-chip implementations) or HV technologies. In summary, this circuit can benefit from HV implementation, which is typically encountered in older and cheaper technological nodes.

6.1.2 Simulations

The circuit simulations were performed with the ISFETs parameters described in APPENDIX B - ISFET DC model implemented on Virtuoso, and with an ideal OPAMP generated with the *modelwriter* tool from Cadence and described in Verilog-A language with the following specs: *Gain* = 120 dB, *pole_freq* = 1.2 Hz, *rin* = 12 MΩ, *rout* = 75 Ω, *slew rate* = ±20 MV/s, V_{Osat} = 0.5 V and 2.7 V. The circuit was designed employing all n-MOSFETs with W = 7 µm and L = 3.5 µm, inversion level i_f = 0.5, V_{DD} = 3.3 V, I_{BIAS} = 75 nA and V_{BIAS} = 0.6 V.

6.1.2.1 pH variations in the reaction chamber

In this simulation, the buffer chamber was kept with pH = 7, while in the reaction chamber, the pH varied between 0 and 10. Figure 22a shows the output voltage in function of the pH in the reaction chamber. As expected from eq. (59), for pH = pH_{pzc} = 7, $\phi_{eo1} = \phi_{eo2}$ = 0 V, and the output is equal to V_{BIAS} = 0.6 V. The pH sensitivity of the output voltage (dV_O/dpH) shown in Figure 22b is in accordance with eq. (60) (-0.045/1.58 ≈ -30 mV/pH).

Figure 22c presents the OPAMP output voltage V_R. It is close to 2 V, which is in accordance with eq. (57). Considering the output saturation levels of the OPAMP V_{Osat}, there is room for trapped charge voltage compensation in order of +0.7 V to -1.5 V (considering

both ISFETs to have same trapped charge offsets). Figure 22d presents the ISFET1 drain current, which the same as I_{BIAS} for all the simulated pH values.

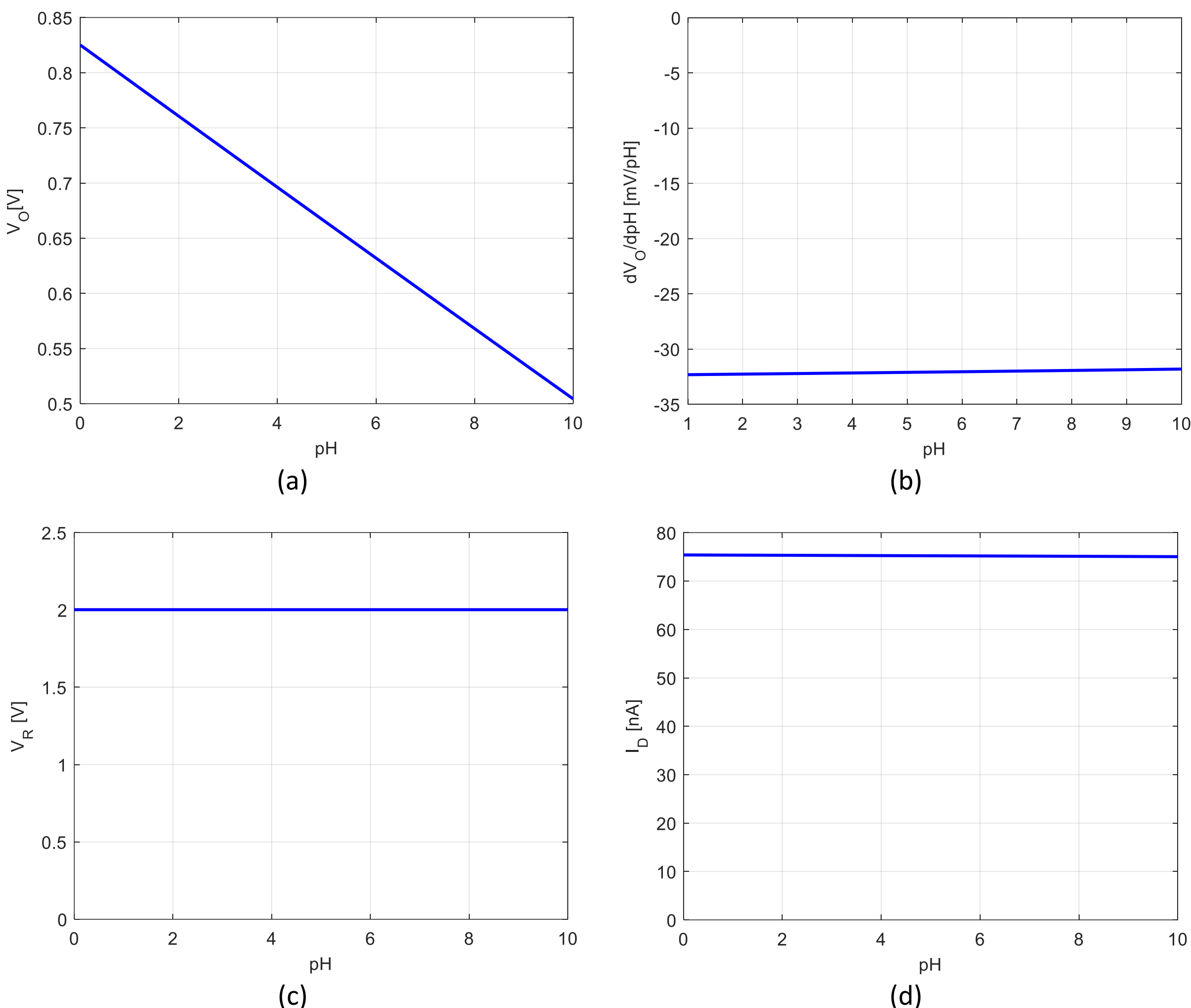
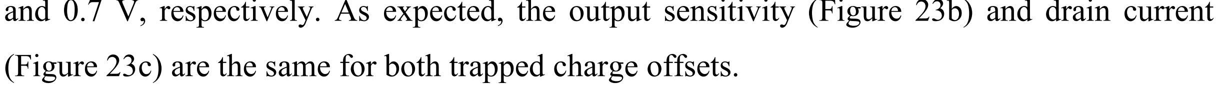


Figure 22 - Differential circuit simulation for pH from 0 to 10: (a) V_O, (b) V_O pH sensitivity, (c) V_R, and (d) ISFET1 drain current.

6.1.2.2 Both ISFETs with same V_{tc}

In this case, both ISFETs were configured with the same trapped charge offset (V_{tc}). Two pH sweeps were simulated: one simulation was set with V_{tc} of -1.5 V, and the other simulation with V_{tc} of + 0.7 V. This situation could be equivalent to measure 2 chips with an inter-die variation in the ISFETs threshold voltage. Figure 23a presents the output voltage V_O and the electrode voltage V_R for a pH variation from 0 to 10. It is possible to observe that the output voltage was the same for both V_{tc} while the electrode voltage was regulated by the OPAMP to compensate for the offsets, generating a V_R of 0.5 V and 2.7 V for V_{tc} of -1.5 V



and 0.7 V, respectively. As expected, the output sensitivity (Figure 23b) and drain current (Figure 23c) are the same for both trapped charge offsets.

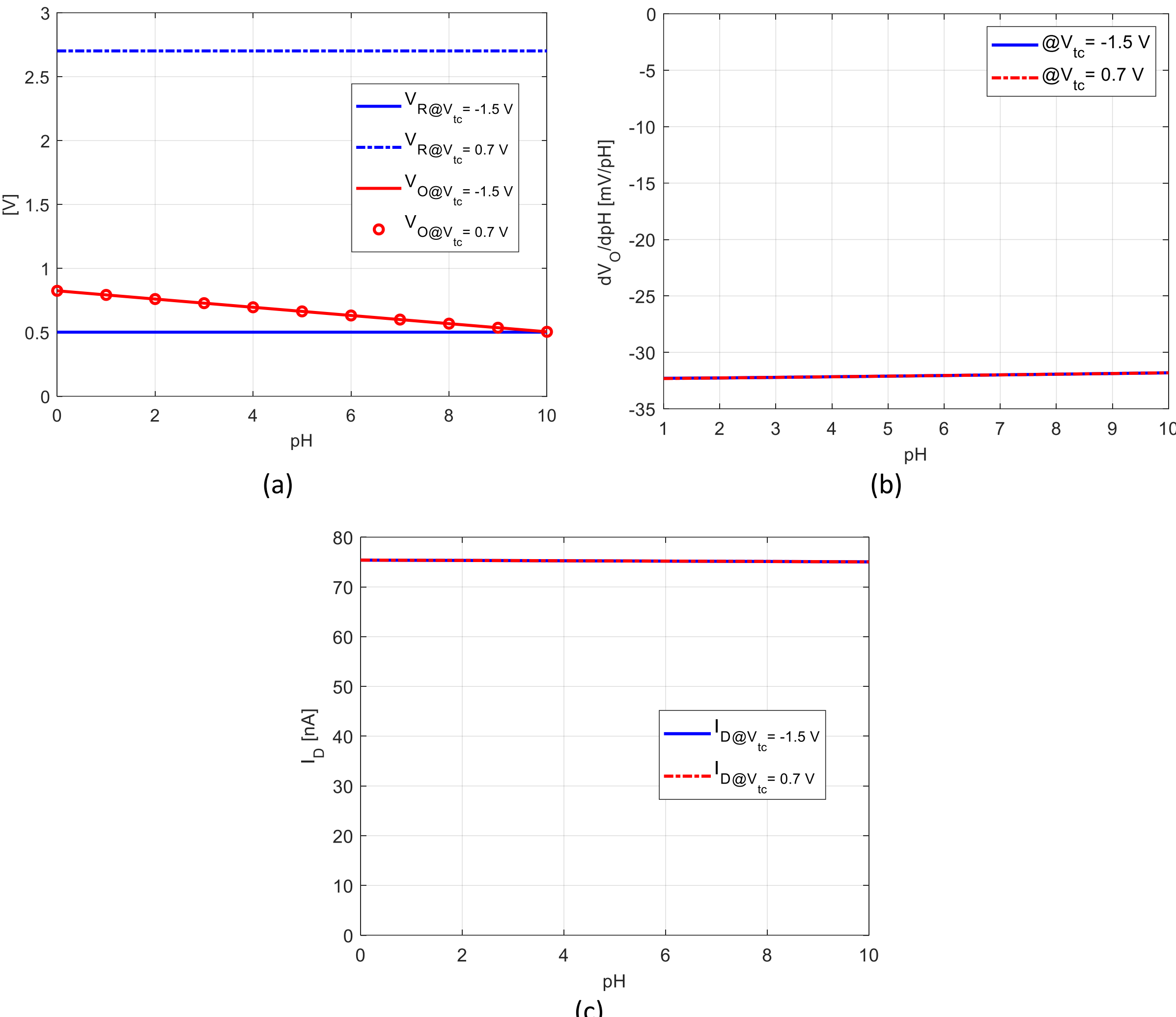


Figure 23 – Differential circuit simulation with both ISFETs with the same V_{tc} of -1.5 V and 0.7 V and pH from 0 to 10: (a) V_R and V_O, (b), Vo pH sensitivity, and (c) ISFET1 drain current.

6.1.2.3 ISFETs with different V_{tc}

In this case, ISFET1 and ISFET2 were configured with different trapped charge offsets (V_{tc1} = -1.5 V, V_{tc2} = 0.7 V, respectively) maintaining others parameters the same. This situation would be equivalent to an intra-die variation in the ISFETs threshold voltage.

Figure 24a shows the output and electrode voltage, and Figure 24b the output pH sensitivity. It is possible to note that the sensitivity is the same as in the previous simulation, while the output voltage level changed, due to the mismatch between threshold voltages of the ISFETs, as can be concluded from eq. (59). The electrode voltage V_R, defined by the OPAMP,

is in accordance with eq. (57). The ISFET1 drain current is close to its designed value (Figure 24c).

From eq. (64), the maximum intra-die variation in the threshold voltage of the ISFETs would be close to 2 V.

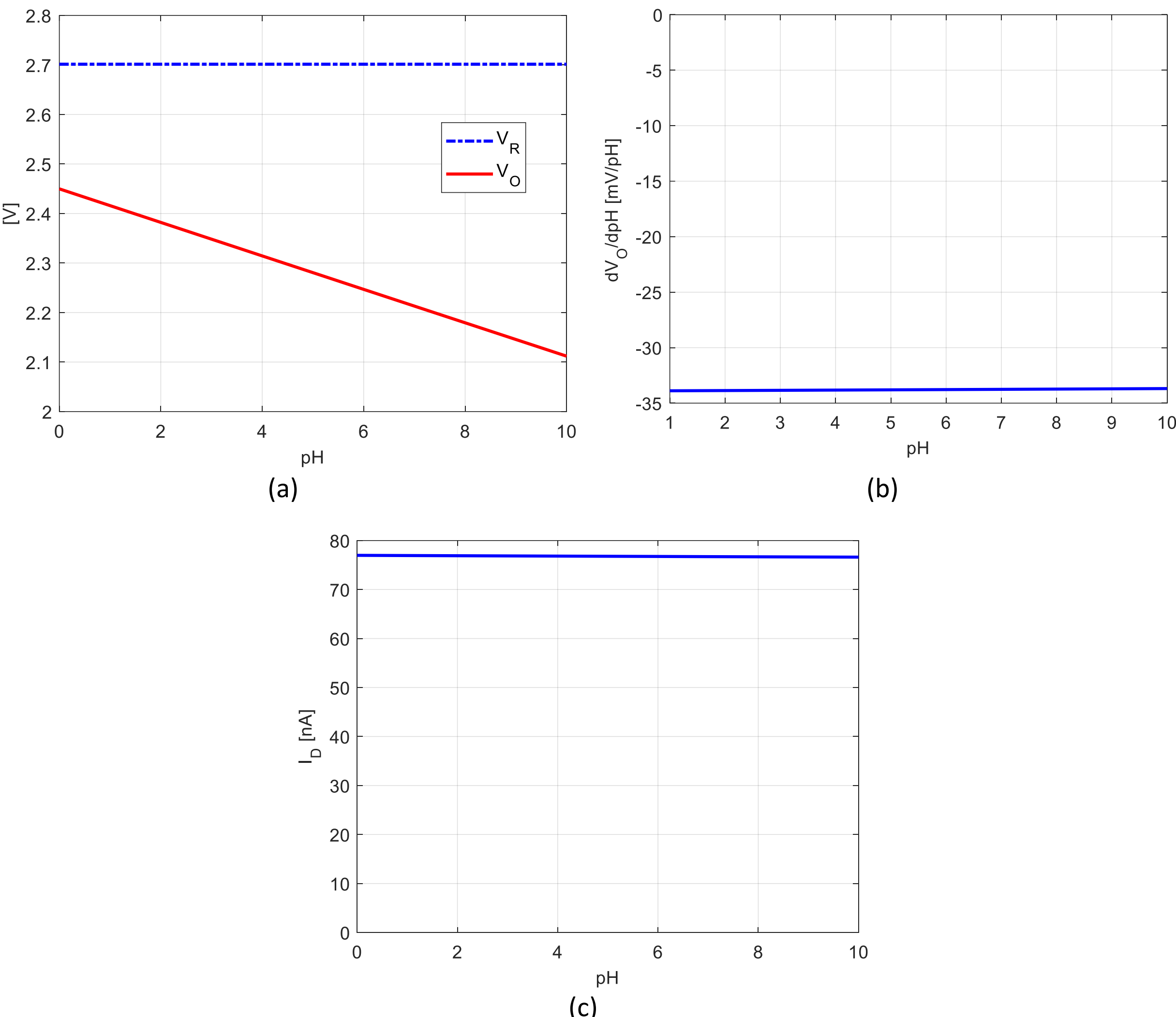


Figure 24 – Differential circuit simulation of intra-die offset variation (V_{tc1} = -1.5 V, V_{tc2} = 0.7 V) and pH from 0 to 10: (a) V_O and V_R, (b) V_O pH sensitivity, and (c) ISFET1 drain current.

6.1.2.4 Common-mode voltage variation

A voltage V_{drift} varying from -0.5 V to +0.5 V was added to both ISFETs gates, while maintaining a constant pH = 7 in both chambers. Figure 25a shows that the output voltage stayed fixed at V_{BIAS} = 0.6 V, while the electrode voltage V_R changed 1 V to compensate for the V_{drift} variation of 1 V. The drain current of the ISFETs stayed constant during the common-mode voltage variation (Figure 25b). Therefore, according to the results of this

simulation, the circuit can compensate for common-mode voltage variations, such as temporal drift of the sensors.

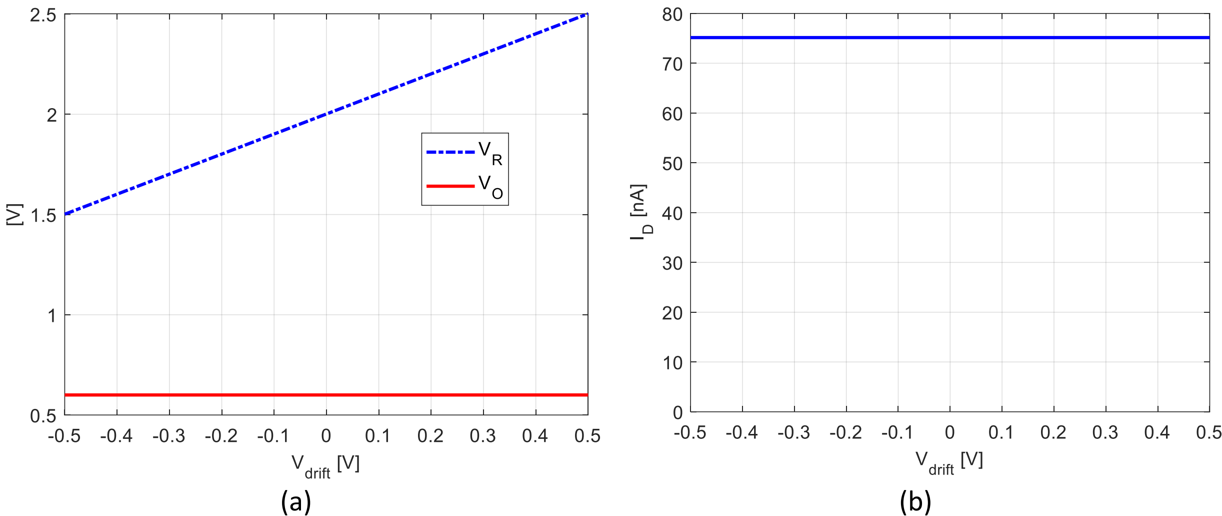


Figure 25 – Differential circuit simulation with a common-mode voltage variation V_{drift}: (a) V_O and V_R, and (b) ISFET1 drain current.

6.2 SINGLE-ENDED CONFIGURATION

By using only one chamber and reading the output voltage from another pin, it is possible to use the circuit previously described in a single-ended configuration, as shown in Figure 26.

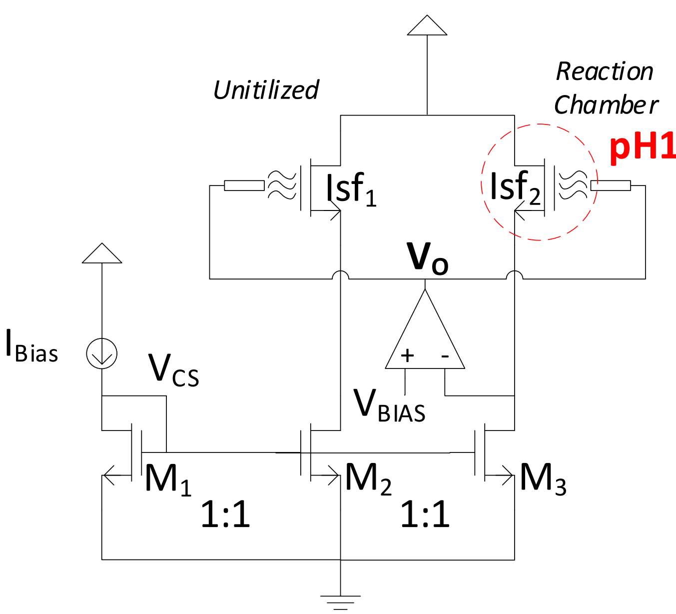


Figure 26 - Single-ended configuration (bulk terminals are connected to ground).

In this case, the previous buffer chamber is used as the reaction chamber, whereas the other chamber is not required. The output voltage is the voltage applied to the reference electrode by the OPAMP output. Any pH variation is reflected in the reference electrode voltage for the ISFET to operate with a source voltage V_{BIAS} and current defined by the current source M3.

6.2.1 DC analysis

Writing the UICM for ISFET2:

$$\frac{V_{REF} - V_{TISF2}}{n_{ISF2}} - V_{\mathrm{SB2}} = \phi_t \left[\sqrt{1+i_{f2}} - 2 + \ln\left(\sqrt{1+i_{f2}} - 1 \right) \right] \quad (66)$$

In this case, the output voltage is the voltage applied to the electrode by the OPAMP output; therefore, $V_O = V_{REF}$ and $V_{SB2} = V_{BIAS}$:

$$V_O = V_{TISF2} + n_{ISF2} \left(\phi_t \left[\sqrt{1+i_{f2}} - 2 + \ln\left(\sqrt{1+i_{f2}} - 1 \right) \right] + V_{\mathrm{BIAS}} \right) \quad (67)$$

Considering that only ϕ_{eo} varies with pH, the output sensitivity is given by:

$$\frac{dV_O}{dpH} = -\frac{d\phi_{eo2}}{dpH} \quad (68)$$

Therefore, compared to the differential configuration, a higher output sensitivity is expected in this configuration, but without common-mode compensation.

6.2.2 Simulations

Simulating the same circuit as in the differential testbench, but now using the previous buffer chamber as a reaction chamber and changing its pH from 0-10, the following results were obtained. Figure 27a shows the output voltage as a function of the pH, while Figure 27b shows the sensitivity of the output voltage with pH, which is in accordance with

eq. (68), resulting in 45 mV/pH. Figure 27c shows the ISFET drain current, which is close to I_{BIAS} for the simulated pH range.

Analyzing the output voltage and considering the output saturation levels of the OPAMP V_{Osat}, the circuit can still work with variations in the ISFET threshold voltage in the order of +1 V to -1 V.

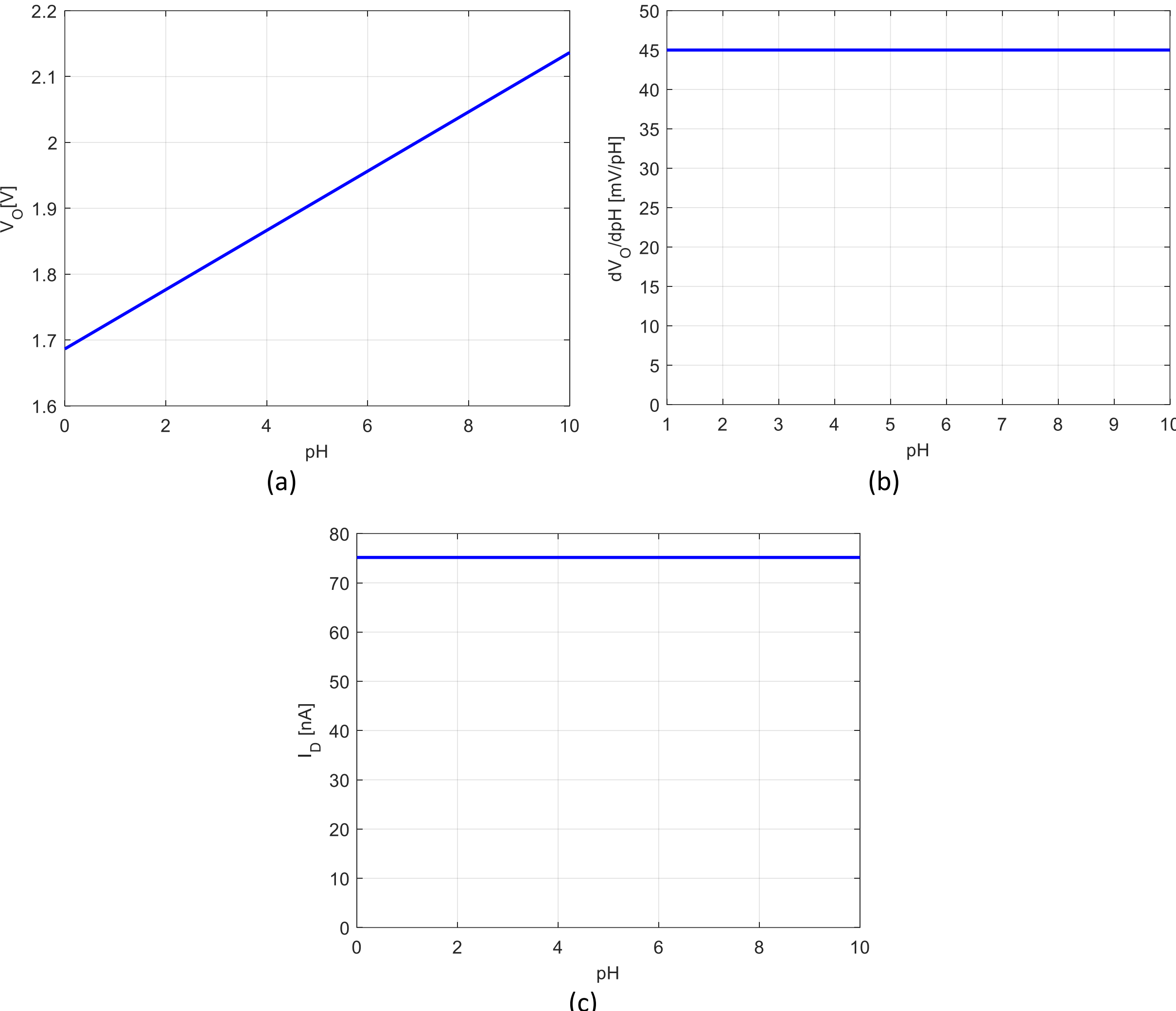


Figure 27 – Single-ended circuit simulation for pH from 0 to 10: (a) V_O, (b) V_O pH sensitivity, and (c) ISFET drain current.

7 EXPERIMENTAL RESULTS

7.1 CHIP SILTERRA

7.1.1 MOSFETs Measurements

For process parameter monitoring, each first-round chip had one n-MOSFET and one p-MOSFET. Table 7 presents the MOSFETs threshold voltage (V_{Tmos}), specific current (I_S), and slope factor (n_{mos}) measured in 15 dies with the g_m/I_D methodology described in [52].

Table 7 - Mean and standard deviation of the measured MOSFETs parameters.

Parameter	n-MOSFET		p-MOSFET	
	Mean	Standard Deviation	Mean	Standard Deviation
V_{Tmos} (mV)	1012.08	117.44	-1213.33	175.78
I_S (nA)	203.51	24.75	75.15	13.82
n_{mos}	2.50	0.34	2.01	0.26

The measured MOSFET parameters were used as a reference for ISFET modelling and estimations, as some of the parameters deviated from the values specified by the PDK.

7.1.2 ISFETs Dry Characterization

The tests of metallized chips were performed using an Agilent 4156C semiconductor parameter analyzer with an Agilent 16442A test fixture (Figure 28). The threshold voltage, specific current and slope factor of the metallized ISFETs were extracted using the g_m/I_D method [52], where g_m is the transconductance given by dI_D/dV_{REF}.

Figure 28 - Test setup (test fixture was closed during the measurements).

Figure 29 presents the spatial distribution of the threshold voltage (V_t) across the n-ISFET and p-ISFET arrays, for four chips. Device malfunctions were mainly caused by open connections in the bonding wires due to the epoxy deposition. Histograms of the threshold voltages are shown in Figure 30.

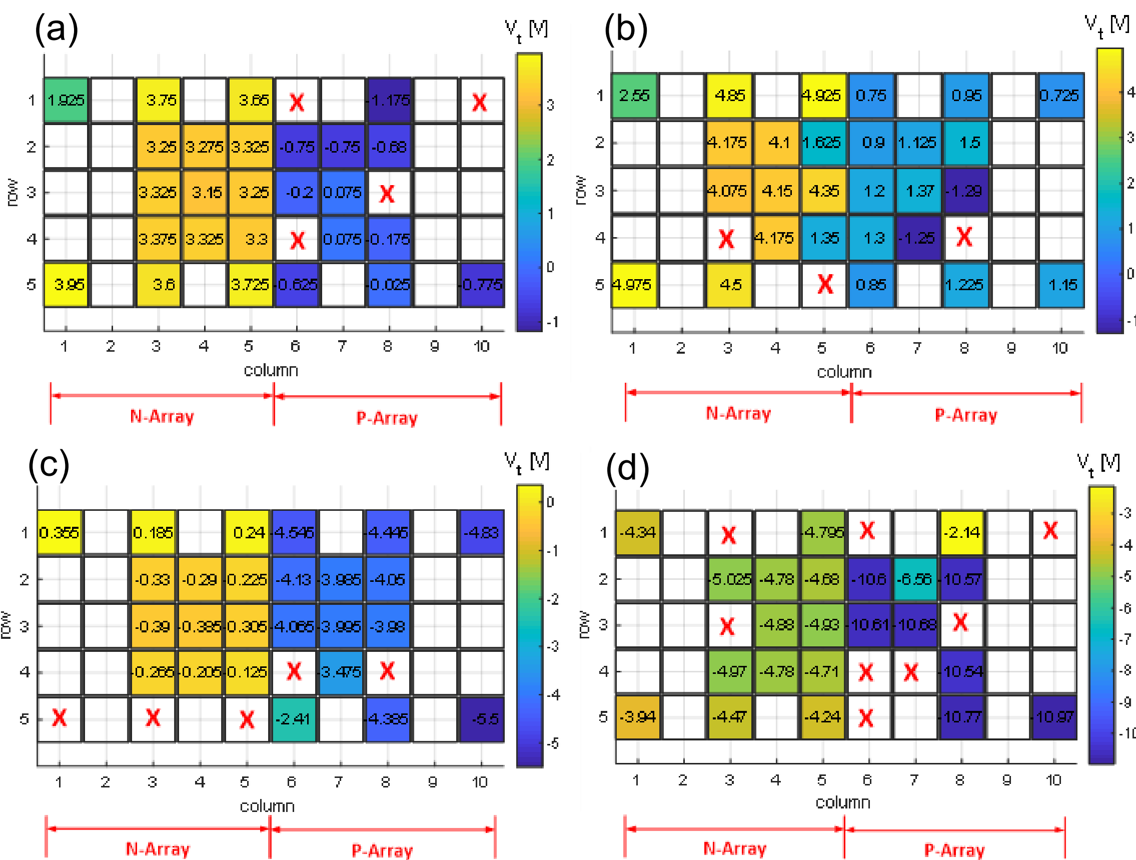


Figure 29 - Spatial variation of ISFETs threshold voltage across the array after the dry characterization of four chips: (a) Chip11, (b) Chip05, (c) Chip03 and (d) Chip16. ("X" indicates a failed device; empty spaces are dummy elements).

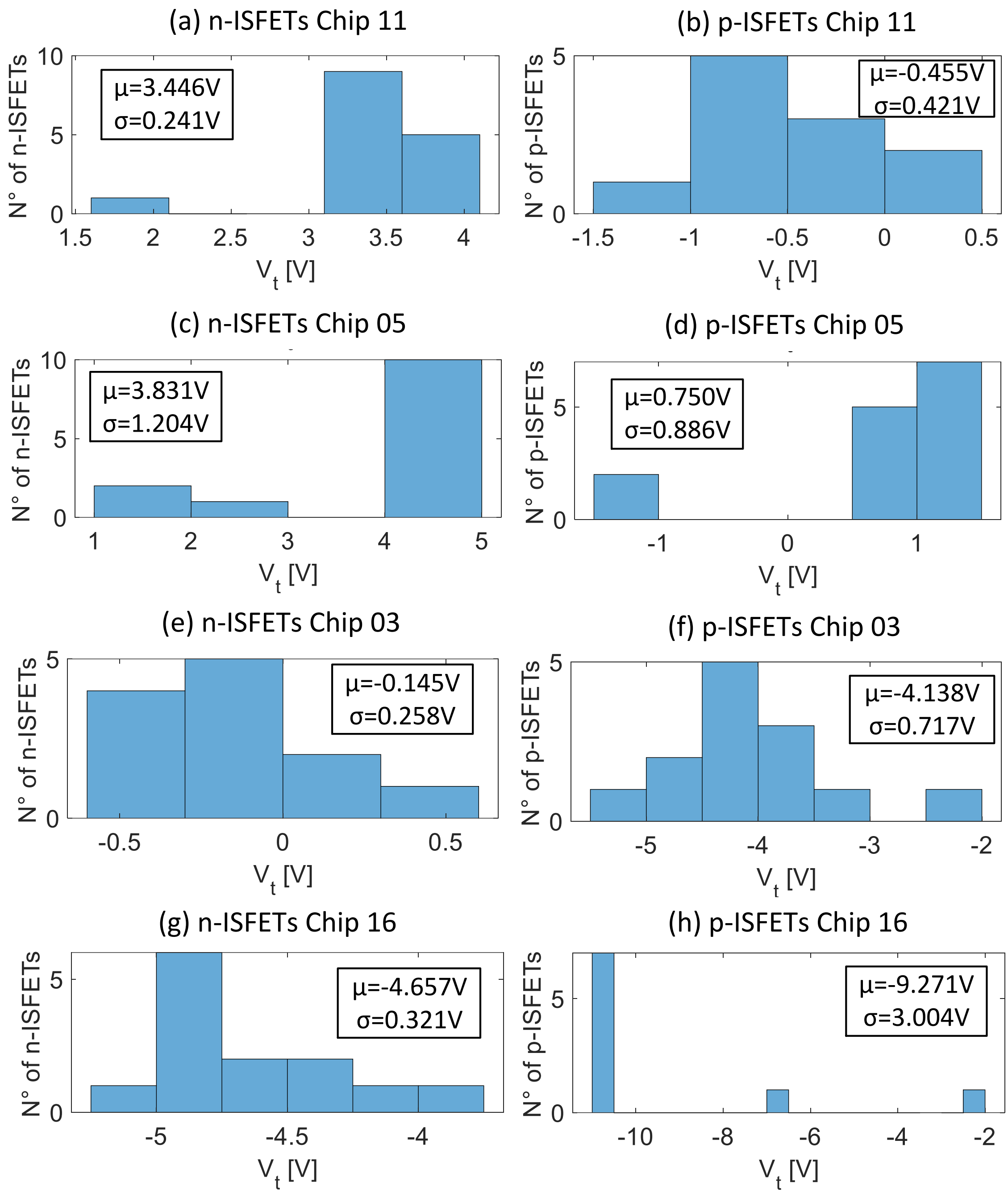
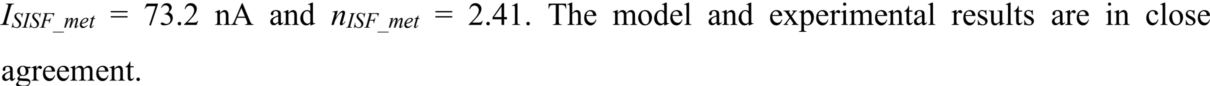


Figure 30 - Histograms of the threshold voltages measured on the n-ISFET and p-ISFET arrays of the four metallized chips.

The I_D vs V_{REF} and g_m/I_D vs V_{REF} curves for the ACM model, implemented in MATLAB®, are compared with the measurement results for an n-ISFET (Figure 31a) and a p-ISFET (Figure 31b). The extracted parameters for the n-ISFET under test are $V_{TISF_met} = 3.32$ V, $I_{SISF_met} = 231$ nA and $n_{ISF_met} = 2.72$, while for the p-ISFET they are $V_{TISF_met} = -0.75$ V,



I_{SISF_met} = 73.2 nA and n_{ISF_met} = 2.41. The model and experimental results are in close agreement.

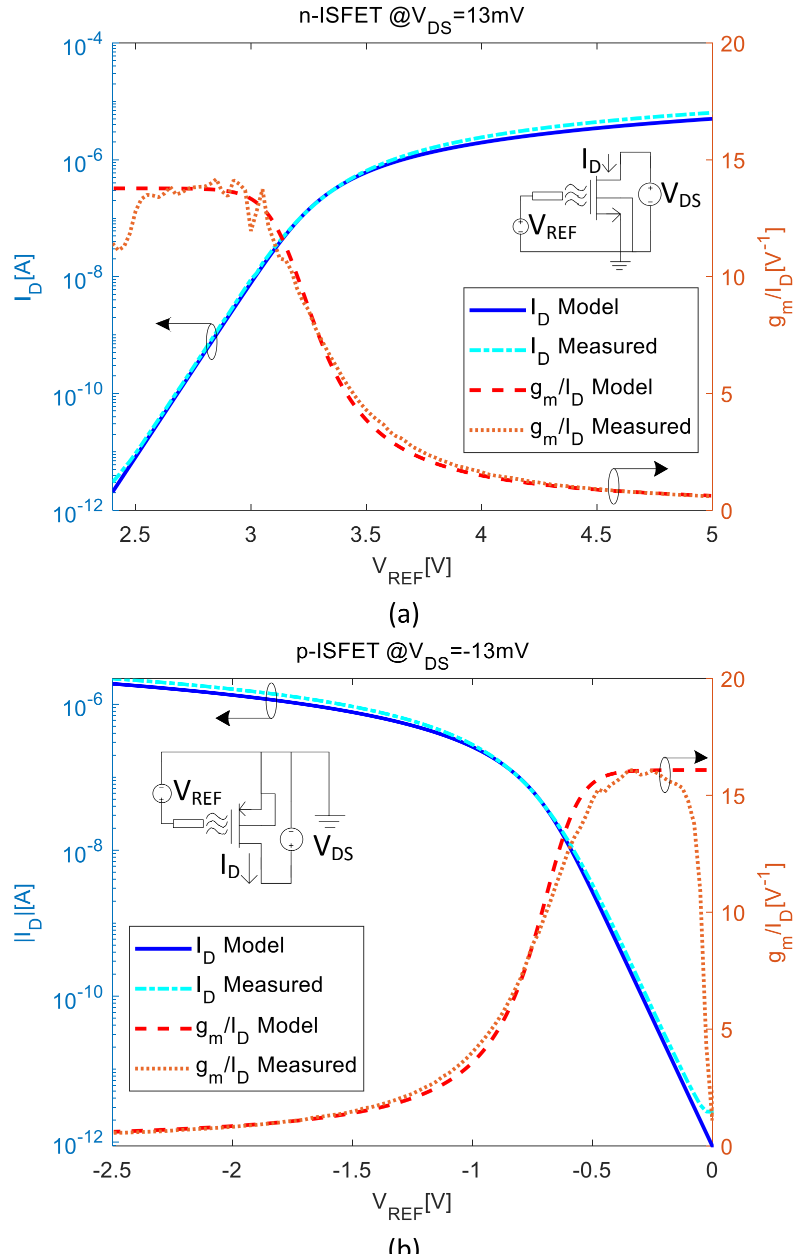


Figure 31 - I_D vs V_{REF} and g_m/I_D vs V_{REF} of the model and measurements for (a) n-ISFET 06 and (b) p-ISFET 05 from Chip 11.

In floating gate devices, charges are trapped in the gate and mostly in the passivation layer during the fabrication process, causing offsets in the threshold voltage. Using the model developed in this thesis and experimental results, it is possible to estimate this charge. Table 8 presents the offset considering the theoretical value of V_{TISF_met}, assuming that there are no charges (Q_{pass} = 0 C) at the passivation layer, and the mean values of V_{TISF_met} measured on metallized chips for both n- and p-ISFETs.

The value of V_{TISF_met} for Q_{pass} = 0 C was calculated using eq. (50) with the mean values for the measured V_{Tmos} and n_{mos} listed on Table 7, $|2\phi_F|$ = 0.8 V, and the previously calculated values of C_{ox} and C_{pass}. The resulting V_{TISF_met} values, assuming Q_{pass} = 0 C, were 2.38 V for the n-ISFETs and −0.76 V for the p-ISFETs. Defining the offset as the difference between the theoretical value of the threshold voltage for Q_{pass} = 0 C and the measured values, the value of Q_{pass} can be calculated using eq. (50).

Table 8 - Estimation of the offset in threshold voltage due trapped charge at passivation.

Sample	n-ISFETs				p-ISFETs			
	V_t [V] (µ measured)	V_{TISF_met} [V] (Q_{pass}=0 C)	Offset [V]	Q_{pass} [fC]	V_t [V] (µ measured)	V_{TISF_met} [V] (Q_{pass}=0 C)	Offset [V]	Q_{pass} [fC]
Chip 11	3.45	2.38	**1.07**	**-214**	-0.46	-0.76	**0.30**	**-61**
Chip 05	3.83	2.38	**1.45**	**-292**	0.75	-0.76	**1.51**	**-303**
Chip 03	-0.15	2.38	**-2.53**	**508**	-4.14	-0.76	**-3.38**	**680**
Chip 16	-4.66	2.38	**-7.04**	**1414**	-9.27	-0.76	**-8.51**	**1711**

For the chips under analysis, the amounts of charges trapped in the passivation layer for both n-ISFETs and p-ISFETs on the same die are similar. However, the inter-die fluctuation of the threshold voltage is relatively high, ranging from approximately -8.5 V to 1.5 V, which indicates different amounts of passivation charges for each die.

Different methods have been reported to measure the threshold voltage offsets, usually using the conventional wet setup. The offset estimation includes removal of the passivation using laser [69] and reactive ion etching [19], and comparison between MOSFETs and ISFETs curves [63]. For example, offset estimations of -1.32 V for one n-ISFET [69] and inter-die averages between -1 V and 4 V for n-ISFETs with different geometries [63] were reported. Compared with the procedures employed in the studies described in [69], [19] and [63], the method developed in this work is neither destructive nor affected by chemical potentials, can cover the entire die area, and is thus suitable for the characterization of ISFET arrays.

Table 9 shows the dispersion of the ISFET threshold voltages obtained in this study for four chips using the dry test compared with those reported in the literature using the conventional wet test. It can be observed that the dispersion in the ISFET threshold voltages in this study is comparable to those reported in other publications for different technologies.

Table 9 - ISFET threshold voltage dispersion compared with previously published values.

Ref.	**Year**	**Technology**	**Threshold voltage dispersion (without compensation)**	**ISFET type**	**Test type**
[8]	1999	Atmel-ES2 1.0 µm	6.4 ± 1.4V (linear gate) -7 ± 0.8 V (Interdigitated)	N	wet (pH 7)
[20]	2008	AMS 0.35 µm	-4 to -1 V	P	wet (pH 7.4)
[18]	2011	0.35-µm 2P3M CMOS	-14 to +8 V	P	wet (pH 7)
This work*	2020	SilTerra 180nm HV	-5.02 to 4.97 V (n-ISFETs) -10.97 to 1.50 V (p-ISFETs)	N and P	dry (gold)

*Considering four chips (totaling around 100 ISFETs).

Using eq. (51) with the mean values of the measured n_{mos} shown on Table 7, and the already calculated values of C_{ox} and C_{pass}, slope factors of 2.82 and 2.23 for the n-ISFETs and p-ISFETs, respectively, are obtained. As expected, there is an increase in the slope factor for ISFETs compared to that for MOSFETs owing to the passivation capacitance. This increase in the slope factor (n) decreases the maximum transconductance efficiency $(g_m/I_D)_{max}$ according to the following equation [52], [89]:

$$\left(g_m / I_D\right)_{max} = \frac{1}{n\phi_t} \qquad (69)$$

This decrease in g_m/I_D in ISFETs compared with that in MOSFETs can be observed in the experimental curves of Figure 32 for both n- and p-type devices.

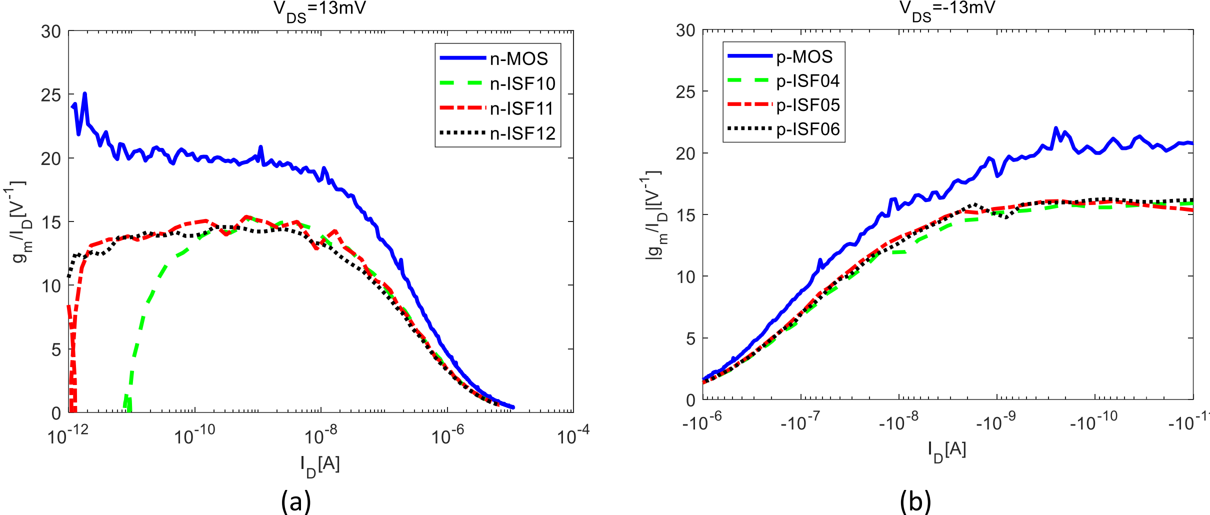


Figure 32 - Measured g_m/I_D vs I_D curves of a MOSFET from Chip 20 and ISFETs from Chip 11 for (a) n-type and (b) p-type.

Table 10 shows the measured and theoretical values of the slope factor and $(g_m/I_D)_{max}$ for the ISFETs of all measured chips in the 3 × 3 central array (devices 04–12, for better matching).

Table 10 - Mean measured and theoretical slope factors and $(g_m/I_D)_{max}$ for ISFETs of the 3 × 3 central array in four dies.

	n-ISFETs		p-ISFETs	
	slope *n*	$(g_m/I_D)_{max}$	**slope *n***	$(g_m/I_D)_{max}$
Measured (μ)	3.10	12.42	2.74	14.05
Theoretical eq. (51)	2.82	13.64	2.23	17.25

Using eq. (53) with the mean values of the MOSFETs specific currents listed on Table 7, and the values of C_{ox} and C_{pass} previously calculated, specific currents of 189 nA and 68 nA are obtained for the n-ISFET and p-ISFET, respectively. Table 11 presents the theoretical and experimental values of specific current for the ISFETs of the measured chips in the 3 × 3 central array.

Table 11 – Mean measured and theoretical specific currents for ISFETs of the 3 × 3 central array in four dies.

	I_{SISF_met}	
	n-ISFETs	**p-ISFETs**
Measured (μ)	204 nA	67 nA
Theoretical eq. (53)	189 nA	68 nA

The differences between the experimental and theoretical values of n_{ISF_met} and I_{SISF_met} indicate possible capacitances deviations from the typical values used for the calculations. In this design, the passivation capacitance is dominant in relation to the oxide capacitance ($C_{pass} \approx 5C_{ox}$). Thus, the slope factor, g_m/I_D characteristic and specific current of the ISFETs are similar to those of the MOSFETs, as can be inferred from eqs. (51) and (53), and can be observed in the experimental results shown in Table 7, Table 10 and Table 11. Therefore, making the passivation capacitance dominant over the oxide capacitance results in ISFETs with a higher g_m/I_D value, close to that of the MOSFET [69].

The results of the electrical parameter extraction of the four metallized chips analyzed previously are presented in APPENDIX G - Chip SilTerra: results of the dry parameters extraction.

7.1.3 ISFETs Wet Tests

7.1.3.1 Wet Test Procedure

To measure the pH sensitivity of the fabricated ISFETs, a discrete readout circuit was built, and non-metallized chips were wet-tested (Figure 33). The wet characterization reported in this section was performed with the contribution of Laboratório de Prototipagem/TECPAR/FioCruz-PR. More details of the readout circuit are provided in APPENDIX H - Discrete readout circuit project for wet tests.

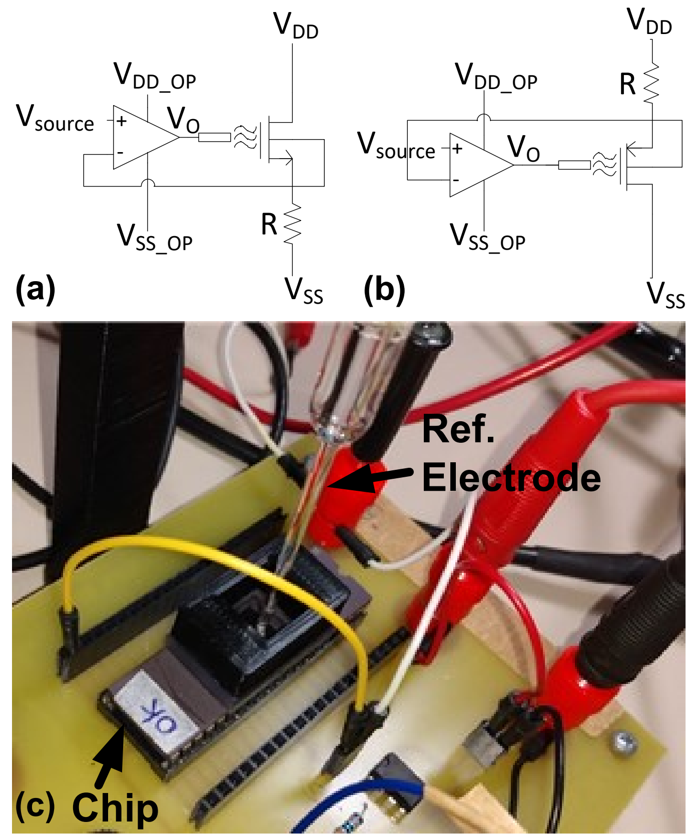


Figure 33 - Readout circuit used to measure pH sensitivity: (a) n-ISFET schematic, (b) p-ISFET schematic, and (c) implementation.

The sensitivity of the devices was characterized using 650 µL of buffers with pH 4, 7, and 9 from Certipur, manipulated with a micropipette from Uniscience. Each buffer was measured during 1 minute. The ISFET was biased with a tiny Ag/AgCl reference electrode (Analyzer 3A45), which had an appropriate tip diameter for the chip chamber. The circuit was powered by an HP E3630 power supply, and the output voltage was measured using a Hikari HM-2090 multimeter. A larger chamber, glued at the top of the chip, and an electrode support were 3D printed in the Laboratório de Prototipagem/Fiocruz-PR. Figure 34 shows the setup for the wet measurements.

APPENDIX I - Homemade chamber implementing a PVC tubing presents an alternative chamber implemented with a PVC tube for low-cost implementation using conventional tools. Because it does not require any specific equipment or affordable materials, it is suitable for prototyping.

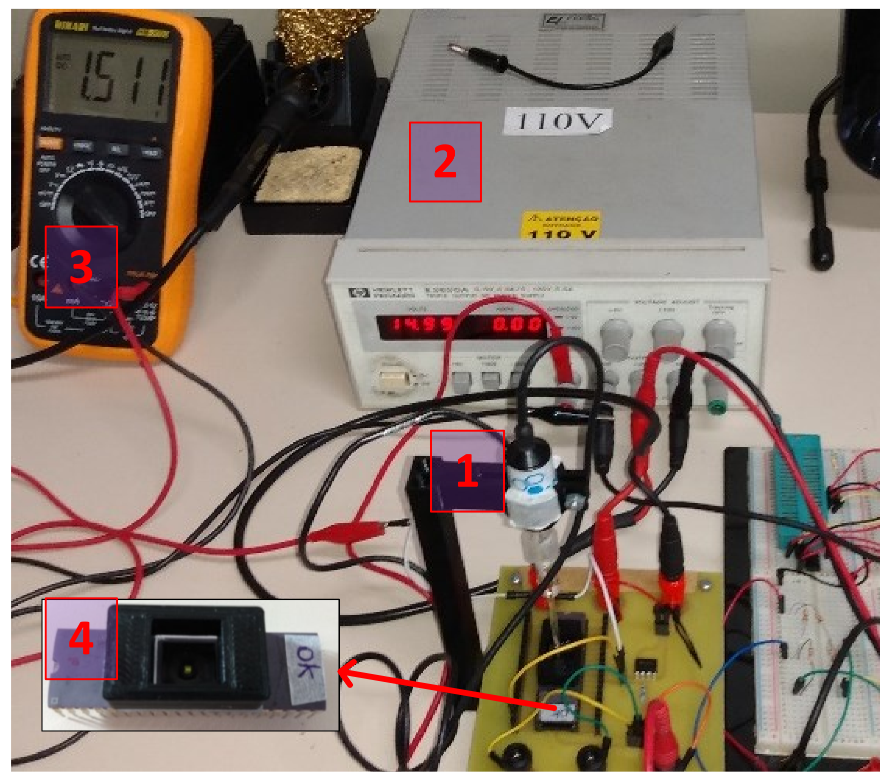
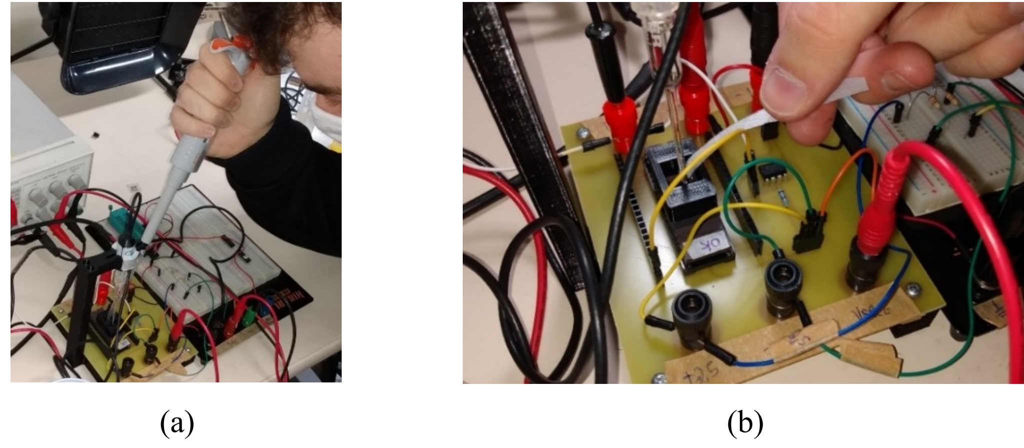


Figure 34 - Wet test setup: (1) reference electrode support, (2) power supply, (3) multimeter, and (4) 3D chamber.

After each measurement, the chip was cleaned twice. The cleaning process consisted in (i) immersing the top of the chip with Milli-Q water for 1 minute, (ii) removing the cleaning solution, (iii) drying the top of the chip with a wiper, and (iv) letting it dry for 1 minute (Figure 35).



(a) (b)

Figure 35 - (a) A micro pipette was used to fill and remove the buffer solution. (b) Drying with a wiper.

7.1.3.2 Wet Test Results

Wet tests indicated a sensitivity of 38 mV/pH for an n-ISFET of one chip and 46 mV/pH for a p-ISFET of another chip (Figure 36), which are close to the value obtained from simulations in our previous work [53]. The n-ISFET was measured by increasing and decreasing values of pH, presenting a good consistency in the measured values, while the p-ISFET was measured only for increasing values of pH.

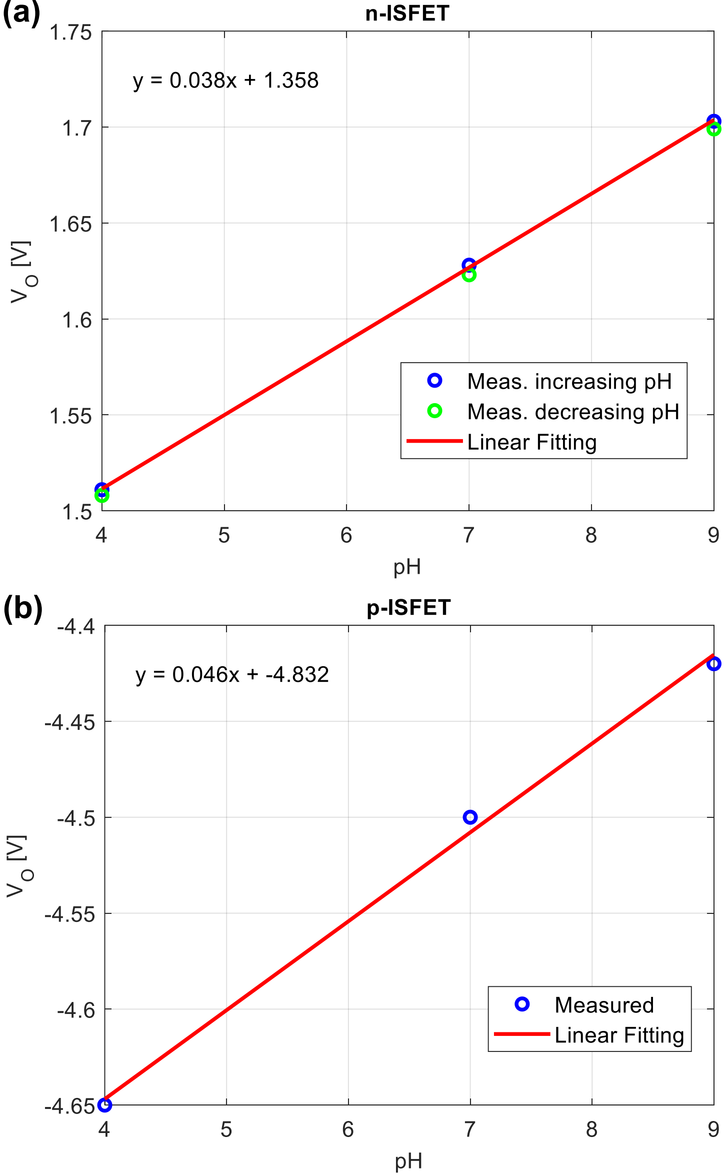


Figure 36 - pH sensitivity at 650 µL: (a) n-ISFET 09 from chip 08 (21/09/2020), (b) p-ISFET 15 from chip 14 (24/09/2020).

To test at a lower volume, the n-ISFET reported above was tested using 50 µL, one day after calibration with 650 µL (Figure 37). The output level increased by approximately 0.2 V, while the sensitivity (36 mV/pH) remained close to the one obtained the previous day. The reference electrode submersion was verified visually.

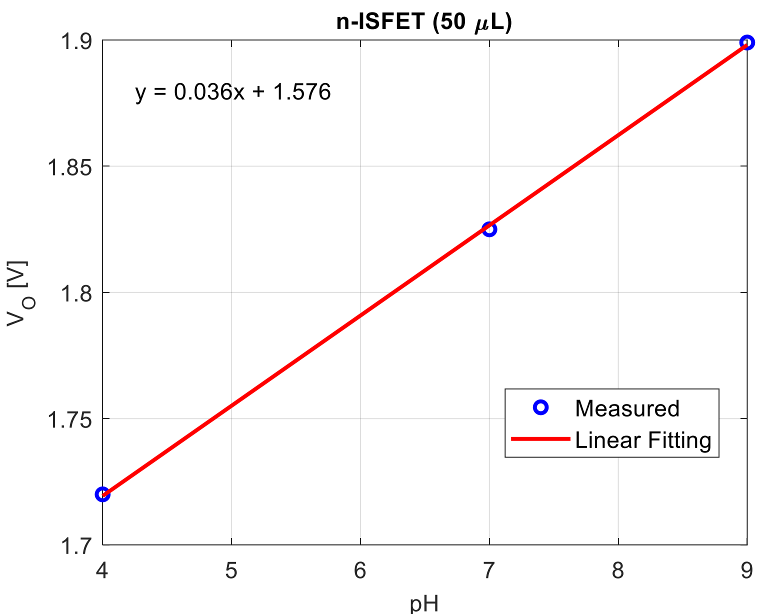


Figure 37 - ISFET sensitivity to pH, 22/09/2020, at 50 µL (n-ISFET 09 from chip 08).

The readout circuit (Figure 33) was designed to generate a current I_D of 8 µA, using the following parameters: $V_{DD_OP} = -V_{SS_OP} = 15$ V, $V_{DD} = -V_{SS} = 2.5$ V, $V_{source} = 0$ V, $R = 300$ kΩ and the TL072 OPAMP. Because $I_D = I_S.i_f$ for a saturated device, and considering the average specific current measured with the dry test shown on Table 11, the corresponding inversion levels (i_f) are 40 and 120 for the n-ISFET and the p-ISFET, respectively. Using once again the UICM, eq. (4), the output voltage (V_O), is given by:

$$V_O = V_{TISF} + n_{ISF}\phi_t\left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right] + V_{source} \tag{70}$$

Using the measured values of n_{ISF} (Table 10) and V_O at pH 7 (Figure 36), we get $V_{TISF} = 1.13$ V and $V_{TISF} = -3.69$ V for the analyzed n-ISFET and p-ISFET respectively. These values are within the measured threshold voltage range using the dry test (Table 9).

After several hours of testing, we obtained some unstable responses, which prevented us from characterizing the full array of each chip. To reduce instabilities, some studies used

more robust techniques for cleaning. For example, immerse the sensors in 2% hydrofluoric (HF) solution for 15s [8], eatch pixels for 30s in 10% buffered HF acid solution [48], or clean the chip with a phosphate buffer solution and dry it with a high pressure nitrogen gun [31].

8 CONCLUSIONS

8.1 SUMMARY OF THE THESIS

This thesis reviewed the main ISFET nonidealities and compensation techniques, proposed a dry test, and developed a physical model for ISFETs in contact with electrolytes and metal layers. Chips designed with ISFETs were fabricated using commercial CMOS technologies and were measured using wet and dry tests. A readout topology for differential and single-ended measurements was analyzed and simulated.

The proposed dry test avoids the influence of the chemical characteristics of both the aqueous solution and the reference electrode in the measurements. The dry gate was realized through a DC-sputtered Au film for electrical contact with the floating gate of ISFETs fabricated using a standard 0.18 μm HV technology, encapsulated with a DIP40 package, and an epoxy chamber.

A physical model, implementing the ACM model of transistor, for wet and dry conditions was proposed. Trapped charges were estimated using the developed model and dry test. The n-ISFETs and p-ISFETs of the same die presented, on average, a similar offset, mainly caused by trapped charges. However, the inter-die measurements of the trapped charges differed considerably. The dispersions of threshold voltage measured with the dry test were in accordance with the reported in the literature for wet tests. The measurements and simulation results obtained using the ACM model adapted to the dry-gate ISFET were in close agreement. Wet tests of an n-ISFET and a p-ISFET of non-metallized chips indicated pH sensitivities close to the expected values.

This thesis also proposed a circuit topology that allows both differential and single-ended measurements, presenting circuit analysis and simulation. A test chip optimized for differential measurements was designed and sent for fabrication in a commercial 0.35 μm CMOS technology.

8.2 MAIN CHALLENGES

A commercial service to install a chamber in the chips was not available in our region at the time of this research, and it took a few months for our partner to develop an epoxy chamber. Considering the fabrication time of the dies at the foundry, the first chips

were available only after several months. Epoxy application can also deteriorate bonding wires, invalidating some sensors or chips.

During the wet test, we faced instability after some hours of testing and could not reuse the chips. This could be improved by a cleaning process to remove oxidation from the passivation layer.

This interdisciplinary research has linked teams from the electronics, fabrication, and chemical laboratories. The interaction between teams was difficult during the COVID-19 restrictions in 2020 and 2021. The COVID-19 situation also delayed the fabrication of the second chip, preventing us from measuring its properties during this study.

8.3 FUTURE WORK

The proposed dry test can be used as a complementary tool to the wet test for ISFET analysis and characterization. Through the improvement of the metallization process and external connection, the setup proposed here could be extended to unpackaged devices, resulting in a less expensive and more rapid characterization of the electrical parameters of ISFETs. A study could be conducted to analyze the use of other metals, such as aluminum, for the dry test. The dry test introduced herein could also be used for a separate analysis of the chemical and electrical contributions of effects like noise and temperature to the ISFETs characteristics.

After wet testing chips for some hours, we faced unstable response. So future works could implement a more robust cleaning technique for the reuse of chips in contact with electrolytes, such as the use of a proper passivation etchant. The development of two chambers in a chip would allow differential measurements between ISFETs of the same chip. With a more complete device characterization, the sensors could be used for the analysis of biological samples and be integrated with an on-chip readout circuit and a built-in quasi reference electrode for a portable system, suitable for lab-on-a-chip applications.

8.4 PUBLICATIONS

Until the writing of this manuscript, the following papers were published:

International Conference:

R. Wrege, M. C. Schneider, J. Gonçalves Guimarães and C. Galup-Montoro, "ISFETs: theory, modeling and chip for characterization," 2019 IEEE 10th Latin American Symposium on Circuits & Systems (LASCAS), Armenia, Colombia, 2019, pp. 109-112, doi: 10.1109/LASCAS.2019.8667572.

Journal:

R. Wrege, C. Peter, B. N. Wesling, C. R. Rambo, M. C. Schneider and C. Galup-Montoro, "A CMOS Test Chip With Simple Post-Processing Steps for Dry Characterization of ISFET Arrays," in IEEE Sensors Journal, vol. 21, no. 4, pp. 4755-4763, 15 Feb.15, 2021, doi: 10.1109/JSEN.2020.3035627.

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APPENDIX A – MATLAB algorithms

```
% Rodrigo Wrege 2018/1 (update 2022/06)
% Calcula potenciais e correntes no ISFET de
acordo com o pH.

close all
clear all
%format short e

%% Constantes:
global q T e0 er z k n0 xh ka kb kn Nsil Nnit
phit Hb

q = 1.6e-19; %eletronic charge [C]
Tc = 25; %temperature [°C]
T = Tc + 273; %[K]
e0 = 8.85e-12; %vacum permissivity [F/m]
er = 78.49; % pg 548 BARD, 2001
z = 1;% z:z electrolyte (NaCl: z=1)
k = 1.38e-23; % Boltzmann cte [J/K]
C = 0.1; %z:z electrolyte ion concentration
[mol/L] (Massobrio, 2000)
C_m= 1e3*C; %electrolyte concentration [mol/m3]
NA = 6.02e23; %Avogadro's number
n0 = NA*C_m; %concentração de íons na solução
número/m3 tabela 13.3.1 (BARD, 2001)
xh = 5e-10; %helmholtz outter plane distance from
electrode [m]
ka=15.8; %positive dissociation constant [mol/L]
Massobrio 1992
kb=63.1e-9; %negative dissociation constant
[mol/L]
kn=1e-10; %dissociation constant for amine sites
[mol/L]
Nsil=3e18; %silanol or oxide surface site density
[m-2]
Nnit=2e18; %amine surface site density [m-2]
Eagcl=0.19; % potential of the ref. electrode
(Ag/AgCl) relative to the hydrogen electrode [V]
Eref = 4.44 + Eagcl; %[V]
phit=k*T/q; %thermal voltage [V]
xsol=3e-3; % electrolyte-insulator surface dipole
potential, [V] (Massobrio, 2000) (Bousse 1982 é
0.03??)
wf_m=4.7; % work function of the metal gate
relative to vacuum. [V] (Massobrio, 2000)
phijl = 1e-3; %liquid-junction potential
difference between the ref. solution and the
electrolyte [V] (Massobrio, 2000)

%% phio

es=12*e0; %surface relative permissivity
ni=1e4; %[m-3] concentration of electron and
holes in the intrinsic semiconductor (Silicon)
N_a=1e11; %[m-3] substrate doping (livro
vermelho)
p_0=N_a; %[m-3] equilibrium hole concentration
n_0=ni^2/p_0; %equilibrium electron concentration
phif=k*T/q*log(N_a/ni) %fermi potential [V]
(2:1:18) livro vermelho
phis=phit; %????? phis=2*phif para strong
inversion (FUNG, A Generalized Theory of an
Electrolyte-Insulator..., 1986)
us=phis/phit;
% sigma_mos = -
us/abs(us)*sqrt(2*q*phit*es)*sqrt(p_0*(exp(-us) +
us -1) + n_0*(exp(us)-us-1)); %2.3.10 livro
amarelo

Hb=1e-1; % proton concentration in the bulk
electrolyte [mol/L]; (Massobrio, 2000)
% Calculando phio:
initial_guess = [0.1; 0.1];
options = optimset('TolFun', 1e-14, 'TolX', 1e-
14); %Default: TolFun=1e-6; TolX=1e-6;

for l=1:19 % de pH 1 a 10
solution = fsolve(@V_pH_phio_phih, initial_guess,
options);
phih(l) = solution(1);
phio(l) = solution(2);
pH(l)=-log10(Hb)
hb(l) = Hb;
Hb=Hb/(10^0.5);
end

%Gouy-Champan-Stern:
 Ch = er*e0/xh; %Helmholtz capacitancie in xh
[F/m2]
 Cgouy =
sqrt(2*er*e0*z^2*q^2*n0/(k*T)).*cosh(z*q*phih/(2*
k*T)); % Gouy-Chapman capacitance [F/m2]
(Massobrio, 2000): phi2<<
Cgoy=sqrt(8*er*e0*k*T*n0)/(2*phit)
 Ceq = (1./Ch + 1./Cgouy).^-1; % Stern
Capacitance [F/m2]

%phio simplified expression:
phio_sensitivity = -mean(diff(phio)./diff(pH)) %
= -dVt/dpH = -2.3.phit.alpha
[m3 posicao3] = min(abs(phio)); %achar o phio=0
pHpzc = pH(posicao3) %pH@ phio=0 = %pH @ point of
zero charge
phio_simp = phio_sensitivity.*(pHpzc - pH); %phio
simplified


%% Sensitivity (VAN HAL et al., 1995):
%hb = hb(1:length(hb)-1);
Hs = hb.*exp(-phio./phit);
Bint = 2.3.*Hs*Nsil.*(ka.*Hs.^2 + 4*ka*kb.*Hs +
ka^2*kb)./(ka*kb + ka.*Hs + Hs.^2).^2;
alpha = (2.3*k*T*Ceq./(q^2.*Bint) + 1).^-1

%my pHd expression:
Bint2 = 2.3.*Hs*Nsil.*(ka.*Hs.^2 + 4*ka*kb.*Hs +
ka^2*kb)./(ka*kb + ka.*Hs + Hs.^2).^2 +
2.3.*Hs*Nnit.*(kn./(Hs + kn).^2);
alpha2 = (2.3*k*T*Ceq./(q^2.*Bint2) + 1).^-1


for l=1:length(pH)-1 % para plotar dVt_dpH
    pH_med(l) = (pH(l)+pH(l+1))/2;
end

%% Resultados:

figure(1) %phio and phih
plot(pH, phio,'b','LineWidth',2); grid on; hold
on;
plot(pH, phih,'r','LineWidth',2);
legend('\phi_eo','\phi_2')
xlabel('pH'); ylabel('[V]');

figure (13) %phio complete vs simplified
expression
plot (pH, phio, 'b','LineWidth',2); grid on; hold
on;
plot (pH, phio_simp, 'r--','LineWidth',2);
xlabel('pH');
ylabel('\phi_eo [V]') % left y-axis
legend ('Complete','Simplified');
xlim([1 10]);
set(findall(gcf,'-
property','FontSize'),'FontSize',12); %troca
todas as fontes:
https://www.mathworks.com/matlabcentral/answers/2
23344-changing-font-size-in-all-the-elements-of-
figures

figure(5)
plot(pH, alpha); grid on;
xlabel('pH'); ylabel('\alpha');

figure(52) %(VAN HAL et al., 1995) vs new
expression
plot(pH, alpha, 'b','LineWidth',2); grid on; hold
on;
plot(pH, alpha2, 'r--','LineWidth',2);
legend('Old','New');
xlabel('pH'); ylabel('\alpha');

figure(53) % pH sensitivity(VAN HAL et al., 1995)
vs new expression
plot(pH_med, -1e3*diff(phio)./diff(pH),  'b-
.','LineWidth',2); grid on; hold on;
```

```
plot(pH, 1e3*2.3*phit.*alpha, 'r--
','LineWidth',2);
plot(pH, 1e3*2.3*phit.*alpha2,
'g','LineWidth',2);
legend('- d\phi_eo/dpH', '2.3\phi_t\alpha w/
B_int(VAN HAL, 1995)','2.3\phi_t\alpha w/
B_int(N_sil, N_nit)');
xlabel('pH'); ylabel('pH sensitivity [mV/pH]');
xlim([2 9]);
set(findall(gcf,'-
property','FontSize'),'FontSize',12); %troca
todas as fontes:
https://www.mathworks.com/matlabcentral/answers/2
23344-changing-font-size-in-all-the-elements-of-
figures

figure(54) %alpha (VAN HAL et al., 1995) vs new
expression
plot(pH_med, -
(1./(2.3.*phit)).*diff(phio)./diff(pH),  'b-
.','LineWidth',2); grid on; hold on;
plot(pH, alpha, 'r--','LineWidth',2);
plot(pH, alpha2, 'g','LineWidth',2);
legend('- d\phi_eo/dpH', 'w/ B_int(VAN HAL,
1995)','w/ B_int(N_sil, N_nit)');
xlabel('pH'); ylabel('\alpha');
xlim([2 9]);
set(findall(gcf,'-
property','FontSize'),'FontSize',12); %troca
todas as fontes:
https://www.mathworks.com/matlabcentral/answers/2
23344-changing-font-size-in-all-the-elements-of-
figures


figure(7) %(VAN HAL et al., 1995)
plot(pH, Bint); grid on;
xlabel('pH'); ylabel('\beta_int [grupos/m^2]');

figure(72) %(VAN HAL et al., 1995) vs new
expression
plot(pH, Bint, 'b','LineWidth',2); grid on; hold
on;
plot(pH, Bint2, 'r--','LineWidth',2);
legend('Old', 'New');
xlabel('pH'); ylabel('\beta_int [grupos/m^2]');

figure(8) %(VAN HAL et al., 1995)
plot(pH, -log10(Hs)); grid on;
xlabel('pHb'); ylabel('pHs');

figure(9) %GCS capacitances
plot(pH, Ceq,'r','LineWidth',2); grid on; hold on
plot(pH, Ch*ones(1, length(pH)),'g--
','LineWidth',2); hold on
plot(pH, Cgouy,'b-.','LineWidth',2);
legend ('C''_eq','C''_H','C''_G');
xlabel('pH'); ylabel('Capacitância por área
[F/m^2]');

figure(91) %GCS capacitances
plot(pH, Ceq,'r','LineWidth',2); grid on; hold on
plot(pH, Ch*ones(1, length(pH)),'g--
','LineWidth',2); hold on
plot(pH, Cgouy,'b-.','LineWidth',2);
legend ('C''_eq','C''_H','C''_G');
xlabel('pH'); ylabel('Capacitance per area
[pF/\mum^2]');
xlim([1 10]);
set(findall(gcf,'-
property','FontSize'),'FontSize',12); %troca
todas as fontes:
https://www.mathworks.com/matlabcentral/answers/2
23344-changing-font-size-in-all-the-elements-of-
figures
```

<u>FUNÇÃO V_pH_phio_phih:</u>

```
function F = V_pH_phio_phih (x) %phih = x(1),
phio = x(2)
%Calcula phih e phio.
global q T e0 er z k n0 xh ka kb kn Nsil Nnit
phit Hb

Ch = er*e0/xh; %Helmholtz capacitancie in xh
[F/m2]
Cgouy =
sqrt(2*er*e0*z^2*q^2*n0/(k*T)).*cosh(z*q*x(1)/(2*
k*T)); % Gouy-Chapman capacitance [F/m2]
Ceq = (1/Ch + 1/Cgouy).^-1; % Stern Capacitance
[F/m2]

sigma_d = -
sqrt(8*k*T*er*e0*n0).*sinh(z*q*x(1)/(2*k*T));%
sigma_o=-sigmadl diffuse layer charge density
[C/m2] eq 28 Bergveld 2003

Hs = Hb*exp(-x(2)/phit); %Hs is the concentration
of the protons at the insulator surface/Hb is in
the bulk electrolyte; (Massobrio, 1991)
sigma_o = (q*Nsil*((Hs)^2 - ka*kb)/((Hs)^2 +
ka*(Hs) + ka*kb) + q*Nnit*((Hs)/((Hs) + kn))); %
charge density of surface sites (Martinoia, 1991)

F =[x(2) + sigma_d/Ch - x(1); % pois phih = phio
- sigma_o(phih)/CH; eq 29 Bergveld 2003
    x(2) - sigma_o/Ceq]; %(Massobrio, 1992)
end
```

APPENDIX B - ISFET DC model implemented on Virtuoso

An ISFET model suitable for DC simulations was implemented in the software Virtuoso®, from Cadence, using the expressions proposed in this thesis. This section will describe the characteristics, code, parameters and DC simulation of the device.

Figure 38 shows the device symbol.

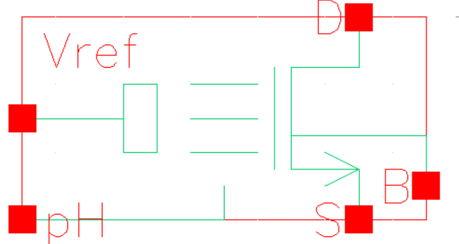


Figure 38 – n-ISFET model symbol.

The inputs/output pins are: the voltage applied to the electrode (*Vref*), the electrolyte pH (*pH*), the drain, bulk and source terminals (*D, B, S*) which are connected to DC voltage sources.

The model is composed of a non-modified MOSFET instance from the PDK (implemented in BSIM4), and a block connected to the gate terminal of the MOSFET (Figure 39). This block was written in Verilog-A language and models potentials due to electrode, passivation and electrolyte, as well as the capacitive attenuation due to capacitive divider formed by the passivation and the oxide/depletion capacitances, considering the ISFET threshold voltage expression proposed in this thesis.

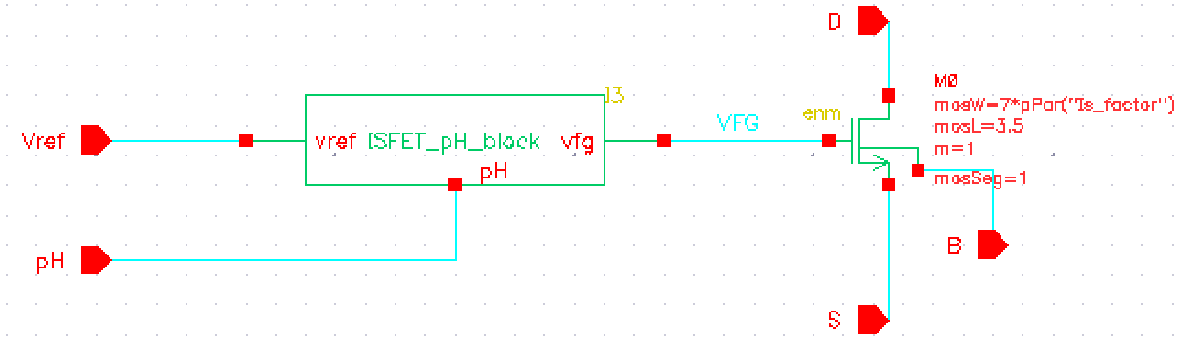


Figure 39 - ISFET model schematic on Virtuoso.

The Verilog-A code is presented in Figure 40.

```
// ISFET pH block - Rodrigo Wrege - 2022/06 LCI/UFSC
// veriloga based in the block generated from modelwriter "Voltage Amp":

`include "discipline.h"
`include "constants.h"

module pH_block (vref, vfg, pH);
  input vref, pH;
  output vfg;
  electrical vref, pH, vfg;
  parameter real CapDiv = 1;          // capacitive attenuation = Cpass/(Cpass+CoxCb/(Cox+Cb))
  parameter real Sens = 56m;          // pH sensitivity [V/pH]
  parameter real pHzc = 7;            // pH @ Point of Zero Charge
  parameter real Vtc = 0;             // Trapped Charges Offset [V]
  parameter real Eref = 4.63;         // Absolute ref. electrode potential [V]
  parameter real Xsol = 3m;           // Potential due to dipoles in the insulator interface [V]
  parameter real phi_lj = 1m;         // Liquid-Junction potential between electrode/solution [V]
  parameter real kt = 4.25;           // Technological parameter [V] (phi_al + Cox/Cpas(phi_poly-phisc-2|phif|)
  parameter real VtCop = 0;           // =(1+Cox/Cpas-1/cap_divider)*Vtmos [V]

  real Ychem = Eref + phi_lj + Xsol;

    analog begin
       V(vfg) <+  CapDiv * ( V(vref) - (Ychem - Sens*(pHzc-V(pH)) + Vtc - kt + VtCop));
    end
endmodule
```

Figure 40 - Verilog-A code of the wet interface block.

The electrolyte/insulator interface potential, ϕ_{eo}, was implemented using the simpler expression, given in eq. (18), resulting in an easier implementation and no need to solve multiple equations, speeding up the simulation.

The list of ISFET parameters to be entered by the user, its default values and descriptions are in Table 12. If the parameter value is not defined by user, the default value is used in the simulation. The parameters expressions will be presented in the next subsection.

Table 12 - User defined parameters of the ISFET DC model on Virtuoso.

Parameter	**Description**	**Default Value**	**Unit**
CapDiv	Capacitive attenuation	1	-
VtCop	Term related to the MOSFET threshold voltage	0	V
kt	Potential due to technological parameters	4.25	V
phi_lj	Liquid junction potential between electrode and solution	1m	V
Xsol	Potential due to dipoles in the insulator interface	3m	V
Eref	Absolute reference electrode potential	4.63	V
Vtc	Trapped charges offset	0	V
pHpzc	pH at the point of zero charge	7	-
Sens_V_pH	pH sensitivity	56m	V/pH
IS_factor	ISFET specific current attenuation from that of the MOSFET	1	-

SPECIFIC CURRENT MODELLING

According to ACM, the specific current is function of the transistor channel width *W*. Therefore, the ISFET specific current was modelled by multiplying the transistor *W* with *Is_factor*, given by:

$$I_{S_factor} = \frac{I_{SISF}}{I_S} = \frac{C_{pass} + \left(C_{ox}C_b\right)/\left(C_{ox} + C_b\right)}{C_{pass} + C_{ox}} \quad (71)$$

Multiply *W* by *Is_factor* allows to change the specific current of the MOSFET without the need to modify any PDK files. In another hand, changing the transistor channel width affects parameters of the BSIM model of the MOSFET related to *W*. Other option would be to apply *Is_factor* in another BSIM parameter, such as electron mobility, which would require edit the MOSFET PDK files containing the BSIM parameters.

FLOATING GATE VOLTAGE

The Verilog-A block generates the ISFET floating gate voltage, which is connected to the gate of the MOSFET. Next paragraphs present the equations implemented on this block and the definition of this block user defined parameters.

In the proposed model (Figure 39), the specific current of the MOSFET is adjusted to be the same as that of the ISFET, using the parameter *Is_factor*. In addition to that, the MOSFET has the same bulk and source terminals as the ISFET. In this case, according to UICM, both ISFET and MOSFET will have the same pinch-off voltages:

$$\frac{V_{REF} - V_{TISF}}{n_{isf}} = \frac{V_{FG} - V_{Tmos}}{n_{mos}} \quad (72)$$

Therefore, the floating gate voltage V_{FG} can be written as:

$$V_{FG} = \frac{n_{mos}}{n_{isf}}\left(V_{REF} - V_{TISF}\right) + V_{Tmos} \quad (73)$$

Substituting V_{TISF} for eq. (28) and considering $n_{mos}/n_{isf} = \alpha_{att}$:

$$V_{FG} = \alpha_{att}\left(V_{REF} - \left(1 + \frac{C_{ox}}{C_{pass}} - \frac{1}{\alpha_{att}}\right)V_{Tmos} - V_{chem} - V_{tc} + \kappa_T\right) \quad (74)$$

The block written in Verilog-A implements this equation. The expressions for the user defined parameters are presented next.

CapDiv is obtained according to the capacitive divider formed by the passivation and the MOSFET capacitances:

$$CapDiv = \alpha_{att} = \frac{n_{mos}}{n_{isf}} = \frac{C_{pass}}{C_{pass} + \left(C_{ox}C_b\right)/\left(C_{ox} + C_b\right)} \quad (75)$$

VtCop parameter is obtained according to:

$$VtCop = \left(1 + \frac{C_{ox}}{C_{pass}} - \frac{1}{CapDiv}\right)V_{Tmos} \quad (76)$$

The parameters *phi_lj*, *Xsol*, *Eref*, *pHpzc*, are used to obtain the voltage V_{chem}, given in eq. (29). The term ϕ_{eo} was implemented using the simpler expression, given in eq. (18).

Sens_V_pH is given by:

$$Sens_V_pH = 2.3\phi_t\alpha \quad (77)$$

ISFET DC SIMULATION ON THE VIRTUOSO SOFTWARE

Figure 41 shows the testbench applied to the modeled n-ISFET for the g_m/I_D characterization. For this testbench, it was used the ONSEMI 0.35 µm PDK, with the electrical parameters listed on Table 5.

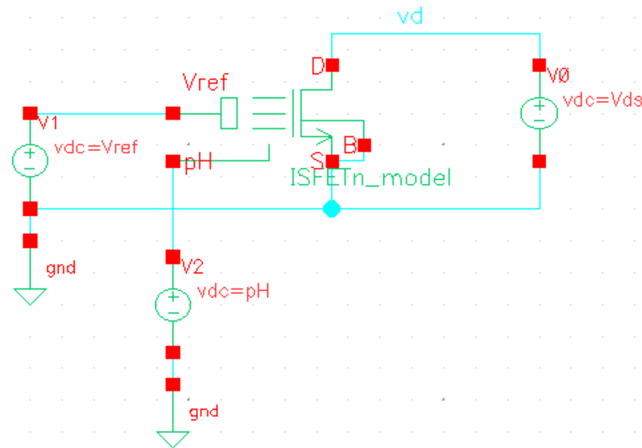


Figure 41 – Testbench schematic applied to the n-ISFET for the g_m/I_D characterization.

MOSFET vs ISFET I-V curves

Figure 42 shows a comparation of g_m/I_D *vs* V_{REF} and I_D *vs* V_{REF} of an n-ISFET and a n-MOSFET with $W = 7\ \mu m$ and $L = 3.5\ \mu m$ for V_{DS} = 13 mV and V_{REF} varying from -1 to 3.3 V. V_{REF} is the voltage applied to the ISFET electrode and to the MOSFET gate terminal. All ISFET parameters are the default values from Table 12, with exception of: *CapDiv* = 0.875, *VtCop* = 0.2 V, I_{S_factor} = 0.76, and *Sens_V_pH* = 45m. The ISFET was simulated in a solution with pH = pH_{pzc} = 7.

As expected, there is an attenuation in the g_m/I_D peak of the ISFET compared to that of the MOSFET due to the higher ISFET slope factor, and also a shift in the ISFET threshold voltage caused by potentials of electrolyte/insulator interface and capacitive attenuation. Table 13 shows the n-MOSFET and n-ISFET simulation results. The ISFET result is in accordance with the theoretical parameters values.

Table 13 - MOSFET vs ISFET simulated parameters using g_m/I_D extraction

Parameter	n-MOSFET Simulated	n-ISFET (@pH=pH_{pzc}) Simulated	n-ISFET (@pH=pH_{pzc}) Calculated
Slope factor	1.35	1.54	1.58
Threshold Voltage (V)	0.557	1.22	1.22
Specific Current (nA)	153	115	116

Figure 42 – DC simulation: n-ISFET @ pH = pH_{pzc} vs n-MOSFET.

<u>ISFET I-V curves varying electrolyte pH</u>

Figure 43 shows simulation results of the ISFET g_m/I_D *vs* V_{REF} and I_D *vs* V_{REF} for pH ranging from 1 to 10:

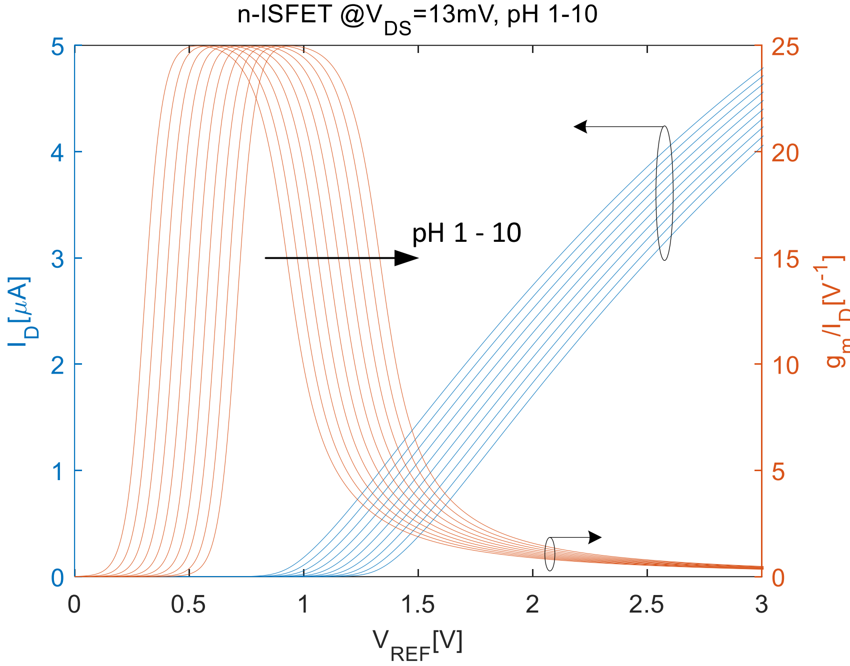


Figure 43 – n-ISFET simulation results of g_m/I_D vs V_{REF} and I_D vs V_{REF} for pH from 1 to 10.

It is possible to observe a shift in the I_D *vs* V_{REF} curve of the order of 45 mV for each unit of pH variation which is a result of the simulated 45 mV/pH sensitivity set by the parameter "*Sens_V_pH*". Figure 44a shows the ISFET threshold voltage, V_{TISF}, extracted using the g_m/I_D methodology, with the V_{TISF} values for pH 4 and 5 indicated, resulting in a 45 mV/pH shift, as expected for the nominal pH sensitivity. Figure 44b shows the floating gate voltage, V_{FG}, in respect to the electrode potential V_{REF}. As expected, V_{FG} is attenuated compared to V_{REF}, due to the effect of the capacitive attenuation set by the "*CapDiv*" parameter, and is also affected by the electrochemical potentials.

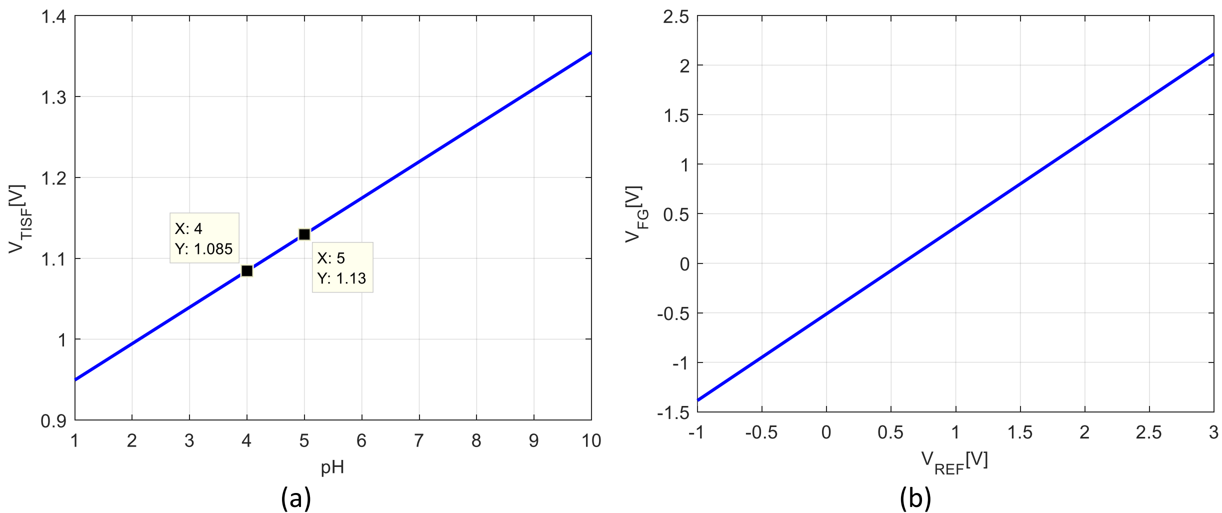


Figure 44 – n-ISFET simulation: (a): V_{TISF} vs pH, and (b) V_{FG} vs V_{REF} @pH = pH_{pzc}.

ISFET I-V curves for different trapped charge offsets V_{tc}

Figure 45 shows the n-ISFET simulation curves for trapped charge offsets (V_{tc}) of -1.5 V, 0 V and +1.5 V with pH = pH_{pzc}. As expected, there is a shift in the I-V curves with the same magnitude as V_{tc}, resulting in threshold voltages of -0.28, 1.22 and 2.72 V, respectively (Figure 46).

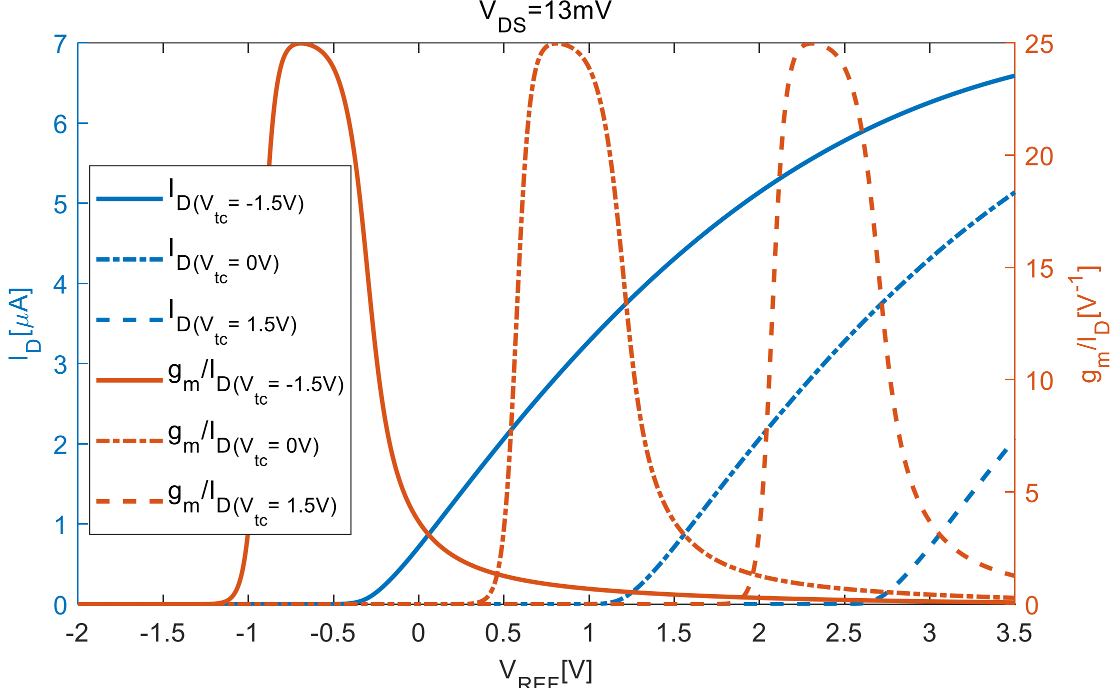


Figure 45 - ISFET g_m/I_D vs V_{REF} and I_D vs V_{REF} for different V_{tc} @pH = pH_{pzc}.

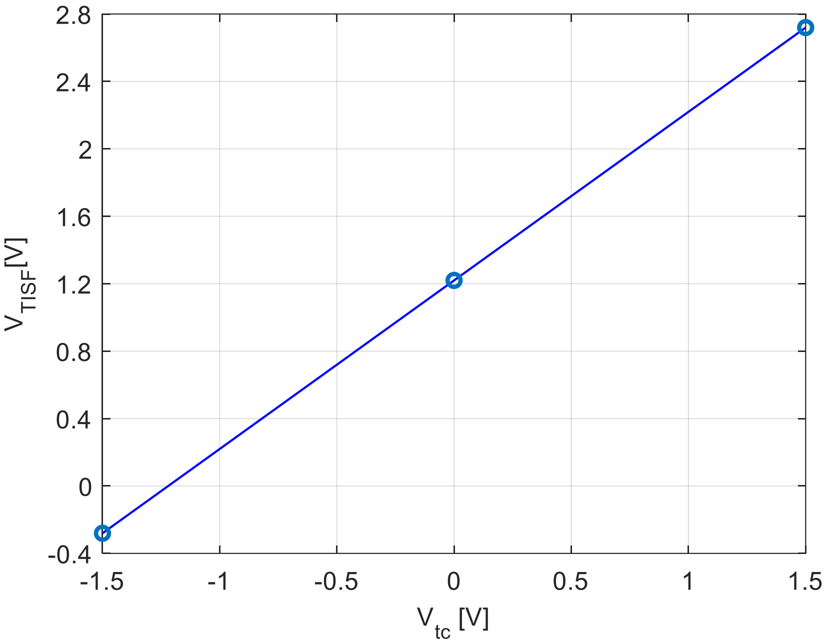


Figure 46 - ISFET threshold voltage for different V_{tc} @pH = pH$_{pzc}$.

ISFET floating gate voltage readout

The circuit shown in Figure 47 makes a copy of the ISFET drain current to the drain of a saturated MOSFET with same W and L as those of the ISFET. This results in an output voltage close to that of the floating gate of the ISFET, allowing an indirect reading of the ISFET floating gate voltage.

In this circuit, all bulk of the n-MOSFETs are connected to ground, and all bulk of the p-MOSFETs are connected do V_{DD}. The ISFET source voltage (V_S) is set by the virtual short-circuit between the inputs of the OPAMP, which sets the ISFET electrode voltage. A p-MOS current mirror, formed by M_3 and M_4, makes a copy of the ISFET drain current into a diode connected n-MOSFET (M_5) with the same dimensions as the one used in the ISFET project. The floating gate voltage is than read as the gate voltage of the n-MOSFET (V_{OUT}).

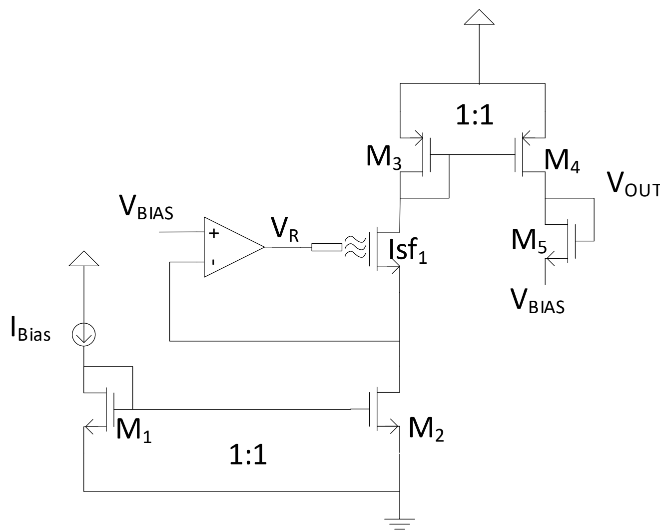


Figure 47 – ISFET floating gate readout.

In this simulation, all MOSFETs have $W = 7$ µm and $L = 3.5$ µm, $V_{DD} = 3.3$ V, $I_{BIAS} = 450$ nA and with $V_{BIAS} = 0.5$ V. An Ideal OPAMP described in Verilog-A language and generated using the *modelwriter* tool from Cadence with the following specs: *Gain* = 120 dB, *pole_freq* = 1.2 Hz, *rin* = 12 MΩ, *rout* = 75 Ω, *slew rate* = ±20 MV/s, V_{Osat} = 0.5 V and 2.7 V was used for the simulations. An electrolyte with pH = pH_{pzc} = 7 was considered.

As expected, in Figure 48 the voltage at the gate of the MOSFET (V_{OUT}) is very close to that at the floating gate of the ISFET (V_{FG}).

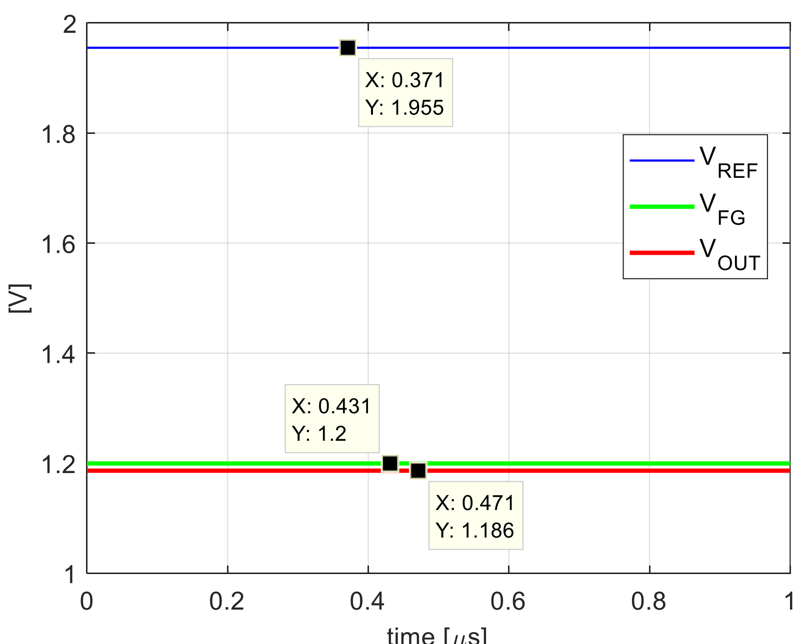
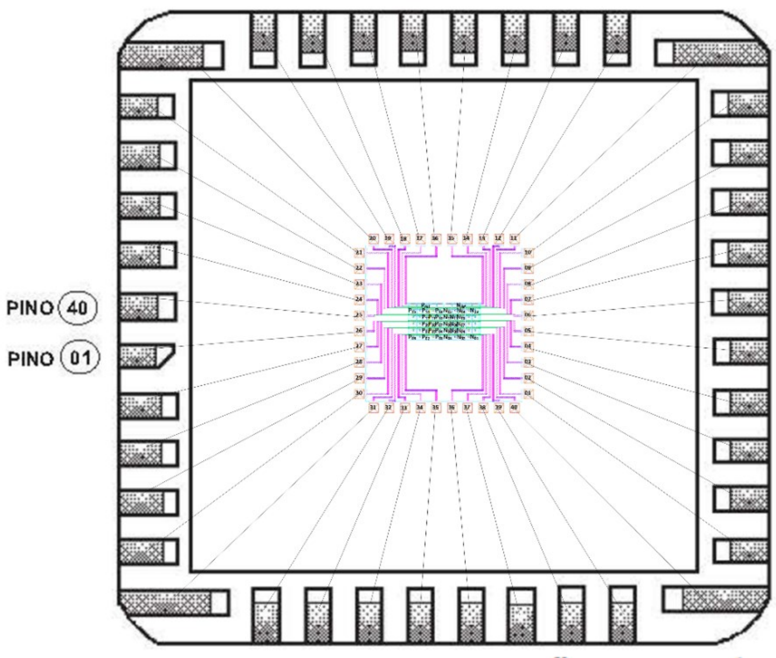


Figure 48 - ISFET floating gate readout simulation.

APPENDIX C - Chip Silterra: pin mapping



Cavity Size: 7.87mm x 7.87 mm
Die Size: 2.28mm x 2.28mm

20 1
TOP VIEW
21 40

PIN DIP40	*PAD*	Description	*PIN DIP40*	*PAD*	Description
16	01	Drain n-ISFET N_{05}	36	21	Drain p-ISFET P_{14}
17	02	Drain n-ISFET N_{06}	37	22	Drain p-ISFET P_{13}
18	03	Drain n-ISFET N_{07}	38	23	Drain p-ISFET P_{12}
19	04	Drain n-ISFET N_{08}	39	24	Drain p-ISFET P_{11}
20	05	Drain n-ISFET N_{09}	40	25	Drain p-ISFET P_{10}
21	06	Drain n-ISFET N_{10}	1	26	Drain p-ISFET P_{09}
22	07	Drain n-ISFET N_{11}	2	27	Drain p-ISFET P_{08}
23	08	Drain n-ISFET N_{12}	3	28	Drain p-ISFET P_{07}
24	09	Drain n-ISFET N_{13}	4	29	Drain p-ISFET P_{06}
25	10	Drain n-ISFET N_{14}	5	30	Drain p-ISFET P_{05}
26	11	Drain n-ISFET N_{15}	6	31	Drain p-ISFET P_{04}
27	12	Drain n-MOS N_{ref}	7	32	Drain p-ISFET P_{03}
28	13	Gate n-MOS N_{ref}	8	33	Drain p-ISFET P_{02}
29	14	Source n-MOS N_{ref}	9	34	Drain p-ISFET P_{01}
30	15	Bulk n-ISFETs and n-MOS	10	35	Source p-ISFETs
31	16	Bulk p-ISFETs and p-MOS	11	36	Source n-ISFETs
32	17	Source p-MOS P_{ref}	12	37	Drain n-ISFET N_{01}
33	18	Gate p-MOS P_{ref}	13	38	Drain n-ISFET N_{02}
34	19	Drain p-MOS P_{ref}	14	39	Drain n-ISFET N_{03}
35	20	Drain p-ISFET P_{15}	15	40	Drain n-ISFET N_{04}

APPENDIX D - Chip Silterra: x-ray verification

We received 40 chips from the SilTerra foundry, number 1 to 40. The epoxy chamber developed by the ITT Chip was successfully applied in 12 chips (numbered as 03, 04, 05, 07, 08, 10, 11, 14, 15, 16, 17 and 18). Six chips were completely covered (01, 02, 06, 09, 12 and 13) and other seven (19-25) did not have any epoxy applied, so these chips are not analyzed here. Table 14 presents X-ray images provided by ITT Chip of the 12 chips with a functional epoxy chamber. These images were used for a visual inspection of the bonding wires connections after the epoxy chamber deposition.

Table 14 – X-ray images of chips with epoxy chamber.

Sample	Epoxy deposition	X-Ray	Defects
CHIP03			ok
CHIP04			ok
CHIP05			ok

Sample	Epoxy deposition	X-Ray	Defects
CHIP07			Open circuit on PIN10 and PIN11. Some epoxy on n-ISFET 01, 13 and p-ISFET 15.
CHIP08			ok
CHIP10			ok
CHIP11			Some epoxy on n-ISFET 01 and p-ISFET 03.
CHIP14			Open circuit on PIN30.

Sample	Epoxy deposition	X-Ray	Defects
CHIP15			ok
CHIP16			Open circuit on PIN11.
CHIP17			Some epoxy on p-ISFET 03. p-n junction test: n and p arrays bad.
CHIP18			Open circuit on PIN5, 6 and 34.

APPENDIX E - Chip Onsemi: PADs connectivity

Figure 49 shows the die of the chip Onsemi with the PADS numbered and Table 15 presents the description of the numbered PADS. Only ISFET sensors and MOSFETs are considered. Fields with "-" are for devices not used in this thesis.

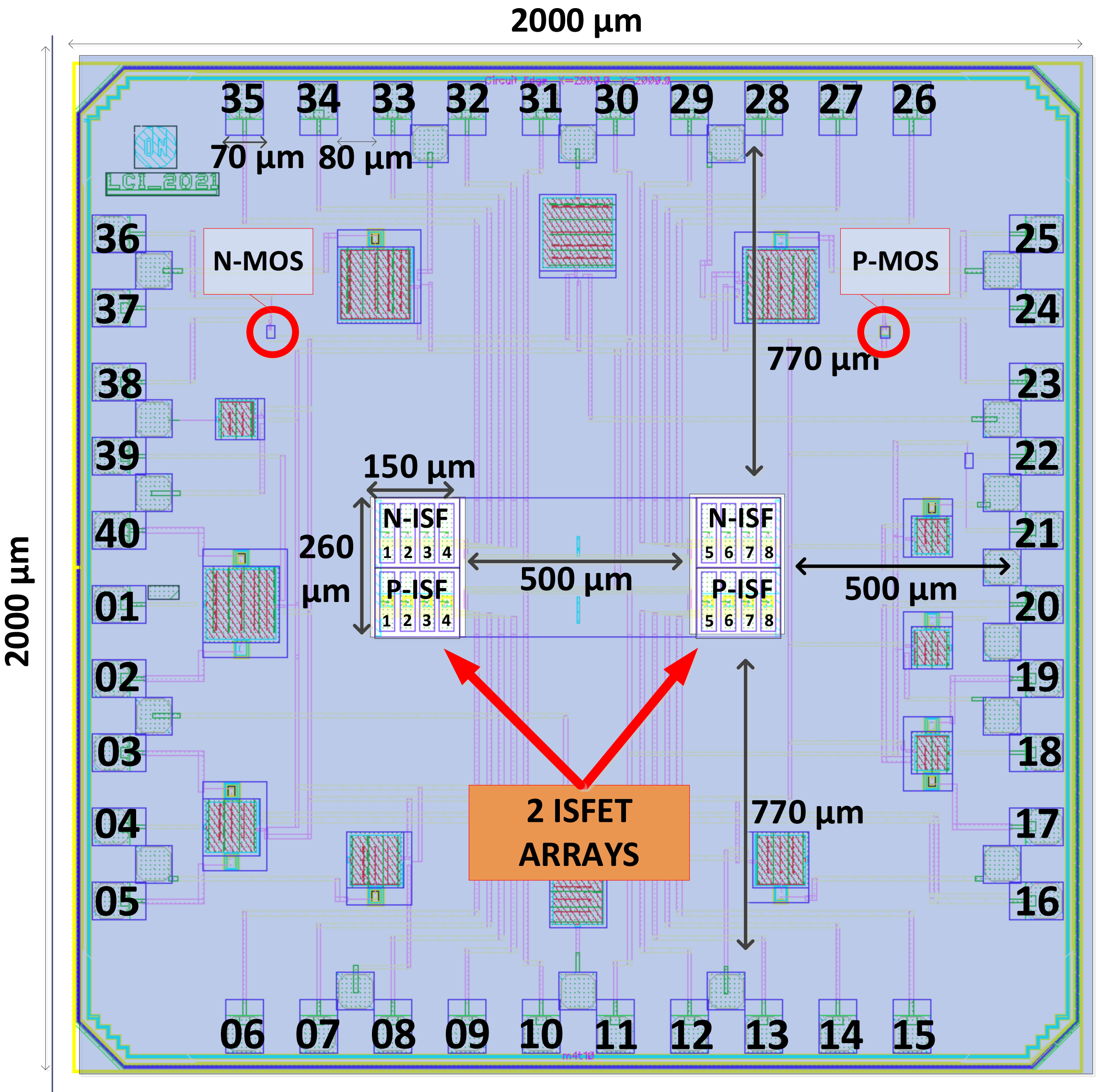


Figure 49 - Die of the chip Onsemi.

Table 15 – PADs connectivity of the Chip ONSEMI.

PAD	Description	PAD	Description
01	-	21	-
02	-	22	-
03	-	23	Source P-MOS
04	-	24	Gate P-MOS
05	-	25	Drain P-MOS
06	Drain P-ISFET01	26	Drain N-ISFET08
07	Drain P-ISFET02	27	Drain N-ISFET07
08	Drain P-ISFET03	28	Drain N-ISFET06
09	Drain P-ISFET04	29	Drain N-ISFET05
10	Source P-ISFETs	30	BULK N
11	BULK P	31	Source N-ISFETs
12	Drain P-ISFET05	32	Drain N-ISFET04
13	Drain P-ISFET06	33	Drain N-ISFET03
14	Drain P-ISFET07	34	Drain N-ISFET02
15	Drain P-ISFET08	35	Drain N-ISFET01
16	-	36	Drain N-MOS
17	-	37	Gate N-MOS
18	-	38	Source N-MOS
19	-	39	-
20	-	40	-

APPENDIX F - Gold metallization with sputtering for dry test

This appendix describes the mains steps and approaches used to create a metallization for the dry test of ISFETs. Our first attempt to create an electrical contact above passivation was performed gluing a connector direct to the passivation using only a conductive silver paste (with the help of LFFS – Laboratório de Filmes Finos, coordinate by professor PhD André Pasa). This method did not create a proper electrical contact and devices did not work in the chip of this first experience (Chip 15).

So, in order to create the electrical contact above the passivation, gold was applied using the sputtering technique. For more practicality during the tests, an external connector was attached to the gold layer using silver paste. It was performed in LAMATE/UFSC – Laboratório de Materiais Elétricos – with the supervision and advices of professor PhD Carlos Rambo in October of 2019. The chips were prepared by Rodrigo Wrege, and sputtering/silver paste deposition processes were performed by the Master Degree student Bruno Neckel Wesling. The summary of the main steps of the process are described above.

Step1 – Mechanical mask application.

A mask was made to permit the implementation of the gold only in the region of interest (the area where ISFETs are implemented, in the center of the chamber). This mask was done using a double-sided tape (due its thickness) with a hole made in the center using a paper punch. The chip was kept in an anti-static foam and all the rest of the surface (package and foam) was protected with a crepe tape (Figure 50).

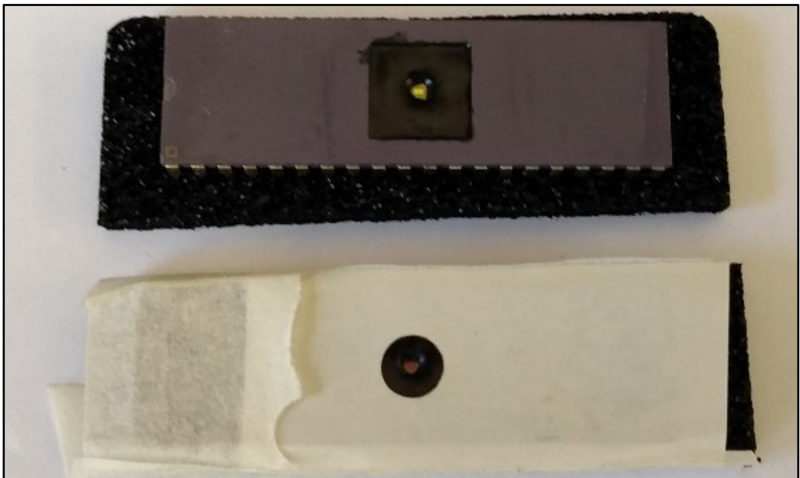


Figure 50 - A chip before and another chip after the mask application.

Step 2 – Sputtering process.

After the mask preparation, the chip went to the sputtering chamber (Figure 51). The Au sputtering was performed with a SPI-Module Sputter Coater with the parameters given in Table 16, forming an estimated Au layer thickness of 40 nm, according to the following equation, informed in the equipment instruction manual [90]:

$$d_{SP} = K_{SP} I_{SP} V_{SP} t_{SP} \tag{78}$$

where d_{SP} is the film thickness in angstrom, K_{SP} is 0.17 for gold used with argon (Ar), I_{SP} is the plasma current in mA, V_{SP} is the inter-electrode voltage in kV and t_{SP} is the sputtering time in seconds.

(a)

(b)

Figure 51 - (a) Sputtering process. (b) Details of the chip on the chamber.

During the process, the sputtering chamber is evacuated, and low-pressure Ar is inserted. The source material (Au) and the substrate (the chip in this case) are placed in parallel plates. With an inter-electrode high voltage occurs the gas ionization, forming the plasma between plates. The Ar^+ ions go in direction of the negative plate, which contains Au. The impact of these ions cause neutral Au atoms to be ejected to the substrate (the chip) forming the Au film [85].

Table 16 - Deposition parameters for Au

Parameter	Value
Sputter target	Au
Substrate temperature	25°C
Deposition time	120 s
Target to substrate distance	5 cm
Cathode voltage	-1000 V
Cathode current	20 mA

Step 3 –Mask removal.

After the process was finished, the entire surface was covered with gold (mask and chamber). Removing the mask, only the ISFETs area and some of the epoxy was covered with gold (Figure 52).

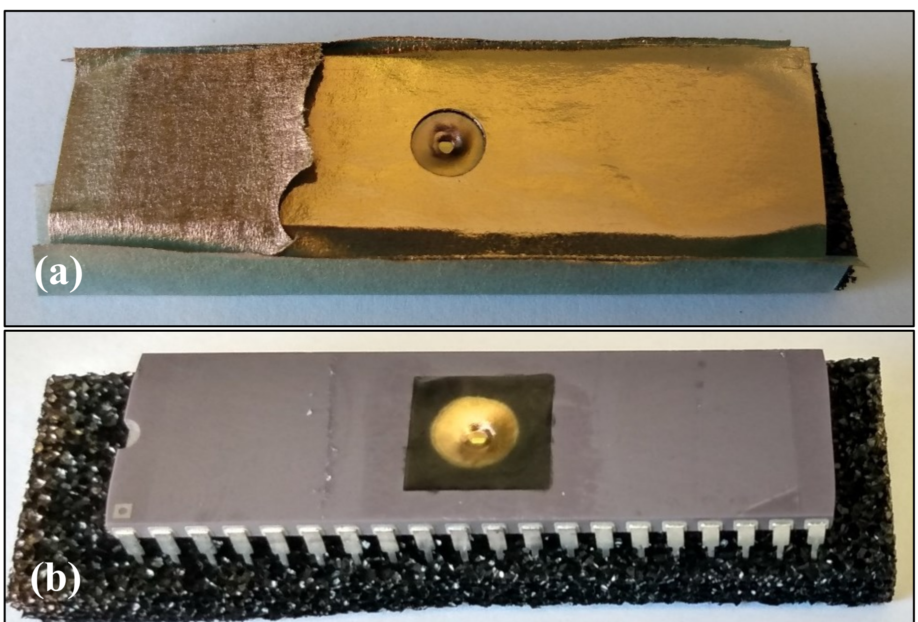


Figure 52 - Chip (a) before and (b) after the removing of the mask.

Step 4 – External connector application.

To make the electrical characterization of the devices more practical, an external connector was glued to the gold layer using a conductive silver paste (Electrolube SCP003). First, the connector was placed near the gold layer and hold with a tape (Figure 53).

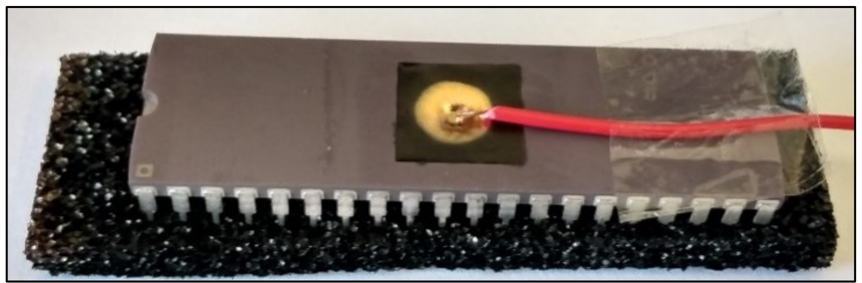


Figure 53 - Connector placed for conductive paste application.

Then, the silver paste was applied with a pipette (Eppendorf Research plus) in the region where the gold was deposited (the chamber) connecting the connector with the gold layer (Figure 54).

Figure 54 - Silver paste application.

A glue (Loctite Super Bonder) was applied between the connector and the DIP40 package, making it more resistant to manipulations (Figure 55).

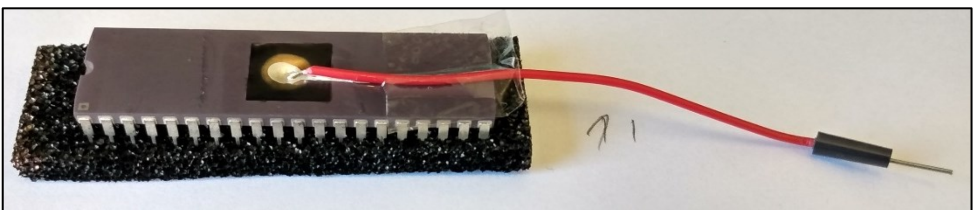


Figure 55 - Chip final assembly after metallization.

APPENDIX G - Chip SilTerra: results of the dry parameters extraction.

This appendix shows results of the dry characterization of 4 metallized chips performed by analyzing I_D *vs* V_{REF} and g_m/I_D *vs* V_{REF} curves according to the g_m/I_D methodology presented in [52].

Table 17 – CHIP11: ISFETs dry characterization using the method g_m/I_D (08/11/2019 at room temperature).

n-Array					p-Array				
Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	*n @WI*	Sample	$(g_m/I_D)_{max}$	V_T (mV)	I_S (nA)	*n @WI*
N01	10.18	1.925	118.125	3.778	P01	-	-	-	-
N02	11.16	3.75	205.909	3.446	P02	13.15	-1175	34.716	2.925
N03	11.03	3.65	197.852	3.487	P03	-	-	-	-
N04	14.7	3.25	231.943	2.616	P04	15.57	-750	62.330	2.470
N05	14.84	3.275	234.716	2.592	P05	15.93	-750	73.159	2.414
N06	14.14	3.325	231.341	2.720	P06	16.03	-680	62.500	2.399
N07	15.5	3.325	220.636	2.481	P07	16.26	-200	74.239	2.365
N08	15.98	3.15	206.784	2.407	P08	16.72	75	84.091	2.300
N09	14.75	3.25	234.068	2.608	P09	-	-	-	-
N10	14.93	3.375	291.011	2.576	P10	-	-	-	-
N11	14.54	3.325	266.886	2.645	P11	16.52	75	80.761	2.328
N12	14.56	3.3	215.443	2.642	P12	16.25	-175	76.705	2.367
N13	10.37	3.95	175.443	3.709	P13	14.18	-625	31.216	2.712
N14	12.04	3.6	196.761	3.194	P14	16.25	-25	67.523	2.367
N15	10.98	3.725	194.967	3.503	P15	13	-775	13.909	2.959

*data with “-“: device did not work properly.

Table 18 - Samples mean and standard deviation.

CHIP11: method g_m/I_D				
Parameter	n-ISFETs		p-ISFETs	
	Mean	Standard Deviation	Mean	Standard Deviation
V_T (V)	3.446	0.241	-0.455	0.421
I_S (nA)	221.697	30.285 (14%)	60.104	23.080 (38%)
n @WI	2.902	0.455	2.510	0.240

Device N01 is covered with epoxy and was not considered for mean and standard deviation estimation.

Table 19 – CHIP05: ISFETs dry characterization using the method g_m/I_D (08/11/2019 at room temperature).

n-Array					p-Array				
Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	n @WI	Sample	$(g_m/I_D)_{max}$	V_T (mV)	I_S (nA)	n @WI
N01	9.53	2.55	165.55	4.036	P01	11	750	30.67	3.497
N02	8.42	4.85	248.659	4.568	P02	11.86	950	54.886	3.243
N03	8.1	4.925	271.22	4.748	P03	15.38	725	63.705	2.501
N04	12.03	4.175	214.477	3.197	P04	13.72	900	55.818	2.803
N05	12.01	4.1	237.136	3.202	P05	13.56	1125	85.580	2.836
N06	13.49	1.625	235.841	2.851	P06	18.93	1500	61.761	2.032
N07	12.78	4.075	224.648	3.010	P07	15.06	1200	84.091	2.554
N08	12.58	4.15	264.227	3.057	P08	17.2	1370	64.773	2.236
N09	11.66	4.35	278.750	3.299	P09	17.5	-1290	90.909	2.198
N10	-	-	-	-	P10	12.62	1300	101.273	3.048
N11	12.41	4.175	266.45	3.099	P11	19.2	-1250	66.523	2.003
N12	15.33	1.35	219.955	2.509	P12	-	-	-	-
N13	8	4.975	256.667	4.808	P13	12.82	850	50.170	3.000
N14	9.5	4.5	216.636	4.049	P14	13.76	1225	84.284	2.795
N15	-	-	-	-	P15	14.78	1150	61.602	2.602

*data with "-": device did not work properly.

Table 20 - Samples mean and standard deviation.

CHIP05: method g_m/I_D				
Parameter	n-ISFETs		p-ISFETs	
	Mean	Standard Deviation	Mean	Standard Deviation
V_T (V)	3.831	1.204	0.750	0.886
I_S (nA)	238.478	30.942 (13%)	68.289	18.824 (28%)
n @WI	3.572	0.772	2.668	0.450

Table 21 – CHIP03: ISFETs dry characterization using the method g_m/I_D (11/12/2019 at room temperature).

n-Array					p-Array				
Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	*n @WI*	Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	*n @WI*
N01	10	0.355	103.648	3.846	P01	10	-4.545	23.068	3.846
N02	11	0.185	173.068	3.497	P02	10.5	-4.445	20.909	3.663
N03	10.5	0.24	168.557	3.663	P03	9	-4.83	21.591	4.274
N04	14.6	-0.33	170.705	2.634	P04	13.2	-4.13	56.818	2.914
N05	13.86	-0.29	208.636	2.775	P05	13.7	-3.985	65.568	2.807
N06	13.2	-0.225	190.114	2.914	P06	13.8	-4.05	69.773	2.787
N07	14.62	-0.39	215.955	2.631	P07	14.1	-4.065	55.455	2.728
N08	14.07	-0.385	215.341	2.734	P08	14.4	-3.995	66.057	2.671
N09	12.9	-0.305	221.080	2.982	P09	15	-3.98	74.545	2.564
N10	12.6	-0.265	227.102	3.053	P10	-	-	-	-
N11	12.56	-0.205	226.830	3.062	P11	12.8	-3.475	81.250	3.005
N12	12.4	-0.125	181.818	3.102	P12	-	-	-	-
N13	-	-	-	-	P13	12	-2.41	20.114	3.205
N14	-	-	-	-	P14	11.9	-4.385	28.580	3.232
N15	-	-	-	-	P15	9.3	-5.5	27.045	4.136

*data with "-": device did not work properly.

Table 22 - Samples mean and standard deviation.

CHIP03: method g_m/I_D				
Parameter	n-ISFETs		p-ISFETs	
	Mean	Standard Deviation	Mean	Standard Deviation
V_T (V)	-0.145	0.258	-4.138	0.717
I_S (nA)	191.904	35.626 (19%)	46.983	23.604 (50%)
n @WI	3.074	0.399	3.218	0.578

Table 23 – CHIP16: ISFETs dry characterization using the method g_m/I_D (30/01/2020 at room temperature).

n-Array					p-Array				
Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	n @WI	Sample	$(g_m/I_D)_{max}$	V_T (V)	I_S (nA)	n @WI
N01	8.7	-4.34	210.227	4.421	P01	-	-	-	-
N02	-	-	-	-	P02	8.7	-2.14	11.818	4.421
N03	9.6	-4.795	209.091	4.006	P03	-	-	-	-
N04	9.2	-5.025	148.864	4.181	P04	10	-10.6	23.409	3.846
N05	10	-4.78	110.227	3.846	P05	10.8	-6.56	27.568	3.561
N06	9.7	-4.68	125.000	3.965	P06	10.75	-10.57	58.443	3.578
N07	-	-	-	-	P07	11	-10.61	56.818	3.497
N08	10.6	-4.88	142.045	3.628	P08	12.38	-10.68	56.250	3.107
N09	9.4	-4.93	143.182	4.092	P09	-	-	-	-
N10	9.93	-4.97	109.318	3.873	P10	-	-	-	-
N11	9.6	-4.78	109.091	4.006	P11	-	-	-	-
N12	8.9	-4.71	127.273	4.322	P12	12	-10.54	53.409	3.205
N13	8.5	-3.94	242.045	4.525	P13	-	-	-	-
N14	8.4	-4.47	130.682	4.579	P14	9.15	-10.77	44.545	4.203
N15	8.4	-4.24	121.193	4.579	P15	7.7	-10.97	40.909	4.995

*data with "-": device did not work properly.

Table 24 - Samples mean and standard deviation.

CHIP16: method g_m/I_D				
Parameter	n-ISFETs		p-ISFETs	
	Mean	Standard Deviation	Mean	Standard Deviation
V_T (V)	-4.657	0.321	-9.271	3.004
I_S (nA)	148.326	43.705(29%)	41.463	16.930 (40%)
n @WI	4.156	0.307	3.824	0.613

APPENDIX H - Discrete readout circuit project for wet tests

Considering the following circuit:

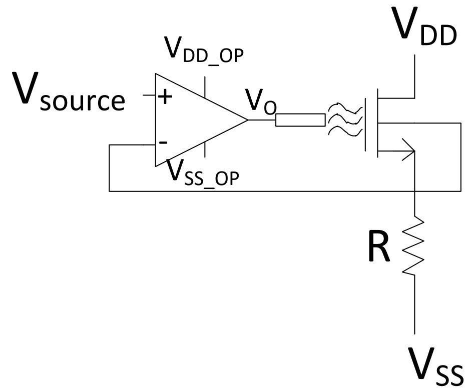


Figure 56 - Readout circuit for n-ISFET.

For an n-ISFET with specific current I_S = 200 nA, working in the saturation region and for a moderate inversion level of i_f= 40, the drain current is obtained by:

$$I_D = I_S(i_f) \quad (79)$$

Resulting in $\boldsymbol{I_D}$ **= 8 µA**. The resistor value R is given by:

$$R = \frac{V_{source} - V_{SS}}{I_D} \quad (80)$$

For $\boldsymbol{V_{DD}}$ **= -**$\boldsymbol{V_{SS}}$ **= 2.5 V** and $\boldsymbol{V_{source}}$ **= 0 V**, results in **R = 300 kΩ** (considering the closest commercial value).

The minimum V_{DS} to maintain the device in saturation is given by:

$$V_{DS_sat} = \phi_t(\sqrt{1+i_f} + 3) \quad (81)$$

Which results in V_{DS_sat} = 0.222 V. The maximum V_{DS} supported by the device is 5 V (V_{DS_MAX} =5 V). Since $V_{DS} = V_{DD} - V_{source}$, V_{DD}-$V_{DS_MAX} < V_{source} < V_{DD}$-$V_{DS_sat}$, resulting in **-2.5 < V_{source} < 2.27 V**. Considering the UICM extended to the ISFET:

$$\frac{V_{REF} - V_{TISF}}{n_{ISF}} - V_{SB} = \phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right] \quad (82)$$

where V_{REF} is the reference electrode voltage referred to bulk and V_{TISF} is the ISFET threshold voltage. Since V_{SB} = 0 V, the output voltage Vo will follow changes in V_{TISF} according to:

$$V_O = V_{REF} + V_{source} = V_{TISF} + n_{ISF}\phi_t \left[\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1 \right) \right] + V_{source} \quad (83)$$

The chosen OPAMP supply voltage is ±15 V in order to reach a large range of threshold voltage values. Table 25 summarizes the components values.

Table 25 – Discrete readout circuit components values.

Component	Value
OPAMP	TL072
R	300 kΩ
V_{DD}/V_{SS}	2.5/-2.5 V
V_{DD_OP}/V_{SS_OP}	15/-15 V
V_{source}	0 V

Simulation Result:

Simulation was performed in LTSPICE, using an ideal AMPOP from LTSPICE and the ISFET model implemented in spice with the following parameters: I_S = 250 nA, n_{ISF} = 3.1, and V_{TISF} = *1 + 0.044pH* (Figure 57a)

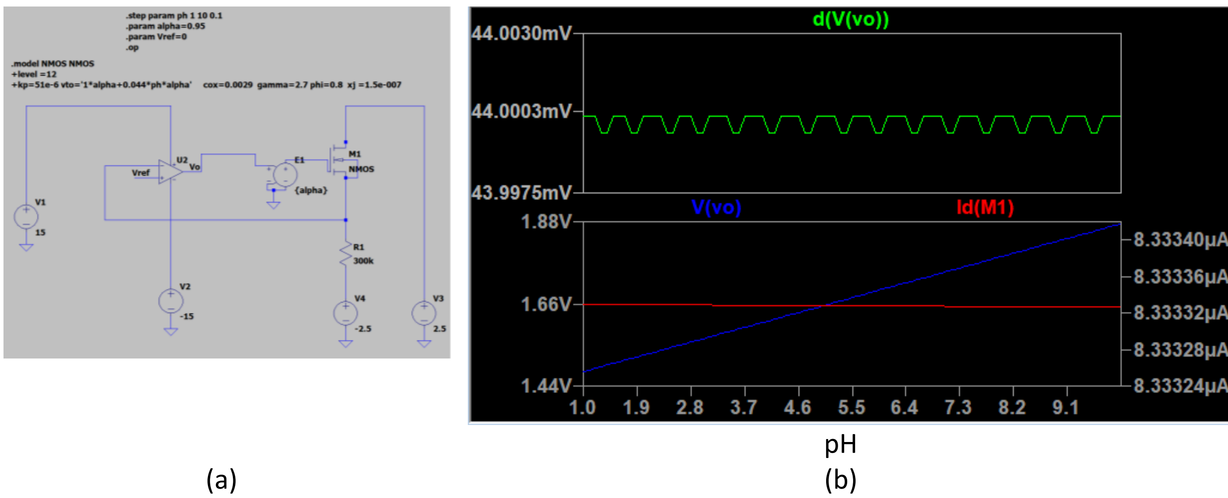


Figure 57 – LTSPICE simulation: (a) circuit schematic, and (b) result.

From Figure 57b is possible to observe that the current *Id* (red) is close to the projected value. The difference occurs because the commercial value used for the resistor is not the exact value obtained from the mathematical expression. The output voltage *Vo* (blue) changes according to pH with a sensitivity *dVo/dpH* (green) in order of 44 mV/pH, which is the sensitivity modeled for the ISFET in this case. For the simulated n-ISFET, the inversion level is $i_f = I_D/I_S = 33$, resulting in an output voltage at pH 7 of $V_{O@pH7} = 1 + 0.044*7 + 3.1\phi_t\left[\sqrt{1+33} - 2 + \ln\left(\sqrt{1+33} - 1\right)\right] = 1.74V$, which is in accordance with the simulation.

PCB implementation:

The PCB was designed in ARES/PROTEUS 7.7 by Rodrigo Wrege and implemented in Laboratório de Prototipagem/Fiocruz-PR (with contributions of Dr. Lucas Blanes, Mateus Stracke, Viviane Klassen De Oliveira and Geovani Mendonça). The chip was connected according to the following schematic.

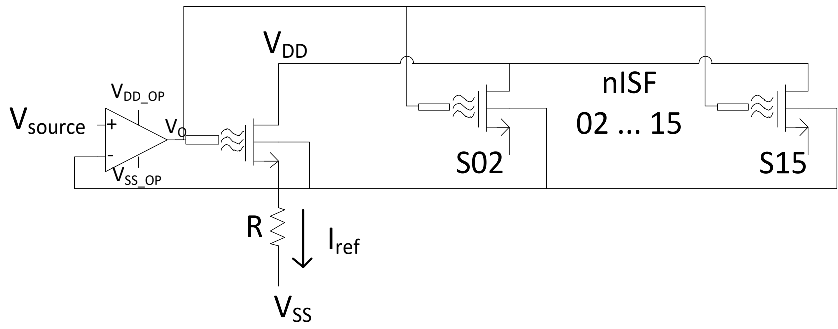


Figure 58 - Chip schematic.

Figure 59 presents the circuit schematic in the Proteus software and Figure 60 shows the PCB project and implementation.

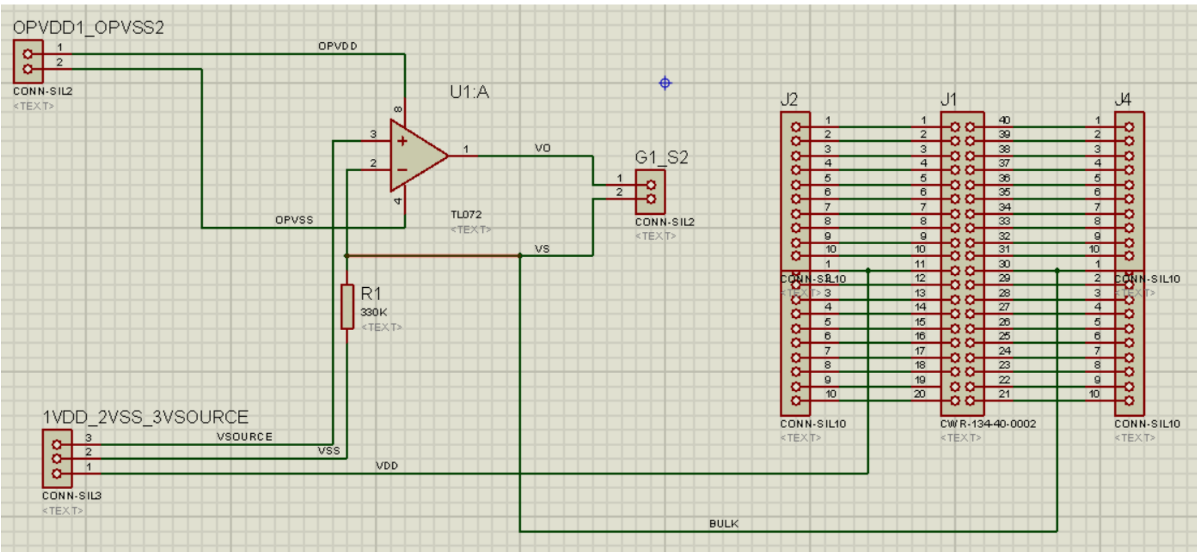
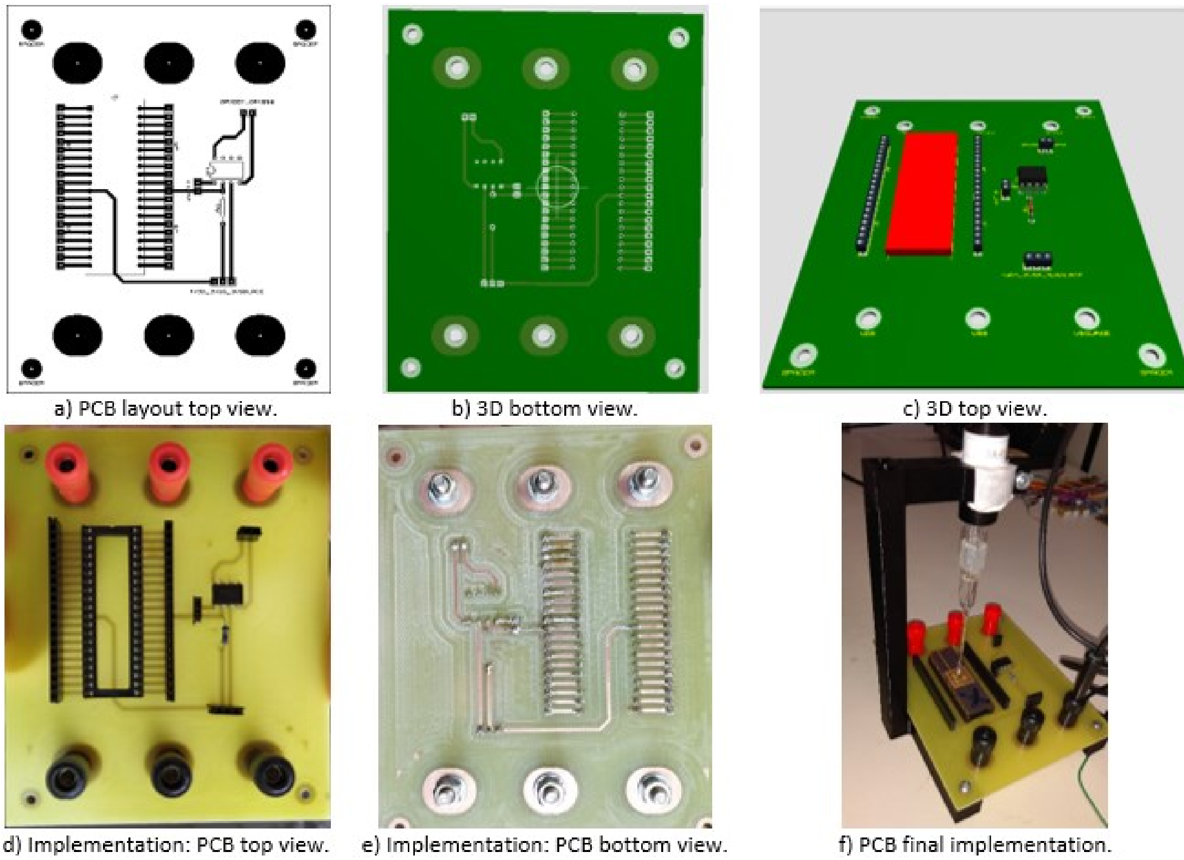


Figure 59 - Circuit schematic in the Proteus software.

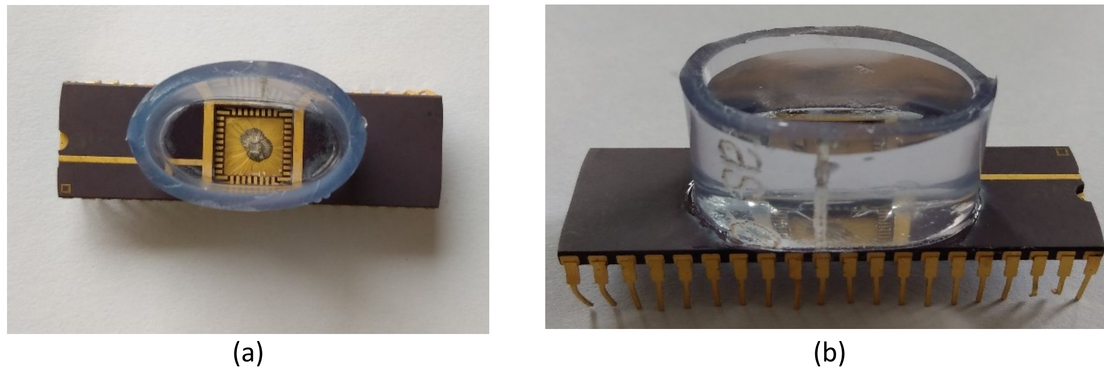


a) PCB layout top view. b) 3D bottom view. c) 3D top view.
d) Implementation: PCB top view. e) Implementation: PCB bottom view. f) PCB final implementation.

Figure 60 - PCB project (a), (b), (c) and implementation (d), (e) and (f).

APPENDIX I - Homemade chamber implementing a PVC tubing

This appendix summarizes the steps performed to create a homemade chamber implementing a PVC tubing, for wet tests in a chip packaged in DIL40. The chamber, created by Rodrigo Wrege, was developed to provide good sealing between the chamber and the chip packaging, allow the insertion of a reference electrode, and not cover the packaging open cavity (so it can be pressed against the packaging without damaging any bonding wire). The PVC tubing presented good malleability, making possible the use of conventional tools to cut, reshape and glue. It is also an affordable material. Damage chips were used for sealing tests. Figure 61 shows a chip implementing the chamber, where is possible to observe the chamber did not cover the open cavity of the packaging and allowed the storage of water without leakages:



(a) (b)

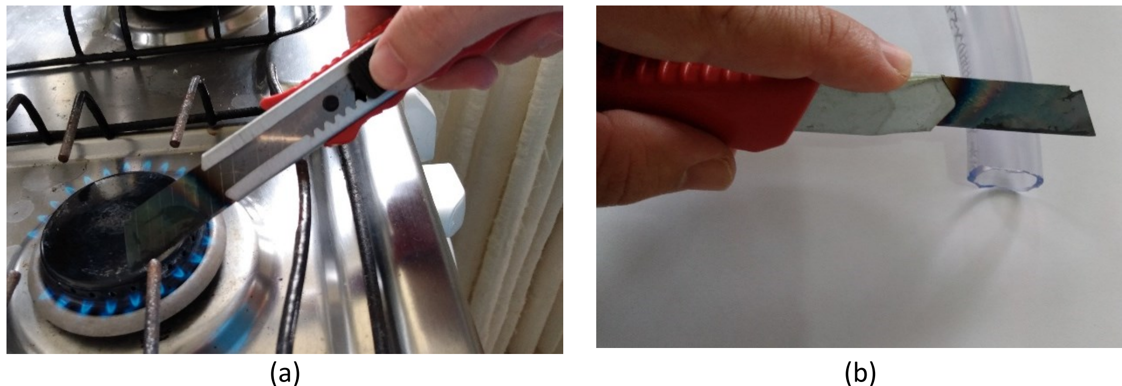
Figure 61 - Chip with the home-made chamber: (a) top view, and (b) chamber filled with water.

The list of materials and steps is below.

List of materials:

- DIL40 Chip
- Plier
- Blade (estilete)
- Clear PVC Tubing 3/4” (19.05 mm) x 2 mm (Mangueira Cristal de PVC 3/4 Pol. x 2,0 mm, Marca: MANTAC).
- Glue (Super Bonder)

Step 1: The PVC tubing was cut with a heated blade. The surface, which will be in contact with the chip, must be planar in order to get in touch with the chip packaging and prevent any solution leakage.



(a) (b)

Figure 62 - Cutting the chamber.

Step 2: The PVC tubing was reshaped in an elliptical format with a plier, so it could be glued around the open cavity of the DIP40, resulting in a width close to 12 mm:

Figure 63 - Reshaping the chamber to an elliptical format.

Step 3: Glue was applied in all border of the chamber:

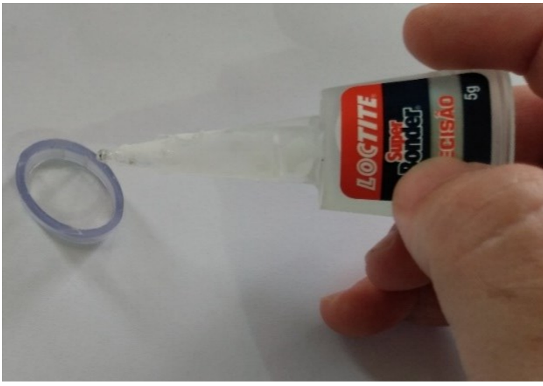
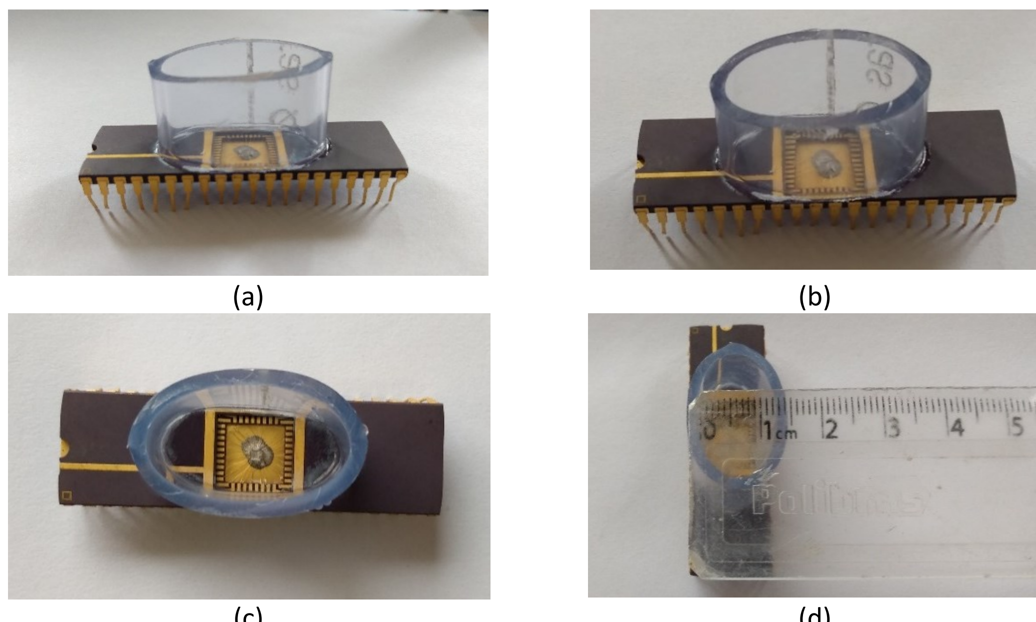


Figure 64 - Applying glue to the chamber.

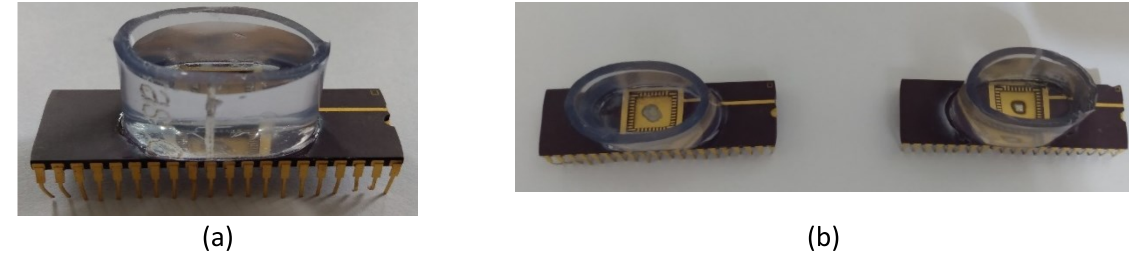
Step 4: The chamber was glued to the chip.



(a) (b) (c) (d)

Figure 65 - Chamber glued to the chip.

Step 5: After the glue was dry, it was tested for any leakage by filling it with water and observing if the water level would drop. The procedure was performed in two chips.



(a) (b)

Figure 66 - (a) Close view of a chip filled with water. (b) Two chips filled with water.

It was not observed any drop in the water level after several hours for both chips:

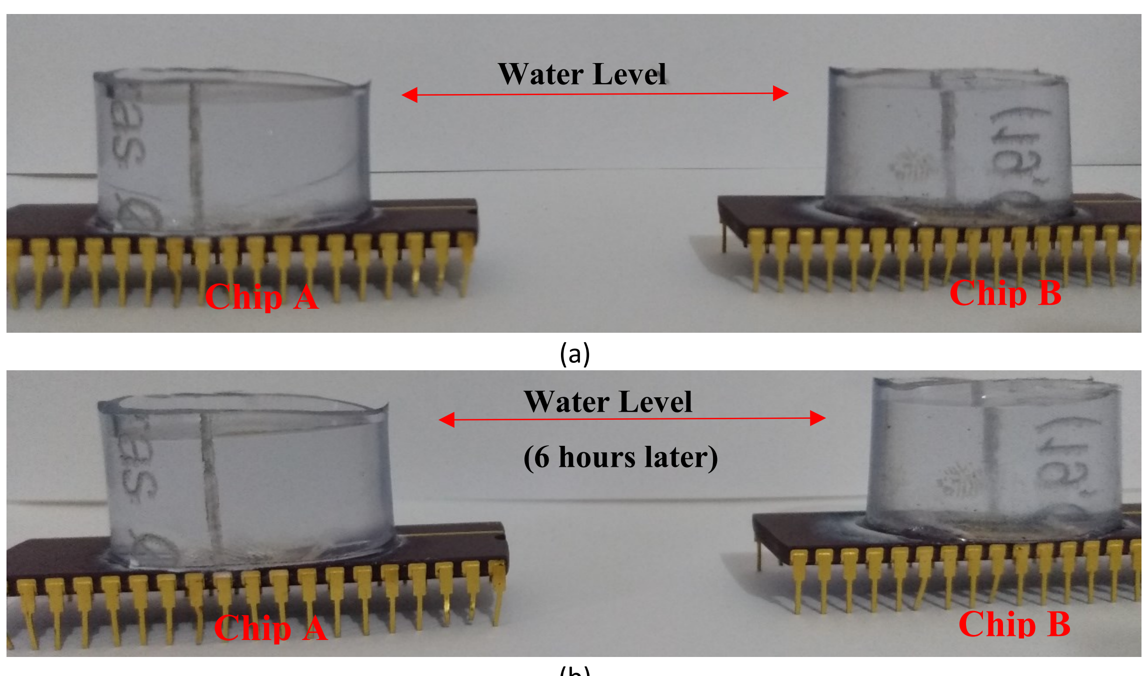


Figure 67 - Sealing test in two chips: 07/09/2020 at (a) 10:22; (b) 16:47.