LUÍS CLÉBER CARNEIRO MARQUES

SWITCHED-MOSFET TECHNIQUE FOR PROGRAMMABLE FILTERS OPERATING AT LOW-VOLTAGE SUPPLY

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SWITCHED-MOSFET TECHNIQUE FOR PROGRAMMABLE FILTERS OPERATING AT LOW-VOLTAGE SUPPLY

Thesis presented to
Federal University of Santa Catarina
as a partial fulfilment of the
requirements for the degree of
Doctor in Electrical Engineering.

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TÉCNICA DE MOSFET CHAVEADO PARA FILTROS PROGRAMÁVEIS OPERANDO À BAIXA TENSÃO DE ALIMENTAÇÃO

Luís Cléber Carneiro Marques

'Esta Tese foi julgada adequada para obtenção do Título de Doutor em Engenharia Elétrica, Área de Concentração em *Sistemas de Informação*, e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina.'

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SWITCHED-MOSFET TECHNIQUE FOR PROGRAMMABLE FILTERS OPERATING AT LOW-VOLTAGE SUPPLY

Luís Cléber Carneiro Marques

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The market and the need to implement portable electronic equipment have pushed the industry to produce circuit designs with very low-voltage power supply. This trend addresses both analogue and digital circuits. For analogue design, a key limitation that arises as the supply voltage is reduced is the difficulty of turning ON the MOS switches over the entire voltage swing. The recently introduced switched-MOSFET (SM) technique is a sampled-data technique suitable for low supply voltage operation since all SM switches operate at a constant voltage within the conduction range of the MOSFET. Besides, the SM technique does not need either dedicated processes or clock voltage multiplication schemes. The basic building block of the SM technique is a low-voltage sample-and-hold (half-delay cell) composed of an operational amplifier and MOS transistors operating in the triode region. Programmability of SM circuits, which is achieved through MOSFET-only current dividers (MOCDs), is simple and does not require a large silicon area. In this work, a mathematical analysis of the very basic SM structure, the half-delay cell, is developed, and offset compensation schemes are discussed. The implementation of a half-delay cell with AMS 0.35μm is described and measurement results presented. An SM programmable low-voltage filter is also implemented, using a 1.6μm CMOS process. The implemented filter contains a v-to-i converter, a half-delay cell, a biquadratic section (using auto-zero offset compensation and MOCDs for programming) and an i-to-v converter.

Resumo da Tese apresentada à UFSC como parte dos requisitos necessários para a obtenção do grau de Doutor em Engenharia Elétrica.

TÉCNICA DE MOSFET CHAVEADO PARA FILTROS PROGRAMÁVEIS OPERANDO À BAIXA TENSÃO DE ALIMENTAÇÃO

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O mercado e a necessidade de se implementar equipamentos portáteis têm pressionado a indústria a produzir circuitos com tensões de alimentação muito baixas. A tendência envolve a ambos circuitos, digitais e analógicos. Para o projeto de circuitos analógicos, uma das mais sérias limitações que surgem quando a tensão de alimentação é reduzida é a dificuldade de se ligar as chaves MOS em toda a excursão de tensão. A técnica de MOSFET chaveado (SM), recentemente introduzida, é uma técnica de dados amostrados útil para operação em baixa tensão de alimentação visto que todas as chaves em circuitos SM operam a tensão constante dentro da faixa de condução do MOSFET. Além disso, a técnica SM não necessita nem de processos dedicados nem de esquemas de multiplicação de *clock*. O bloco básico de construção da técnica SM é um *sample-and-hold* (célula de meio atraso) para baixa tensão composto de um amplificador operacional e transistores MOS operando na região triodo. A programação dos circuitos SM, a qual é executada através de divisores de corrente totalmente com MOSFETs (MOCDs), é simples e não requer muita área de silício. Neste trabalho, é desenvolvida uma análise matemática da estrutura básica SM, a célula de meio atraso, e esquemas de compensação de *offset* são discutidos. A célula é implementada com tecnologia AMS 0,35μm e resultados de testes são apresentados. Um filtro programável SM para baixa tensão também é implementado, em um processo CMOS de 1,6μm. O filtro contém um conversor v/i, uma célula de meio atraso, uma seção biquadrática (contendo compensação de offset por auto-zero e MOCDs para programação) e um conversor v/i.

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Introduction 1

1.1 Digital and analogue

The advances in very large scale integrated (VLSI) circuits have made possible to integrate several million transistors onto a single silicon chip. This has given a tremendous impetuous to digital signal processing. Digital implementations offer several advantages when compared to analogue solutions: programmability, flexibility, additional product functionality, good immunity to both noise and manufacturing process tolerances, and shorter design cycles. However, the need for analogue circuits will remain. Analogue signal conditioning and data conversion circuits are required for a digital circuit to interact with an inherently analogue world. In fact, the tendency now is to realise complex systems containing both the digital core and the analogue interface circuitry on a single chip, which claims for mixed-mode design strategies. The dominant processing technology to realise very densely packed integrated circuits is CMOS (Complementary Metal Oxide Semiconductor). Thus, an analogue technique that can be implemented in a single CMOS process will find large range of applications.

Other than interfacing the analogue world with a digital signal processor, analogue design still is and will continue to be used for complete systems [1]. This applies to systems where the frequency of operation is too high for digital implementation, to circuits

where the low complexity does not justify a digital implementation and in very low power applications, where the overhead introduced by the necessary analogue-to-digital (A/D) and digital-to-analogue (D/A) converters can not be tolerated.

1.2 Low-voltage low-power analogue design

During the last years the power supply voltage for VLSI circuits has been decreasing, and will continue to decrease to further lower levels. This trend is driven mostly by three interrelated factors [2, 3]. The first one is the technology driven scaling of VLSI technology (deep-submicron). As the channel length is scaled down into submicron dimensions and the gate-oxide thickness becomes only several nanometres thick, the supply voltage has to be reduced in order to ensure device reliability. The second reason for the supply voltage lowering is the power management in large VLSI chips. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip. The third reason for supply voltage lowering is the increased market demands for mobile or portable battery-operated products.

It is important to define the term low-voltage. Nowadays, we consider low-voltage integrated circuits those that operate at 1.5V or less. Another definition relates the supply voltage with technological parameters and the number of stacked devices that can be put in a circuit. Serdijn [4] considers as low-voltage analogue circuits those that do not have two or more junctions in series between two supply rails (in the case of bipolar transistors). Similarly, for MOSFETs, Hogervorst [5] considers as low-voltage circuits those able to operate on a supply voltage of two stacked gate-source voltages and two saturation

voltages, and considers as extremely low-voltage circuits those that need only a minimum supply voltage of one gate-source voltage and one saturation voltage.

For the necessary reduction in the size of portable equipments, the batteries are now becoming the limiting factor. Thus, the reduction of power dissipation has become an extra constraint. For implantable medical electronic devices, for example, this constraint always applies.

With the reduction of the supply voltage, analogue designers are faced with new problems in circuit design. Important device characteristics such as gain and linearity are strongly dependent on the supply voltage. But the key limitations that arise as the supply voltage is reduced are the reduced number of devices that can be stacked between the rails, the reduced linear voltage swing, and the difficulty of turning ON the MOS switches over the entire voltage range [6]. The first problem limits the type of circuit configurations that can be used. The second problem reduces the dynamic range for a given current consumption. The third problem is particularly severe in sampled-data circuits (see sub section 1.2.1 below) but may also limit the ability to digitally program continuous-time circuits [6].

As already explained in section 1.1, in many cases analogue circuits share a single chip with complex digital circuits. As digital circuits in such systems constitute the bigger part in the chip, the electrical parameters of transistors are optimised for them, which makes the design of analogue circuits harder. Analogue circuit designers would profit from the lowering of the threshold voltage with the scaling down of the MOS technologies. But the reduction of the threshold voltage produces two negative effects on digital circuits, namely, the reduction of noise margin and higher leakage currents. Owing to these two negative effects, as the technological process scales down the MOSFET threshold voltage of standard (and cheap) processes remains almost the same.

Analogue filters can be implemented with both continuous-time circuits and sampled-data techniques. Traditionally (i.e., non low-voltage), sampled-data implementations (especially with the switched-capacitor technique, SC) are used for low-frequency high-precision applications and continuous-time solutions (especially g_m-C implementations) are used for high-frequency medium/low-precision applications [6].

For operation under low-voltage supply, there is a tendency of using techniques that process currents instead of voltages [1, 7]. Current-mode analogue signal processing can loosely be defined as analogue signal processing in which current rather than voltage is the primary, although not necessarily exclusive, information-carrying medium [1]. The wide range of applications in which current-mode techniques can be applied to advantage is documented in [7]. Fig. 1-1 illustrates some of the existing analogue techniques for integrated circuits. We will focus on discrete-time circuits and will demonstrate the usefulness of the switched-MOSFET technique, which also processes currents.

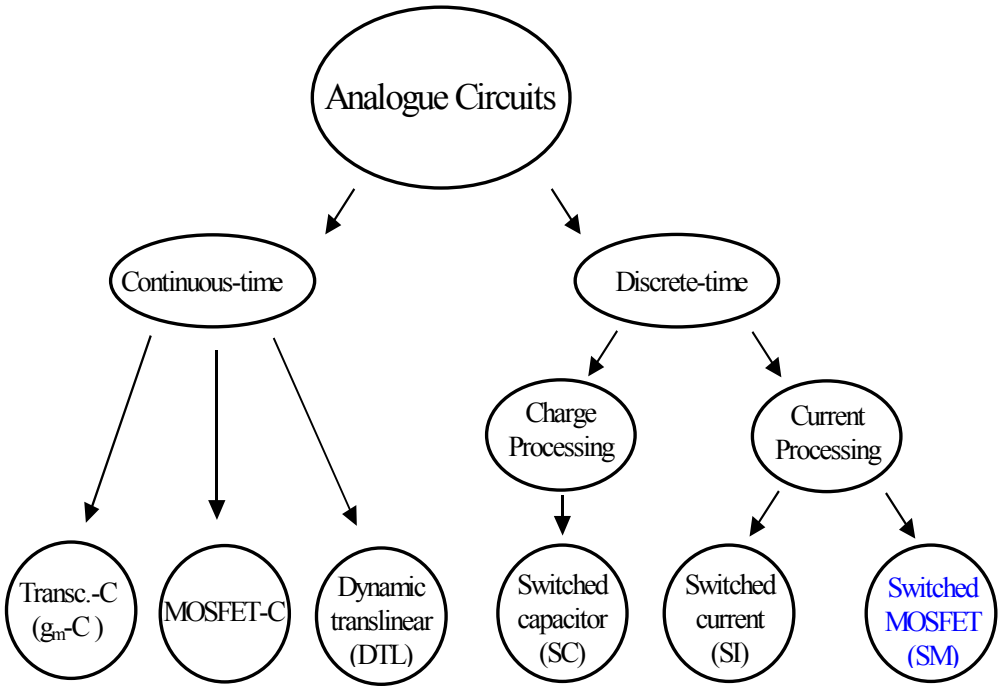


Fig. 1-1. Analogue IC techniques.

1.2.1 Conduction gap of the switches

One of the key problems to be faced with at low-voltage operation is the conduction gap of the switches. The complementary MOS switch has been largely employed in sampled-data (switched-capacitor and switched-current) analogue circuits. Fig. 1-2 shows a common S/H circuit. Around $V_S = V_D = V_{in}$, the conductance of an n-MOS switch in strong inversion [8] is

$$g_{DSn} = \mu_n C'_{ox} \frac{W}{L} (V_{DD} - V_{Ton} - nV_{in}) \tag{1-1}$$

where n is the slope factor, μ_n is the electron mobility, C'_{ox} is the oxide capacitance per unit area, W/L is the aspect ratio (W is the channel width and L is the channel length) and V_{Ton} is the threshold voltage in equilibrium for the NMOS transistor. The expression for the conductance g_{DSp} of the p-MOS switch is similar to (1-1). The switch conductance is dependent of both the supply voltage and the input signal. Fig. 1-3 illustrates the rail-to-rail operation of the CMOS switch. Note the dependence of the total switch conductance ($G_{on} = g_{DSn} + g_{DSp}$) on the input signal. Reducing the supply voltage reduces the overlapping conduction range of the nMOS and the pMOS devices. When the supply voltage is lower than $(V_{Ton} + |V_{Top}|) / (2 - n)$ [9] (V_{Top} is the threshold voltage in equilibrium for the PMOS transistor), as in Fig. 1.3b, the on-resistance becomes prohibitively large for intermediate values of V_{in} and rail-to-rail operation is no longer possible. In conclusion, the conduction gap, which affects both conventional SC and SI circuits, is one of the most significant obstacles for low-voltage operation of sampled-data circuits.

Some proposals to deal with the switch gap problem are found in the technical literature. One of them is to use costly low threshold processes [6, 10], incompatible with standard processes used for digital circuits.

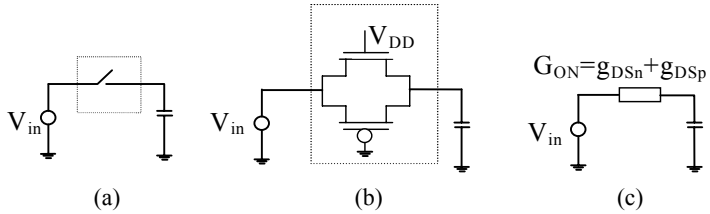
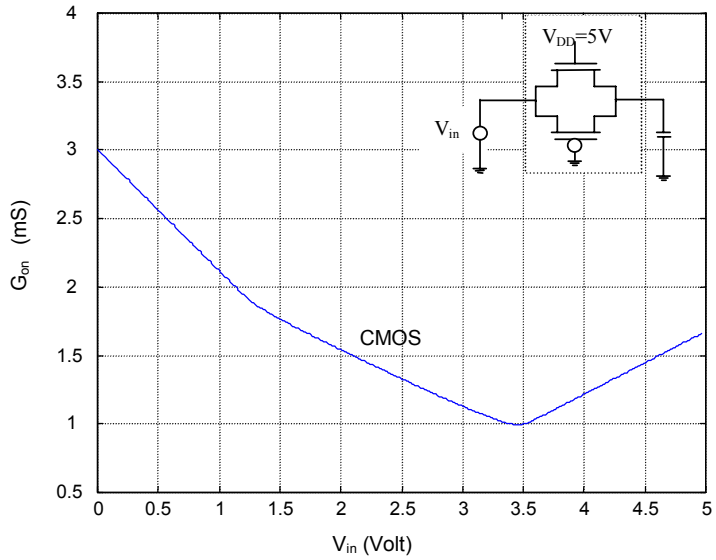
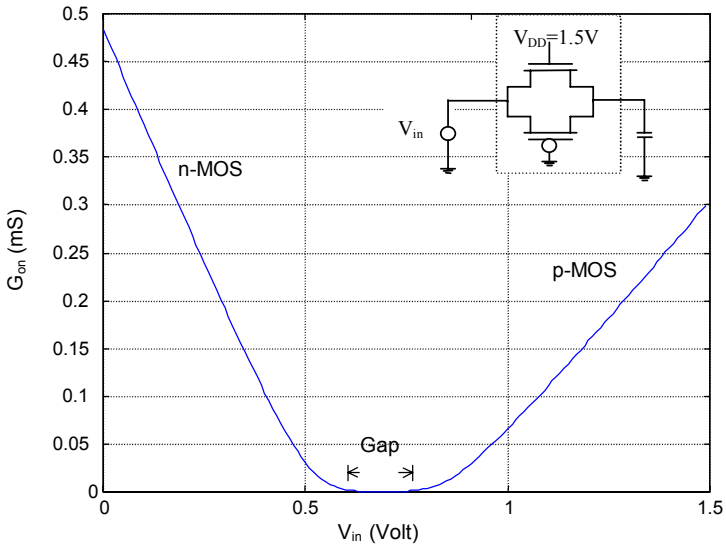


Fig. 1-2. The basic sample-hold circuit.
(a) Scheme. (b) With CMOS switch. (c) The on-conductance of the CMOS switch.



(a)



(b)

Fig. 1-3. On-conductance of a CMOS switch, (a) V_{DD}=5V, and (b) V_{DD}=1.5V.

Another solution frequently adopted in the past for avoiding the switch gap in SC is the use of voltage multipliers that generate on-chip clock signals higher than the supply voltage [11, 12]. However, for sub-micron technology the use of voltage doublers to enhance the circuit performance is seldom recommended due to the low breakdown voltage of transistors [13]. Moreover, this solution introduces potential long-term reliability oxide problems.

Bootstrap circuits offer another possible solution for the switch gap problem [14]. Their operation allows for the application of a constant voltage equal to V_{DD} across the gate to source terminals thus establishing a low on-resistance from drain to source independent of the input signal. For achieving this, several components must be added to create a "composed" switch. Fig. 1-4 shows a bootstrap circuit [14] together with the NMOS switch itself (*M11*). During the OFF phase ϕ is low. Devices *M7* and *M10* discharge the gate of *M11*. At the same time, V_{DD} is applied across capacitor *C3* by *M3* and *M12*. This capacitor acts as a battery across the gate and source of *M11* during the ON phase. *M8* and *M9* isolate the switch from *C3* while it is charging. When ϕ goes high, *M5* pulls down the gate of *M8*, allowing charge from the battery capacitor *C3* to flow into the gate *G*. This turns on both *M9* and *M11*. *M9* enables the gate *G* to track the input voltage *S* shifted by V_{DD}, keeping the gate-source voltage constant regardless of the input signal. For example, if the source *S* is at V_{DD}, then gate *G* is at $2V_{DD}$, however, $V_{gs} = V_{DD}$. Note that node *S* is best driven by a low-impedance due to the added capacitance at this node. Devices *M7* and *M6* are not functionally necessary but improve the circuit reliability. *M1*, *M2*, *C1* and *C2* form a clock multiplier that enables *M3* to unidirectionally charge *C3* during the OFF phase.

The problem with the bootstrap solution is the huge overhead (as can be seen in Fig. 1-4) that must be added to each critical switch (i.e., the switch in the signal path) on the sampled-data circuit.

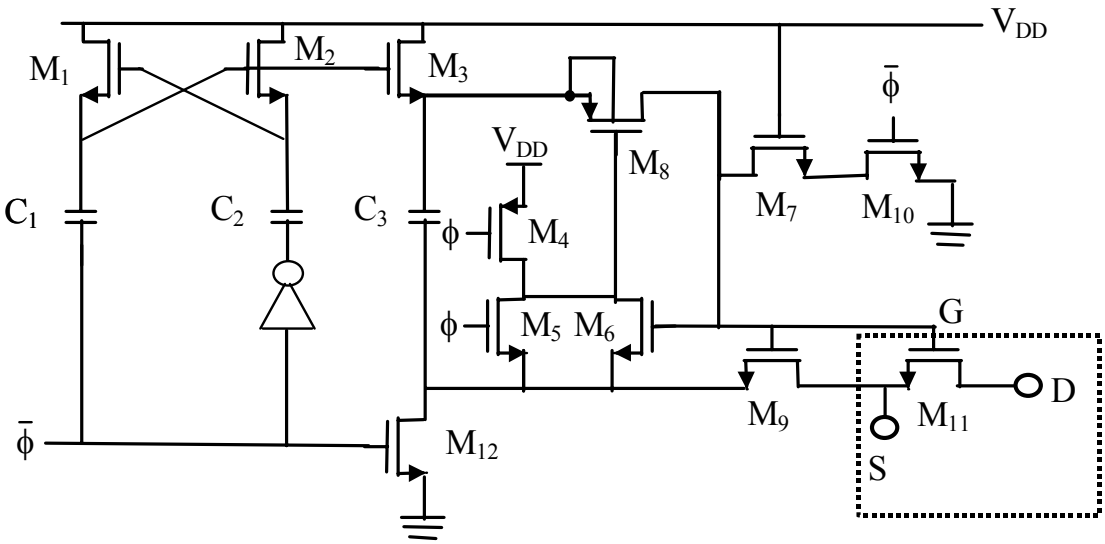


Fig. 1-4. Composed switch for the bootstrap technique [14].

Another approach to allow for proper operation of switches in low-voltage SC circuits is the switched-opamp technique [15, 16]. In this technique, the critical switch is eliminated, and its function is realised by turning on and off the operational amplifier (op-amp) attached to this switch. Fig.1-5 shows the conventional SC circuit and the switched-opamp equivalent circuit. This technique is based on the switched-opamp output to be in a high impedance state during the low state of the clock, as shown in Fig. 1-5 (c). One of the drawbacks of this technique is that the feedback circuit cannot be present in all phases. For example, in the circuit in Fig. 1-5b, the overall feedback circuit is not allowed during ϕ_1. Cheung et al [41] propose a solution to this problem, which consists in putting an additional switchable opamp in parallel with the original one and operating it during ϕ_2. As can be seen, this solution demands extra area and current consumption.

Another problem to be faced with by the switched-ampop technique is the need for an input switch in most circuits, so that a front-end interface must be added. Some solutions can be found in [17, 18]. Still, more complexity is added. Moreover, in the switched-opamp technique the maximum sampling frequency is limited by the time necessary to turn on and off the op-amp.

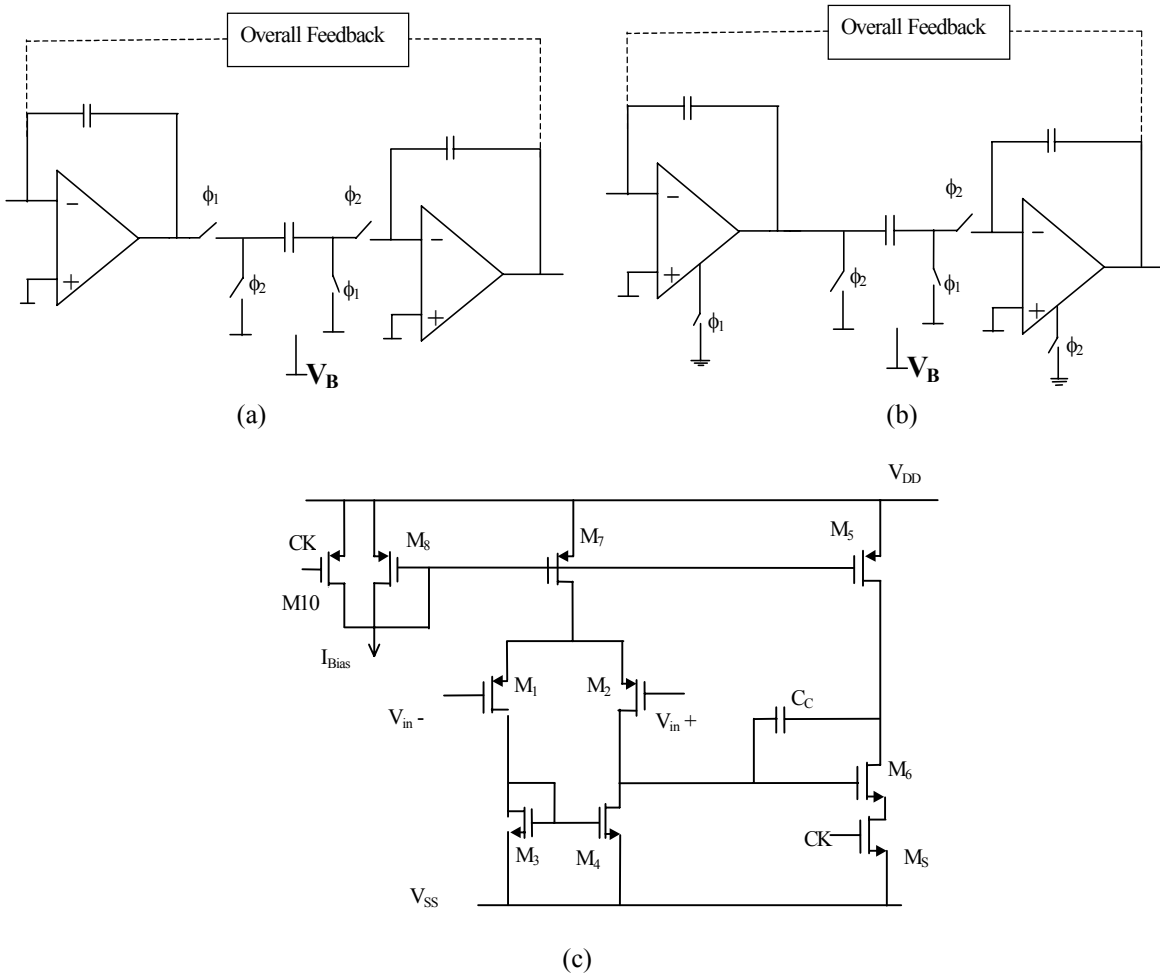


Fig. 1-5. Switched-opamp technique [15].
(a) Conventional SC integrator. (b) Switched-opamp equivalent SC circuit. (c) Switched op-amp.

In chapter 2, we will see that the switched-MOSFET technique solves naturally the problem of the conduction gap of the switches.

1.2.2 Operational amplifier under low-voltage

The operational amplifier is a widely used building block in analogue circuits. The power supply voltage must be higher than a minimum value to allow for correct operation of the amplifier. Fig.1-6 shows a conventional input stage of operational amplifiers. The maximum common-mode input voltage V_{CM} is around V_{DD}-(|V_{Top}|+V_{DSsat}). This constraint makes the use of certain topologies at low supply voltage impossible with simple op-amps. In switched-MOSFET circuits, as will be seen in chapter 2, all op-amps operate with a common-mode input voltage very close to the negative supply V_{SS}, which allows conventional input stages like the one in Fig. 1-6 to be used even at low supply voltages.

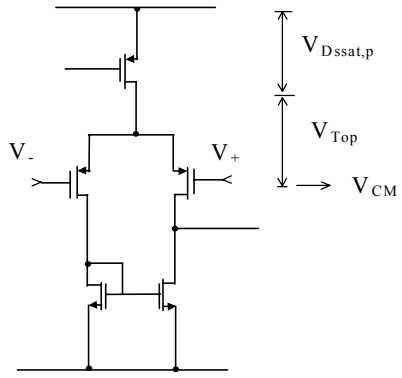


Fig. 1-6. The common-mode input range of an op-amp.

1.3 Programmability

Several applications demand programmable filters, sometimes with the extra constraint of low-voltage. Hearing-aid circuits [19-22] are one example of application that demand low-voltage low-power programmable filters. In this case, the audiologist, or the system itself, must adjust the filter section to manage the audio spectrum according to the kind of hearing impairment of the patient.

Switched-capacitors circuits can be programmed through the use of programmable capacitors arrays (PCAs) [23]. A 3-bit PCA is shown in Fig. 1-7. It consists basically of binary-weighted capacitors connected in parallel. Through digital signals, the right-hand side of the capacitors in the figure are connected either to node X' or to ground.

Switched-current circuits can be programmed through binary-weighted current mirrors, as shown in Fig. 1-8 [1]. The mirror gain $a = (W/L)_A /(W/L)_{REF}$, where $(W/L)_A = (W/L)_{NP} + b_0(W/L)_0 + b_1(W/L)_1$. An important problem to take into account with this system is the quantisation errors due to the limitations imposed by the technological grid [1].

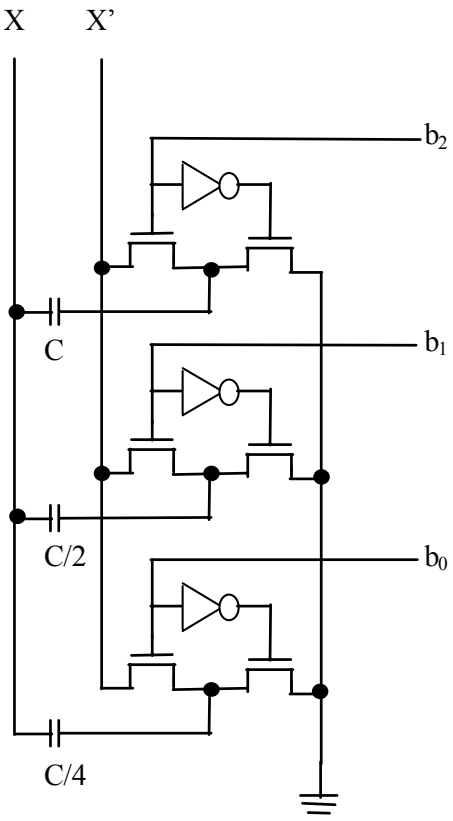


Fig. 1-7. Binary-programmable capacitor array [23].

The both above described techniques for programming present the disadvantage of using binary-weighted structures, which require silicon area that increases exponentially with the number of bits. We will see in chapter 2 that switched-MOSFET circuits can be

programmed using MOSFET-only current dividers, whose area increases linearly with the number of the bits.

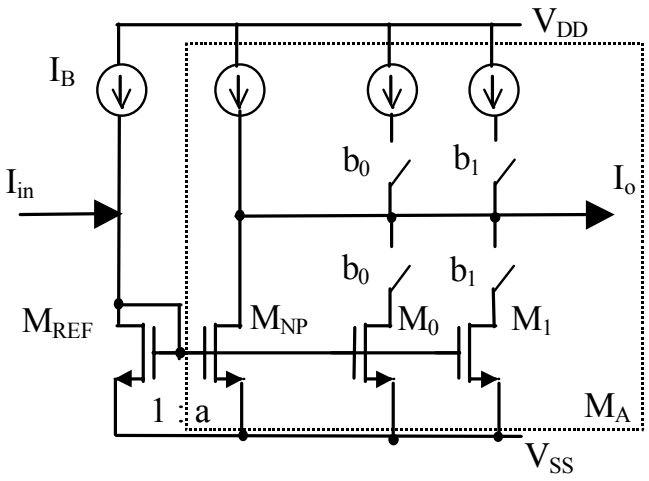


Fig. 1-8. Basic programmable current mirror [1].

1.4 Organisation of the work

This work has been divided into six chapters. Following this introduction, chapter 2 explains the principle of the switched-MOSFET (SM) technique and presents some basic SM structures. In chapter 3, a mathematical analysis of the very basic SM structure, the half-delay cell, is developed, and offset compensation schemes are discussed. Also in chapter 3, the implementation of a half-delay cell is described and measurement results presented. Chapter 4 focuses on other practical aspects of SM technique, such as voltage-to-current and current-to-voltage converters that may be required. Chapter 5 describes the implementation of several basic switched-MOSFET structures contained in a programmable low-voltage band-pass filter. Experimental results are presented and discussed. Finally, in chapter 6, some conclusions are drawn.

Switched-MOSFET technique 2

2.1 Introduction

As explained in the previous chapter, the conventional sampled-data techniques, switched-capacitor and switched-current are not "natural" for low-voltage operation. In this chapter the switched-MOSFET (SM) technique is considered and its suitability for low supply voltage operation is emphasised. Firstly, in section 2.2, an overview of the basic building blocks of sampled-data techniques is presented with emphasis on the SM basic building block. Section 2.3 describes the bias voltage generation for SM circuits and its appropriateness for low-voltage operation. Section 2.4 focuses on MOSFET-only current dividers, the small area consuming elements used for programmability of SM circuits. In section 2.5, other SM structures, such as integrators and biquadratic sections (biquads) are described. Finally, in section 2.6, a summary is drawn.

2.2 Basic building block of the SM technique

For sampled-data circuits, three basic elements (unitary elements) have been used, namely capacitors, current sources and resistors, as shown in Fig. 2-1 [24]. The first element is the base of the well-known switched-capacitor (SC) technique, the second one is

used in the switched-current technique (SI) [50] and the third one is at the base of the switched-MOSFET technique.

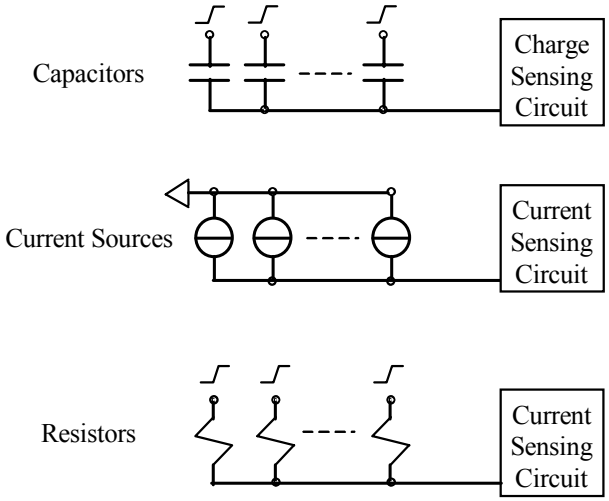


Fig. 2-1. Analogue computing modes.

The basic elements of the computing modes shown in Fig. 2-1 must not necessarily be linear for the practical implementation of the techniques [25]. Considering linear elements for simplicity, the basic building blocks of some of the possible sampled-data techniques are shown in Fig. 2-2. For the SC technique the basic building block is an integrator, while for SI and for the technique using resistors (which could be called in this case switched-resistor, SR) the basic building block is a half-delay cell.

The operation of the circuits in Fig. 2 is briefly described as follows. In Fig. 2-2a, on clock phase ϕ_2 capacitor C holds the output voltage while capacitor αC is discharged. On the next phase (ϕ_1), capacitor αC is charged to $v_I(n)$ while capacitor C charges to $v_O(n)$, which gives the z-domain transfer function $H(z) = \frac{v_O^{\phi_1}(z)}{v_I^{\phi_1}(z)} = -\frac{\alpha}{1 - z^{-1}}$. In Fig. 2-2b, transistor M_1 operates in saturation and the output voltage is assumed to drive M_2 also into saturation. The input current is stored as a voltage across the gate capacitor of M_1. When switch M_s is closed (sample phase), the drain currents of M_1 and M_2 are equal, i.e., the

output current follows the input current. When switch M_s opens (hold phse), the drain current of M_2 is held constant at its previous value. In Fig. 2-2c, when the switch is closed, we have,

$$i_o = -[R_1/R_2]i_{in} \tag{2-1}$$

since R_1 and R_2 are both biased with the same set of voltages. The output current i_o is an inverted replica of the input current i_{in}. The capacitor C is charged to a voltage V whose value depends on both i_{in} and R_1. When the switch opens, the voltage V is held on the memory capacitor and the current is sustained at the output.

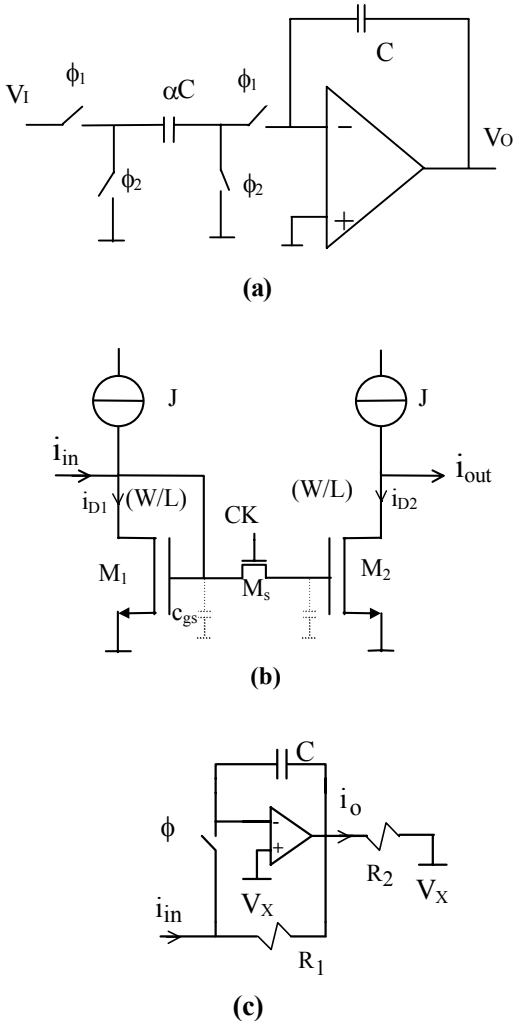


Fig. 2-2. Basic building blocks for sampled-data techniques.
(a) SC, integrator. (b) SI, half-delay cell. (c) SR, half-delay cell.

The main drawback of the circuit in Fig. 2-2c is the use of resistors, which demand large area. In fact, as previously mentioned, the basic elements for a sampled-data technique can be non-linear as well. Consider now the circuit in Fig. 2-3. It consists of an operational amplifier (op-amp), a memory capacitor C_M (which may be non-linear) and two transistors with matched non-linearities (M_1 and M_2) operating in the triode region. The reason for operation of MOSFETs in the triode region is apparent – the current of MOSFETs in the triode region is very sensitive to drain voltage, whereas the drain current in saturation is almost insensitive to the drain voltage.

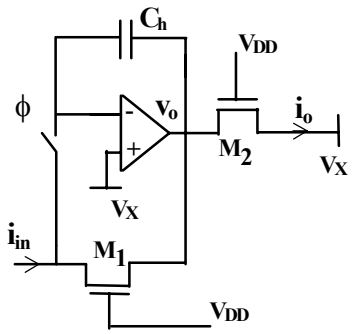


Fig. 2-3. The half-delay cell of the SM methodology [27].

Now assume that the op-amp is ideal and the transistors are matched in Fig. 2-3. Then, when the switch is closed, we have

$$i_o = -\left|(W/L)_{M2}/(W/L)_{M1}\right| i_{\text{in}} \tag{2-2}$$

since M_1 and M_2 are both biased with the same set of voltages. The output current i_o is, like in Fig. 2-2c, an inverted replica of the input current i_{in}. The capacitor C_h is charged to a voltage V whose value depends on $i_{in,}$ on the parameters of transistor M_1 and on the gate voltage. When the switch opens, the voltage V is held on the memory capacitor and the current is sustained at the output. The n-MOS switch operates at a constant voltage equal to

V_X, which can be set to a value that allows for operation of the switch within its conduction range as well as equal maximum positive and negative currents.

It is important to emphasise that the SM half-delay cell also allows for current amplification, with the gain determined by the aspect ratios of the transistors M_1 and M_2.

The sampled-data technique that we are presenting here has only more recently been coined switched-MOSFET technique. In early papers, we denominated it "A switched-current technique for low-voltage applications" [26-30]. This new designation (SM) describes more appropriately the operation of the technique we are dealing with and prevents the SM technique to be mistaken for the conventional switched-current technique.

2.3 Bias voltage generation for SM circuits

In the SM technique, all n-MOS switches operate at a constant voltage equal to V_X, which is generated by the series association of two identical transistors, as shown in Fig. 2-4b.

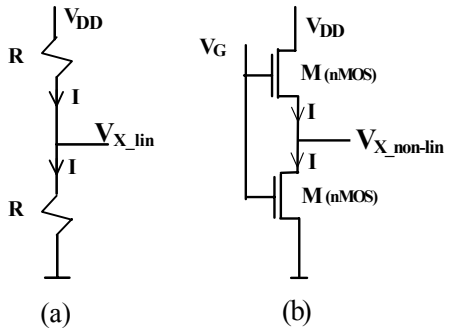


Fig. 2-4. V_X generation for highest symmetric current swing.

In order to understand the circuit of Fig. 2-4b, let us first examine the linear divider of Fig. 2-4a, where it is clear that $V_{X\_lin} = V_{DD}/2$. This voltage, $V_{DD}/2$, allows for the maximum current swing in both positive and negative directions in a circuit like the one in Fig. 2-2c, if the op-amp is assumed to be rail-to-rail at the output. In Fig. 2-4b, the current

is the same in the (identical) transistors; thus, the application of V_{X_nonlin} obtained from the voltage divider in Fig. 2-4b to the non-inverting input of the op-amp allows for the highest symmetric current swing in a circuit like the one in Fig. 2-3.

Consider the drain current in strong inversion [8, 51]:

$$i_D = \frac{\mu_n C'_{ox}(W/L)n}{2}\left[(V_P - v_S)^2 - (V_P - v_D)^2\right] \tag{2-3}$$

where v_S, v_D are the bulk-referred source and drain voltages, n is the slope factor, V_p is the pinch-off voltage [8], μ_n is the electron mobility, C'_{ox} is the oxide capacitance per unit area and W/L is the aspect ratio. The current in a n-MOS transistor for $V_S = V_{X\_nonlin}$ is illustrated in Fig. 2-5. As can be seen in Fig. 2-5, the voltage V_{X_nonlin} is much closer to the negative supply (ground) than to the positive supply. In strong inversion, it is given by [31]

$$V_{X\_nonlin} = V_P\left(1 - 1/\sqrt{2}\right) \tag{2-4}$$

The maximum bidirectional current in the transistor is obtained either with $v_S = 0$V and $v_D = V_{X\_nonlin}$ (in this case, $-I_{max}$) or with $v_D = V_p$ and $v_S = V_{X\_nonlin}$ (in this case, $+I_{max}$). This current, illustrated in Fig. 2-5, is given by

$$I_{max} = \frac{\mu_n C'_{ox}(W/L)n}{4} V_P^2 \tag{2-5}$$

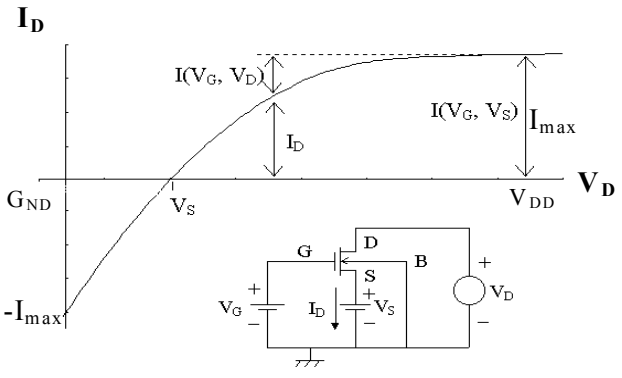


Fig. 2-5. Current in a MOS transistor having $V_S = V_{X\_nonlin}$.

The voltage V_{X_nonlin} (from now on called only V_X) provided by the circuit in Fig. 2-4b not only allows for the highest current swing in both directions but also guarantees that the n-switch operates within its conduction range. All switches in SM circuits operate at V_X, and all op-amps have V_X as common-mode input voltage, making SM suitable for low-voltage operation.

2.4 Programmability and the MOCD

In the SM technique, the digital programmability is achieved by means of MOSFET-only current dividers (MOCDs) [32]. The schematic of an MOCD together with its symbol is shown in Fig. 2-6. All MOCD transistors have same width and length, and a common substrate connected to V_{SS} (the negative supply). The output current of the MOCD is a digitally controlled fraction '*a*' of the input current, according to

$$a = \sum_{i=0}^{M-1} b_i 2^{(i-M)} \tag{2-6}$$

where M is the number of bits of the MOCD, b_i = 0 or 1, b_0 is the least-significant bit and b_{M-1} is the most-significant bit.

The MOCD has an input impedance which is independent of both the digital word and the number of bits, thus providing a constant load impedance to the op-amps. Without trimming techniques, MOCDs easily achieve 6-bit resolution, which is sufficient for some applications [33]. The high linearity of the MOSFET-only current division technique has been proved appropriate for analogue signal processing [32].

In the SM half-delay cell in Fig. 2-3, the current gain, given by (2-2), can be controlled through the use of an MOCD in place of $M1$ or M_2.

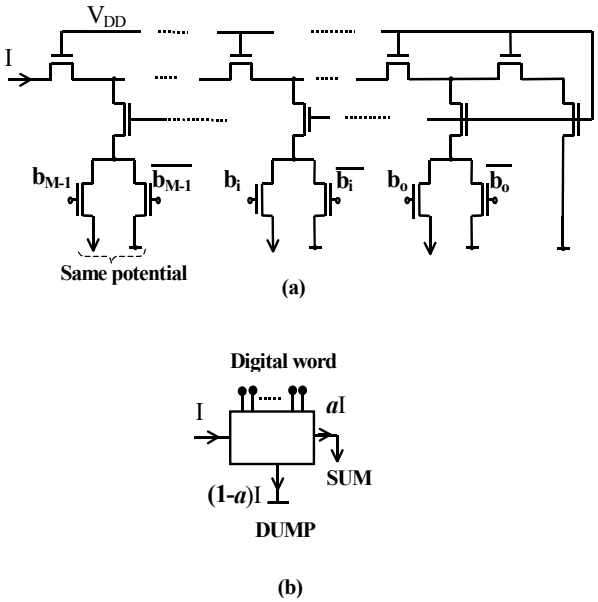


Fig. 2-6. The MOSFET-only current divider, MOCD. (a) Circuit scheme. (b) Symbol.

2.5 Other SM structures

Basic building blocks of the SM technique other than the half-delay/amplifier cell in Fig. 2-3 are the first and second generation integrators. Other very useful structures are universal biquads, which can perform different filtering functions. Those structures are considered in this section.

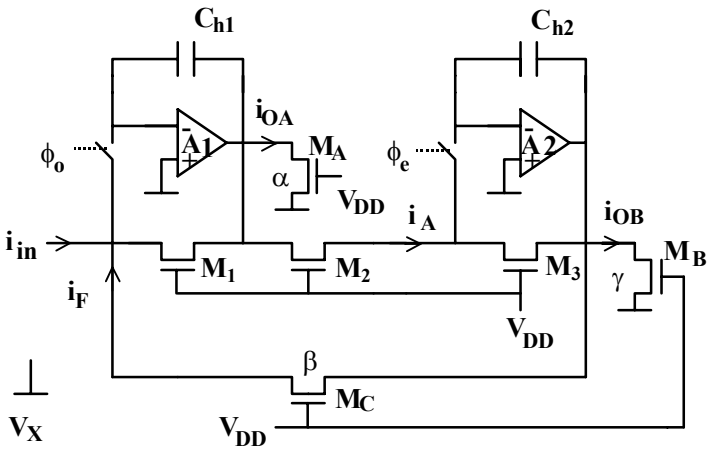
2.5.1 First generation integrator

The first generation SM integrator is implemented using two half-delay cells, as shown in Fig. 2-7 [27]. The integrator operates as follows: during ϕ_o, the sum of input (i_{in}) and feedback (i_F) currents is stored in the first memory cell as a voltage across C_{h1}; during ϕ_e, the input (i_A) to the second cell is stored as a voltage signal across C_{h2}. Assuming M_1, M_2 and M_3 with the same aspect ratios, the integrator presents the following transfer functions at its outputs [27]:

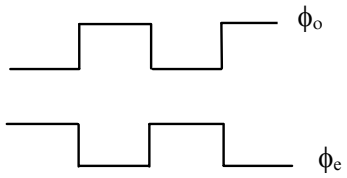
$$\frac{I_{OA}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = -\alpha \frac{1}{1-\beta z^{-1}} \tag{2-7a}$$

$$\frac{I_{OB}^{\phi_o}(z)}{I_{IN}^{\phi_o}(z)} = \gamma \frac{z^{-1}}{1-\beta z^{-1}} \tag{2-7b}$$

where $\alpha=(W/L)_{MA}/(W/L)_{M1}$, $\beta=(W/L)_{MC}/(W/L)_{M3}$ and $\gamma=(W/L)_{MB}/(W/L)_{M3}$. Parameters α, β and γ can be implemented with MOCDs replacing M_A, M_C, and M_B, respectively, resulting in a digitally programmable integrator. As in the half-delay cell, the switches in the integrator operate at constant voltage.



(a)



(b)

Fig. 2-7. First generation SM Integrator.
(a) Circuit. (b) Clock sequence.

A universal integrator can be easily obtained with a few modifications, as shown in Fig. 2-8 [34]. Table 2-1 shows the complete set of transfer functions for the universal integrator. Note that lossless integrators and analogue inverters are obtained with $\beta = 1$.

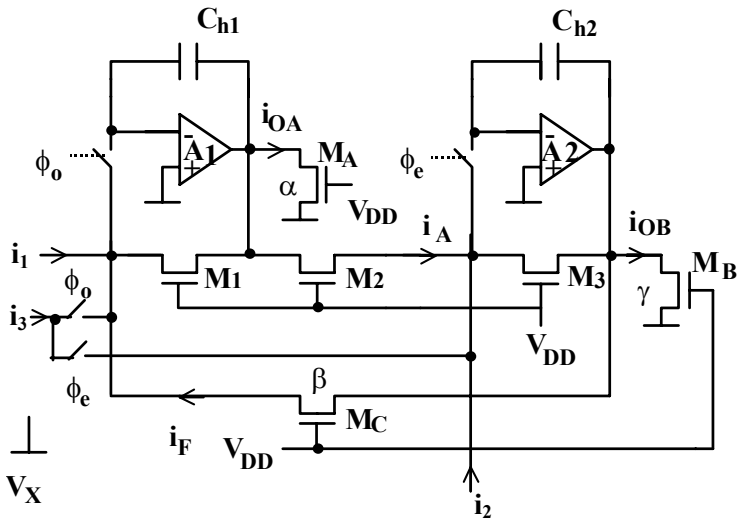


Fig. 2-8. Universal 1st generation integrator.

Table 2-1 Transfer functions for the universal 1st generation integrator.

	$I_1^{\phi_o}$	$I_2^{\phi e}$	I_3	
			S^o/H^e [1]	S^e/H^o [2]
$I_{OA}^{\phi_o}$	$-\alpha\frac{1}{1-\beta z^{-1}}$	$\alpha\frac{z^{-1/2}}{1-\beta z^{-1}}$	$-\alpha\frac{1-z^{-1}}{1-\beta z^{-1}}z^{-1/2}$	0
$I_{OA}^{\phi e}$	$-\alpha\frac{z^{-1/2}}{1-\beta z^{-1}}$	$\alpha\frac{z^{-1}}{1-\beta z^{-1}}$	$-\alpha\frac{1-z^{-1}}{1-\beta z^{-1}}0$	0
$I_{OB}^{\phi_o}$	$\gamma\frac{z^{-1}}{1-\beta z^{-1}}$	$-\gamma\frac{z^{-1/2}}{1-\beta z^{-1}}$	0	$-\gamma\frac{1-z^{-1}}{1-\beta z^{-1}}$
$I_{OB}^{\phi e}$	$\gamma\frac{z^{-1/2}}{1-\beta z^{-1}}$	$-\gamma\frac{1}{1-\beta z^{-1}}$	0	$-\gamma\frac{1-z^{-1}}{1-\beta z^{-1}}z^{-1/2}$

1. A S^o/H^e signal is sampled at ϕ_o and held constant at ϕ_e.
2. A S^e/H^o signal is sampled at ϕ_e and held constant at ϕ_o.

2.5.2 Second generation integrator

The implementation of high-Q filters [1] is extremely difficult with the first generation integrator. The reason for this difficulty is that high-Q filters require lossless

and/or low-loss integrators. As can be observed in expression (2-7), low-loss integrators require β close to 1. Such accurate value of β relies on tight matching between transistors. On the other hand, the second generation integrator shown in Fig. 2-9 [28] overcomes this problem since the sensitivity of the pole of low-loss integrators to β is not as critical as in the first generation integrator.

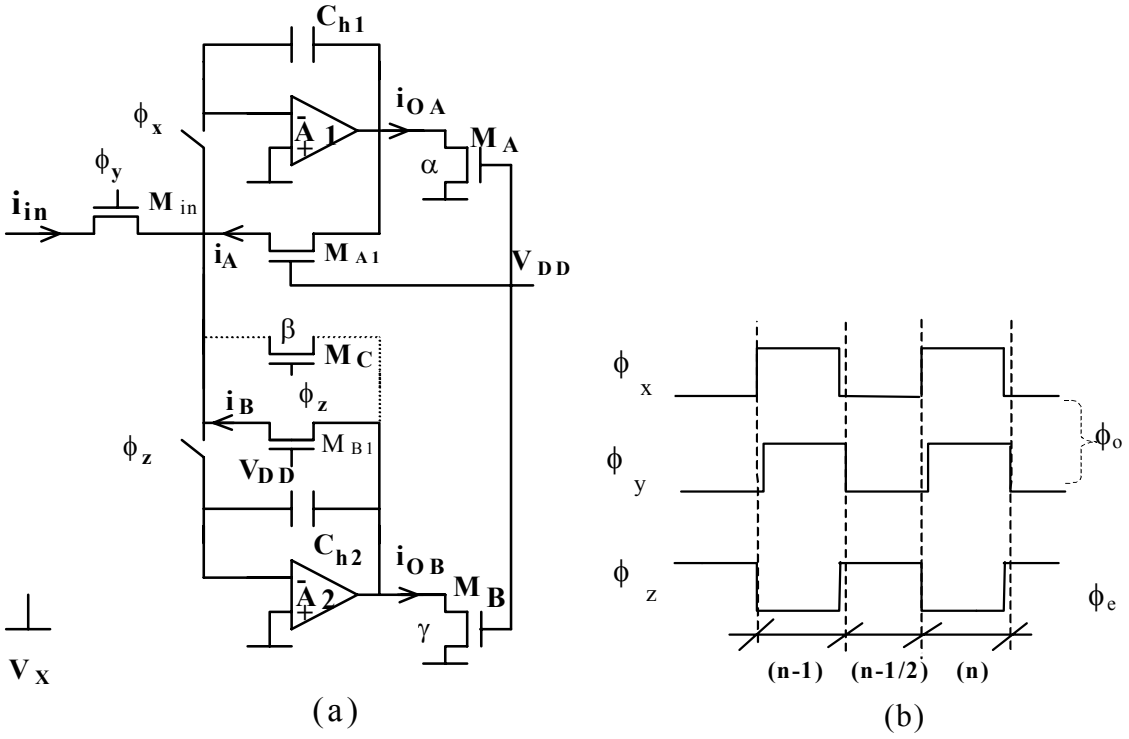


Fig. 2-9. Second generation SM Integrator.
(a) Circuit. (b) Clock sequence.

In Fig. 2-9, assuming transistors M_{A1} and M_{B1} to have the same aspect ratios, the second generation integrator presents the following transfer functions [28]:

$$\frac{I_{OA}^{\phi_o}(z)}{I_{in}^{\phi_o}(z)} = -\alpha \frac{1}{1+\beta-z^{-1}} \tag{2-8a}$$

$$\frac{I_{OB}^{\phi_o}(z)}{I_{in}^{\phi_o}(z)} = \gamma \frac{z^{-1}}{1+\beta-z^{-1}} \tag{2-8b}$$

where $\alpha=(W/L)_{MA}/(W/L)_{MA1}$, $\beta=(W/L)_{MC}/(W/L)_{MB1}$ *and* $\gamma=(W/L)_{MB}/(W/L)_{MB1}$. As in the first generation integrator, parameters α, β and γ can be implemented with MOCDs. Note from (2-8) that a lossless integrator is realised by simply disconnecting M_C in Fig. 2-9.

The use of 3 clock signals is necessary in order to prevent loss of information during clock transitions in a practical implementation. A universal integrator can be obtained with a few modifications, as shown in Fig. 2-10. The clock sequence is the same as for the circuit in Fig. 2.10. The output/input relations for the universal second generation integration [30] in Fig. 2-10 are summarised in Table 2-2.

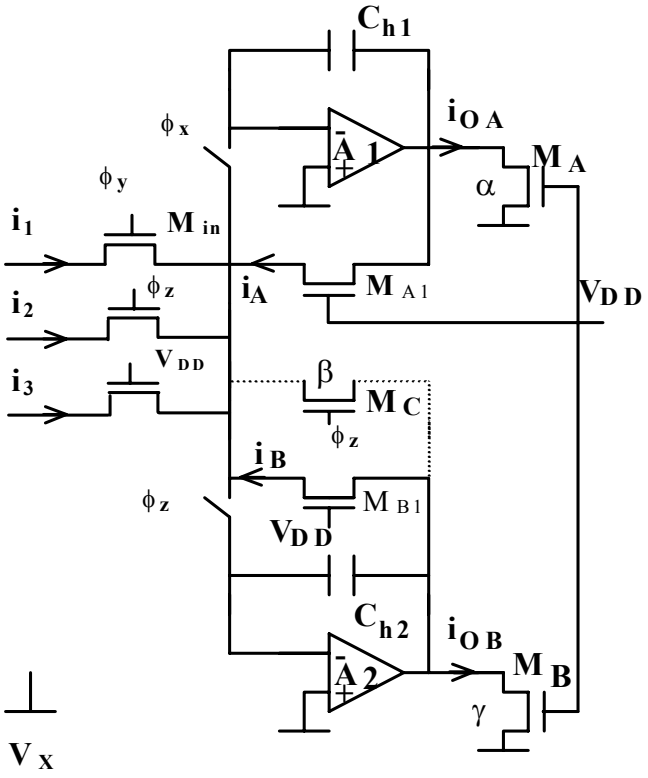


Fig. 2-10. Universal 2nd generation integrator.

Table 2-2 Transfer functions for the universal 2nd generation integrator.

	$I_1^{\phi_o}$	$I_2^{\phi_e}$	I_3	
			S^o/H^e [1]	S^e/H^o [2]
$I_{OA}^{\phi_o}$	$-\alpha\frac{1+\beta}{1+\beta-z^{-1}}$	$\alpha\frac{z^{-1/2}}{1+\beta-z^{-1}}$	$-\alpha\frac{1-\beta-z^{-1}}{1+\beta-z^{-1}}$	$\alpha\frac{z^{-1/2}}{1+\beta-z^{-1}}(-\beta)$
$I_{OA}^{\phi_e}$	$-\alpha\frac{1+\beta}{1+\beta-z^{-1}}z^{-1/2}$	$\alpha\frac{z^{-1}}{1+\beta-z^{-1}}$	$-\alpha\frac{1-\beta-z^{-1}}{1+\beta-z^{-1}}z^{-1/2}$	$\alpha\frac{z^{-1}}{1+\beta-z^{-1}}(-\beta)$
$I_{OB}^{\phi_o}$	$\gamma\frac{z^{-1}}{1+\beta-z^{-1}}$	$-\gamma\frac{z^{-1/2}}{1+\beta-z^{-1}}$	0	$-\gamma\frac{z^{-1/2}}{1+\beta-z^{-1}}\left(1-z^{-1}\right)$
$I_{OB}^{\phi_e}$	$\gamma\frac{z^{-1/2}}{1+\beta-z^{-1}}$	$-\gamma\frac{1}{1+\beta-z^{-1}}$	0	$-\gamma\frac{1}{1+\beta-z^{-1}}\left(1-z^{-1}\right)$

1. A S^o/H^e signal is sampled at ϕ_o and held constant at ϕ_e.
2. A S^e/H^o signal is sampled at ϕ_e and held constant at ϕ_o.

2.5.3 Universal SM biquad

Using an inverting and a non-inverting integrators, a second order filter (biquad) can be constructed. The biquad shown in Fig. 2-11 [28] utilizes two second order SM integrators and was designed using backward LDI transformation [35]. This transformation leads to smaller frequency prewarping errors than the Euler transformations. In Fig. 2-11, input 1 is the low-pass input, input 2 is the band-pass input and input 3 is the high-pass input, being thus the circuit considered a universal biquad. The input/output relation for the biquad is:

$$I_o^{\phi e}(z) = -\frac{K_3 \mathrm{I}_3^{\phi e}\left(1-z^{-1}\right)^2 + K_2 \mathrm{I}_2^{\phi e}\,\mathrm{af}\left(1-z^{-1}\right)z^{-1} + K_1 I_1^{\phi e}\mathrm{a}\,z^{-1}}{1-\left(2-\mathrm{af}-\mathrm{a}^2\right)z^{-1}+\left(1-\mathrm{af}\right)z^{-2}} \tag{2-9}$$

In (2-9), the input currents I_2 and I_3 are, in fact, sampled at ϕ_e and held constant at ϕ_o, which means that a sample and hold must be used for these inputs.

In the biquad in Fig. 2-11, the programmability can also be achieved by using MOCDs. The term "ϕ.x" means that the digital word "x" is ANDing with clock "ϕ" to implement the switching of the MOCD. The centre frequency (ω_o) and quality factor (Q) can be controlled independently if the sampling frequency is much higher than the centre frequency. In this case:

$$\omega_o T \cong a \tag{2-10a}$$

where T is the sampling period, and

$$Q \cong 1/f \tag{2-10b}$$

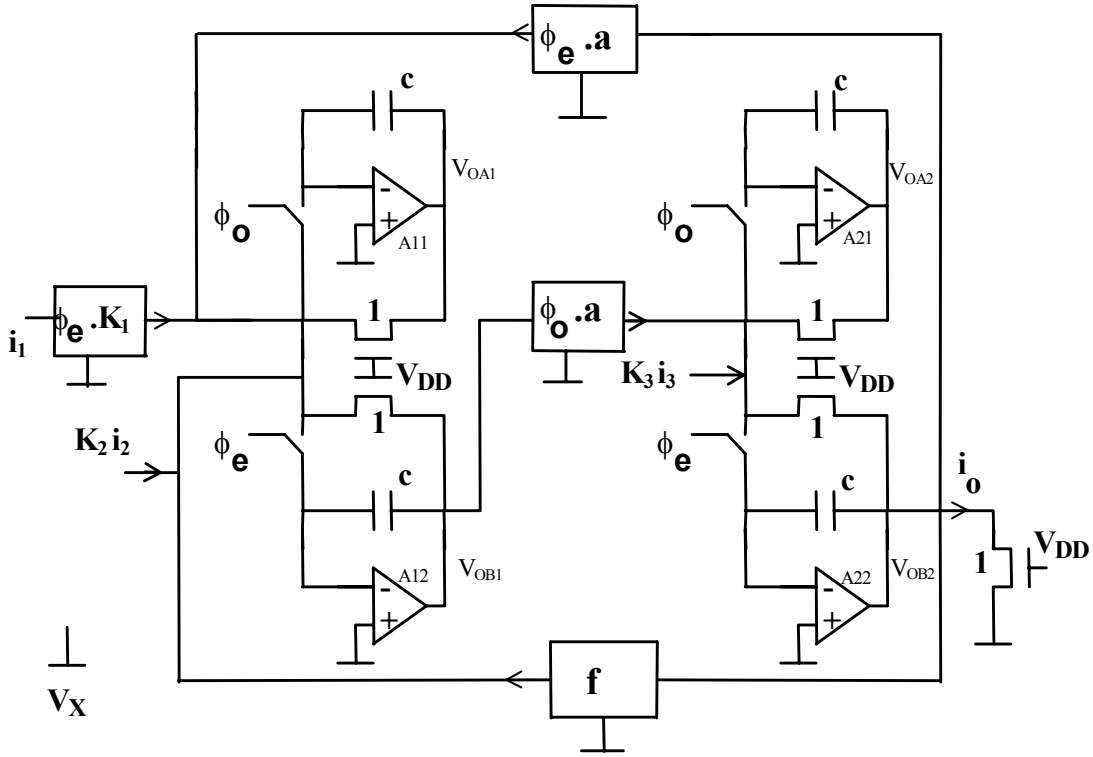


Fig. 2-11. Universal SM biquad.

2.6 Conclusions

The switched-MOSFET technique is an alternative technique for low-voltage discrete-time signal processing without the need for a special process. All switches in the SM structures operate at constant voltage and thus the conduction gap of the switch is avoided. The common-mode input voltage of all operational amplifiers in SM circuits is close to the negative supply; thus, very simple input stages are allowed for the operational amplifiers. No linear capacitor is needed. Thus, for low-voltage operation the SM technique compares advantageously with the traditional switched-capacitor and switched-current techniques. Switched-MOSFET also excels at simplicity of programming. Thus, the SM technique is very useful in applications where programmable low-voltage filters are required, such as in hearing aid circuits.

Half-delay cell analysis 3

3.1 Introduction

The half-delay cell is the basic building block of the switched-MOSFET technique. It is thus very important to perform a detailed analysis of the half-delay cell and achieve a formalisation for establishing the limits of the technique and comparing SM with other techniques. In this chapter, such analysis is carried out. In section 3.2, the problems due to the offset voltage of the operational amplifier are considered and offset compensation schemes are proposed. Section 3.3 focuses on settling time, which is important to determine the maximum values of capacitors to be used. Noise in the SM half-delay cell is analysed in section 3.4. Both the broad-band and sampled noise are considered. Charge injection and residual offset are focused in section 3.5. Section 3.6 addresses the imperfections that contribute to harmonic distortion. In all those sections numerical examples are given for a given technology. In section 3.7 the implementation of an SM half-delay cell with AMS 0.35μm is described and measurements results are presented. Finally, in section 3.8, a summary of the chapter is drawn.

3.2 Effects of the op-amp offset voltage and offset compensation

Consider the current mirror in Fig. 3-1, which is the SM half-delay cell without sampling. The offset voltage V_{OS} of the op-amp gives rise to a DC error Δi_O in the output current [27] given by

$$\frac{\Delta i_O}{I_{max}} = 2\sqrt{2}\frac{V_{OS}}{V_P} \tag{3-1}$$

where I_{max} is given by (2-5), $M_1 \equiv M_2$. In (3-1), the op-amp gain is considered to be infinite.

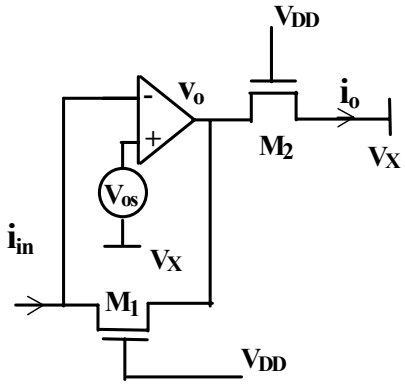


Fig. 3-1. A low-voltage current mirror [27].

The SM half-delay cell is a sampled current mirror (S/H), as in Fig. 3-2. In the S/H circuit, the error in the output current is also proportional to the offset voltage of the op-amp. For the circuit in Fig. 3-2, we have, for identical transistors:

$$i_o(n+1) = \frac{-i_{in}(n+1/2)}{1+A^{-1}} + \left(\frac{V_{OS}}{1+A^{-1}} - A^{-1}V_X\right)\frac{1}{R} \tag{3-2}$$

where $\mathrm{R} = \left(\partial I_D / \partial V_S\right)^{-1}\Big|_{V_S=V_D=V_X} = \left[0.707\mu_n C'_{ox}(W/L)(V_{DD}-V_{T0})\right]^{-1}$ and A is the DC gain of the op-amp.

This error will affect the dynamic range of the circuits. Thus, in some applications, it will be necessary to overcome this drawback by using offset compensation techniques.

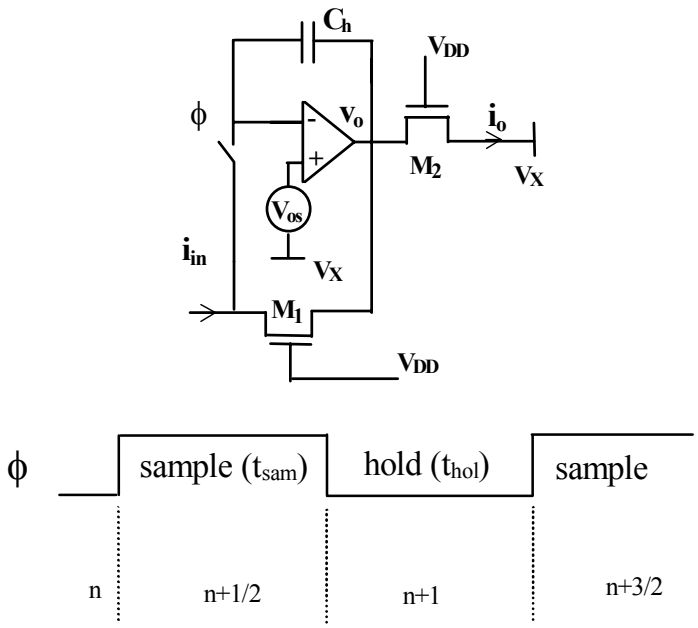


Fig. 3-2. The basic half-delay cell of the SM methodology [27].

3.2.1 Correlated double sampling in SM circuits

The offset compensation circuit suggested in [30] is shown in Fig. 3-3. It is based on Nagaraj's correlated double-sampling (CDS) circuit for switched-capacitor circuits [36]. The operation of the circuit is as follows. When ϕ_c is high, the offset voltage is stored in C_c. Consequently, when ϕ_c is low the offset appears as an input signal and its effect on the output is ideally cancelled out. For the circuit in Fig. 3-3 (identical transistors):

$$i_o(n+1) \cong -\frac{i_{in}(n+1/2)}{1+A^{-1}} + \frac{A^{-1}.V_{OS}}{\left(1+A^{-1}\right)^2}\frac{1}{R} - \frac{A^{-1}.i_{in}(n-1/2)}{1+\left(2+K_c\right)A^{-1}} \tag{3-3}$$

where $K_c \equiv (C_c/C_h)$.

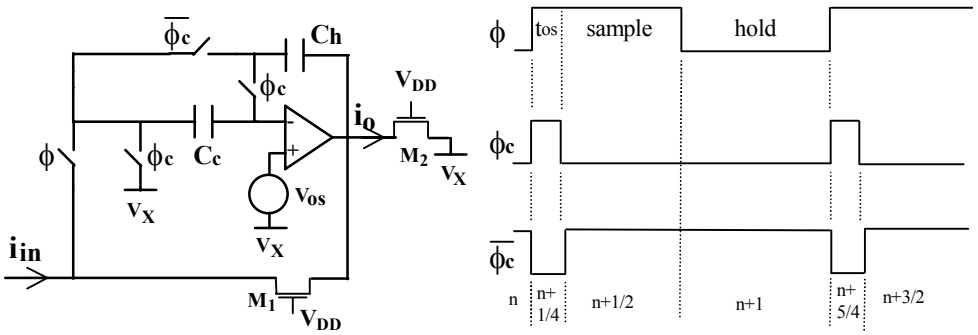


Fig. 3-3. SM half-delay cell with CDS for offset compensation.

Comparing (3-3) with (3-2) we note that the circuit in Fig. 3-3 not only attenuates V_{OS} by the DC gain of the op-amp but also eliminates the effect of V_X at the output. As a drawback, there is a term (the right-most one in (3-3)) that depends on the previous sample. Nevertheless, this term is attenuated by the DC gain of the op-amp and, in most cases, is not significant.

An appropriate switching sequence is fundamental for the correct operation of the circuit in Fig. 3-3. If ϕ_c closes before $\overline{\phi_c}$ opens, a fraction of the charge stored in C_C may be lost.

The result shown in (3-3) is similar to that obtained for schemes of offset correction in SC circuits [36].

3.2.2 Auto zero in the SM half-delay cell

We propose the auto-zero (AZ) structure shown in Fig. 3-4 for offset compensation. In this structure, the compensation capacitor is inserted in anti-series with the bias voltage during sampling and holding, and the holding capacitor does not need any switching during AZ. As a result, the AZ structure is less susceptible to charge injection and distortion than the CDS circuit in Fig. 3-3. However, to prevent glitches a more complicated clock scheme, as the one shown in Fig. 3-5, is necessary. The circuit operates

as follows: during t_{az}, only the switches controlled by ϕ_{c1} and ϕ_{c2} are closed. C_{AZ} is in parallel with the inputs of the op-amp and thus, considering an ideal operational amplifier, the voltage across C_{AZ} equals V_{OS}. After t_{az}, ϕ_{c1} and ϕ_{c2} are open and ϕ_{cn} is closed. The voltage across C_{AZ} is equal to V_{OS} but its polarity is opposite to the op-amp offset voltage. Ideally, a complete compensation of the offset voltage is achieved.

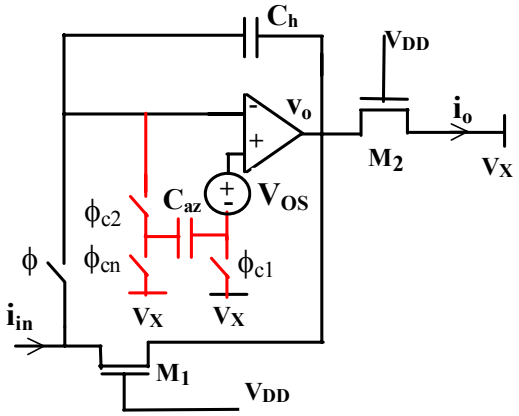


Fig. 3-4. SM half-delay cell with AZ for offset compensation.

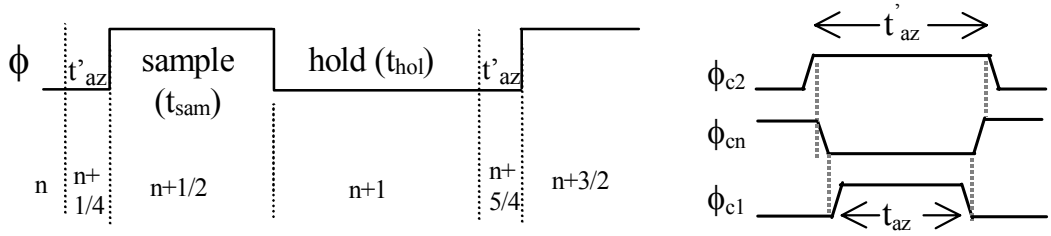


Fig. 3-5. Clock sequence for the circuit in Fig. 3-4.

Considering the op-amp to have a finite DC gain A, we have for the circuit in Fig. 3-4:

$$i_o(n+1) \cong -\frac{i_{in}(n+1/2)}{1+A^{-1}} + \frac{A^{-1}.V_{OS}}{\left(1+A^{-1}\right)^2}\frac{1}{R} - \frac{A^{-1}.i_{in}(n-1/2)}{1+(2+K_a)A^{-1}} \tag{3-4}$$

where $K_a \equiv (C_{AZ}/C_h)$ and $R = \left(\partial I_D / \partial V_S\right)^{-1}\Big|_{V_S=V_D=V_X} = \left[0.707\mu_n C'_{ox}(W/L)(V_{DD}-V_{T0})\right]^{-1}$.

Expression (3-4) is identical to (3-3), i. e., the offset compensation achieved with the proposed AZ circuit is the same as for the CDS circuit. We will concentrate, in the coming chapters and sections, on offset compensation with the AZ circuit.

Time to perform AZ

During consecutive AZ intervals, charge is injected into the AZ capacitor (C_{AZ}). Thus, a certain amount of time is required to recharge C_{AZ} to V_{OS}. Fig. 3-6 shows the small signal equivalent circuit for the circuit in Fig. 3-4 during t_{az}.

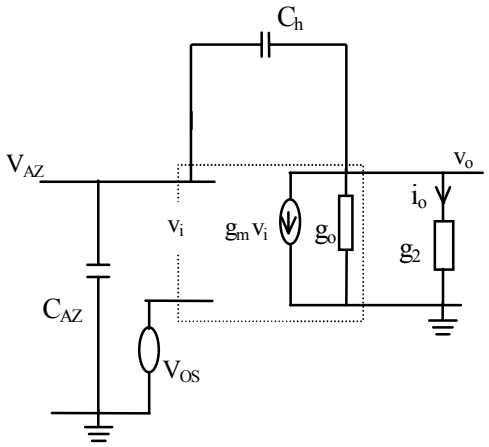


Fig. 3-6. Small signal equivalent circuit for determining t_{az}.

Considering now that the op-amp finite transconductance is represented by a single-pole function, that is, $g_m = g_m(s) = \dfrac{g_{mo}}{1 + s/\omega_1}$ where ω_1 is the dominant pole of the loaded op-amp, we have (appendix A):

$$t_{az} \geq \frac{(1+K_a)g_L}{g_{mo}\omega_1} ln(1/|\gamma|) = \frac{(1+K_a)}{\omega_u} ln(1/|\gamma|) \qquad (3\text{-}5)$$

where γ is the maximum percent error in the voltage across C_{AZ}, ω_u is the open loop unity-gain frequency of the loaded op-amp, $K_a \equiv C_{AZ}/C_h$ and $g_L = g_o + g_2$. g_2 is the drain-source conductance of transistor M_2, which in strong inversion is given [31] by:

$$g_{mS(D)} = \mu_n n C'_{ox}(W/L)(V_P - v_{S(D)}) \tag{3-6}$$

In SM, for zero input signal we have $v_S = v_D = V_X \cong 0.293V_P$. Thus, (3-6) can be rewritten as

$$g_{mS} = \mu_n n C'_{ox}(W/L)(0.707V_P) \tag{3-6a}$$

The result in (3-5) means that the time for auto-zero does not depend on C_{AZ} but on the ratio $K_a \equiv C_{AZ}/C_h$, and also on op-amp gain-bandwidth (GBW).

As an example, using technology CXE (0.8μm) from Austria Micro Systems (AMS), $C_{AZ} = C_h$ = 5pF, transistors with (W/L)=10μm/20μm and 1.5V supply voltage, the amp-op designed for use in the first chip (chapter 5) presents $\omega_u = 2\pi.700$kHz. Thus, we have $t_{az} \geq (0.45\mu s)ln(1/|\gamma|)$. For an 8-bit error (γ=0.004) , $t_{az} \geq 2.5\mu$s. It is important to note that (3-5) is based on a worst case approximation (appendix A). Thus, this value for t_{az} of 2.5μs can be considered to be a lower bound.

Clock generation for the AZ circuit

Even though the AZ circuit uses a more complicated clock scheme than the circuit with CDS, a clock generator for the AZ circuit can be carried out with a simple circuit such as the one in Fig. 3-7. For obtaining the clock signals ϕ_{c2}, ϕ_{cn} and ϕ_{c1} (Fig. 3-5) with t_{az} of about 1/8 of the sampling period, an input signal frequency 4 times higher than the sampling frequency is required. Thus, with a sampling frequency of 50kHz, t_{az} is about

2.5µs. It is important to mention that the time for AZ is not critical. In the example shown in the previous section an 8-bit error was considered.

The circuit in Fig. 3-7 was simulated with OrCAD/Pspice for several different gate propagation times. The response of the circuit can be seen in Fig. 3-8 (more than two cycles) and in Fig. 3-9 (detail). The correspondence between the clock lines in Fig. 3-5 and the labels in Fig. 3-8 and 3-9 is as follows: ϕ_{c2} = *X2B:A*, ϕ_{cn} = *ezcnB:Q* and ϕ_{c1} = *ezc1B:Q*. For obtaining the signal ϕ, Fig. 3-5, a very simple circuit like the one in Fig. 3-10 must be added.

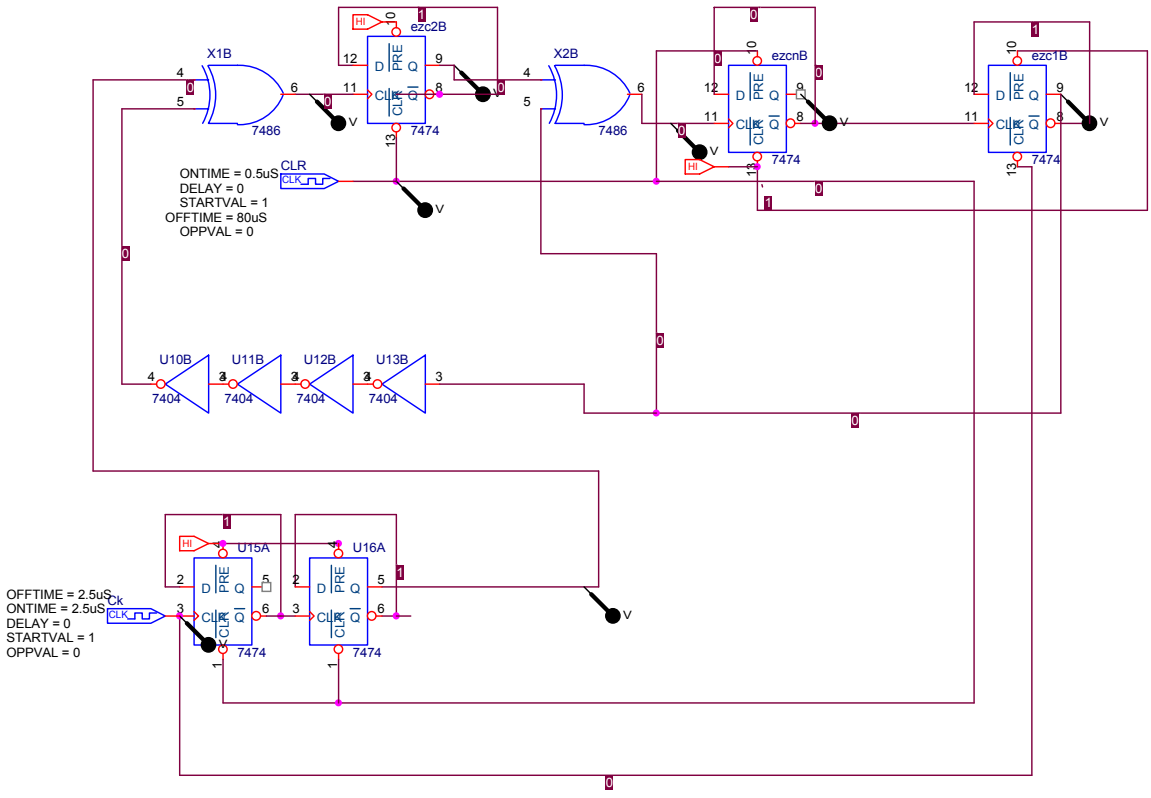


Fig. 3-7. Clock generator for the AZ circuit.

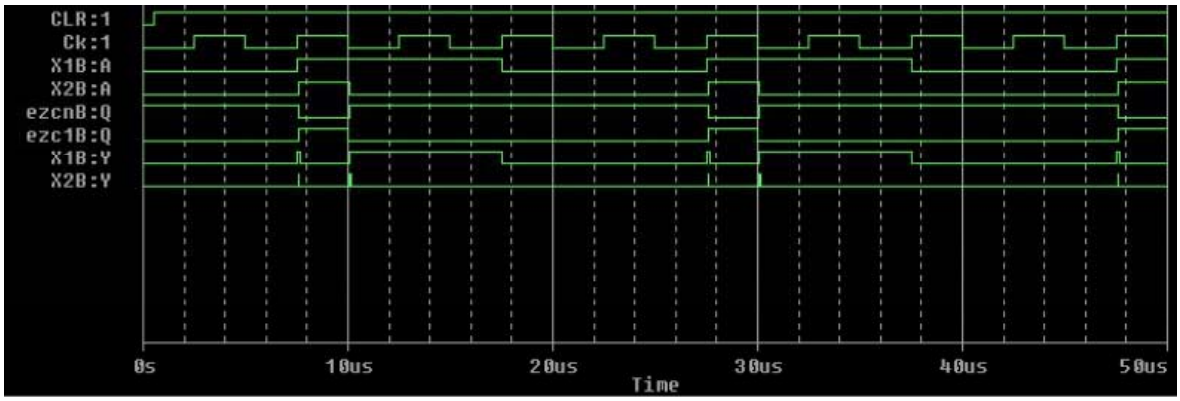


Fig. 3-8. Signals for the circuit in Fig. 3-7.

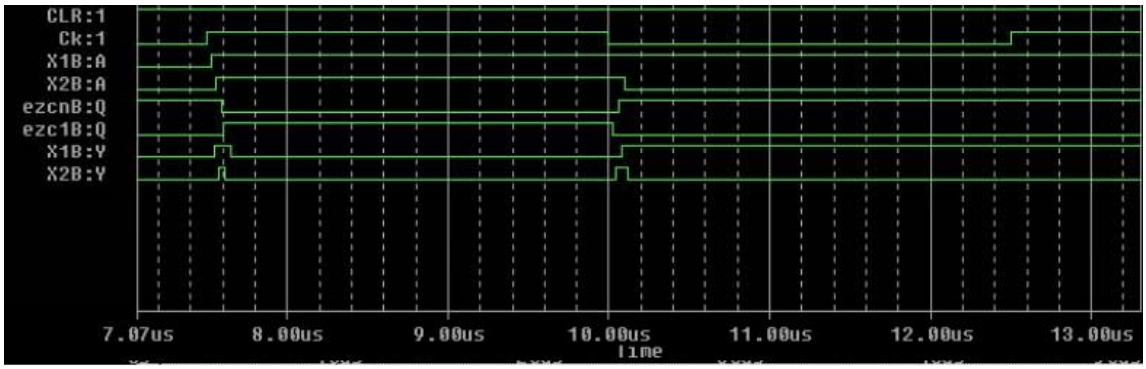


Fig. 3-9. Signals for the circuit in Fig. 3-7 - detail.

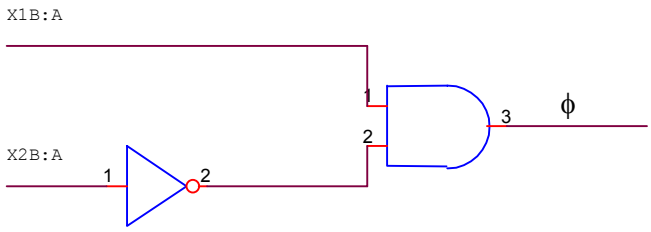


Fig. 3-10. Circuit for obtaining the signal ϕ.

3.2.3 Comparison between half-delay cells with and without offset correction

Analytically, the difference between the circuits without offset correction (Fig. 3-2) and with offset correction (Fig. 3-3, CDS and Fig. 3-4, AZ) is expressed in equations (3-2)

through (3-4). To show more details of the imperfections, some simulation results will now be presented. For the simulations, SMASH simulator together with BSIM 3v3 models for technology CXE (0.8μm) from Austria Micro Systems (AMS) were used. The circuits of Fig. 3-2, Fig. 3.3 and 3-4 were simulated in 3 different cases: (i) no offset in the operational amplifier; (ii) a +10mV offset in the op-amp; and (iii) a –10mV offset in the op-amp. For the three circuits, C_C=C_{AZ}=C_h = 5pF, the transistors have (W/L)=10μm/40μm, and the switches are minimum size, i. e., (W/L)=0.8μm/0.8μm. The supply voltage is 1.5V and the op-amp presents a unity-gain frequency of 1MHz and a DC gain of 64dB (with a load of a 10μm/40μm transistor).

Table 3-1 sums up the results obtained. In Table 3-1, I_{M2a}, I_{M2b}, and I_{M2c} are the currents in the circuits in Fig. 3-2 (no offset correction), Fig. 3-3 (CDS), and Fig. 3-4 (AZ), respectively.

Table 3-1 Simulations of offset current in the circuits of Fig. 3-2, Fig. 3-3 and Fig. 3-4.

Offset op-amp	I_{M2a} (no offset correction)	I_{M2b} (CDS)	I_{M2c} (AZ)
0	1nA	2.8nA	-0.8nA
+10mV	156nA	23nA	0.3nA
-10mV	-162nA	-18nA	-1.8nA

The results in Table 3-1 indicate the circuit with CDS does not compensate the offset as well as the circuit with AZ. This is mainly due to the fact that the offset voltage is stored in C_C with the main switch (clock ϕ, Fig. 3-3) closed and, thus, the voltage in the left side of C_C is not exactly V_X during t_{os} due to the resistances of the switches (compare the clock schemes in Fig. 3-3 and Fig. 3-5). This problem can be attenuated either with a different clock scheme or with larger switches (in this case the charge injection is increased), but still the circuit with AZ will behave better than the circuit with CDS. Hence, in the next sections only AZ will be considered.

3.3 Settling Time

In the SM half-delay cell, as in any sampled circuit, during sampling an error due to settling will occur. To keep distortion within acceptable values, the settling error must be small. The analysis that follows is valid for both previous circuits, be it with or without offset compensation. The only difference is that the time available for sampling (t_{sam}) is smaller in the circuit with offset compensation due to t_{az}.

For both the circuits in Fig. 3-2 and Fig. 3-4, the settling error is given by

$$\gamma = e^{-t_{sam}/\tau} \tag{3-7}$$

where t_{sam} is either $T/2$ (T is the clock period), in the circuit without offset compensation; or $(T/2)$-t_{az}, in the circuit with AZ; and τ is a time-constant which depends on the hold capacitor, the transistor conductances, and the gain-bandwidth product of the op-amp. In the analysis that follows, we will calculate the value of C_h in order to keep the settling error below a given value.

The small-signal equivalent circuit for the half-delay cell during sampling, for both circuits in Fig. 3-2 and in Fig. 3-4, is shown in Fig. 3-11. The resistance of the switches is assumed to be negligible. The output impedance of the previous stage is added to g_s.

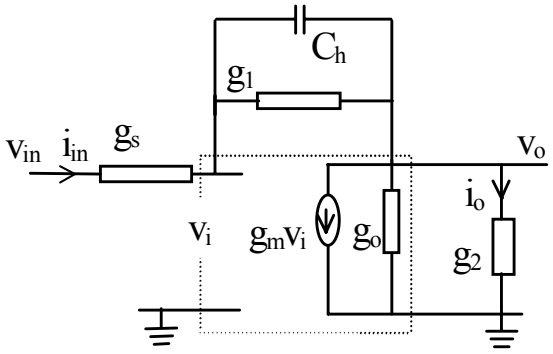


Fig. 3-11. Small-signal equivalent circuit for the SM half-delay cell.

For the circuit in Fig. 3-11, considering the op-amp finite transconductance represented by a single-pole function, that is, $g_m = g_m(s) = \frac{g_{m0}}{1 + s/\omega_1}$ where ω_1 is the pole frequency of the loaded op-amp and $g_L = g_o + g_2$, we have (appendix B):

$$C_h \le g_1 t_{sam} \frac{1}{ln(1/|\gamma|)} - \frac{g_s g_1 / g_L + g_s + g_1}{2\pi f_u} \tag{3-8}$$

in order to have a settling error smaller than γ. Here, f_u is the unity-gain frequency of the loaded op-amp, g_1 and g_2 are the drain-source conductances of the transistors, which in strong inversion are given by (3-6).

Considering an 8-bit settling error (γ = 0.004), g_s=g_1=g_2 and g_o>>g_1, (3-8) can be rewritten as:

$$C_h \le \frac{g_1}{2(5.52)} \frac{1}{f_s} - \frac{g_1}{\pi} \frac{1}{f_u} \tag{3-9}$$

where f_s is the sampling frequency. Therefore, if $f_u < 3.5 f_s$, (3-9) has no solution. This constraint on f_u is the same as for SC circuits [23].

The values calculated using (3-9) for maximum capacitance present very good agreement with the maximum capacitance obtained from simulation (appendix B).

3.4 Noise

The dynamic range of a circuit is the ratio of the maximum signal to be applied to the circuit (limited by distortion) to the minimum signal that can be processed by the circuit. The last one is limited by noise. Hence, it is very important to determine the noise levels for the SM circuits.

For noise analysis, the methodology proposed in [37] has been employed. It consists in decomposing the equivalent noise circuit into time-invariant subcircuits, valid for specific time intervals, and into a transientless sampled-data network with band-limited noise sources. First, in the next subsection, the noise sources will be analysed.

3.4.1 Noise in transistors and in operational amplifier

The MOSFET noise is composed of both flicker (1/*f*) noise and white noise. However, the flicker noise contribution is generally submerged by aliased broadband components [37], if either CDS or AZ is used [38]. Thus, only the white noise component will be considered here.

The power spectral density of the thermal noise (current) in MOSFETs valid from weak to strong inversion is given [8] by

$$S_{Id,th}(f) = \frac{-4\theta\mu_{n(p)}Q_I}{L^2} \tag{3-10a}$$

where Q_I is the total inversion charge, θ = kT, k is the Boltzmann's constant and T is the absolute temperature. From (3-10a), it follows that the MOSFET thermal noise is the same as the one produced by a conductance $G_{N,th}$ whose value is [8]

$$G_{N,th} = \frac{\mu_{n(p)}|Q_I|}{L^2} = g_{ms}\frac{Q_I}{Q_{IS}^{'}WL} \tag{3-10b}$$

where $Q_{IS}^{'}$ is the inversion charge density at source. In the linear region, the inversion charge density along the channel is almost uniform; thus, $Q_{IS}^{'} \cong Q_I / WL$ and the conductance $G_{N,th}$ equals the source transconductance. In saturation, the relation between $G_{N,th}$ and g_{ms} becomes

$$G_{N,th} = \frac{1}{2}\ g_{ms} \text{ in weak inversion} \tag{3-10c}$$

$$G_{N,th} = \frac{2}{3}\ g_{ms} \text{ in strong inversion} \tag{3-10d}$$

For the accurate calculation of the thermal noise, one can refer to [8]. For both the calculation of thermal noise in the linear region or its estimation in saturation, one can use

$$S_{Id,th}(f) \cong 4\theta g_{ms} \tag{3-10e}$$

A very common mistake in the calculation of the thermal noise is the substitution of g_{ms} with g_{mg}, the gate transconductance, in (3-10e). This substitution gives completely erroneous values for the thermal noise in the nonsaturation region because $g_{mg} << g_{ms}$, particularly near the origin ($V_D = V_S$) [8].

For the op-amp in Fig. 3-12, the spectral density (unilateral representation) of the white noise referred to the input is given by [8, 39]:

$$S_{eq}(f) = 8\theta\frac{n^2}{g_{ms\_M1}} + 8\theta\left(\frac{g_{m\_M3}}{g_{m\_M1}}\right)^2 \frac{1}{g_{ms\_M3}} \tag{3-11}$$

For the derivation of (3.11), the noise contributed by the op-amp second stage has been assumed to be negligible.

Besides the noise generated in the op-amp, in the SM half-delay cell the transistors and switches also generate noise. The derivation of the noise contribution of the transistors or of the ON switches yields a series connected noiseless resistor with a noise voltage source of uniform spectral density given by

$$S_i(f) = 4\theta R_i = \frac{4\theta}{g_{ms\,i}} \tag{3-12}$$

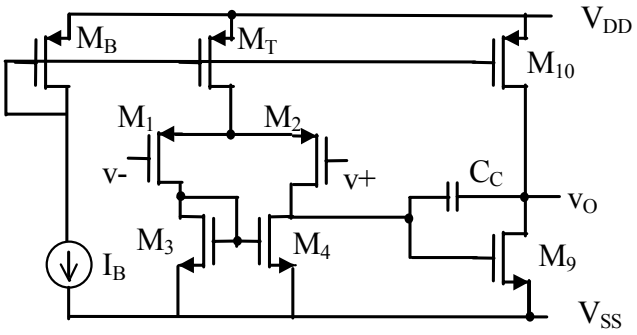


Fig. 3-12. Simple op-amp.

3.4.2 Noise in the delay cell

In any sampled-data technique, the output noise spectrum consists in general of a broad-band component due to a continuous-time noise signal (direct noise) and of a narrow-band contribution resulting from a sampled noise signal. In the SM half-delay cell with AZ, the output noise spectrum consists of three different direct noise components, coming from 3 different subcircuits (one valid during AZ, one valid during sampling, and one valid during holding) and of two sampled-and-held components (in C_h and in C_{AZ}).

Consider first the simple sample-and-hold circuit in Fig. 3-13 with $v_{in} = 0$. When the switch is ON (during time t_{on}) , there is broad-band noise present at the output due to the switch resistance R_{on}. When the switch opens, the noise is sampled-and-held in the capacitor. Considering that in the S/H circuit a nearly complete charging of C must occur (say, within a 0.1% settling accuracy) when the switch is ON, t_{on} must be at least $7R_{on}C$, which makes the direct noise bandwidth $f_{SW} = \dfrac{1}{4R_{on}C}$ at least 3.5 times bigger than the sampling frequency f_s. This means that aliasing occurs, concentrating the full noise power of the switch resistor into the baseband [23]. The direct (broad-band) noise contribution, $S^b(f)$, and the sampled-and-held noise contribution $S^{S/H}(f)$ to the output are given [23] by (one-sided)

$$S^b(f) \cong 4m\theta R_{on} \tag{3-13}$$

$$S^{S/H}(f) = 2(1-m)^2 \frac{\theta}{Cf_s} \tag{3-14}$$

where $m \equiv t_{on}/T$. For low (baseband) frequencies, with $m \leq 0.5$ the ratio $r = \frac{S^{S/H}(f)}{S^b(f)} \geq 3.5$. For $m = 0.25$, $r = 31.5$.

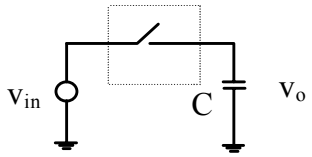


Fig. 3-13. Simple sample-and-hold circuit.

The above considerations imply that the direct noise contribution of the AZ noise subcircuit is negligible when compared with the sampled-and-held noise in C_{AZ} and that the direct noise contribution of the sampling noise subcircuit is negligible when compared with the sampled-and-held noise in *Ch*. Thus the noise analysis will concentrate in the direct noise in the holding period and in the sampled-and-held noise in both C_{AZ} and C_h.

In the holding period, the direct noise contribution to the output is (appendix C):

$$S^b_{hol}(f) \cong \frac{t_{hol}}{T} 4\theta \left[(R_{eq}) \frac{1}{1+\left(\frac{\omega}{\omega_u}\right)^2} \right] \tag{3-15}$$

where R_{eq} is an equivalent resistor for the op-amp input referred noise.

The contribution to the output of the sampled-and-held noise in C_{AZ} is (appendix C):

$$S^{S/H}_{Caz\_out}(f) = \frac{2\theta}{f_s C_{AZ}} \left(1 + \frac{R_{eq} C_{AZ} \omega_u}{1+K_a}\right) \left[\left(1+\frac{R_1}{R_s}\right)^2 (t_{sam}/T)^2 + (t_{hol}/T)^2 \right] \tag{3-16}$$

where $K_a \equiv C_{AZ}/C_h$, R_{eq} is an equivalent resistor for the op-amp input referred noise, and ω_u is the unity-gain frequency of the op-amp. The first term in the first parenthesis appears due to the noise sources of the transistors and the switches, which are not filtered by the op-amp rolloff.

The contribution to the output of the sampled-and-held noise in C_h is divided into two non-correlated components and is (appendix C):

$$S_{Ch\_1}^{S/H}(f) \cong \frac{2\theta}{f_s C_h}\left(1 + R_{eq} C_h \omega_u\right)(1 - t_{sam}/T)^2 \tag{3-17a}$$

and

$$S_{Ch\_2}^{S/H}(f) = \frac{2\theta}{f_s C_{AZ}}\left(1 + \frac{R_{eq} C_{AZ} \omega_u}{1 + K_a}\right)\left[\left(\frac{R_1}{R_s}\right)^2 (1 - t_{sam}/T)^2\right] \tag{3-17b}$$

The total noise in the output is the sum of the contributions given by (3-15), (3-16) and (3-17), i. e.,

$$S_{OUT}(f) = S_{hol}^{b}(f) + S_{Caz\_out}^{S/H}(f) + S_{Ch\_1}^{S/H}(f) + S_{Ch\_2}^{S/H}(f) \tag{3-18}$$

If we consider the circuit without offset compensation, as in Fig. 3-2, (3-16) and (3-17b) equal to zero.

An example will be given using technology CXE (0.8μm) from Austria Micro Systems (AMS), $C_{AZ} = C_h = 5$pF, transistors with (W/L)=10μm/20μm, sampling frequency of 50kHz, 1.5V supply voltage and the op-amp designed for use in the first chip (chapter 5) with $\omega_u = 2\pi.700$kHz. We have, from (3-18), considering the baseband frequency range (up to 25kHz):

$$\overline{(v_{OUT})}^2 = (5.7\mu\text{V})^2 + (31\mu\text{V})^2 + (40\mu\text{V})^2 + (27\mu\text{V})^2 = (58\mu\text{V})^2$$

We note from the example above that the main noise contribution is the sampled-and-held noise, being the broad-band noise negligible when integrated over the baseband.

However, as in general the next stage will sample the output of the half-delay cell, the broad-band noise sources are important due to aliasing in the next stage. Moreover, we note by (3.16) and (3.17) that the band-limiting performed by the op-amp is important in reducing the aliasing which enhances the sampled-and-held noise. Hence, ω_u should be chosen as low as possible while still allowing the adequate settling of the circuit.

3.5 Charge Injection

The charge injected by the switches is one of the main problems to be handled in a sampled-data technique. Charge injection can produce both residual offset and harmonic distortion. The charge injected by a MOS switch when it is turned OFF has two components [38, 40]. The first one is called clock feedthrough and is caused by the overlap gate/drain and gate/source capacitances. The second one is due to the channel charge, which has to flow through drain and source when the switch opens. In general, the channel charge is the dominant one [38]. These two contributions will be analysed separately in the following subsections.

3.5.1 Charge injection due to overlap capacitances

When a MOS switch turns off, the voltage variation in a linear capacitor C connected to the switch due to the overlap capacitances is

$$\Delta V_{ov} \cong \Delta V_{GB(OFF)} \frac{C_{ov}}{C_{ov} + C} \tag{3-19}$$

where $\Delta V_{GB(OFF)}$ is the gate-substrate voltage variation when the transistor is cut off. Roughly speaking, the transistor cuts off when $(V_{GB} - V_{T0})/n < V_{SB}$, where V_{T0} is the

transistor threshold voltage and n is the slope factor [8]. In the switched-MOSFET technique, according to what was explained in the previous chapter, all switches operate at constant voltage $V_X = V_P(1\text{-}1/\sqrt{2}) \cong 0.3(V_{DD} - V_{T0})/n$, V_p is the pinch-off voltage [8, 31]. Hence, in the SM switch, $\Delta V_{GB(OFF)} \cong 0.7V_{T0} + 0.3\ V_{DD}$. Also, as generally $C >> C_{ov}$, we have:

$$\Delta V_{ov} = \left(0.7V_{T0} + 0.3V_{DD}\right)\frac{C_{ov}}{C_{ov} + C} \cong \left(0.7V_{T0} + 0.3V_{DD}\right)\frac{C_{ov}^{'}W}{C} \tag{3-20}$$

3.5.2 Charge injection due to channel charge

For the analysis of the effect of the channel charge, we assume the inversion charge density in strong inversion to be given [8] by:

$$Q_I^{'} \cong -nC_{ox}^{'}\left(V_p - V_c\right) \tag{3-21}$$

where V_c is the channel voltage, equal to V_X in switched-MOSFET. Substituting $V_c = V_X$ and $V_p = (V_{DD}\text{-}V_{T0})/n$ [8] into (3-21) yields

$$Q_I = WLQ_I^{'} \cong -WLC_{ox}^{'}\frac{V_{DD} - V_{T0}}{\sqrt{2}} \tag{3-22}$$

where W and L are the effective width and length of the channel, respectively. When the transistor turns off, this charge is removed from the channel through the source and the drain. The amount of charge that flows through each terminal has been determined elsewhere and depends on the equivalent capacitance on each terminal and on the switching parameter [40, 49], determined mainly by the transistor ON resistance R_{on} and the slope of the clock signal applied to the gate. In the worst case, all the channel charge would be transferred to the (hold or auto-zero) capacitor, i. e.:

$$\Delta V_{cc\_c\_max} = \frac{Q_I}{C} \tag{3-23}$$

The subscript in (3-23) means *Channel Charge in capacitor C, MAXimum value*, with Q_I given by (3.22).

3.5.3 Charge injection in the SM half-delay cell

Consider the basic half-delay cell of the Switched-MOSFET technology, repeated in Fig. 3-14 for convenience. When S_W opens, charge is injected into the holding capacitor C_h. The total maximum (worst case) voltage variation in C_h due to both clock feedthrough and channel charge is

$$\Delta V_{ch\_max} = \left(0.7V_{T0} + 0.3V_{DD}\right)WC'_{ov}\left(\frac{1}{C_h}\right) + WLC'_{ox}\frac{V_{DD} - V_{T0}}{\sqrt{2}}\left(\frac{1}{C_h}\right) \tag{3-24}$$

Now consider the SM half-delay cell with auto-zero offset compensation, repeated for convenience in Fig. 3-15. The effects of the 4 switches of the offset compensated SM half-delay cell will be analysed separately:

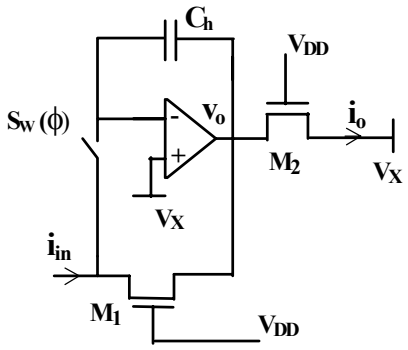


Fig. 3-14. The basic half-delay cell of the SM methodology.

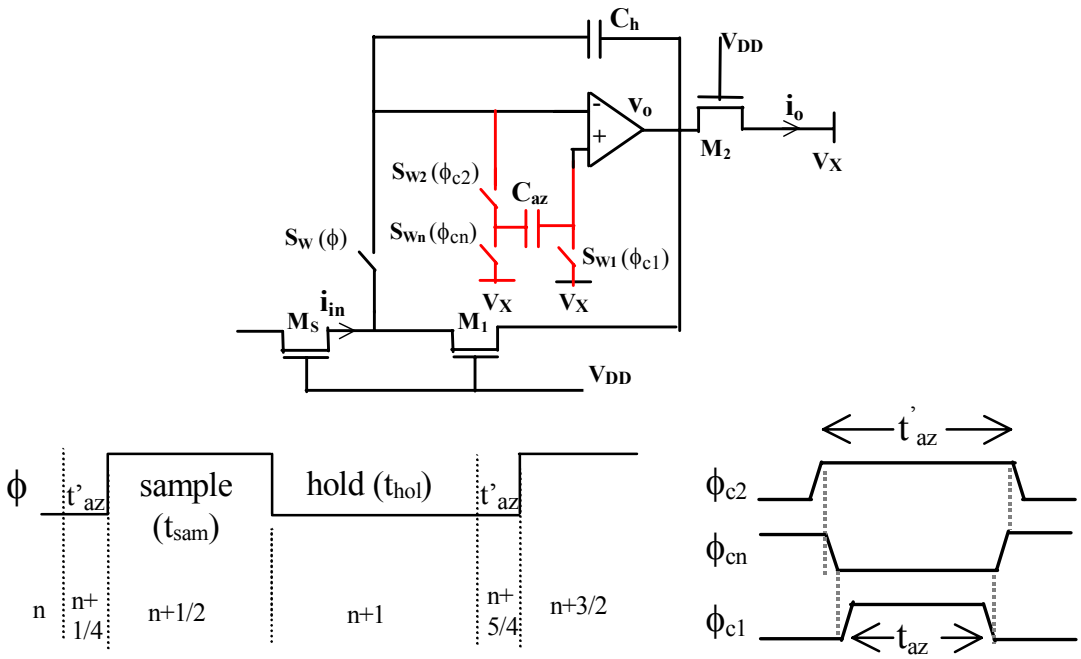


Fig. 3-15. The SM half-delay cell with auto zero.

Effect of S_{W2}

When S_{W2} opens, the charge stored in C_{AZ} does not change (see clock scheme in Fig. 3-15), considering a very high input impedance for the op-amp. After S_{W2} opens, the sampling period will begin. So, the charge injected by S_{W2} into C_h is also irrelevant.

Effect of S_{Wn}

The very same considerations as for S_{W2}.

Effect of S_{W1}

Considering that the whole channel charge from S_{W1} transfers to C_{AZ} (worst case), the voltage variation in C_{AZ} due to the charge injected by S_{W1} at the end of the AZ phase is:

$$\Delta V_{caz} \le \Delta V_{max\_caz} = (0.7V_{T0} + 0.3V_{DD})WC'_{ov}\left(\frac{1}{C_{AZ}}\right) + WLC'_{ox}\frac{V_{DD} - V_{T0}}{\sqrt{2}}\left(\frac{1}{C_{AZ}}\right) \quad (3\text{-}25)$$

The charge injected by S_{W1} is equivalent to a non-compensated offset. Considering $M_1 = M_S$ (Fig. 3-15), the output offset voltage due to the charge injected into C_{AZ} is

$$\Delta V_{o\_caz} = \left[2\Delta V_{caz} / \left(1 + 2 / A\right)\right] \cong 2\Delta V_{caz} \tag{3-26}$$

where A is de DC gain of the op-amp.

Using AMS CXE (0.8μm), which presents $C'_{ov} = 0.34\, fF/\mu m, C'_{ox} = 2\, fF/\mu m^2$, V_{DD} =1.5V, 10μm/20μm transistors, 2μm/0.8μm switches and C_{AZ} = 5pF, the maximum voltage variation in C_{AZ} due to the charge injected by S_{W1} is 0.4mV and the maximum offset current caused in M_2 (Fig. 3-15, considering the operating point $V_S = V_X$) is 9nA. This offset current corresponds to 0.2% of I_{max} for the transistor, being I_{max} given by (2-5) .

Effect of S_W

The charge injected by S_W does not influence C_{AZ}. The voltage variation in C_h due the charge injected by S_W is equal to the case without offset compensation and is given by (3-26). This charge produces an effect in direction opposite to the effect produced by the charge injected by S_{W1}. Unfortunately, even if these two switches are matched and if we consider that the whole charge of S_W flows to C_h and that the whole charge of S_{W1} flows to C_{AZ}, there is no complete cancellation of the two effects because the voltage stored in C_{AZ} is doubled at the output (considering equal transistors), while the voltage stored in C_h appears directly at the output.

3.6 Harmonic distortion

In this section, we analyse the influences of op-amp offset, charge injection, component mismatch and finite op-amp DC gain on the harmonic distortion, for the half-delay cells in Fig. 3-2 and 3-4. When the analysis is valid for both circuits we will refer to both simply as “the SM half-delay cell”.

3.6.1 Effect of op-amp offset voltage

Considering the op-amp DC gain to be very high and neglecting other sources of error, the op-amp offset voltage will have influence on the output current in the SM half-delay cell as given by (appendix D)

$$i_{o(n)} = -\frac{(W/L)_2}{(W/L)_1} i_{in(n-1/2)} + \frac{\sqrt{2}}{2} \mu C'_{ox} n (W/L)_2 V_{OS} V_P \tag{3-27}$$

According to (3-27), the offset voltage of the op-amp does not introduce harmonic distortion, but just an offset in the output current.

3.6.2 Effect of the charge injected

In the SM half-delay cell, the channel charge of the switches is signal-independent because the switches operate at constant voltage. Nevertheless, the fraction of the charge that flows to C_h depends on the impedances on both sides of the switch, which are assumed to be signal-independent [40]. Thus, the voltage error introduced in C_h due to charge injection will be considered to be constant (for that, C_h has to be linear). Even though the charge injected into the capacitor is signal-independent, this error will give rise to harmonic distortion since the voltage to current (v-to-i) conversion is nonlinear. As the harmonic distortion caused by charge injection is independent of the frequency of the input

signal, the distortion can be analysed by considering a signal distorted by a static non-linear transfer function; thus (appendix D):

$$i_{O(t)} \cong 2\sqrt{2}\frac{\Delta V_{ch}}{V_P} I_{max} - \hat{I}\cos(\omega t) - \frac{\sqrt{2}}{8}\frac{\Delta V_{ch}}{V_P}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{\sqrt{2}}{32}\frac{\Delta V_{ch}}{V_P}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t)... \quad (3\text{-}28)$$

where $\hat{I} \le I_{MAX} = \frac{\mu C'_{ox} n}{4}\frac{W}{L}V_P^2$ is the peak input current, and ΔV_{ch} is the voltage variation in C_h due to charge injection. The first term on the right hand side of (3-28) is the offset current. If we neglect clock feedthrough, the offset current becomes:

$$\frac{I_{OS}}{I_{max}} \le 2n\frac{C_{switch}}{C_h} \quad (3\text{-}29)$$

where $C_{switch} \equiv C'_{ox}(WL)_{switch}$.

In the circuit of Fig. 3-4, the charge injected into C_{AZ} does not produce any distortion but only residual offset because the effect of the charge injected into C_{AZ} is similar to the one produced by the op-amp offset voltage.

The calculation of the offset current with 1.5V supply voltage, 10µm/20µm transistors and 2µm/0.8µm switches, C_h=5pF and CXE 0.8µm AMS technology using (3.35) results in:

Offset current (I_{OS}/I_{Omax}) ≤ 0.22%.

The total harmonic distortion due to charge injection (THD_{ci}) ≤ 0.015%.

3.6.3 Effect of component mismatch.

A difference in the transconductance parameters $\left(\mu C'_{ox}(W/L)\right)$ produces a relative gain error proportional to the mismatch in the transconductance parameters. A mismatch in

the threshold (pinch-off) voltage causes gain error and harmonic distortion, summarised by the following expression [27]:

$$x_2 = \left(1 + \frac{\Delta V_P}{V_P}\right) x_1 + \frac{\Delta V_P}{V_P}\left(\frac{x_1^2}{8} + \frac{x_1^3}{32} + ..\right) \tag{3-30}$$

where $\frac{\Delta V_P}{V_P} = \frac{\Delta V_{TO}}{V_{DD} - V_{TO}}$ is the threshold voltage mismatch normalised to the overdrive voltage and $x_1 = i_{in}/i_{in\,max}, x_2 = i_o/i_{o\,max}$ are the normalised input and output currents.

3.6.4 Effect of finite op-amp DC gain

The influence of the finite op-amp DC gain A on the output current of the SM half-delay cell is given by (appendix D)

$$i_{O(t)} \cong \frac{2\left(1-\sqrt{2}\right)}{A} I_{max} - \hat{I}\cos(\omega t) - \frac{1}{8A}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{1}{32A}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t)... \tag{3-31}$$

As an example, in a half-delay cell with 1.5V supply voltage, 10μm/20μm transistors and 2μm/0.8μm switches, C_h=5pF, op-amp with A=100 and CXE 0.8μm AMS technology we have: (I_{OS}/I_{Omax}) = 0.83% and THD = 0.13%.

3.7 Implementation of an SM half-delay cell

An SM half-delay cell was implemented using AMS CSI, a 0.35μm CMOS process with V_T of 0.5V.

The operational amplifier was designed following the methodology described in chapter 5, section 5.2. The op-amp schematic and design values are shown in Fig. 3-16 and Table 3-2, respectively.

The op-amp and delay cell were integrated as test structures for a hearing-aid directional adapter and designed using Cadence/Virtuoso/AMSDesignKit. The measurement results will be described in this section. To meet the specifications for the adapter, 8pF holding capacitors, 2µm/10µm transistors and minimum size switches (0.6µm/0.35µm) were used.

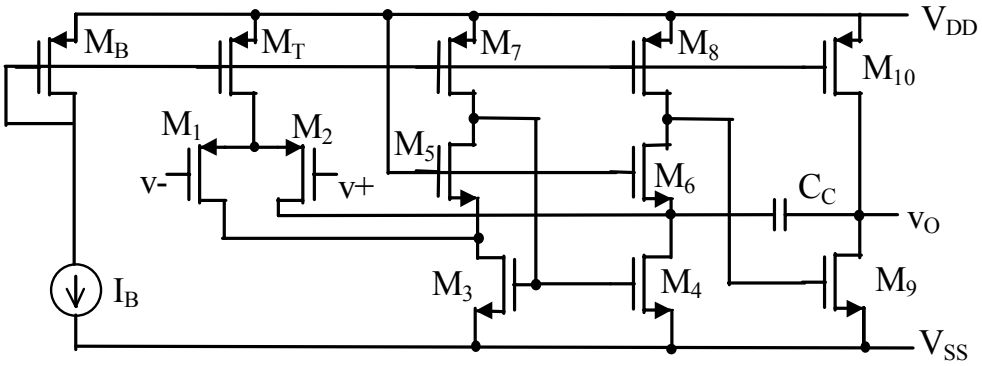


Fig. 3-16. Low-voltage class A op-amp [6, 43].

Table 3-2. Design values for the class A op-amp (Fig. 3-17).

L, all transistors	2.5µm
M1, M2	W=100µm
M3, M4	W=15µm
M5, M6	W=8µm
M7, M8	W=8µm
MB, MT	W=16µm
M9	W=67.5µm
M10	W=72µm
C_c	1.8pF
I_B	0.7µA

3.7.1 Op-amp measurements

The DC measurements were carried out using parameter analyser HP 4145B. Table 3-3 summarises the results.

Table 3-3 DC measurements for the AMS op-amp.

# op-amps tested	**Input offset voltage**	**Unloaded DC gain**	**Loaded DC gain** (R_L = 39kΩ)
4 samples	$\|V_{OS}\| <$ 4mV	≅ 74dB	≅ 49dB

The unity-gain frequency (f_u) and phase margin (PM) were measured in a unity-gain non-inverting amplifier configuration, like the one shown in Fig. 3-17. Measurements were performed both with V_{DD}=1V and V_{DD}=1.5V, and the results are almost the same for both supply voltages. The unity-gain frequency $f_u \cong$ 520kHz. The AC response of the circuit is shown in Fig. 3-18, where can be seen that there is an undesirable peak for some frequencies. Moreover, it was observed that the output signal for frequencies in the range where the gain is > 0dB (i.e., 200kHz- 440kHz) is distorted. The measured phase margin is only 20^o.

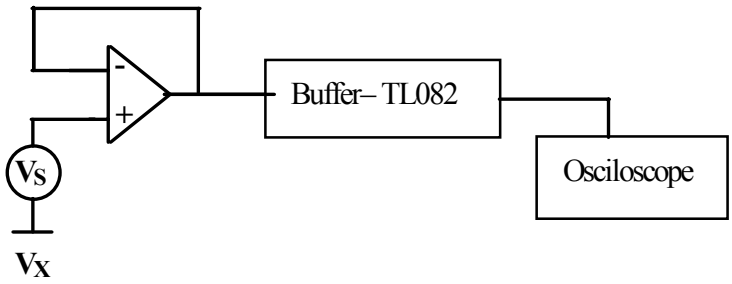


Fig. 3-17. Circuit for measuring f_u and PM.

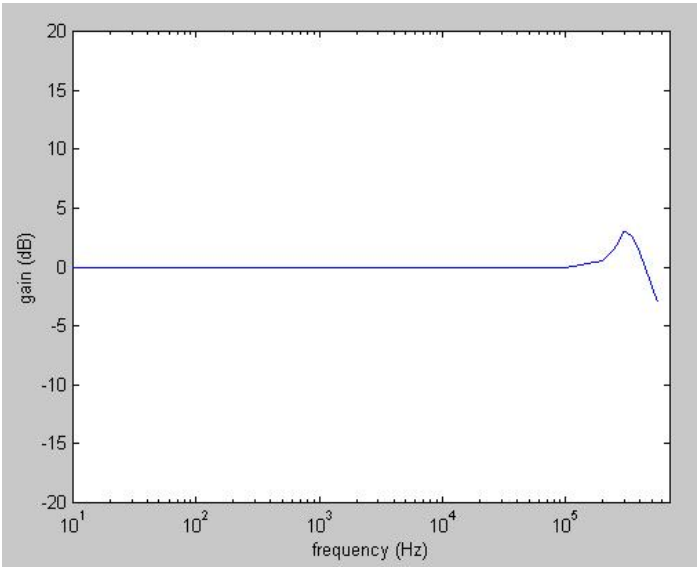


Fig. 3-18. AC response for circuit in Fig. 3.17.

3.7.2 Measurements in the half-delay cell

The schematic for the integrated SM half-delay cell is shown in Fig. 3-19.

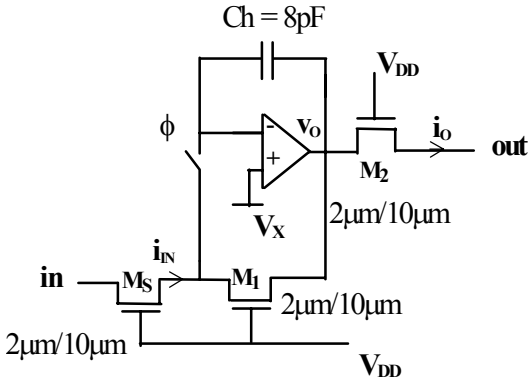


Fig. 3-19. The integrated SM half-delay cell.

For settling time measurements, a step of 100mV was applied at the input. The input voltage was changed from V_X to V_X + 100mV and then from V_X + 100mV to V_X. The measured settling time within 0.4% of the final value < 2.5μs. The total available time for settling = 7.5μs for a 50kHz sampling frequency with offset compensation. In fact, such a short time for settling was expected because following (3-8) the maximum allowable capacitor value for a 0.4% settling error is 22pF, and 8pF capacitors were used.

For distortion measurements, a voltage-to-current converter using off-the-shelf op-amps TL082 was designed. Distortion was measured for several input currents and several input frequencies. Fig. 3-20 shows the results thus obtained. The delay cell was designed to work with currents up to 1μA. The maximum current in the delay cell is 3μA[1]. In the input frequency (f_{in}) range up to 5kHz (f_s/f_{in} = 10), the distortion levels were < 1% for $I_{in} \leq$ 1μA (peak). For input currents up to 2μA, the distortion is function only of the second harmonic.

[1] In fact, according to (2-5), the maximum current is 6.6μA. But the measured delay cell is part of a bigger circuit where an offset current of 3.6μA flows (putting v_{out_DC} closer to V_{SS}).

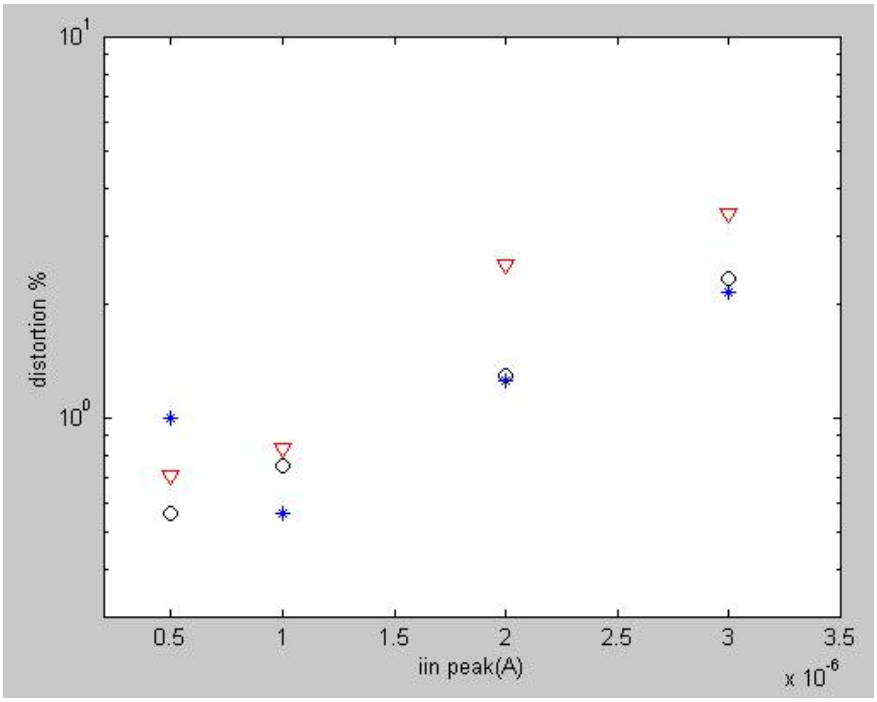


Fig. 3-20. Distortion as a function of the input current and input frequency. f_{in} = 500Hz (*), 1kHz (O), and 4kHz (∇).

For noise measurements, we used a low-noise amplification circuit, composed of 3 CA744 low-noise operational amplifiers, as shown to the right of the dashed lines in Fig. 3-21. The low-noise amplifier was powered by batteries and its characteristics are as follows: voltage gain = 10^4 and frequency range from 800Hz to 20kHz.

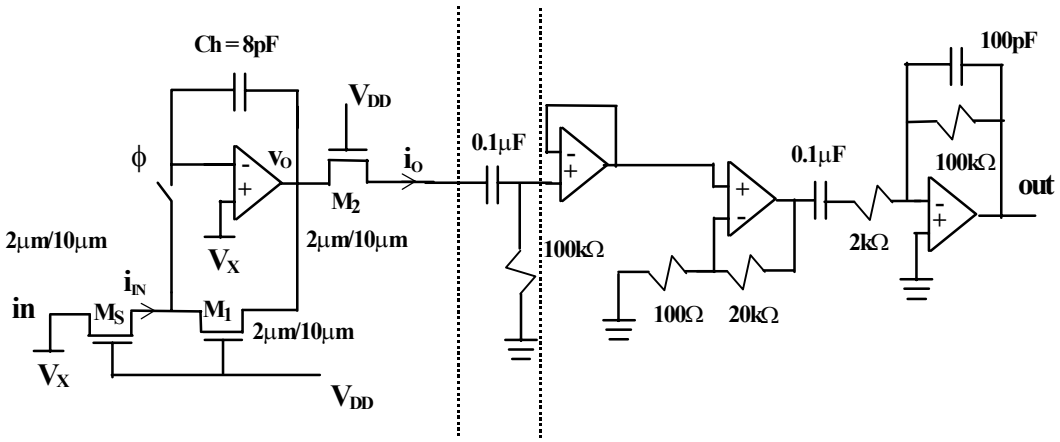


Fig. 3-21. Noise measurement of the SM half-delay cell.

The measured rms output noise was 135mV, which corresponds to a 18.9μV at the output of the operational amplifier of the SM half-delay cell. The expected value using (3-17a) is 16.3μV.

3.8 Summary

In this chapter, we analysed the basic SM half-delay cell, which is the basic building block of SM circuits.

The main imperfections in the SM half-delay cell are related to op-amp imperfections. The op-amp offset voltage can cause offset in the output current that will affect the dynamic range of the circuits, and in some applications offset compensation techniques, such as the AZ technique, must be used.

In section 3.3, the analysis of the settling time allowed to determine the maximum value of the holding capacitor, C_h, and the minimum value required for the op-amp gain-bandwidth. According to our results, op-amp bandwidth should be at least 3.5 times the sampling frequency in order to achieve a settling error consistent with an 8-bit resolution.

The noise analysis, important to determine the dynamic range of the circuits, includes both continuous-time (broad-band) noise and sampled-and-held noise. The sampled and-held noise, proportional to kT/C, is the most important source of noise.

Charge injection in SM circuits causes both residual offset and harmonic distortion, as shown in this chapter. Thus, the switches should be minimum size, being as main limitation the ratio between switch conductance/transistor conductance. The aspect ratio of the transistors depends on the operating current, and in some cases the width of the switch must be bigger than the minimum allowed by the technology to keep a good ratio of conductances.

In section 3.6, the main sources of harmonic distortion were considered. The analysis presented therein allows the determination of the minimum op-amp DC gain for a given distortion.

Finally, in section 3.7 the implementation of an SM half-delay cell was described and measurements results were presented.

Switched-MOSFET: system analysis 4

4.1 Introduction

In this chapter, we consider some other practical aspects that are important for the designer at the system level.

Firstly, in section 4.2, the influence of imperfections such as op-amp offset voltage in other important switched-MOSFET structures like the first- and second generation integrators and the universal biquad is analysed.

Switched-MOSFET circuits process currents. In some applications, the input and/or the output of the system is a voltage. In this case, additional voltage-to-current (v-to-i) and current-to-voltage (i-to-v) converters are required. Section 4.3 focuses on these converters. Finally, in section 4.4, a summary of the chapter is drawn.

4.2 Offset in other SM structures

The performance of integrators is affected by the op-amp offset voltage. The influence of the op-amp offset voltage on first and second generation integrators and on the biquad (built with 2 second generation integrators) will be analysed.

4.2.1 Effect of the offset voltage in the first generation integrator

In the first generation integrator in Fig. 2-7, considering the only non-ideal characteristic to be the op-amp offset voltage, we have (small signal analysis) [34]:

$$V_{OA}(z) = \frac{2V_{OS1} + \beta V_{OS1} - 2\beta V_{OS2}}{1-\beta z^{-1}} - \frac{V_i(z)}{1-\beta z^{-1}} \tag{4-1}$$

$$V_{OB}(z) = \frac{2V_{OS2} - \beta V_{OS1} - 2V_{OS1}}{1-\beta z^{-1}} + \frac{z^{-1}V_i(z)}{1-\beta z^{-1}} \tag{4-2}$$

where V_{OA} and V_{OB} are the voltages in the outputs of A_1 and A_2, respectively, V_{OS1} and V_{OS2} are the offset voltages of A_1 and A_2, respectively, and V_i is the input voltage, function of the input current.

According to (4-1) and (4-2), the output voltages resulting from the offset voltages of the op-amps tend to a very large value when $\beta \to 1$ (lossless integrator).

4.2.2 Effect of the offset voltage in the second generation integrator

In the second generation integrator in Fig. 2-9, considering the only non-ideal characteristic to be the op-amp offset voltage, we have [34]:

$$V_{OA}(z) = \frac{3V_{OS1} + 3\beta V_{OS1} - 2V_{OS2} - \beta V_{OS2}}{1+\beta-z^{-1}} - \frac{V_i(z)}{1+\beta-z^{-1}} \tag{4-3}$$

$$V_{OB}(z) = \frac{2V_{OS2} + \beta V_{OS2} - 3V_{OS1}}{1+\beta-z^{-1}} + \frac{z^{-1}V_i(z)}{1+\beta-z^{-1}} \tag{4-4}$$

where V_{OA} and V_{OB} are the voltages in the outputs of A_1 and A_2, respectively, and V_{OS1} and V_{OS2} are the offset voltages of A_1 and A_2, respectively.

According to (4-3) and (4-4), the output voltages resulting from the offset voltages of the op-amps tend to a very large value when $\beta \to 0$ (lossless integrator).

4.2.3 Offset in the biquad

In the universal switched-MOSFET biquad in Fig. 2-11, the output voltage as a function of the op-amp offset voltages is (appendix E):

$$V_{OB2}^{\phi_e} = -\frac{(V_{11} - V_{12})}{\omega_o T}\left[2 + \frac{1}{Q} + \frac{K_{BP}}{Q}\right] + 2V_{12} \tag{4-5}$$

where V_{11} and V_{12} are the offset voltages of A_{11} and A_{12}, respectively, and K_{BP} is the band-pass input gain.

According to (4-5), the DC output voltage is a function of the offset voltage of the op-amps of the first stage in the biquad only (i. e., the offset voltage of A_{21} and A_{22} are not important). In fact, the presence of offset voltages in A_{21} and A_{22} produces DC currents at the input of the second integrator, a high-pass input, and thus these DC currents are eliminated.

It is also very important to notice that the closer the centre frequency to the sampling frequency (i. e., the higher $\omega_o T$) the smaller the DC output voltage. However, the higher $\omega_o T$, the higher the mapping error. Thus, the DC output voltage should be minimised through some offset compensation scheme to allow for a small $\omega_o T$.

4.3 Voltage-to-current and current-to-voltage converters

SM circuits process current signals. Therefore, if the input and output signals are voltages rather than currents, v-to-i and i-to-v converters are required. Fig. 4-1 shows a v-

to-i converter that can be employed for SM circuits [30]. The bias voltage labelled V_X is determined by a voltage divider composed of the series connection of two identical n-MOS transistors, one connected to the positive supply and the other to the negative supply and with both gates are connected to V_{DD}, as explained in chapter 2. The voltage V_X at the intermediate node of the series association is closer to V_{SS} than to V_{DD} (see Fig. 2-5). The v-to-i converter in Fig. 4-1 presents a serious drawback: the allowable negative voltage swing of V_{in} is smaller than the positive voltage swing since V_X is closer to V_{SS} than to V_{DD}. An alternative structure that avoids this drawback and thus allows for increasing the dynamic range of the filter by a significant amount is conceptually shown in Fig. 4-2 and is similar to the proposal in [43].

In the circuit in Fig. 4-2, the current source $-V_X/R$, must be independent of technology. Such a circuit is shown in Fig. 4-3. The current $-V_X/R$ flows through R and M_{X1}. With $M_{X1} \equiv M_{X2}$, the current through M_{X2} is also $-V_X/R$, because the two transistors are under the same set of potentials.

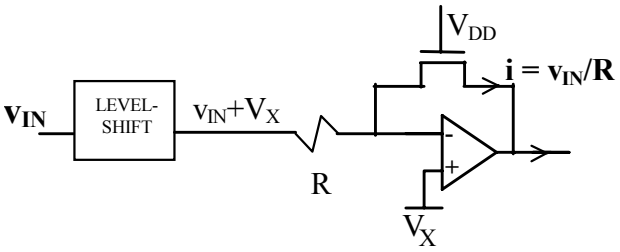


Fig. 4-1. SM v-to-i converter used in [30].

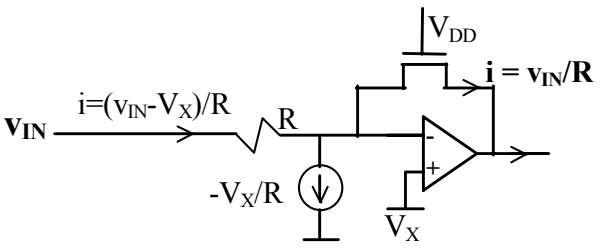


Fig. 4-2. Improved v-to-i converter.

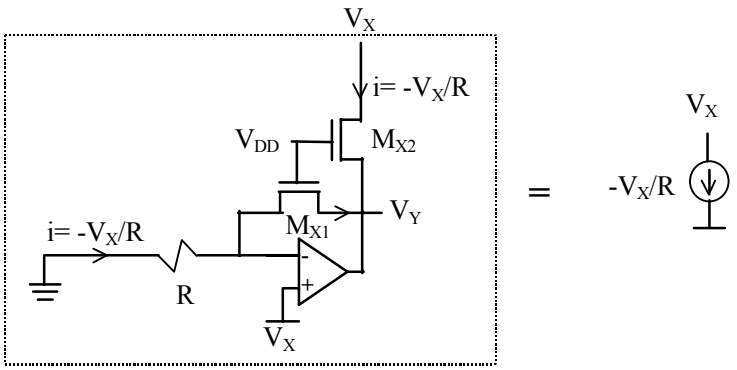


Fig. 4-3. Current source $-V_X/R$ for the v-to-i converter.

The full v-to-i converter is presented in Fig. 4-4. Note that the current source that has been included in the v-to-i converter can be applied to any technology and its relative accuracy relies on matching and op-amp properties.

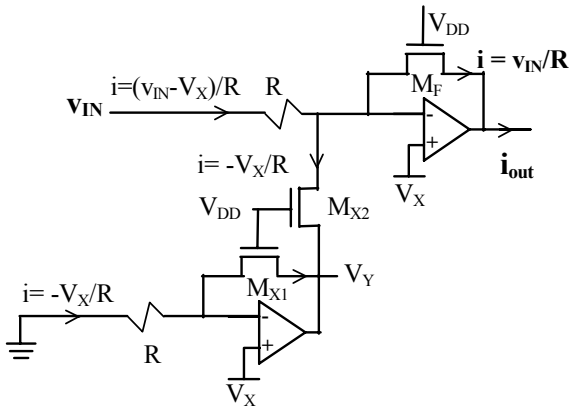


Fig. 4-4. Complete circuit of the v-to-i converter.

The i-to-v converter is the complementary circuit of the v-to-i converter and is shown in Fig. 4-5.

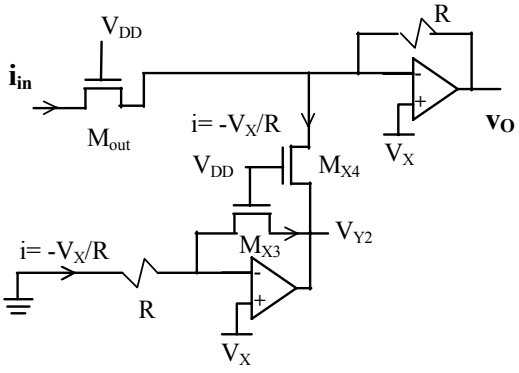


Fig. 4-5. Complete circuit of the i-to-v converter

4.4 Summary

In this chapter, some practical aspects concerning the SM technique were considered. In section 4.2, the influence of the op-amp offset voltage in SM integrators and biquad was analysed. In the SM universal biquad the output offset is proportional to the difference in the op-amps offset voltage of the first stage and inversely proportional to $\omega_o T$. As $\omega_o T$ cannot be made large due to mapping errors and due to the Nyquist theorem, offset compensation techniques must be used at least in the first stage of the biquad.

In some applications, the use of voltage-to-current and/or current-to-voltage converters may be necessary. In section 4.3, we presented rail-to-rail v-to-i and i-to-v converters.

Implementation of basic switched-MOSFET structures 5

5.1 Introduction

A brief summary of what has been done so far with the switched-MOSFET technique is as follows. In [26], the SM technique was introduced and a half-delay cell and integrator were presented. In [27], an improved half-delay cell and an integrator were presented. These are the basic half-delay cell that is shown in Fig. 2-3 and the first generation integrator in Fig. 2-7. A prototype of the integrator was built with n-MOS integrated transistors and discrete op-amps, switches and capacitors. In [28] a second-generation SM integrator, as shown in Fig. 2-9, and a second order SM filter were presented and implemented. The implementation of the integrator used operational amplifiers TL 082, n-MOS integrated transistors (W=48μm, L=1.2μm), n-MOS switches CD 4007 and holding capacitors of 1.8nF. Programmability was achieved through a 6-bit MOCD integrated on a Sea of Transistors (SoT) array in 1.2μm technology from ES2. The filter is the biquadratic section shown in Fig. 2-11. A discrete prototype was implemented, where the transistors were replaced by resistors and programmability was obtained by scaling the resistances. In [29, 30] a single-ended Finite Impulse Response (FIR) filter suitable for equaliser architectures was integrated and tested. The basic cell of the FIR filter is the half-delay cell in Fig. 2-3. The FIR filter has been designed using AMS 0.8 μm CMOS technology. In

[30], a fully balanced FIR filter was designed and integrated, also using AMS 0.8 μm CMOS technology.

As can be seen by what was related above, only FIR SM filters had been integrated. These filters do not use either integrators or biquads. The SM integrators had been tested only at simulation level and through discrete prototypes but had not been integrated. The same is valid for the biquad. Hence, it is necessary to integrate these structures to prove their full functionality. In this chapter, we discourse about the integration of such structures and also of other important structures like the v-to-i and i-to-v converters presented in chapter 4.

Through a co-operation with Delft University of Technology (TUDelft) a chip was made using a 1.6μm CMOS process. The implemented chip contains a v-to-i converter, a half-delay cell, a biquad (using AZ offset compensation and MOCDs for programming) and an i-to-v converter, forming a programmable band-pass filter where both the input and the output are voltages. The supply voltage chosen for the circuits is 1.5V.

In section 5.2, we present the design of the low-voltage class A op-amp to be used in the chip, using the current-based equations of the ACM MOSFET model [8]. Also in section 5.2, we consider the use of class AB op-amps. In section 5.3 we analyse the output stage of the op-amp in the context of the SM technique. To prevent the output transistors of the op-amps to leave the saturation region, we propose the use of a bias voltage, V_X, slightly higher than the one defined in chapter 2. Section 5.4 describes the chip itself zooming in the integrated structures. Section 5.5 focuses on test results. Finally, in section 5.6 a summary of the chapter is drawn.

5.2 Operational amplifier

In the switched-MOSFET technique, all operational amplifiers operate with constant common mode voltage very close to V_{SS}. Therefore, the design of the op-amp is made easy and even a simple Miller-compensated op-amp, like the one shown in Fig. 5-1, operates under 1.5V supply voltage. However, we chose the op-amp in Fig. 5-2 [6, 43] for the SM filter for two reasons: i) its gain and bandwidth are larger than those of the Miller-compensated op-amp; and ii) it works well under supply voltages as low as 1V [6, 43].

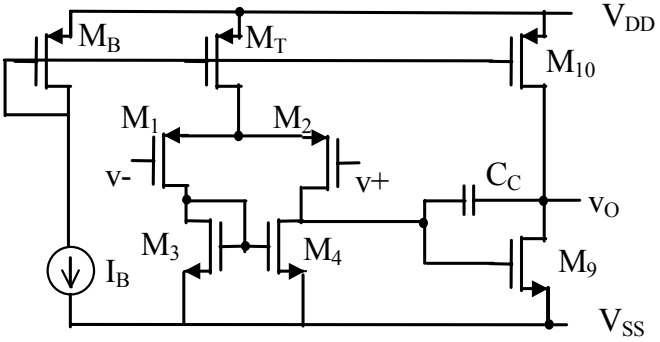


Fig. 5-1. Miller-compensated class A op-amp.

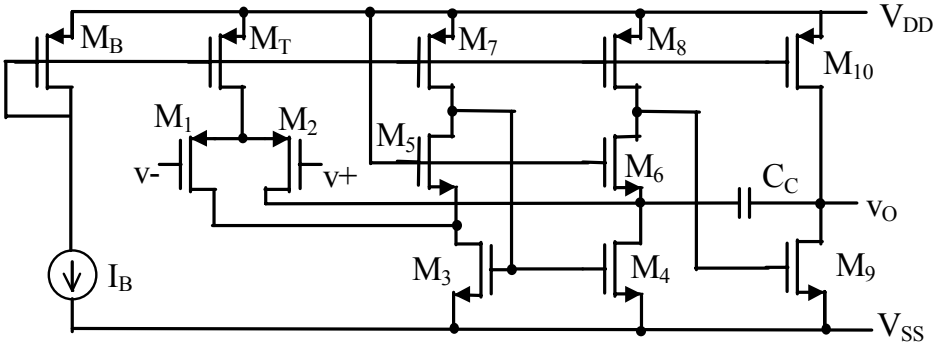


Fig. 5-2. Low-voltage class A op-amp [6, 43].

The op-amp in Fig. 5.2 was designed using the current-based ACM model [8], whose equations are written in terms of the transistor current density. The ACM equations used for the design of the op-amp are expressed in (5-1) to (5-5).

$$\frac{W}{L} = \frac{I_F}{i_f I_{SQ}} \tag{5-1}$$

where I_F is the direct current, i_f is the normalised direct current, and I_{SQ} is the sheet normalisation current, dependent on the process. For AMS 0.8µm CXE, for example, $I_{SQ\_N} \cong 42\text{nA}$ and $I_{SQ\_P} \cong 14\text{nA}$;

$$g_m = \frac{2n}{\phi_t}\frac{I_F}{\left(1+\sqrt{1+i_f}\right)} \tag{5-2}$$

$$GBW = \frac{g_{mI}}{2\pi C_c} = \frac{g_{m1}}{2\pi C_c} \tag{5-3}$$

$$V_{DSsat} \cong \phi_t\left(\sqrt{1+i_f}+3\right) \tag{5-4}$$

In (5-3) g_{mI} is the transconductance of the first stage. For a better matching in the differential pair, $i_{f1} = i_{f2} = 1$ has been used ($i_{f\,i}$ is the normalised direct current of transistor M_i), because the closer to weak inversion the smaller the systematic offset voltage. For the current mirrors $i_{fB} = i_{fT} = i_{f7} = i_{f8} = i_{f10} = 8$ were used. For M_3, M_4 and M_9, smaller inversion levels (if=4) were used in order to obtain smaller saturation voltage for transistor M_9, V_{DSsat9}. The definitions in Table 5-1, which include the values for a typical half-delay cell circuit, were used for op-amp design.

Table 5-1 Definitions for op-amp and filter design.

Supply Voltage	1.5V
Maximum input voltage swing	± 0,5V
Resistor for V/I conversion	400kΩ
└> working current per unit-load	1.25µA
Reference transistors Switches	10µm/20µm 2.0µm/0.8µm
└> $R_{transistors}/R_{switches}$	5
Hold capacitors	5pF
Op-amp compensating capacitor	$C_C = 0.24C_h = 1.2\text{pF}$
"High" V_X generation (section 5.3)	$V_{Xh} = 0.42V_P$
Sampling frequency, f_S	64kHz
GBW	≥ 640kHz

The choice of some of the parameters in Table 5-1 was based on factors like settling time, charge injection, and noise.

From (5-5), we get the minimum g_{mII} for the op-amp. [45]:

$$t_S = \left[\frac{3g_{ms} + g_{mII}}{2\pi GBW g_{mII}} + \frac{C_h}{g_{ms}} \right] ln(1/\gamma) \qquad (5\text{-}5)$$

where g_{mII} is the transconductance of the second stage and t_S is the time for settling within a defined error γ. For safety we consider available for settling only 60% of sampling time, i. e., $t_S = 4.7\mu s$. Thus,

$$g_{mII} \geq 2.8\mu S,$$

according to (5-5).

In the SM filter, op-amps with load of 1, 2 or 4 transistors will be used, depending on the function of the op-amp. In the design for a 1-transistor load, the quiescent current in the output stage I_Q=2.5μA (100% safety margin, i.e., the output current is twice the load peak current); for 2-transistor load, I_Q=4μA (60% safety margin); and for 4-transistor load, I_Q=7μA (50% safety margin), respectively. A higher safety margin in the 1-transistor load circuit is justified because it improves phase margin of the 1 load op-amp (the more critical one).

The bias current (I_B) was the last parameter to be defined. Through an iterative process design/simulation, we got I_B = 0.6μA as a good value for the specifications in Table 5-1. Table 5-2 sums up the transistor widths and electrical parameters for the op-amp (the channel length L equals 4μm for all transistors).

Fig. 5-3 presents the frequency response for the op-amp with 1 transistor load.

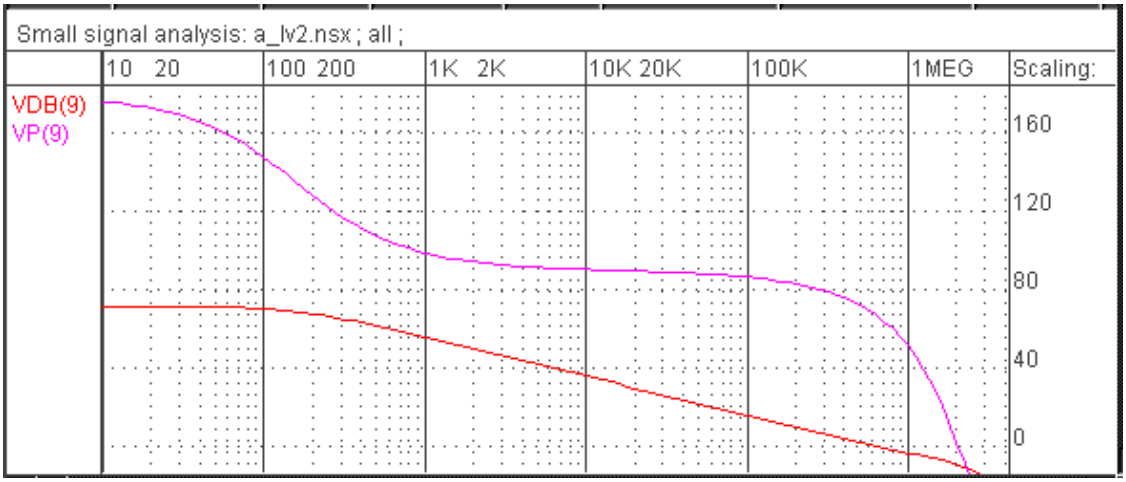


Fig. 5-3. Simulated frequency response of low-voltage class A op-amp for 1-transistor load.

Table 5-2 Obtained values for the class A op-amps (Fig. 5-2).

M1, M2	W=76µm
M3, M4	W=11.7µm
M5, M6	W=6.8µm
M7, M8	W=9.5µm
MB, MT	W=19µm
M9 (for 1 t. load)	W=57µm
M10 (for 1 t. load)	W=79µm
M9 (for 2 t. load)	W=91.1µm
M10 (for 2 t. load)	W=128.5µm
M9 (for 4 t. load)	W=159.6µm
M10 (for 4 t. load)	W=221.2µm
g_{mI} (calculated)	12,4µS
g_{mII} (calculated, 1 t. load)	77µS
GBW (calculated, 1 t. load)	1.65MHz
GBW (simulated, 1 t. load)	950kHz
GBW (simulated, 2 t. load)	850kHz
GBW (simulated, 4 t. load)	700kHz
A_{v0} (simulated, 1 t. load)	72.5dB
A_{v0} (simulated, 2 t. load)	73.5dB
A_{v0} (simulated, 4 t. load)	72dB
PM (simulated, 1 t. load)	63°
PM (simulated, 2 t. load)	65°
PM (simulated, 4 t. load)	66°
Consumption (simulated, 1 t. load)	6.5µW
Consumption (simulated, 2 t. load)	9.2µW
Consumption (simulated, 4 t. load)	14.5µW

5.3 Changing the bias voltage

According to what has been stated in chapter 2, the voltage V_X not only guarantees switch operation outside the conduction gap but also allows for maximum current swing in

both directions, as shown in Fig. 2-5. However, the maximum current in the MOS transistor that operate as i-v and v-i converters cannot be allowed to be I_{max} due to the following problems:

1 – The op-amp offset voltage;

2 – Mismatch;

3- The op-amp is not a rail-to-rail output op-amp.

A possible solution is to use a safety margin of, say, 80% of the maximum current. To clarify more, let us show a numeric example. Using AMS 0.8μm technology, 10μm/20μm transistors and 1.5V supply voltage, $V_X - V_{SS}$ = 165mV. This means that, with V_{Dssat9} (M_9, Fig.5-2) designed for about 130mV (see equation 5-4), the negative voltage swing for several op-amps would be limited to 35mV to prevent M_9 from working outside the saturation region. As this imperfection does not occur for positive output voltage swing, a solution is to operate with a higher V_X voltage level, *when possible* (see the paragraph below). Using the "high" V_X voltage circuit in Fig. 5-4, it is possible to work (neglecting mismatches) with 66% of I_{max} in the positive direction and with 133% of I_{max} in the negative direction. We can now use as working current $I_{work} = 0.5I_{max}$ and we will have a good safety margin in the positive direction [(0.5/0.66)=75%] and the output transistors stay in the saturation region in the negative direction. Of course, a reduction of the output voltage swing in the negative direction will occur, but a small one compared to the maximum possible output swing.

It is important to emphasise that this strategy of using a higher V_X voltage is not always possible. The limitation is the common mode input voltage. As seen in chapter 1, the maximum common-mode input voltage V_{CM} is around V_{DD}-($|V_{Top}|$+V_{DSsat}). For example,

if we were to use AMS 0.8μm technology under 1V supply voltage, the use of the higher V_X voltage, V_{Xh}, is not possible.

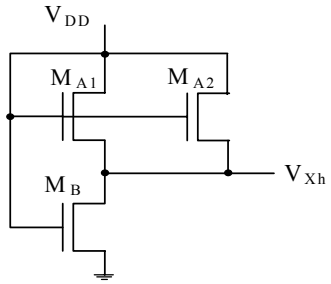


Fig. 5-4. "High" V_X. generation with identical transistors.
$V_{Xh} = V_P(1\text{-}1/\sqrt{3})$.

5.4 Implementation of the SM filter using DIMOS

The cooperation with Delft University of Technology brought the possibility of using (for free) the CMOS process DIMOS 01, available at DIMES, the Delft Institute of Microelectronics and Submicron Technology. DIMOS 01 is a 1.6 micron CMOS process, adopted from Philips. Thus, we adapted the design of the SM filter (and of the op-amp) to this process. The minimum transistor dimensions in DIMOS 01 are 2.4μm/1.6μm. Thus, these are the dimensions to be used in the switches. Also, due to the small sheet resistance, 25Ω/□, we decided to use smaller values for the resistors in the v-to-i and i-to-v converters than the ones defined in Table 5-1. Table 5-3 sums up the new definitions for the SM filter and op-amp to be used with DIMOS 01. Table 5-4 shows the new class A op-amp dimensions and simulated results.

For all the simulations for DIMOS 01, Philips level 9 MOSFET models and the simulator Pstar (from Philips) under Cadence/Analog Artist were used.

The layout of the circuits of the SM filter was drawn using Cadence/Virtuoso editor. The layout of the class A op-amp is shown in Fig. 5-5. It occupies an area of 295μm x 265μm.

Table 5-3 Definitions for op-amp and filter design using DIMOS 01.

Supply Voltage	1.5V
Maximum input voltage swing	± 0,2V
Resistor for V/I conversion	200kΩ
└> working current per load	1μA
Reference transistors Switches	10μm/20μm 2.4μm/1.6μm
└> $R_{transistors}/R_{switches}$	3
Hold capacitors	5pF
Op-amp compensating capacitor	$C_C = 0.24C_h = 1.2pF$
"High" V_X generation (section 5.3)	$V_{Xh} = 0.423V_P$
Sampling frequency, f_S	50kHz
GBW	≥ 500kHz

To minimise the effects of mismatch, matching techniques [47] such as interdigitized stacked differential pair (e.g., in M_1 and M_2, Fig. 5-5), common controid and dummy poly strips (e.g. in M_3 and M_4, Fig. 5-5) have been used not only in the op-amps but also in the whole filter.

Table 5-4 Obtained values for the class A op-amps (Fig. 5-2) using DIMOS 01.

M1, M2	W=152 μm
M3, M4	W=11.8μm
M5, M6	W=6.8μm
M7, M8	W=10μm
MB, MT	W=20μm
M9 (for 1 t. load)	W=47.2μm
M10 (for 1 t. load)	W=80μm
M9 (for 2 t. load)	W=70.8μm
M10 (for 2 t. load)	W=120μm
M9 (for 4 t. load)	W=130μm
M10 (for 4 t. load)	W=220μm
All transistors	L=8μm
I_B	0.5uA
GBW (simulated, 1 t. load)	790kHz
GBW (simulated, 2 t. load)	810kHz
GBW (simulated, 4 t. load)	710kHz
A_{v0} (simulated, 1 t. load)	75dB
A_{v0} (simulated, 2 t. load)	95dB
A_{v0} (simulated, 4 t. load)	82dB
PM (simulated, 1 t. load)	60^o
PM (simulated, 2 t. load)	58^o
PM (simulated, 4 t. load)	60^o
Consumption (simulated, 1 t. load)	3.5μW
Consumption (simulated, 2 t. load)	5.5μW
Consumption (simulated, 4 t. load)	7.1μW

As stated in section 5.1, the chip is composed of a v-to-i converter, a bandpass programmable filter (using 6-bit MOCDs) and an i-to-v converter. The simplified schematic for the SM filter is shown in Fig. 5-6. Auto-zero compensation was used in the biquad. The circuit for generation of V_{Xh} was implemented with 10µm/40µm transistors, according to the scheme shown in Fig. 5-4.

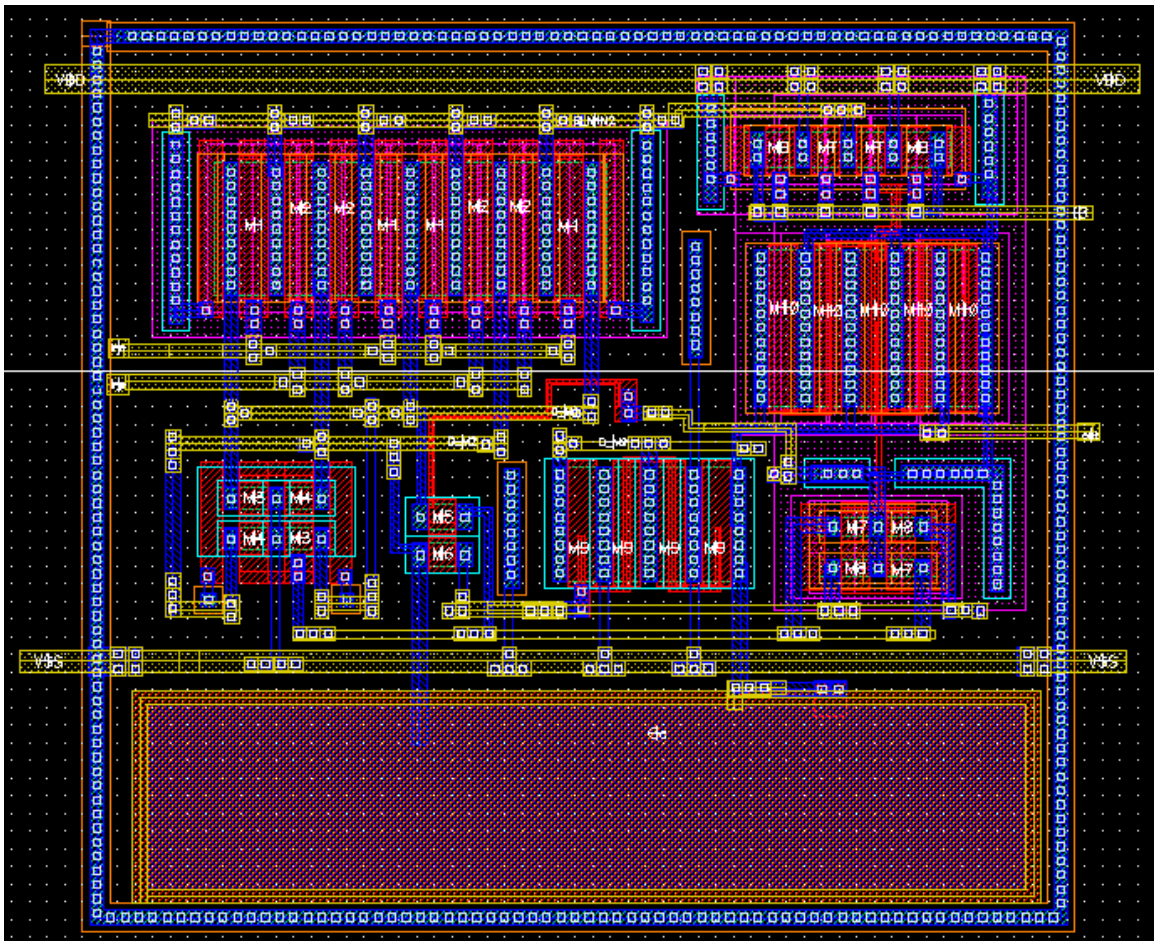


Fig. 5-5. Layout of the class A op-amp (4t. load) in Fig. 5-2.

The layout of the whole SM filter is shown in Fig. 5-7. It occupies an area of approximately 3600µm x 1950µm with PADs. Its foorplan is shown in Fig. 5-8. Note the small area occupied by the two 6-bit MOCDs, responsible for programming the filter centre frequency. The PADs for the digital inputs include protection diodes.

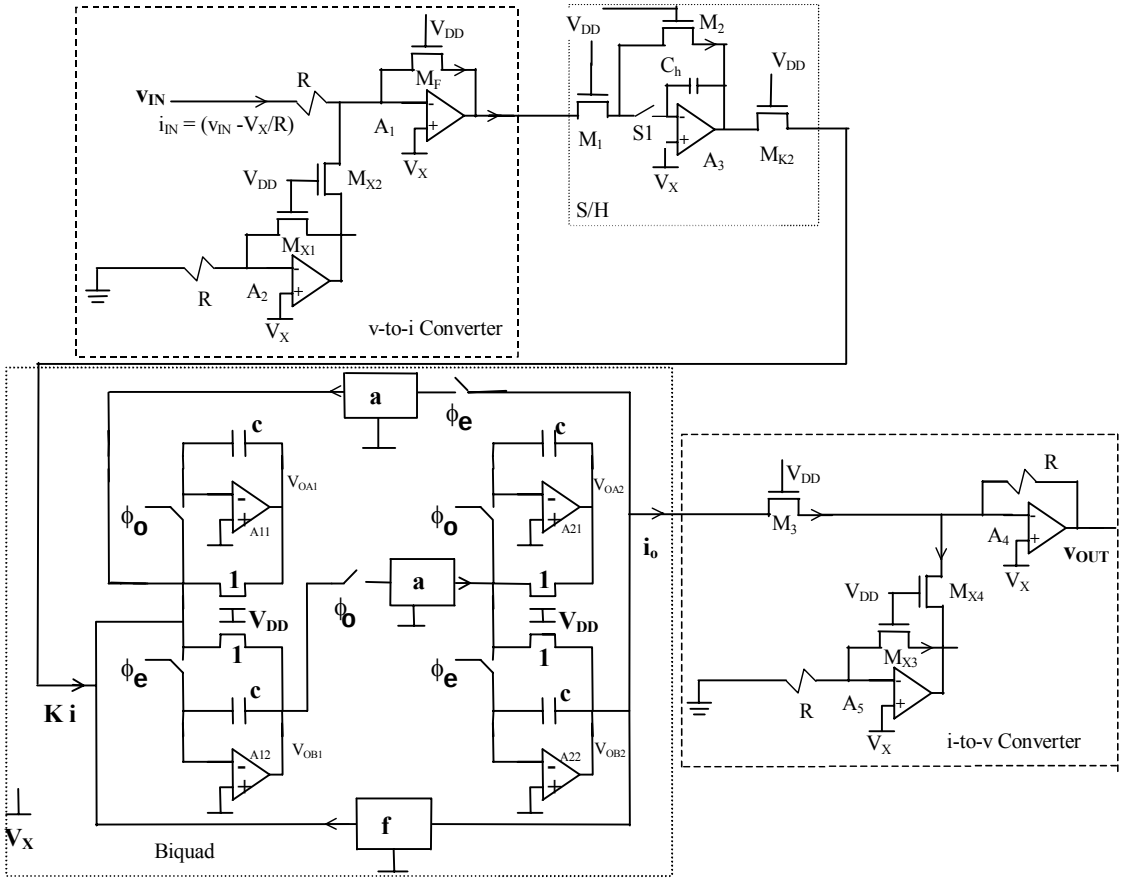


Fig. 5-6. Simplified schematic for the SM filter.

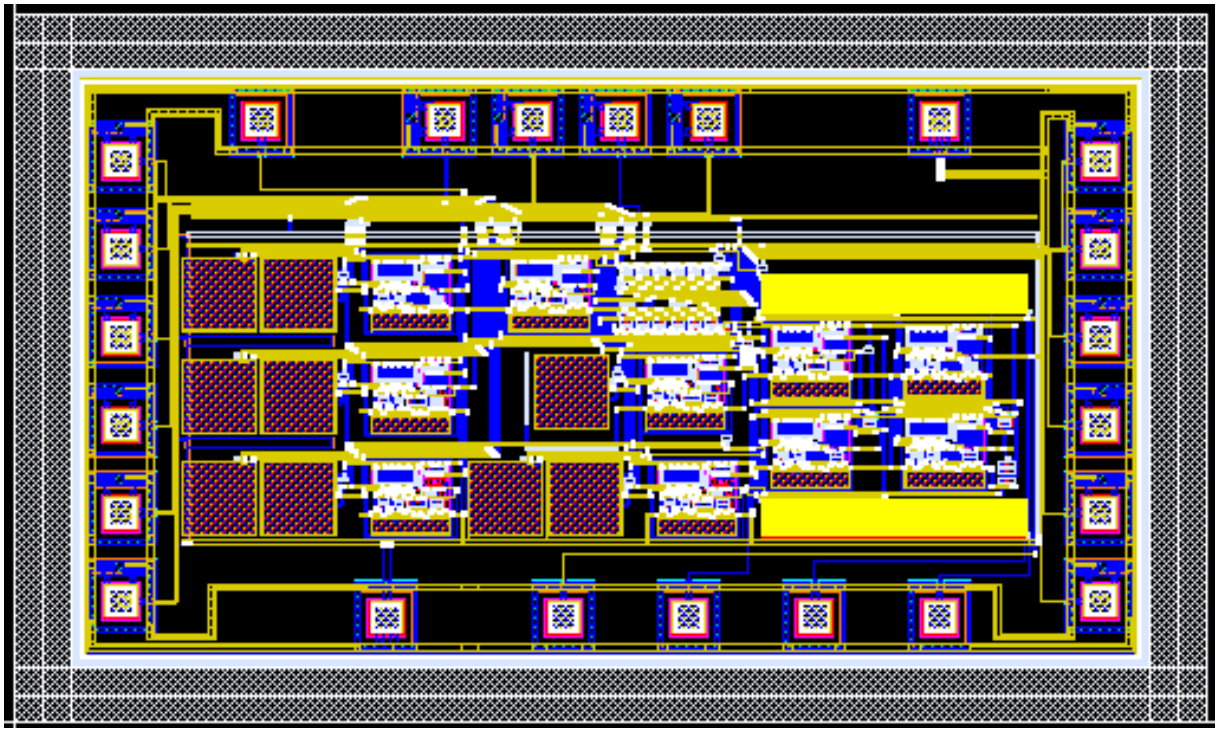


Fig. 5-7. Layout of the SM filter.

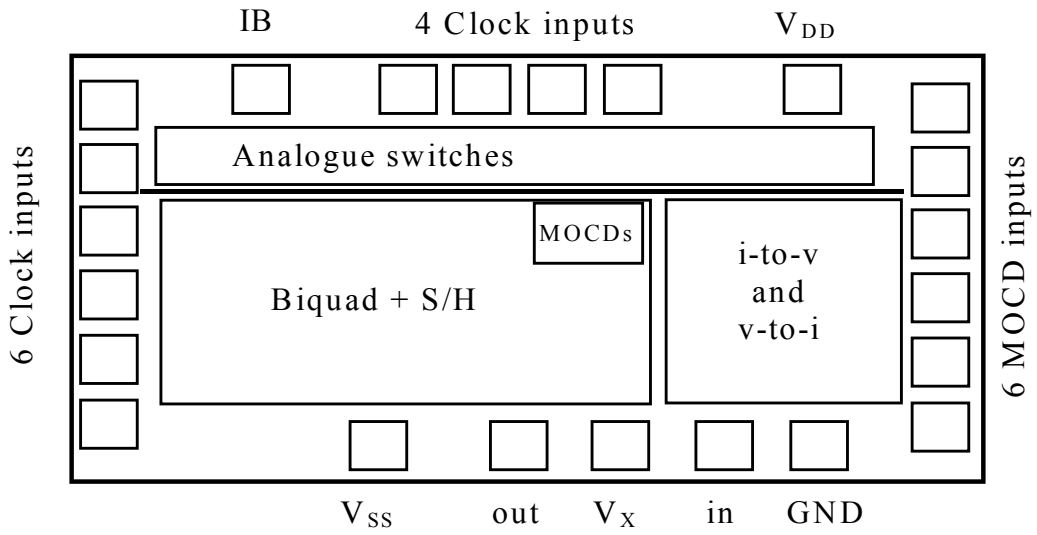


Fig. 5-8. Floorplan of the SM filter.

5.5 Experimental results

Besides the SM filter, some test structures were also integrated. These are 10μm/20μm and 20μm/20μm transistors, and op-amps for 1-, 2- and 4-transistor load. The test structures have test PADs measuring 120μm x 120μm. The measurement results for these structures, as well as for the SM filter, will be presented in this section.

5.5.1 Measurements in the op-amps

The operational amplifiers are present in all stages of the SM filter. So, their performance must be known to allow for a better understanding of filter behaviour. In fact, some problems were found in the performance of the op-amps. They will be addressed here.

Measurements were performed in the class A op-amp for 1-transistor load (1tl), 2-transistor load (2tl), and 4-transistor load (4-tl), in several samples of each.

The DC measurements were carried on using parameter analyser HP 4145B. Table 5-5 summarises the obtained results.

Table 5-5 DC measurements for the DIMES op-amps.

Op-amp[1]	Input offset voltage	Unloaded DC gain	Loaded DC gain[2]
1tl – sample 1	+171mV	76dB	50dB
1tl – sample 2	+165mV	76dB	49dB
1tl – sample 3	+21mV	75dB	49dB
1tl – sample 4	-75mV	76dB	51dB
1tl – sample 5	+60mV	77dB	52dB
2tl – sample 1	+75mV	80dB	51dB
2tl – sample 2	+90mV	82dB	52dB
4tl – sample 1	+170mV	85dB	60dB
4tl – sample 2	+175mV	85dB	61dB

1 –The bias current for all op-amps was set to 0.7μA.
2 – The 10μm/20μm test transistor, the unitary transistor in the SM filter, was used as load.

The input offset voltages obtained for the op-amps were much higher than expected. They were much lower (up to 4mV) for the op-amps implemented with AMS technology (chapter 3), which use the same topology and were designed using the same methodology/equations. This huge input offset voltage for the DIMES op-amps imposes some limitations. For example, consider the simple unity-gain inverting amplifier configuration shown in Fig. 5-9. The op-amps were designed for operation under 1.5V supply voltage. With 1.5V, the V_X generator (Fig. 5-4) yields V_X = 0.24V (measured). In this case, with a V_{OS} = 150mV, the DC voltage at the inverting input would be ≅ 240mV – 150mV = 90mV. This imposes a DC current in M_S. With M_S=M_1, the output DC voltage would be 90mV –150mV, i.e., the op-amp saturates to the negative supply (ground). This explains why the SM filter could not operate under 1.5V (next sub-section). In the SM filter, only the biquad presents offset compensation schemes, so the other stages (i.e., v-to-i and i-to-v converters and half-delay cell) suffer from this huge offset voltage. The SM filter started to be functional under 1.7V, but acceptable distortion levels were obtained for V_{DD} = 2.2V. The measured V_X for V_{DD} = 2.2V is 0.46V, witch puts the DC output voltages

to a higher value. So, all other measurements performed in the op-amp will consider a supply voltage of 2.2V.

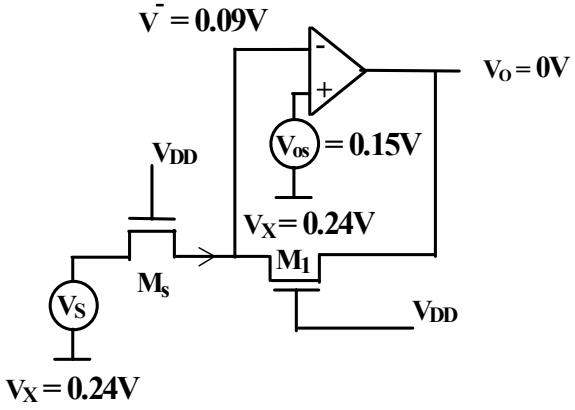


Fig. 5-9. DC voltages in a simple unit gain inverting amplifier with V_{OS}=150mV.

The unity-gain frequency (f_u) was measured in a unity-gain non-inverting amplifier configuration, like the one shown in Fig. 3-17. The obtained $f_u \cong$ 550kHz. The AC response for the circuit is shown in Fig. 5-10. As can be seen in Fig. 5-10, there is an undesirable peak in the AC response (this also happened for the AMS op-amp that uses the same topology, chapter 3). Moreover, it was observed that the output signal for frequencies in the range where the gain is > 0dB (i.e., 30kHz- 440kHz) is distorted. The measured phase margin (PM) at 550kHz is only 26°.

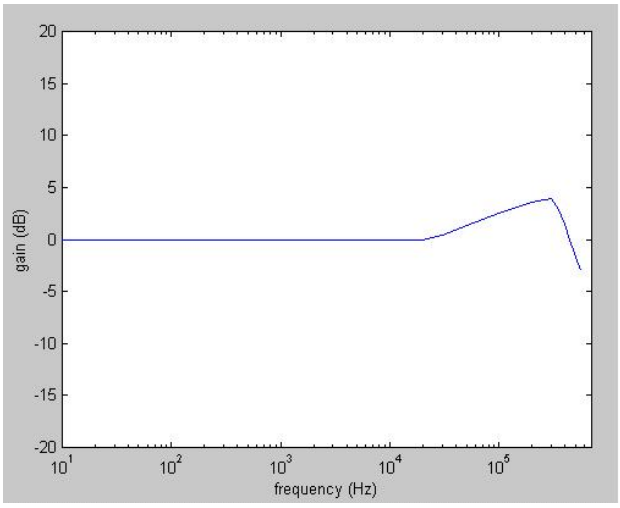


Fig. 5-10. AC response for circuit in Fig. 5-10.

Another imperfection was identified in the op-amp performance. The op-amp was also tested in an inverting unity-gain amplifier configuration, as shown in Fig. 5-11, with the use of linear resistors. The circuit worked well with R_1=R_2=180kΩ, but with larger resistor values (R_1=R_2=820kΩ), the circuit starts to oscillate. Maybe the capacitances of the PADs play a decisive role in this problem, besides the poor phase margin.

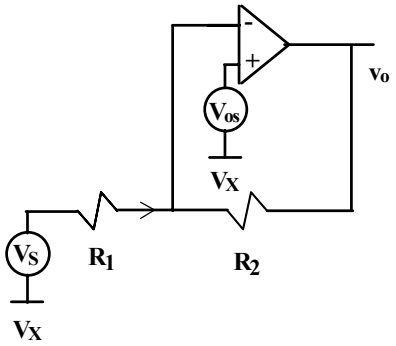


Fig. 5-11. Inverting amplifier.

5.5.2 Measurements in the SM filter

Several measurements were performed on the SM filter. The AC response for several digital words in the MOCDs is shown in Fig. 5-12. Table 5-6 summarises the obtained results. As can be seen in Table 5-6, some imperfections were detected through the measurements. These are the centre frequency deviation, the Q error and the gain error. However, none of this errors is unacceptable as the filter is programmable. In applications such as hearing aids, the audiologist (or the system itself) must program the filter response to compensate the hearing impairment of each patient.

Fig. 5-13 shows the noise measurement for the chip. Using a 200mV_{peak} input signal the achieved dynamic range is 63.8dB. This is very close to the calculated dynamic range, 66.8dB.

The maximum measured output swing without clipping was ± 450mV$_{peak}$. Fig. 5-14 illustrates the measured distortion as a function of the input voltage for the centre frequency (f_o), the –3dB lower frequency (f_i) and the –3dB upper frequency (f_s). Table 5-7 summarises the obtained results. The results are considered adequate for the specified input voltage range (up to the input voltage of 200mV$_{peak}$).

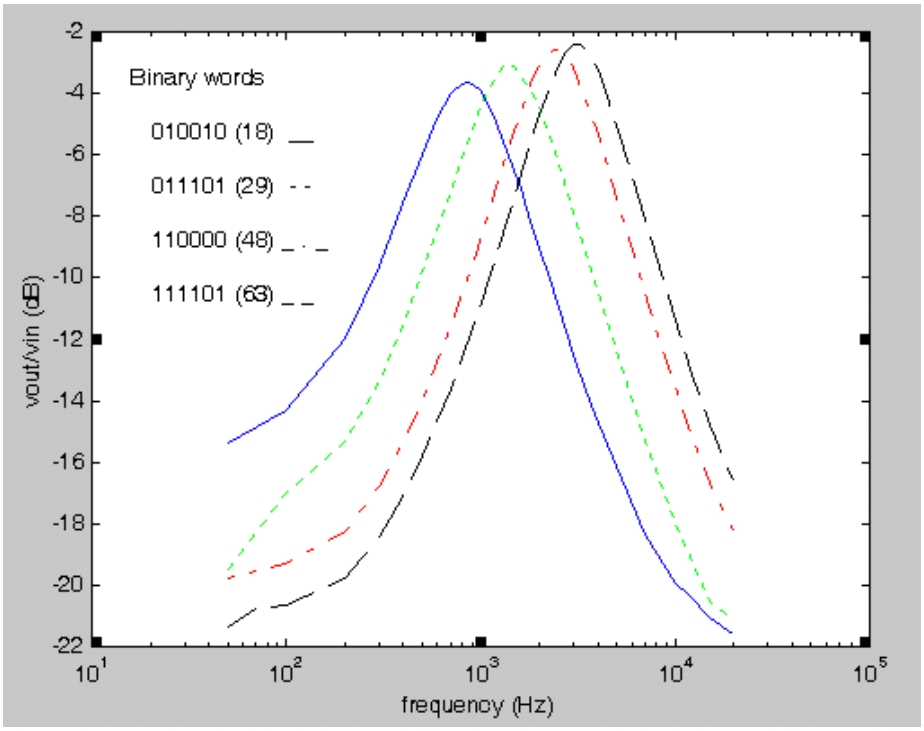


Fig. 5-12. Measured AC response for several MOCD words.

Table 5-6. AC response details.

Digital word (DW)	Calculated centre frequency f_o	Measured centre frequency f_o	f_o error	Calculated Q	Measured Q	Q error	Gain error
$010010_2 = 18_{10}$	1130 Hz	860 Hz	23.9%	0.92	0.81	- 13%	-3.6dB
$011101_2 = 29_{10}$	1810 Hz	1400 Hz	22.6%	0.88	0.92	+ 4%	-3.1dB
$110000_2 = 48_{10}$	3000 Hz	2420 Hz	19.3 %	0.81	0.90	+ 10%	-2.6dB
$111101_2 = 61_{10}$	3834 Hz	3200 Hz	16.5 %	0.76	0.88	+ 13%	-2.4dB

All the above measurements were performed under a supply voltage of 2.2V. The circuit was designed to operate under 1.5V, but the op-amp did not operated properly under this supply voltage (see sub-section 5.2.1). In fact, the chip is still functional down to a supply voltage of 1.7V. However, the distortion levels with this supply voltage are

considerably higher than the ones obtained under 2.2V supply. The most likely reason for this is that the DC voltages in some op-amp outputs can be very close to ground due to the huge op-amp input offset voltages. A V_{DD} of 2.2V produces a V_{Xh} of 0.46V, much higher than both the V_{Xh} = 0.24V obtained for V_{DD} = 1.5V and V_{Xh} = 0.3V obtained for V_{DD}=1.7V. These V_{Xh} values are measured values.

It is important to notice that the process used, DIMOS 01, presents threshold voltages higher than 1V. The supply voltage of 2.2V is less than two stacked gate-source voltages and two saturation voltages and thus the SM filter can be considered to be a low-voltage circuit [4].

The total current consumption for the SM filter is 93μA. It is important to emphasise that this current consumption can be reduced significantly with the use of class AB operational amplifiers.

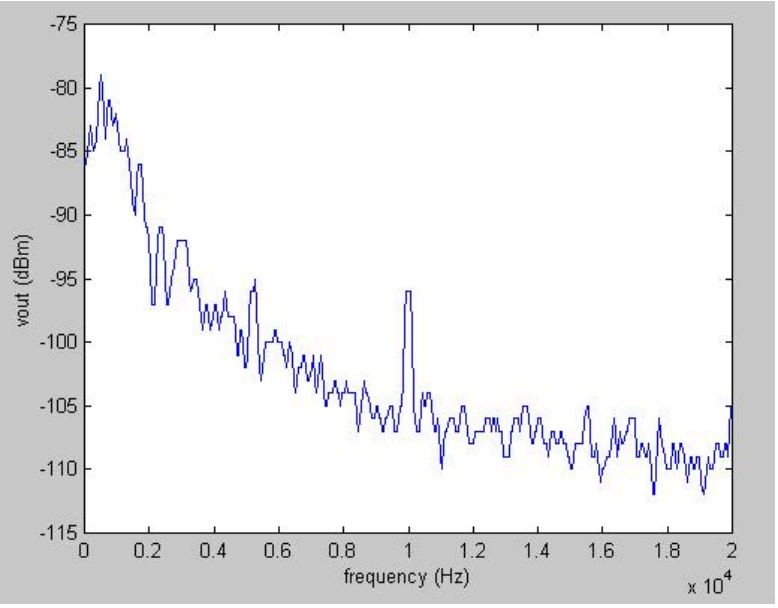


Fig. 5-13. Measured noise.

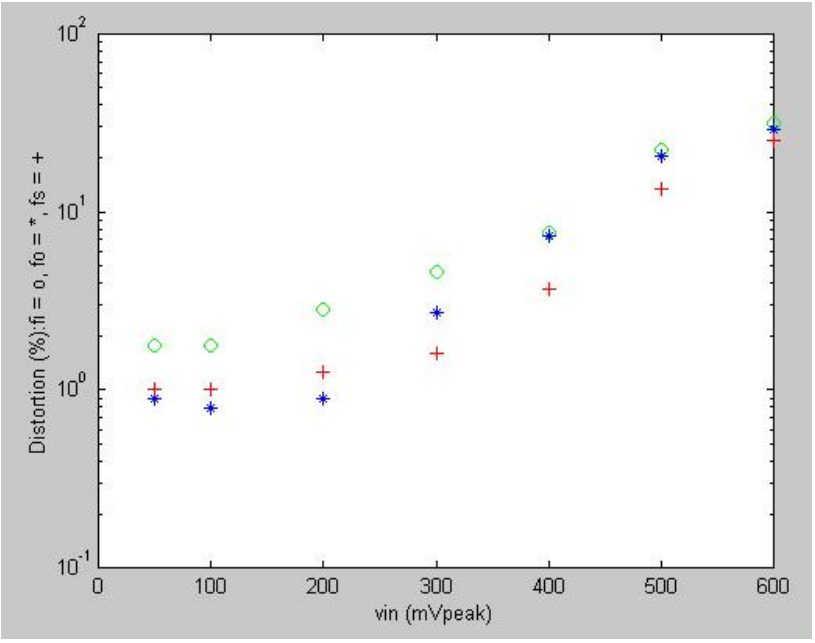


Fig. 5-14. Measured distortion.

Table 5-7. Distortion results.

v_{in} (mV_{peak})	50	100	200	300	400	500	600
distortion, f_i (%)	1.8	1.8	2.8	4.6	7.6	22.3	31.5
distortion, f_o (%)	0.9	0.8	0.9	2.7	7.3	22.7	29.1
distortion, f_s (%)	1	1	1.26	1.6	3.7	13.4	25.2

The microphotograph of the chip is shown in Fig. 5-15.

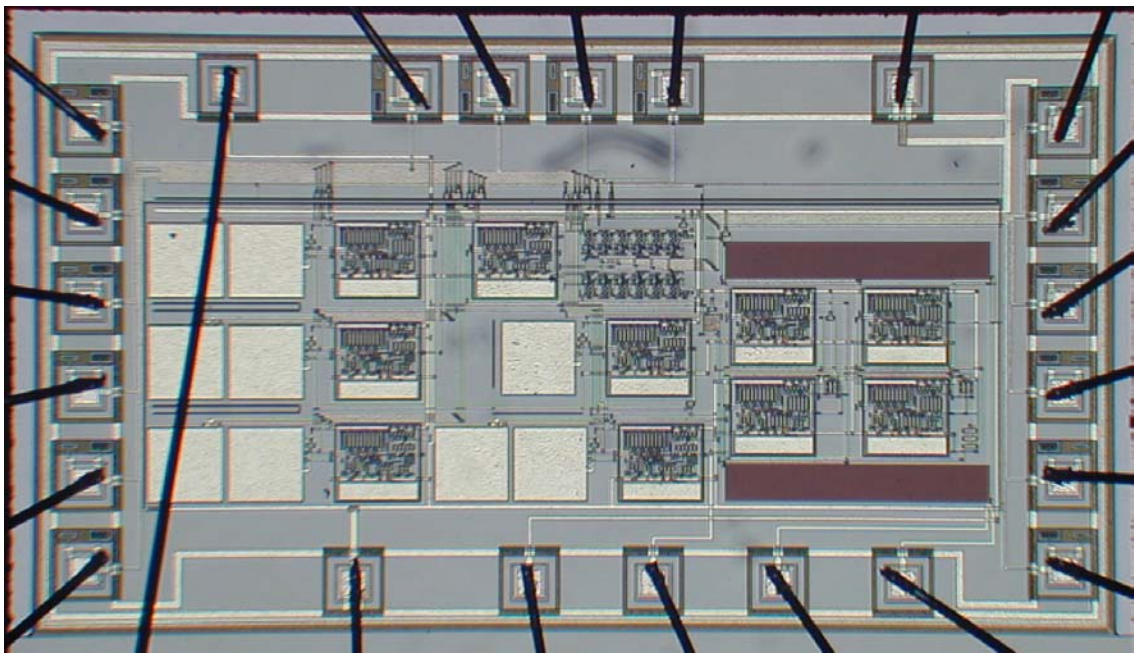


Fig. 5-15. Chip microphotograph.

5.6 Conclusions

A digitally programmable low-voltage low-power filter suitable for hearing instruments was described. The circuit contains a v-to-i converter, a half-delay cell, a biquadratic section and an i-to-v converter and was implemented in a 1.6 micron CMOS process. The programmability is achieved by means of MOCDs and does not require a large silicon area. The results show applicability of the switched-MOSFET technique as an alternative technique for low-voltage discrete-time signal processing without the need for a special process.

Even with the problems identified for the op-amps, the SM filter perform almost as expected. It is important to emphasise the functionality of the auto-zero offset compensation scheme in the biquad, face to the large op-amps offset voltages.

Some non-ideal characteristics presented by the filter are due to op-amp imperfections. However, it would be better to have a biquad topology in which there are no undesirable switches in series with the programming MOCDs. For a bandpass filter, this can be achieved with the use of first generation SM integrators.

Conclusions and future research 6

6.1 Conclusions

The switched-MOSFET technique has proven to be an alternative technique for low-voltage discrete-time signal processing without the need of both a special process or voltage doublers. The SM technique achieves design simplicity compared to switched-opamp, the SC technique for low-voltage operation. SM also excels at programming simplicity, making use of the small area-demanding MOCDs.

In this work, an analysis of the basic delay cell has been carried out. Regarding offset correction, settling time, noise, charge injection and harmonic distortion, SM presents results similar to those presented by the SC and SI techniques.

Offset compensation schemes have been proposed and analysed. Rail-to-rail voltage-to-current and current-to-voltage converters have also been proposed.

A digitally programmable low-voltage low-power filter suitable for hearing instruments was described. and implemented in a 1.6 micron CMOS process. Even with the problems identified for the op-amps, the SM filter performed well. The AZ offset compensation scheme proved its functionality and compensated the large offset of the op-amps in the biquadratic section.

6.2 Future research in switched-MOSFET

As already commented in chapter 5, it would be good to find a biquad topology in which there are no undesirable switches in series with the programming MOCDs. The challenge is to achieve this while allowing for the independent programming of the filter characteristics (centre frequency, quality factor and gain).

In the SM technique, the op-amps drive resistive loads. Thus the use of class AB op-amps probably will lead to smaller power consumption. This should be investigated.

Also, it would be interesting to implement a practical low-voltage low-power application using switched-MOSFET, in a well known CMOS process, and to compare the results with those obtained with other techniques. The application could be, for example, the directional hearing-aid adapter implemented at the Delft University of Technology (TUD) with translinear circuits [48].

Appendix A – Auto-zero analysis

Consider the circuit in Fig. A-1, which is the same as in Fig. 3-6.

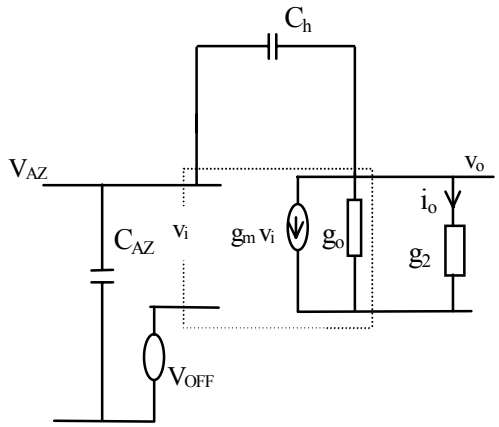


Fig. A-1 Small signal equivalent circuit for determining t_{az}.

Considering the op-amp finite transconductance represented by a single-pole function, that is, $g_m = g_m(s) = \dfrac{g_{m0}}{1 + s/\omega_1}$ where ω_1 is the dominant pole of the loaded op-amp, we have for the circuit in Fig. A-1:

$$\frac{V_{AZ}}{V_{OFF}} = \frac{1}{1 + \left[\dfrac{(1+K_a)g_L}{g_{mo}}\dfrac{1}{\omega_1} + \dfrac{C_{AZ}}{g_{mo}}\right]s + \dfrac{C_{AZ}}{g_{mo}}\dfrac{1}{\omega_1}s^2}. \qquad \text{(A-1)}$$

where $K_a \equiv C_{AZ}/C_h$ and $g_L = g_o + g_2$.

The denominator of (A-1) can be rewritten as:

$$D(s) = 1 + \frac{2\xi}{\omega_o}s + \frac{1}{\omega_o^2}s^2 \qquad \text{(A-2)}$$

where ξ is the damping factor, which in this case is given by

$$\xi = \frac{1}{2}\sqrt{\frac{(1+K_a)^2}{\omega_u}\frac{g_L}{C_{AZ}}} \tag{A-3}$$

The slowest circuit response occurs when k>1 (overdamped circuit response). In this case, we have for the settling error [42]:

$$\gamma = \frac{1}{2\sqrt{\xi^2-1}}\left(\frac{1}{\xi_1}e^{-\xi_1.\omega_o.t_{az}} - \frac{1}{\xi_2}e^{-\xi_2.\omega_o.t_{az}}\right) \tag{A-4}$$

where

$$\xi_1 \equiv \xi - \sqrt{\xi^2-1} \qquad \text{and} \qquad \xi_2 \equiv \xi + \sqrt{\xi^2-1} \tag{A-4a}$$

If $4\xi^2>>1$, (A-4) can be approximated by [42]

$$\gamma \cong e^{-\omega_o t_{az}/2\xi} \tag{A-5}$$

The highest value for γ appears in the case when the approximation in (A-5) is used. Thus, the use of the approximation in (A-5) favours safety. From (A-1), (A-2) and (A-5) we arrive to

$$t_{az} \geq \frac{(1+K_a)g_L}{g_{mo}\omega_1} ln(1/|\gamma|) = \frac{(1+K_a)}{\omega_u} ln(1/|\gamma|) \quad . \tag{A-6}$$

where ω_u is the angular unity-gain frequency of the loaded op-amp.

Appendix B – Equations and simulations for settling time in the SM half-delay cell

B.1 Ideal switches and op-amp with infinite bandwidth

In this case consider the circuit in Fig. B-1, which is the same as in Fig. 3-11.

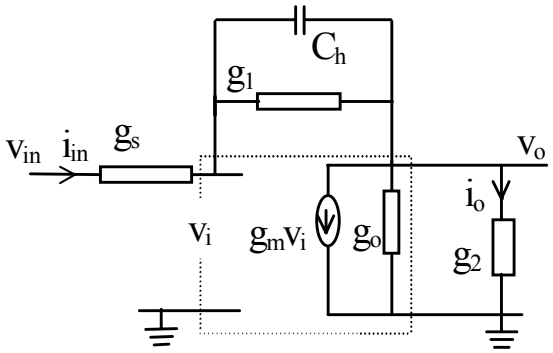


Fig. B-1 Small signal equivalent circuit for the SM delay cell Ideal switches and op-amp with infinite bandwidth.

The transfer function for the circuit in Fig. B-1 is:

$$H(s)=\frac{v_o(s)}{v_{in}(s)}=\frac{-g_s\left[g_m-\left(g_1+sC_h\right)\right]}{g_s g_L+g_1\left(g_s+g_L+g_m\right)+sC_h\left(g_s+g_L+g_m\right)}. \tag{B-1}$$

where $g_L = g_2 + g_o$.

Equation (B-1) can be rewritten as:

$$H(s)=\frac{N(s)}{1+s\tau} \tag{B-2}$$

where

$$N(s)=-\frac{g_s}{g_1}\frac{1-g_1/g_m-sC_h/g_m}{1+\dfrac{g_s+g_L+g_Lg_s/g_1}{g_m}} \tag{B-2a}$$

and

$$\tau = \frac{C_h}{g_1} \frac{1}{1 + \dfrac{g_L g_s / g_1}{g_m + g_L + g_s}} \tag{B-2b}$$

The proper operation of the inverting S/H circuit is assumed if

$$g_m >> g_s + g_L + g_L g_s / g_1 \tag{B-3}$$

Moreover, considering (B-3),

$$\tau \cong \frac{C_h}{g_1} \tag{B-4}$$

And thus from (3-7) and (B-4) we have

$$C_h \le g_1 t_{sam} \frac{1}{ln(1/|\gamma|)} \tag{B-5}$$

B.2 Real switches and op-amp with infinite bandwidth

In this case consider the circuit in Fig. B-2.

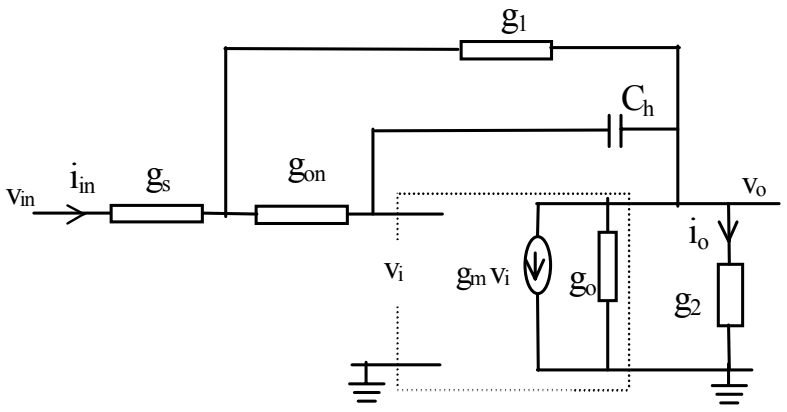


Fig. B-2 Small signal equivalent circuit for the SM delay cell Real switches and op-amp with infinite bandwidth.

In the circuit in Fig. B-2, we obtain:

$$\frac{v_o(s)}{v_{in}(s)} = \frac{-g_s\left[g_m g_{on} - g_{on}g_1 + sC_h\left(-g_{on}-g_1\right)\right]}{g_m g_{on}g_1 + g_{on}g_s g_1 + g_{on}g_s g_L + g_{on}g_1 g_L + sC_h\left(g_m\left(g_{on}+g_s+g_1\right)+g_{on}g_s + g_{on}g_L + g_s g_1 + g_s g_L + g_1 g_L\right)} \quad \text{(B-6)}$$

Making the same assumptions as in section B.1, we obtain:

$$\tau \cong \frac{C_h}{g_1}\left(1+\frac{g_1}{g_{on}}+\frac{g_s}{g_{on}}\right) \quad \text{(B-7)}$$

Therefore, from (3-7) and (B-7):

$$C_h \le g_1 \frac{g_{on}}{g_{on}+g_1+g_s}\, t_{sam}\, \frac{1}{ln\left(1/|\gamma|\right)} \quad \text{(B-8)}$$

We note, comparing (B-5) with (B-8) that the maximum value for C_h as a function of the sampling error gets lower if we consider switch resistance, as expected.

B.3 Ideal switches and op-amp with finite bandwidth

Starting from (B-1) and considering now the op-amp finite transconductance represented by a single-pole function, that is, $g_m = g_m(s) = \frac{g_{m0}}{1+s/\omega_1}$ where ω_1 is the dominant pole of the loaded op-amp, we have:

$$H(s) = N(s)\frac{1}{1+\left(\frac{g_L g_s/g_1 + g_L + g_s}{g_{m0}\omega_1}+\frac{C_h}{g_1}\right)s+\frac{C_h}{g_1}\frac{g_L+g_s}{g_{m0}\omega_1}s^2}\ , \quad \text{(B-9)}$$

$$N(s) = \frac{-g_s\left[g_{m0}\omega_1 - \left(g_1+sC_h\right)\left(\omega_1+s\right)\right]}{g_s g_L\omega_1 + g_1\left(g_s+g_L\right)\omega_1 + g_1 g_{m0}\omega_1} \cong -\frac{g_s}{g_1}+\left(\frac{g_1}{g_{m0}\omega_1}+\frac{C_h}{g_{m0}}\right)s+\frac{C_h}{g_{m0}\omega_1}s^2 \quad \text{(B-9a)}$$

The denominator of (B-9) can be rewritten as:

$$D(s) = 1 + \frac{2\xi}{\omega_o} s + \frac{1}{\omega_o^2} s^2 \tag{B-10}$$

$$\gamma = \frac{1}{2\sqrt{\xi^2 - 1}} \left(\frac{1}{\xi_1} e^{-\xi_1 . \omega_o . t_{az}} - \frac{1}{\xi_2} e^{-\xi_2 . \omega_o . t_{az}} \right) \tag{B-11}$$

where

$$\xi_1 \equiv \xi - \sqrt{\xi^2 - 1} \qquad \text{and} \qquad \xi_2 \equiv \xi + \sqrt{\xi^2 - 1} \tag{B-11a}$$

If $4\xi^2 >> 1$, (B-11) can be approximated by [42]

$$\gamma \cong e^{-\omega_o t_{sam} / 2\xi} \tag{B-12}$$

The highest value for γ appears in the case when the approximation in (B-12) is used. Thus, the use of the approximation in (B-12) favours safety. Considering this approximation we arrive form (B-9) to

$$C_h \le g_1 t_{sam} \frac{1}{ln(1/|\gamma|)} - \frac{g_s g_1 + g_s g_L + g_1 g_L}{g_{m0} \omega_1} . \tag{B-13}$$

Being $g_{m0}\omega_1 = \omega_u g_L$, where ω_u is the angular unity gain frequency of the loaded op-amp, we have

$$C_h \le g_1 t_{sam} \frac{1}{ln(1/|\gamma|)} - \frac{g_s g_1 / g_L + g_s + g_1}{2\pi f_u} \tag{B-14}$$

B.4 Real switches and op-amp with finite bandwidth

For complexity this item has not been analysed. According to simulations (Table B-1, below), we expect that we can consider as an approximation the results for ideal

switches, finite bandwidth, which are for worst case conditions and thus include a safety margin that compensates for the switches resistance.

B.5 Numerical examples and simulations

To prove the results above, some calculations/simulations were performed. For the examples we used the following specifications/parameters:

Supply voltage: 1.5V.

Technology: AMS CXE 0.8μm.

Sampling frequency: 50kHz → t_{sam} = 7μs (circuit with AZ).

Maximum sampling error, γ = 0.004 (8-bits).

Equal transistors with (W/L) = 10μm/20μm.

Switches with (W/L) = 2μm/0.8μm → $(W/L)_{\text{switches}} / (W/L)_{\text{transistors}} = 5$.

For the simulations, SMASH simulator together with BSIM3v3 models provided by AMS were used. The op-amp with infinite bandwidth was implemented with a voltage controlled voltage source with gain of 100dB. The op-amp with finite bandwidth presents f_{ul}=1MHz and g_o=0.5μS and DC gain of 96dB (unloaded) and 64dB (loaded). The results are summarised in Table B-1.

Table B-1 Calculated and simulated maximum capacitor for an .8-bit settling error.

Case	Maximum capacitor, Calculated	Maximum capacitor, Simulated
Ideal switches, GBW = ∞	from (B-5): 27.6pF	26.5pF
Real switches, GBW = ∞	from (B-8): 19.7pF	19.9pF
Ideal switches, GBW = finite	from (B-13): 17.3pF	22.5pF
Real switches, GBW = finite		17.5pF

We note the excellent agreement in the results for the two first lines in Table B-1. When then op-amp presents finite bandwidth, the difference between the calculated and

simulated values is higher. This was expected because the approximation used in the calculations for finite bandwidth considers worst case conditions.

Appendix C – Noise analysis

According to the stated in chapter 3, the noise analysis will concentrate in the direct noise in the holding period and in the sampled-and-held noise in both C_{AZ} and C_h.

These contributions will be analysed separately.

C.1 Broadband noise in the holding interval

For the broadband noise calculation in the holding interval, consider the noise circuit shown in Fig. C-1, which is equivalent to the circuit in Fig. 3-4 for the holding interval. Modelling the op-amp gain as a single pole function, the total broadband noise in the output is given by

$$S_{hol}^{b}(f) = \frac{t_{hol}}{T} 4\theta \left[\left(R_{eq} + R_{on}\right) \frac{1}{1+\left(\frac{\omega}{\omega_u}\right)^2} + \left(R_1 + R_s\right) H_1^2 + \left(R_2\right) H_2^2 \right] \qquad \text{(C-1)}$$

where R_{eq} is an equivalent resistor for the op-amp input referred noise, $R_i = \left(\partial I_D / \partial V_S\right)^{-1}\Big|_{V_S=V_D=V_X}$ for transistor M_i, ω_u is the unity-gain frequency of the op-amp and

$$H_1 = \frac{R_2}{R_1 + R_s + R_2 + \left(R_1 R_2 + R_s R_2\right)/R_0} \qquad \text{(C-1a)}$$

$$H_2 = \frac{R_1 + R_s}{R_1 + R_s + R_2 + \left(R_1 R_2 + R_s R_2\right)/R_0} \qquad \text{(C-1b)}$$

In general, the most important contribution to (C-1) comes from R_{eq}.

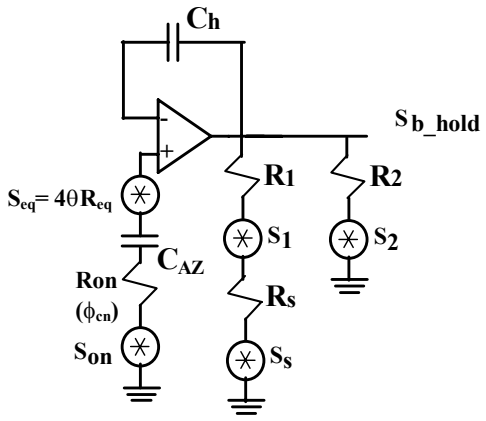


Fig. C-1. Noise equivalent circuit for the holding period.

If we consider the circuit without offset compensation, as in Fig. 3-2, R_{on}=0 in (C-1).

C.2 Sampled-and-held noise

The undersampling of the broadband noise present in the SM half-delay cell produces a sampled-and-held noise component whose power spectral density concentrates in the baseband. This holds for both C_h and C_{AZ}. Moreover, C_h also charges to a amplified copy of the noise held in C_{AZ}. Thus, 3 different noise contributions will be analysed in this section.

C.2.1 Sampled-and-held noise in C_{AZ}

At the end of the AZ phase, C_{AZ} samples the broadband noise due to the noise sources and holds this noise during t_{sam} and t_{hol}. However, the transfer of this noise to the output is different in t_{sam} and t_{hol}. The spectra of the white noise sources present during t_{az} (Fig. C-2) are low-pass filtered by the corresponding RC time constants and/or by the op-amp rolloff.

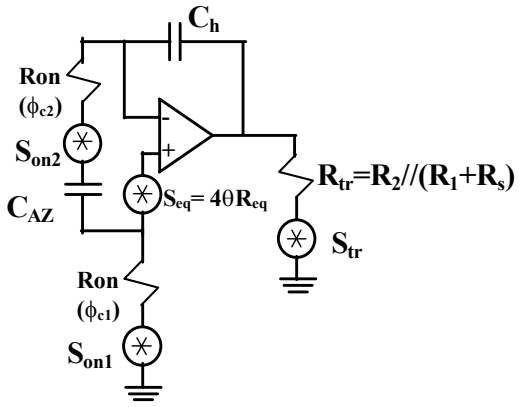


Fig. C-2. Noise equivalent circuit for the AZ period.

In the circuit in Fig. C-2, the undersampling of the broadband noise components occurs. The sampled-and-held noise in a generic capacitor C_x where the switch conducts during a time t_{on}, considering the white noise bandwidth (limited by the RC time constant or another element) $f_{WH} >> f_s$, is given [23] by

$$S_{Cx}^{S/H}(f)(f) = (1 - t_{on}/T)^2 \frac{2\theta}{C_x} T \frac{sin^2\left[(1 - t_{on}/T)\pi Tf\right]}{\left[(1 - t_{on}/T)\pi Tf\right]^2} \qquad \text{(C-2)}$$

In the circuit in Fig. C-2, the unity-gain frequency of the op-amp f_u is the bandwidth limiting element for S_{eq} while the other noise sources can be considered low-passed filtered by filters whose RC time constants are several times higher than the op-amp bandwidth. Thus, we have for the sampled-and-held noise in C_{AZ} (one-sided).

$$S_{Caz}^{S/H}(f) = \frac{2\theta}{C_{AZ}} T \left(1 + \frac{R_{eq} C_{AZ} \omega_u}{1 + K_a}\right) (1 - t_{az}/T)^2 \frac{sin^2\left[(1 - t_{az}/T)\pi Tf\right]}{\left[(1 - t_{az}/T)\pi Tf\right]^2} \qquad \text{(C-4)}$$

where $K_a \equiv C_{AZ}/C_h$, R_{eq} is an equivalent resistor for the op-amp input referred noise, and ω_u is the unity-gain frequency of the op-amp. The first term in the first parenthesis appear due to the noise sources of the transistors and the switches, which are not filtered by the op-amp rolloff.

As stated above, the transfer of this noise to the output is different in t_{sam} and in t_{hol}. In t_{sam} the transfer function to the output is $(1+R_1/R_S)^2$, $R_i = \left(\partial I_D / \partial V_S\right)^{-1}\Big|_{V_S=V_D=V_X}$ for transistor M_i. In t_{hol} the transfer function to the output is 1. The noise held in C_{AZ} contribution to the output for low (baseband) frequencies is thus given by:

$$S_{Caz\_out}^{S/H}(f) = \frac{2\theta}{f_s C_{AZ}}\left(1+\frac{R_{eq}C_{AZ}\omega_u}{1+K_a}\right)\left[\left(1+\frac{R_1}{R_s}\right)^2 (t_{sam}/T)^2 + (t_{hol}/T)^2\right] \quad \text{(C-5)}$$

C.2.2 Sampled-and-held noise in C_h

The noise sampled in C_h at the end of the sampling phase can be divided into two non-correlated noise spectral densities. The first one is due to the broadband noise sources present in t_{sam}. The second one is a function of the noise held in C_{AZ} during t_{az}.

For the white noise sources present during t_{sam}, consider the circuit in Fig. C-3. The white noise sources are low-pass filtered by the corresponding RC time constants and/or by the op-amp rolloff. The resulting contribution for low (passband) frequencies is:

$$S_{Ch\_1}^{S/H}(f) = \frac{2\theta}{f_s C_h}\left(1+\left(R_{on}+R_{eq}\right)C_h\omega_u\right)(1-t_{sam}/T)^2 \quad \text{(C-6a)}$$

The sampled-and-held noise in C_{AZ} is transferred C_h with a gain $(R_1/R_s)^2$. Thus,

$$S_{Ch\_2}^{S/H}(f) = \frac{2\theta}{f_s C_{AZ}}\left(1+\frac{R_{eq}C_{AZ}\omega_u}{1+K_a}\right)\left[\left(\frac{R_1}{R_s}\right)^2 (1-t_{sam}/T)^2\right] \quad \text{(C-6b)}$$

Both (C-6a) and (C-6b) are transferred to the output with a unity-gain. If we consider the circuit without offset compensation, as in Fig. 3-2, R_{on}=0 in (C-6a) and (C-6b) also equals to zero.

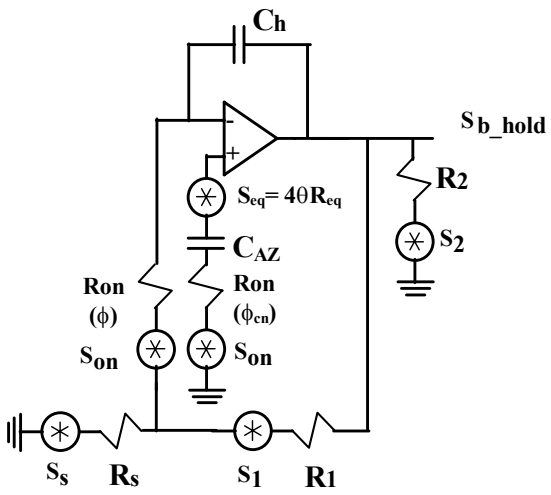


Fig. C-3. Noise equivalent circuit for the sample period.

C.3 Total noise in the output

The total noise in the output is the sum of the contributions given by (C-1), (C-5) and (C-6), i. e.,

$$S_{OUT}(f) = S_{hol}^{b}(f) + S_{Caz\_out}^{S/H}(f) + S_{Ch\_1}^{S/H}(f) + S_{Ch\_2}^{S/H}(f) \qquad \text{(C-7)}$$

Appendix D – Harmonic distortion analysis

The analysis in this section is valid for both circuits in Fig. 3-2 and in Fig. 3-4. In fact, any imperfections in the operation of the AZ circuit will produce a residual offset, which can be treated as an op-amp offset voltage that has not been corrected for. Thus, the analysis for the circuit without offset correction, repeated here for convenience in Fig. D-1, will be performed.

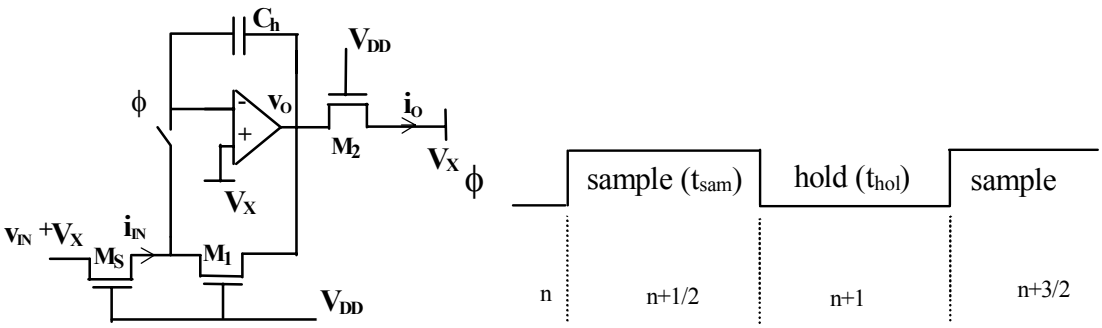


Fig. D-1 The basic delay cell of the SM methodology.

D.1 Effect of the op-amp offset voltage.

In strong inversion the drain current in a MOSFET is given [8] by

$$i_D = K\left[\left(V_P - v_S\right)^2 - \left(V_P - v_D\right)^2\right] \tag{D-1}$$

where v_S, v_D are the source and drain voltages referred to the substrate, $K \equiv \frac{\mu C_{ox}^{'} n}{2}\frac{W}{L}$.

In the circuit in Fig. D-1 we have, considering the op-amp offset voltage:

$$i_{D\_M1(n+1/2)} = -i_{IN(n+1/2)} = K_1\left[\left(V_P - V_X - V_{OS}\right)^2 - \left(V_P - v_{O(n+1/2)}\right)^2\right] \tag{D-2}$$

$$i_{O(n+1)} = K_2\left[\left(V_P - V_X\right)^2 - \left(V_P - v_{O(n+1)}\right)^2\right] \tag{D-3}$$

$$v_{O(n+1)} = v_{O(n+1/2)} \tag{D-4}$$

From (D-2), (D-3) and (D-4), we have:

$$i_{o(n+1)} = -\frac{K_2}{K_1} i_{in(n+1/2)} + \sqrt{2} K_2 V_{OS} V_P \tag{D-5}$$

D.2 Effect of the charge injected.

In this case, we have for the current in M_1:

$$i_{D\_M1(n+1/2)} = -i_{IN(n+1/2)} = K_1\left[\left(V_P - V_X\right)^2 - \left(V_P - v_{O(n+1/2)}\right)^2\right] \tag{D-6}$$

From (D-6), after some algebraic manipulations:

$$v_{O(n+1/2)} = -\sqrt{\frac{i_{IN(n+1/2)}}{K_1} + \left(V_P - V_X\right)^2} + V_P \tag{D-7}$$

Considering the charge injection as being constant, we have:

$$v_{O(n+1)} = v_{O(n+1/2)} + \Delta V_{ch} \tag{D-8}$$

where ΔV_{ch} is the constant charge injected into C_h at the end of the sampling phase. Considering worst case, $\Delta V_{ch} = \Delta V_{ch\_max}$, given by (3-29). ΔV_{ch_max} is the maximum voltage variation in C_h due to charge injection.

We have, for the (n+1) interval:

$$i_{O(n+1)} = K_2\left[\left(V_P - V_X\right)^2 - \left(V_P - v_{O(n+1)}\right)^2\right] \tag{D-9}$$

From (D-8) and (D-9):

$$i_{O(n+1)} = K_2\left[\left(V_P - V_X\right)^2 - \left(V_P - v_{O(n+1/2)} - \Delta V_{ch}\right)^2\right] \qquad \text{(D-10)}$$

Substituting (D-7) in (D-10) and making $K_1 = K_2$ (equal transistors) we arrive to:

$$i_{O(n+1)} = -i_{IN(n+1/2)} + 2\Delta V_{ch} K\left(V_P - V_X\right)\sqrt{1 + \frac{i_{IN(n+1/2)}}{K\left(V_P - V_X\right)^2}} \quad . \qquad \text{(D-11)}$$

Making Taylor series expansion and keeping the lower order terms:

$$i_{O(n+1)} = \sqrt{2}K_2\Delta V_{ch}V_P - i_{IN(n+1/2)}\left(1 - 2\sqrt{2}\frac{\Delta V_{ch}}{V_P}\right) - i_{IN(n+1/2)}^2\frac{\sqrt{2}}{2}\frac{\Delta V_{ch}}{K_2 V_P^3} + \\ + i_{IN(n+1/2)}^3\frac{\sqrt{2}}{2}\frac{\Delta V_{ch}}{K_2^2 V_P^5}\cdots \qquad \text{(D-12)}$$

As can be seen in (D-12), charge injection causes harmonic distortion. As the harmonic distortion caused by charge injection is independent of the frequency of the input signal, the distortion can be analysed by considering a harmonic signal distorted by a static non-linear transfer function; thus:

$$i_{O(t)} \cong 2\sqrt{2}\frac{\Delta V_{ch}}{V_P}I_{max} - \hat{I}\cos(\omega t) - \frac{\sqrt{2}}{8}\frac{\Delta V_{ch}}{V_P}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{\sqrt{2}}{32}\frac{\Delta V_{ch}}{V_P}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t)... \qquad \text{(D-13)}$$

where. $\hat{I} \le I_{MAX} = \frac{\mu C_{ox}' n}{4}\frac{W}{L}V_P^2 = \frac{K}{2}V_P^2$ and $\hat{I}\cos(\omega t) = i_{IN}$.

D.3 Effect of the finite DC gain of the op-amp

Considering for the MOSFET's the current in strong inversion given by (D-1), we have in this case:

$$i_{D\_M1(n+1/2)} = -i_{IN(n+1/2)} = K_1\left[\left(V_P - V_X + \frac{v_{O(n+1/2)}}{A}\right)^2 - \left(V_P - v_{O(n+1/2)}\right)^2\right], \qquad \text{(D-14)}$$

where A is the op-amp DC gain. Also,

$$i_{O(n+1)} = K_2\left[(V_P - V_X)^2 - (V_P - v_{O(n+1)})^2\right] \quad \text{(D-15)}$$

and

$$v_{O(n+1)} = v_{O(n+1/2)} \quad \text{(D-16)}$$

From (D-14), (D-15) and (D-16), we have:

$$i_{O(n+1)} = -\frac{K_2}{K_1} i_{IN(n+1/2)} - 2K_2(V_P - V_X)\frac{v_{O(n+1/2)}}{A} \quad \text{(D-17)}$$

Equation (D-14) can be rewritten as

$$v_{O(n+1/2)} = -(V_P - V_X)\sqrt{1 + \frac{i_{in(n+1/2)}}{K_2(V_P - V_X)^2} + \frac{2\sqrt{2}}{A}} + V_P + \frac{1}{A}(V_P - V_X) \quad \text{(D-18)}$$

From (D-17) and (D-18) we have, considering $K_1 = K_2 = K$:

$$i_{O(n+1)} \cong -i_{IN(n+1/2)} + \frac{2K}{A}(V_P - V_X)^2\sqrt{1 + \frac{i_{IN(n+1/2)}}{K(V_P - V_X)^2} + \frac{2\sqrt{2}}{A}} - \frac{2K}{A}(V_P - V_X)V_P \quad \text{(D-19)}$$

Expanding (D-19) into Taylor series and keeping the lower order terms:

$$i_{O(n+1)} \cong \frac{1}{A}KV_P^2\left(1 - \sqrt{2}\right) - i_{IN(n+1/2)}\left(1 - \frac{1}{A}\right) - i_{IN(n+1/2)}^2 \frac{1}{2A}\frac{1}{KV_P^2} + i_{IN(n+1/2)}^3 \frac{1}{2A}\frac{1}{K^2V_P^4} \ldots \quad \text{(D-20)}$$

As can be seen in (D-20), the op-amp finite DC gain causes harmonic distortion. As the harmonic distortion caused by the op-amp finite DC gain is independent of the frequency of the input signal, the distortion can again be analysed by considering a harmonic signal distorted by a static non-linear transfer function; thus:

$$i_{O(t)} \cong \frac{2\left(1 - \sqrt{2}\right)}{A} I_{max} - \hat{I}\cos(\omega t) - \frac{1}{8A}\frac{\hat{I}^2}{I_{max}}\cos(2\omega t) + \frac{1}{32A}\frac{\hat{I}^3}{I_{max}^2}\cos(3\omega t) \ldots \quad \text{(D-21)}$$

where $\hat{I} \le I_{MAX} = \frac{\mu C_{ox}^{'} n}{4} \frac{W}{L} V_P^2 = \frac{K}{2} V_P^2$ $\hat{I}\, cos(\omega t) = i_{IN}$.

Appendix E – Analysis of the offset effects on the universal SM biquad

Considering in the universal switched-MOSFET biquad in Fig. 2-11 V_{ij} as the offset voltage of op-amp A_{ij}, with i=1,2 and j=1,2, we have

$$V_{OA1}^{\phi_o} = (2 + K_2 + f)V_{11} - fz^{-1/2}V_{OB2}^{\phi_e} - z^{-1/2}V_{OB1}^{\phi_e}, \tag{E-1}$$

$$V_{OA2}^{\phi_o} = (2 + K_3 + a)V_{21} - az^{-1/2}V_{OB1}^{\phi_e} - z^{-1/2}V_{OB2}^{\phi_e}, \tag{E-2}$$

$$V_{OB1}^{\phi_e} = (2 + a + f + K_1 + K_2)V_{12} - (a + f)V_{OB2}^{\phi_e} - z^{-1/2}V_{OA1}^{\phi_o}, \tag{E-3}$$

$$V_{OB2}^{\phi_e} = (2 + K_3)V_{22} - z^{-1/2}V_{OA2}^{\phi_o}, \tag{E-4}$$

Solving (E-1) to (E-4), we arrive to

$$V_{OB2}^{\phi_e} = \frac{-(2 + f + K_2)V_{11} + (3 + a + f + K_2)V_{12}}{a}. \tag{E-5}$$

Equation (2-10), will be repeated here:

$$\omega_o T \cong a \tag{E-6a}$$

$$Q \cong 1/f \tag{E-6b}$$

where T is the sampling period, ω_o is the centre frequency and Q is the quality factor. Substituting (E-6) in (E-5) we arrive to

$$V_{OB2}^{\phi_e} = -\frac{(V_{11} - V_{12})}{\omega_o T}\left[2 + \frac{1}{Q} + \frac{K_{BP}}{Q}\right] + 2V_{12} \tag{E-7}$$

where $K_{BP} = K_2 / f$ is the band-pass input gain.

References

[1] C. Toumazou, J. B. Hughes, and N. C. Battersby (eds.), *Switched-currents: an analogue technique for digital technology*, Peter Peregrinus, London, 1993.

[2] A. Rodriguez-Vázquez and E. Sánchez-Sinencio (eds.), "Special issue on low-voltage and low power analog and mixed-signal circuits and systems," *IEEE Trans. on Circuits and Systems I*, vol 42, November 1995.

[3] W. Serdijn, A. C. Van der Woerd, and J. C. Kvenen (eds.), "Special issue on low-voltage, low power analog integrated circuits," *IEEE, J. Analog Integrated Circuit and Signal Processing*, vol. 83, no. 4, July 1995.

[4] W. Serdijn, *The design of low-voltage low-power analog integrated circuits and their applications in hearing instruments*, Doctorate thesis, Delft University Press, Delft, The Netherlands, 1994.

[5] R. Hogervorst, *Design of low-voltage low-power CMOS operational amplifier cells*, Doctorate thesis, Delft University Press, Delft, The Netherlands, 1996.

[6] R. Castello, F. Montecchi, F. Rezzi, and A Baschirotto, "Low-voltage analog filters," *IEEE Trans. on Circuits and Systems I*, vol. 42, pp. 827-840, November 1995.

[7] C. Toumazou, F. J. Lidgey, and D. G. Haigh (eds.), *Analogue IC design: the current-mode approach*, Peter Peregrinus, London, 1990.

[8] C. Galup-Montoro, A. I. A. Cunha, and M. C. Schneider, "A current-based MOSFET model for integrated circuit design," in *Low-voltage low power integrated circuits and systems*, E. Sánchez-Sinencio and A. G. Andreou (eds), IEEE press, Piscataway, 1999.

[9] E. A. Vittoz , "Micropower techniques," in *Design of analog-digital VLSI circuits for telecommunications and signal processing*, J. E. Franca and Y. P. Tsividis (eds), Prentice Hall, New Jersey, 1994.

[10] Y. Matsuya, and J. Tamada, "1V power supply, low-power consumption A/D conversion technique with swing- suppression noise shaping," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1524-1530, December 1994.

[11] R Castello and L. Tomasini, "A BiCMOS speech circuit with only two external components," *IEEE J. Solid-State Circuits*, vol. 28, pp. 770-777, July 1991.

[12] D. Wayne et al, "A single chip hearing aid with one volt switched-capacitor filters," in *IEEE 1992 Custom IC Conference*, pp. 7.5.1-7.5.4, 1992.

[13] S. Yan, and E. Sanchez-Sinencio, "Low-voltage analog circuit design techniques: a tutorial," *IEICE Trans. Analog Integrated Circuits and Systems*, vol. e00-A, no. 2, February 2000.

[14] A. Masami, *Design for reliability of low-voltage, switched-capacitor circuits*, Doctorate thesis, University of California, Berkeley, 1999.

[15] J. Crols, and M. Steyaert, "Switched-Opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE J. Solid-State Circuits*, vol. 29, pp. 936-942, August 1994.

[16] M. Steyaert, J. Crols, and S. Gogaert, "Low-voltage analog CMOS filter design," in *Low-voltage/low-power integrated circuits and systems*, E. Sánchez-Sinencio, and A.

G. Andreou (eds.), IEEE Press, 1999.

[17] A. Baschirotto , R. Castello, and G. P. Montagna, "Active series switch for switch-opamp circuits," *Electron. Lett*., vol. 34, no. 14, pp.1365-1366, July 1998.

[18] S. Karthikeyan, A. Tamminneedi, C. Boecker, and E. K. F. Lee, "Design of low-voltage front-end interface for switched-opamp circuits", *IEEE Trans. Circuits and Systems - II*, vol. 48, no. 7, pp. 722-726, July 2001.

[19] J. Silva-Martínez, S. Solís-Bustos, J. Salcedo-Suñer, R.Rojas-Hernández, and M. Schellenberg, "A CMOS hearing aid device," in *Analog Integrated Circuits and Signal Processing*, 21 pp. 1-10, 1999.

[20] J. F. Duque-Carrillo, P. Malcovati, F. Maloberti, R. Pérez-Aloe, A. H. Reyes, E. Sánchez-Sinencio, G. Torelli, and J. M. Valverde, "VERDI: An acoustically programmable and adjustable CMOS mixed-mode signal processor for hearing aid applications," *IEEE J. Solid-State Circuits*, vol. 31, no. 5, pp. 634-645, May 1996.

[21] F. Callias, F. Salchli, and D. Girard, "A set of four IC's in CMOS technology for a programmable hearing aid," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 301-312, April 1989.

[22] W. A. Serdijn, A. C. van der Woerd, J. Davidse and A.H.M. van Roermund, "A low-voltage low-power fully-integratable front-end for hearing instruments," *IEEE Transactions on Circuits and Systems I*, Vol. 42, No. 11, pp. 920-932, November 1995.

[23] R. Gregorian and G. C. Temes, *Analog MOS integrated circuits for signal processing*, John Wiley & Sons, New York, USA, 1986.

[24] M. J. M. Pelgrom and M. Vertregt, "CMOS technology for mixed signal ICs," *Solid-State Electron*., vol. 41, pp. 967-974, 1997.

[25] J. C. M. Bermudez, M. C. Schneider, and C. Galup-Montoro, "Compatibility of switched capacitor filters with VLSI processes," *IEE Proc., Part G*, vol. 139, no. 4, pp. 413-418, August 1992.

[26] R. T. Gonçalves, S. Noceti F., M. C. Schneider, and C. Galup-Montoro, "Programmable switched current filters using MOSFET-only current dividers," *in Proc. 38th Midwest Symposium on Circuits and Systems*, vol. 1, pp. 1046-1049, Rio de Janeiro, August 1995.

[27] R. T. Gonçalves, S. Noceti F., M. C. Schneider, and C. Galup-Montoro, "Digitally programmable switched current filters," in *Proc. ISCAS*, vol. 1, pp. 258-261, May 1996.

[28] F. A. Farag, R. Faustino, S. Noceti F., C. Galup-Montoro, and M. C. Schneider, "A programmable second generation SI integrator for low-voltage applications," in *IX IFIP, Tutorials of International Conference on VLSI*, pp. 129-137, Brazil, August 1997.

[29] F. A. Farag, C. Galup-Montoro, and M. C. Schneider, "Digitally programmable switched-current FIR filter for low-voltage applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 637-641, April 2000.

[30] F. A. Farag, *Digitally programmable low-voltage switched-current filters*, Doctorate thesis, Federal University of Santa Catarina, Brazil, 1999.

[31] C. C. Enz. *High precision CMOS micropower amplifiers*. Ph.D. thesis no. 802, EPF-

Lausanne, Switzerland, 1989.

[32] K. Bult, and G. J. G. M Geelen, "An inherently linear and compact MOST-only current division technique," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1730-1735, December 1992.

[33] B. C. Rothenberg, S. H. Lewis, and P. J. Hurst, "A 20-M sample/s switched-capacitor finite-impulse-response filter using a transposed structure," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1350–1356, December 1995.

[34] R. Faustino, *Filtros a correntes chaveadas programáveis digitalmente*, Master thesis, Federal University of Santa Catarina, Brazil, 1999, in Portuguese.

[35] J. Silva-Martinez, and E. Sánchez-Sinencio, "Biquadratic programmable SC filters with additional flexibility and reduced total capacitance," *Int. Journal of Circuit Theory and Applications*, vol. 17, no. 2, pp. 241-248, April 1989.

[36] K. Nagaraj, J. Vlach, T. R. Viswanathan, and K. Singhal, "Switched-capacitor integrator with reduced sensitivity to amplifier gain". *Electronic Lett.*., vol. 22, pp. 1103-1105, 1986.

[37] C. A. Gobet, and A. Knob "Noise analysis of switched capacitor networks," *IEEE Trans. on Circuits and Systems*, vol. CAS-30, pp. 37-43, January 1983.

[38] C. C. Enz, and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correleted double sampling, and chopper stabilization," in *Proc. of the IEEE*, pp. 1584-1614, November 1996.

[39] D. A. Johns and K. Martin, *Analog integrated circuit design*, John Wiley & Sons, New York, 1997.

[40] G. Wegmann et al, "Charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. 22, pp. 1091–1097, December 1987.

[41] V. S. Cheung, H. C. Luong, and W. Ki, "A 1-V CMOS switched-opamp switched-capacitor pseudo-2-path filter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 14–22, January 2001.

[42] J. Millman, and A. Grabel, "Microelectrónica," McGraw-Hill, Lisbon, 1992, in Portuguese.

[43] S. Karthikeyan, S. Mortezapour, A. Tammineedi, And E. K. F. Lee, "Low-voltage analog circuit design based on biased inverting opamp configuration," *IEEE Transaction on Circuits and Systems II: Analog and Digital Signal Processing*, vol 47, no. 3, pp. 176-184, March 2000.

[44] SMASH users manual, Dolphin Integration, Meylan, France, 1997.

[45] V. C. Vincence, "Projeto de amplificadores operacionais para a tecnologia de MOSFET-chaveado," *Exame de qualificação*, Federal University of Santa Catarina, Brazil, in Portuguese, to be published.

[46] V. C. Vincence, C. Galup-Montoro, and M. C. Schneider, "Low-voltage class AB operational amplifier," in *14th Symposium on Integrated Circuits and Systems Design*, pp. 207-211, Pirenópolis, Brazil, September 2001.

[47] F. Maloberti, "Layout of analog and mixed analog-digital circuits," in *Design of analog-digital VLSI circuits for telecommunications and signal processing*, Chapter 11,

pp. 341-367, Prentice-Hall, New Jersey, 1994.

[48] D. Rocha, M. M. Boone, and W. A. Serdijn, "A strong directional, wearable hearing aid adapter," in *Proc. of the ProRISC 2000*, pp. 465-470, Veldhoven, The Netherlands, December 2000.

[49] E. A. Vittoz, "Dynamic Analog Techniques," in *Design of analog-digital VLSI circuits for telecommunications and signal processing*, J. E. Franca and Y. P. Tsividis (eds), Prentice-Hall, New Jersey, 1994.

[50] J. B. Hughes, N. C. Bird, and I. C. Macbeth, "Switched currents - a new technique for analog sampled-data signal processing," in Proc. ISCAS, pp. 1584-1587, May 1989.

[51] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design", *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510-1519, October 1998.

Published papers

[1] L. C. C. Marques, C. Galup-Montoro, S. Noceti Filho, and M. C. Schneider, "Switched-MOSFET technique for programmable filters operating at low-voltage supply," *Proceedings of XV SBMicro - International Conf. on Microelectronics & Packaging*, pp. 170-174, Manaus, Brazil, September, 2000.

[2] L. C. C. Marques, C. Galup-Montoro, S. Noceti Filho, and M. C. Schneider, "Switched-MOSFET sampled-data technique for low-voltage supply: a brief tutorial," *Proceedings of ProRISC2000 - 11th Workshop on Circuits, Systems and Signal Processing*, pp.395-400, Veldhoven, The Netherlands, November 2000.

[3] L. C. C. Marques, C. Galup-Montoro, S. Noceti Filho, and M. C. Schneider. "A switched-MOSFET filter for application in hearing aid devices". *Proc. ISCAS,* I-77 – I-80, Sidney, Australia, May 2001.

[4] L. C. C. Marques, C. Galup-Montoro, S. Noceti Filho, and M. C. Schneider. "Switched-MOSFET technique for programmable filters operating at low-voltage supply". *Proc. ISCAS,* I-73 – I-76, Sidney, Australia, May 2001.

[5] W. A. Serdijn, J. Mulder, D. Rocha, and L. C. C. Marques, "Advances in low-voltage ultra-low-power analog circuit design," *Proceedings of ICECS2001 - International IEEE Conference on Electronics, Circuits, and Systems,* pp.1533-1536, Malta, September 2001.

[6] L. C. C. Marques, W. A. Serdijn, C. Galup-Montoro, and M. C. Schneider, "A switched-MOSFET programmable low-voltage filter," *Proceedings of SBCCI2002 – 15th Symposium on Integrated Circuits and Systems Design*, pp. 254-257, Porto Alegre, Brazil, September, 2002.