Analysis and Design of the Three-Inverter Schmitt Trigger for Supply Voltages Down to 50 mV

Thiago Darós Fernandes, Carlos Galup-Montoro and Márcio Cherem Schneider

***Abstract*—This brief analyzes the operation of the three-inverter Schmitt trigger (TI-ST) at ultra-low supply voltages. Included in the analysis is a model to predict the supply voltage at which the TI-ST changes from the amplifier mode to the hysteresis mode. We show theoretically that the TI-ST can exhibit hysteresis for a supply voltage as low as the fundamental limit of unity gain of the CMOS inverter. We also demonstrate experimentally that, with a suitable design, hysteresis starts to occur from a supply voltage as low as 48.5 mV. A relaxation oscillator built with a TI-ST and standard inverters is experimentally demonstrated to start to oscillate from supply voltages as low as 62 mV.**

***Index Terms*—CMOS, ultra-low voltage, subthreshold, Schmitt trigger, hysteresis, relaxation oscillator.**

I. Introduction

Devices that operate in inaccessible environments cannot have regular battery replacements and, in most cases, must be of small size. Harvesting energy from the surroundings is a common choice to operate such devices, but, in many cases, the harvesting devices provide voltages of the order of 100 mV or less [1]. CMOS electronics is possible at such low supply voltages [2]–[8], which are well below the standard supply voltages.

In 1972, in the first paper on the subthreshold operation of the CMOS inverter [2], the authors observed that the smallest supply voltage for the proper function of the inverter was approximately $8kT/q$, 200 mV at room temperature. This statement remained valid until the 2000s, when sub-200 mV circuits [3]–[5], [7] started to appear. The interest in the ultra-low-voltage domain keeps on, as demonstrated by recent papers on sub-100 mV circuits [6], [8]–[10].

There are two main driving forces for supply voltages below the typical values in the range of 200 to 350 mV, commonly used to minimize the energy per logic operation. Firstly, ultra-low voltages reduce the power consumption of circuits with long standby times, such as sensor nodes for the IoT [6], [8]. Secondly, ultra-low voltage circuits can operate from thermal or electrochemical harvesting devices which often provide extremely low voltages, of the order of 100 mV or even less [1], [11], [12]. Additionally, potentials in the range 50-100 mV are close to the Nernst potentials found in biological cells [13], which can be harvested from living systems [7].

The use of feedback to match the N- and P-channel MOSFET currents allows digital CMOS circuits in a standard 180 nm CMOS technology to operate at 100 mV [3]. Operation at room temperature with a supply of 62 mV was achieved using logic gates built around the classical Schmitt trigger (ST) [6] shown in Fig. 1; however, in practice the ST operates as an amplifier for supply voltages below 100 mV. A recent paper by Pasini et al. [14] provides expressions that describe the DC transfer function of the classical ST at ultra-low voltages. One of the main results of [14] is the theoretical minimum supply voltage (V_{DDH}) at which the classical ST switches from the amplifier mode to the hysteresis mode, given by

$$V_{DDH} = 2\phi_t \ln\left(2+\sqrt{5}\right) = 75 \text{ mV at } 300 \text{ K} \qquad (1)$$

where ϕ_t is the thermal voltage (25.9 mV at 27°C). In structures used in practice, the measured values are usually higher than 100 mV. So far, a Schmitt trigger for sub-100 mV operation has not been devised yet.

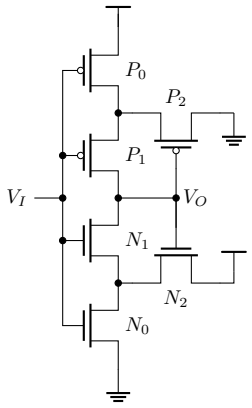

Fig. 1. Classical Schmitt trigger.

In this study, the alternative Schmitt trigger shown in Fig. 2, referred to herein as the three-inverter ST (TI-ST), is revised and analyzed for operation at ultra-low voltages. The TI-ST, described in [15], more commonly seen as a non-inverter ST [16]–[19] and frequently detailed in textbooks [20], consists of three balanced CMOS inverters with a positive feedback path. However, the weak inversion analysis of this circuit has yet to be carried out. For the sake of simplicity, we assume that the P transistors are well-balanced with the N transistors. Here, K

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and J represent the ratios S_3/S_1 and S_2/S_1, respectively. $S = W/L$ is the aspect ratio whereas W and L are the transistor width and length, respectively.

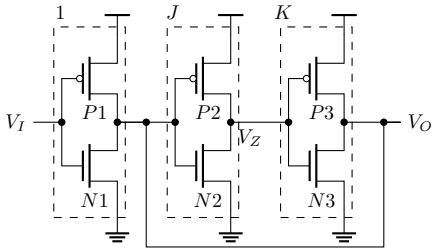

Fig. 2. Three-inverter Schmitt trigger (TI-ST) circuit.

For the purpose of a first-order analysis of the TI-ST, we used the symmetrical weak inversion current-voltage model of the MOS device [21] shown below,

$$I_{DN(P)} = I_{N(P)} \mathrm{e}^{\frac{V_{GB(BG)}}{n_{N(P)}\phi_t}} \left(\mathrm{e}^{\frac{-V_{SB(BS)}}{\phi_t}} - \mathrm{e}^{\frac{-V_{DB(BD)}}{\phi_t}} \right) \quad (2)$$

where $I_{N(P)}$ is the NMOS (PMOS) transistor strength or scaling factor, $n_{N(P)}$ is the slope factor, and G, S, D and B are the gate, source, drain and bulk nodes, respectively.

The numerical solutions of the TI-ST nodal equations for the ratios and supply voltages indicated in the captions, result in the voltage transfer characteristics (VTCs) shown in Figure 3. The curves in Figure 3 were determined in this work as in [14]. For each value of the input voltage V_I, the current through a voltage source V_O at the output node, swept from 0 to V_{DD}, was determined. The values of V_O for which the current is zero determine a point of the characteristic curve. If the value of V_I is within the hysteresis window, there are three values of V_O for which the current is zero. Figure 4 shows the

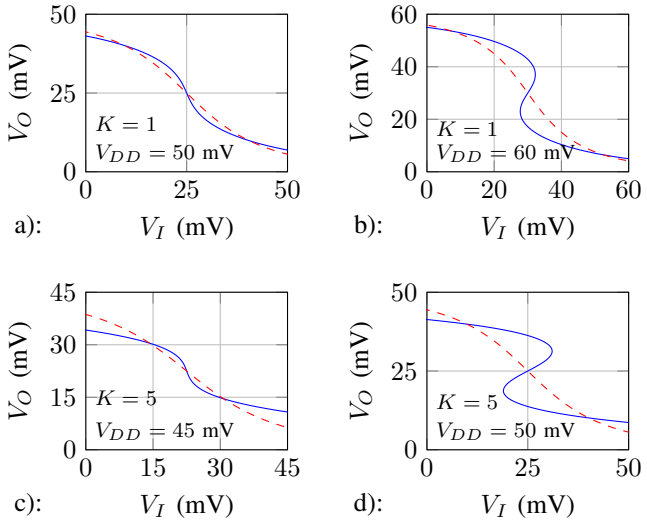

Fig. 3. VTCs of TI-ST (solid line) with $J = 1$ and classical ST (dashed line) with relative current strengths of $I_0/I_1 = I_0/I_2 = 2$ for balanced transistors with $n = 1.3$.

simulated VTCs for a balanced inverter, a classical ST, and a TI-ST for which $K = 5$ and $J = 1$. As demonstrated in [14], the classical ST is not able to provide hysteresis for supply voltages below 100 mV, but the TI-ST can achieve this for 50 mV, as shown in Figure 4.

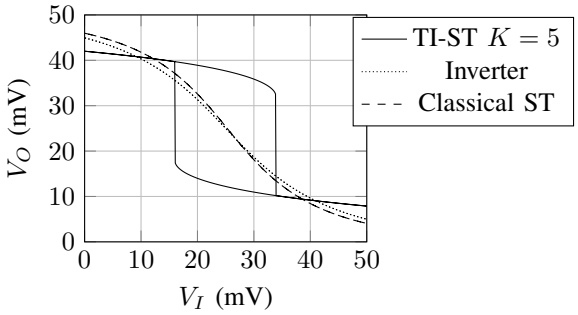

Fig. 4. VTCs of the cells indicated in the inset in a 0.18 μm technology for $V_{DD} = 50$ mV. Classical ST with $I_0/I_1 = I_0/I_2 = 2$.

In this communication, we analyze the subthreshold operation of the TI-ST. In addition, we demonstrate that the TI-ST is theoretically capable of generating hysteresis from V_{DD} as low as the fundamental limit of 36 mV at room temperature [22]. Section II describes the small-signal model of the TI-ST used to find its voltage gain. Based on the results reported in Section II, we find the value of the supply voltage for which the TI-ST changes from amplification to hysteretic mode, as described in Section III. Section IV reports simulation and experimental results for the DC characteristics of the TI-ST, along with a prototype of a relaxation oscillator that demonstrates the usefulness of the TI-ST at ultra-low voltages.

II. Small-Signal Analysis

In this Section, the transition between the amplifier and hysteresis modes is determined. The analysis that follows is valid for the DC operating point $V_I = V_Z = V_O = V_{DD}/2$. Each inverter is modeled as a voltage-controlled current source ($g_m V_g$) with g_{md} as the output conductance (g_m is the gate transconductance), as shown in Figure 5. The values of g_m and g_{md}, calculated from (2), are shown in Table I.

TABLE I
Transconductances of the TI-ST for $V_I = V_O = V_{DD}/2$

g_{mi}	g_{mdi}
$2\frac{I_i}{n\phi_t}\mathrm{e}^{\frac{V_{DD}}{2n\phi_t}}\left(1-\mathrm{e}^{-\frac{V_{DD}}{2\phi_t}}\right)$	$2\frac{I_i}{\phi_t}\mathrm{e}^{\frac{V_{DD}}{2\phi_t}}\left(\frac{1}{n}-1\right)$
$I_{N_i} = I_{P_i} = I_i$	$i = 1, 2, 3.$

The values for the (trans)conductance of inverters 2 and 3 are J and K times greater, respectively, than that of inverter 1. The small-signal gain at the midpoint of the VTC is

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = -\frac{g_{m1}}{g_{md1}} \frac{1}{1 - \frac{g_{m2}}{g_{md2}}\frac{g_{m3}}{g_{md1}} + \frac{g_{md3}}{g_{md1}}} \quad (3)$$

Since $g_{m3}/g_{m1} = g_{md3}/g_{md1} = K$ and the inverter gain $A_V = -g_{mi}/g_{mdi}$, where i=1, 2, 3 is the same for the three inverters, the previous result can be further written as

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = \frac{A_V}{1 + K(1 - A_V^2)} \quad (4)$$

Figure 6 shows the voltage gain of both the standard inverter and the TI-ST with identical inverters ($J = K = 1$) in terms

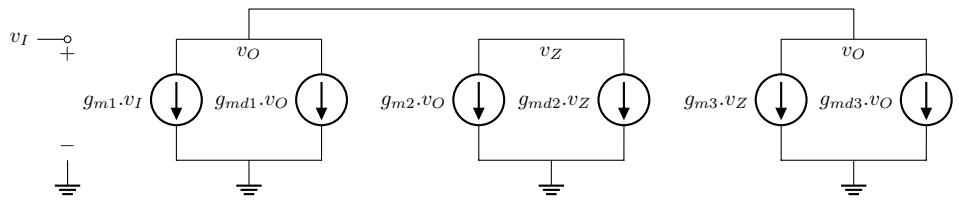

Fig. 5. TI-ST small-signal model.

of the supply voltage. The left branch of the TI-ST curve is associated with the amplification operation, whereas the right branch is associated with the hysteresis operation. The value of the supply voltage at which the gain changes sign or, in other terms, the supply voltage at which the gain is infinity, is the minimum V_{DD} required for the appearance of hysteresis. In

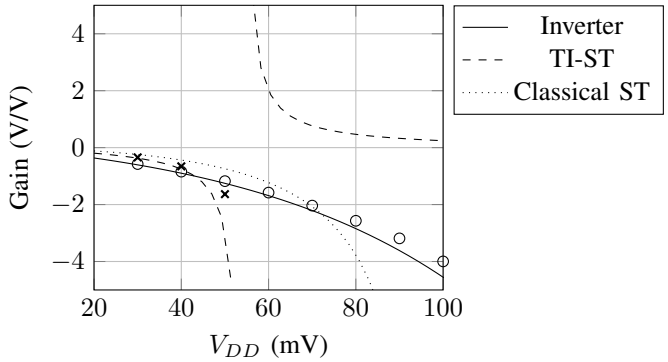

Fig. 6. Calculated and measured gains for an inverter, a TI-ST ($K = 1$) and a classical ST ($I_0/I_1 = I_0/I_2 = 2$), with $n = 1.3$ at 27°C. Circles: inverter measurements. Crosses: TI-ST measurements.

the general case of an NMOS/PMOS imbalance, the inverter voltage gain is affected; consequently, the TI-ST gain is also affected. Figure 7 shows the dependence of both the inverter switching voltage V_M and the voltage gain A_V deduced from (2). Here, α= I_N/I_P is the imbalance factor.

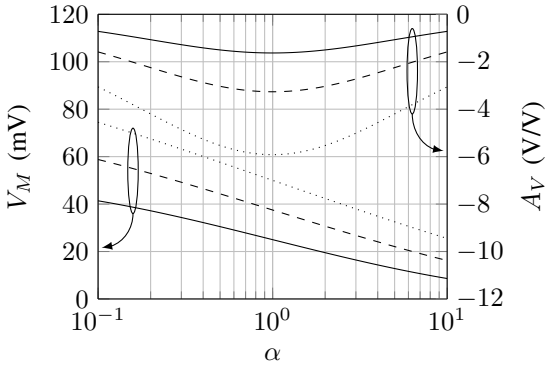

Fig. 7. Inverter switching voltage V_M and voltage gain A_V in terms $\alpha = I_N/I_P$ for $n = 1$ and 27°C. The solid, dashed and dotted lines correspond to $V_{DD} = 50$, 75 and 100 mV, respectively.

III. Minimum V_{DD} required for the appearance of hysteresis

For the purpose of finding the discontinuous transition between amplification and hysteresis modes, the condition $v_O/v_I = \infty$ is applied to (4) [14], yielding

$$A_V = \sqrt{1 + \frac{g_{m1}}{g_{m3}}} \tag{5}$$

Thus, the minimum inverter gain for the occurrence of hysteresis in the TI-ST is given by (5). Applying the inverter gain equation for $V_{DD}/2$, $g_{m1}/g_{md1} = (e^{\frac{V_{DDH}}{2\phi_t}} - 1)/n$ as shown in Table I, yields

$$V_{DDH} = 2\phi_t \ln\left(1 + n\sqrt{\frac{1+K}{K}}\right) \tag{6}$$

where n is the slope factor. Figure 8 shows the dependence of V_{DDH} on K, for two values of n and α. Theoretically, for $n = 1$ and $\alpha = 1$, a scale factor $K = 3$ is sufficient to reach infinity gain at $V_{DD} \approx 40$ mV. With $n = 1$ and $K >> 1$, (6) reduces to $V_{DDH_{min}} \approx 2\phi_t \ln(2)$. Hence, the TI-ST is able to exhibit hysteresis for a supply voltage as low as the fundamental limit of unity gain for the CMOS inverter [22]. The gain decreases symmetrically around $\alpha = 1$, which in turn implies on a higher V_{DDH} and $V_{DDH}|_\alpha = V_{DDH}|_{1/\alpha}$.

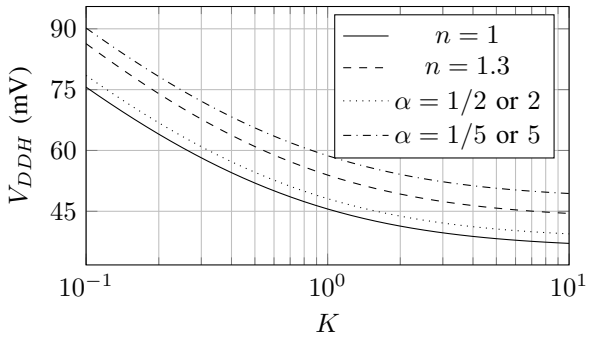

Fig. 8. Minimum V_{DD} required for infinity gain at 27°C versus K. $n = 1$ and $\alpha = 1$, except when indicated.

IV. Simulation and Experiment

Two designs for $K = 1$ ($S_{P1} = 2\mu$m$/0.6\mu$m) and $K = 5$ ($S_{P1} = 10\mu$m$/0.6\mu$m) were simulated with process variations and mismatch in a 0.18 μm technology. The histograms of the hysteresis widths are plotted in Fig. 9. For $K = 1$, none of the samples showed hysteresis, as expected from (6), whereas for $K = 5$ all samples with wider transistors and 97.5 percent of those with narrower transistors exhibited hysteresis. The ratio (equal to 3) of the widths of the NMOS transistors to those of the PMOS transistors provides symmetry to the TI-STs for typical technology parameters and supply voltages from 50 mV to 100 mV.

Three TI-STs with scale factors of $K = 5$, 1, and $1/5$, along with an inverter, were integrated in a 0.18 μm technology, as shown in Fig. 10. The aspect ratio of the unit PMOS transistor is $S = 2\mu$m$/0.6\mu$m, whereas that of the NMOS transistor is $S = 6\mu$m$/0.6\mu$m. Inverter 3 is composed of five inverters connected in parallel for $K = 5$. The same procedure was

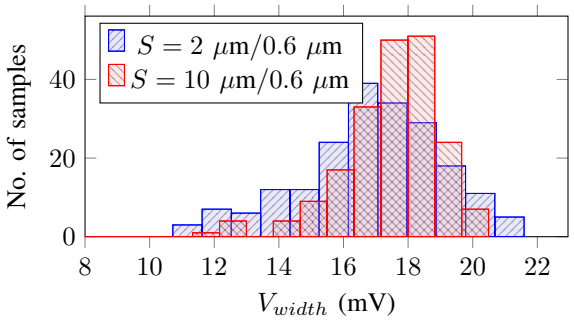

Fig. 9. Simulated hysteresis widths for 200 samples, $V_{DD} = 50$ mV, $K = 5$. Inset: aspect ratios of PMOS transistors. NMOS transistors are 3 times wider than PMOS transistors.

adopted with inverter 1 for $K = 1/5$. The measured slope factor n for both N- and P-channel transistors, extracted using the g_m/I_D method described in [23], is around $n = 1.3$. Therefore, the expected minimum V_{DDH}, according to (6), is approximately 46 mV for $K = 5$.

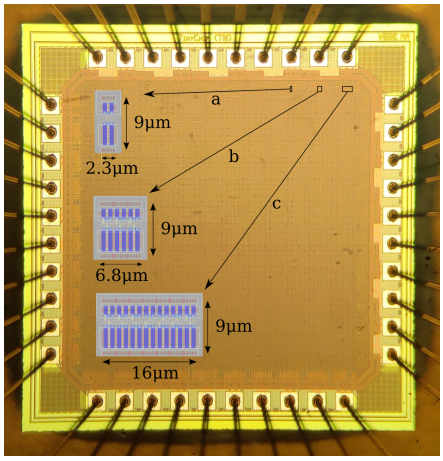

Fig. 10. Photo of the 2 mm × 2 mm die, fabricated in a 0.18 μm technology node. a: CMOS inverter cell, b: TI-ST $K = 1$, c: TI-ST $K = 5$.

Figure 11 shows the measured VTCs for each design. As can be seen, the gain increases with the scale factor. Also, as predicted, the VTC presents hysteresis for $K = 5$ and $V_{DD} = 50$ mV. The measured minimum voltage for the appearance of hysteretic behavior is $V_{DD} = 48.5$ mV, which matches closely the value (46 mV) predicted using small-signal analysis.

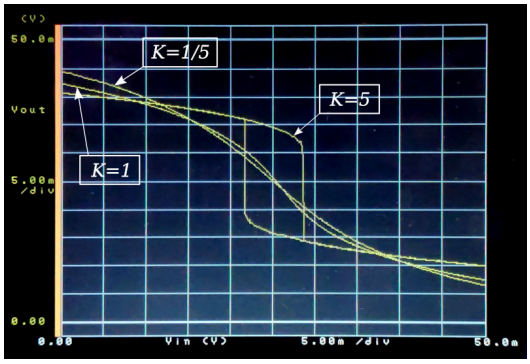

Fig. 11. Measured VTCs for the TI-STs ($K = 1/5$, 1, 5), $V_{DD} = 50$ mV.

Figure 12 shows the measured hysteresis widths (V_{width}) for different supply voltages. The hysteresis curves start to appear for values of the supply voltage predicted by (6). For the case of high positive feedback ($K = 5$), the hysteresis window is wider than the supply voltage for $V_{DD} \geq 70$ mV. Figure 13 shows the VTC curves for the TI-STs with $K = 5$ and $K = 1$, as well as that of the classical ST. Note that the classical ST does not presents hysteresis, whereas the TI-ST with $K = 5$ presents a window of around 160 mV, which is wider than the supply voltage.

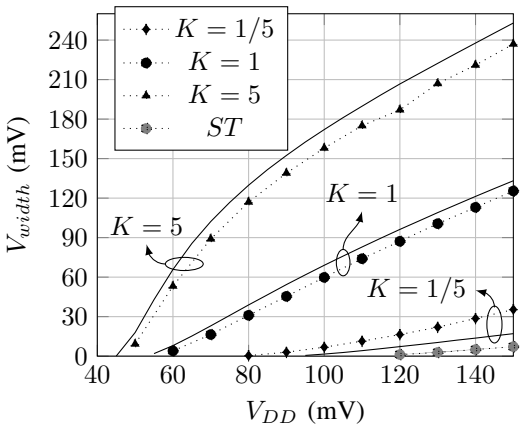

Fig. 12. Measured (symbols) and simulated (solid lines) hysteresis widths versus V_{DD}.

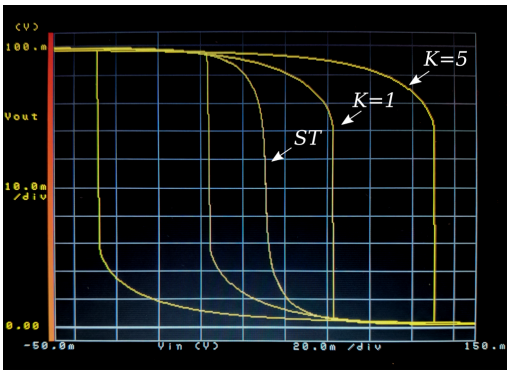

Fig. 13. Measured VTCs for the TI-STs ($K = 1$ and $K = 5$) and the classical Schmitt trigger (ST), $V_{DD} = 100$ mV.

In order to verify the hysteresis effectiveness, inverters and a TI-ST from different chips of the same batch were interconnected to build the relaxation oscillator, shown in Figure 14, which consists of a $K = 1$ TI-ST followed by a two-stage inverter that operates as a voltage-controlled current source (VCCS), along with an off-chip capacitor.

Figure 15 shows the waveform for supply voltages of $V_{DD} = 65$ mV and $V_{DD} = 100$ mV, with $C_L = 10$ pF. The oscillation frequency measured over a range of supply voltages from 60 mV to 180 mV is shown in Figure 16. Oscillations start from $V_{DD} = 62$ mV and disappear above $V_{DD} = 180$ mV, since V_{width} becomes greater than V_{DD}, as expected from the extrapolation of the curve for $K = 1$ in Fig. 12. The frequency does not increase proportionally with the inverse of C_L owing to parasitic capacitances introduced by pad sharing with other circuits of our chip.

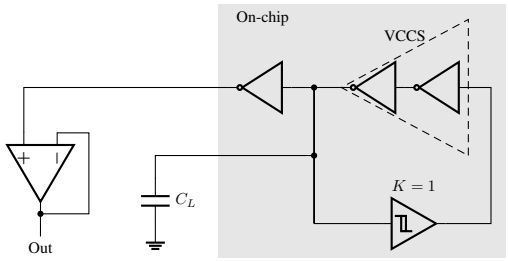

Fig. 14. Schematic of the relaxation oscillator (TI-ST, VCCS and C_L), along with the measurement interface circuit (inverter and voltage follower).

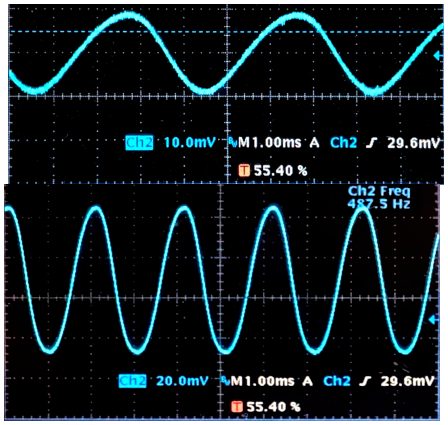

Fig. 15. Measured output waveforms of the relaxation oscillator for $V_{DD} =$ 65 mV (top) and $V_{DD} = 100$ mV (bottom).

V. Summary

In this paper we have analyzed and measured the characteristics of the three-inverter Schmitt trigger for ultra-low voltages. The TI-ST is able to achieve hysteresis starting from supply voltages as low as 50 mV. A prototype of a relaxation oscillator demonstrated the usefulness of the TI-ST for ultra-low voltage applications. With the increasing demand for sub-200 mV circuits, the TI-ST could be a suitable choice for the realization of noise reduction interfaces, pulse-signal processing and oscillators.

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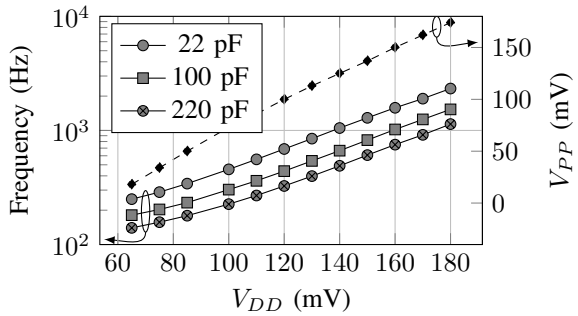

Fig. 16. Measured frequency of the relaxation oscillator for $K = 1$ and different values of C_L . The peak-to-peak voltage was measured for C_L= 100 pF.

References

[1] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants," *IEEE journal of solid-state circuits*, vol. 49, no. 12, pp. 2812–2824, 2014.

[2] R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE J. Solid-State Circuits*, vol. 7, no. 2, pp. 146–153, 1972.

[3] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, and E. Nowak, "Low-power CMOS at Vdd = 4kT/q," in *Device Research Conference. Conference Digest (Cat. No. 01TH8561)*. IEEE, 2001, pp. 22–23.

[4] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin *et al.*, "Performance and variability optimization strategies in a sub-200 mV, 3.5 pJ/inst, 11 nW subthreshold processor," in *2007 IEEE Symposium on VLSI Circuits*. IEEE, 2007, pp. 152–153.

[5] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, 2007.

[6] N. Lotze and Y. Manoli, "A 62 mV 0.13 μm CMOS standard-cell-based design technique using Schmitt-trigger logic," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 47–60, 2012.

[7] J. Choi, E. Aklimi, C. Shi, D. Tsai, H. Krishnaswamy, and K. L. Shepard, "Matching the power, voltage, and size of biological systems: A nW-scale, 0.023-mm^3 pulsed 33-GHz radio transmitter operating from a 5 kT/q-supply voltage," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 8, pp. 1950–1958, 2015.

[8] N. Lotze and Y. Manoli, "Ultra-sub-threshold operation of always-on digital circuits for IoT applications by use of Schmitt trigger gates," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 11, pp. 2920–2933, 2017.

[9] C. Qian, A. Peschot, B. Osoba, Z. A. Ye, and T.-J. K. Liu, "Sub-100 mV computing with electro-mechanical relays," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1323–1329, 2017.

[10] A. A. Vatanjou, T. Ytterdal, and S. Aunet, "An ultra-low voltage and low-energy level shifter in 28-nm UTBB-FDSOI," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 899–903, 2018.

[11] C. J. Love, S. Zhang, and A. Mershin, "Source of sustained voltage difference between the xylem of a potted Ficus benjamina tree and its soil," *PloS one*, vol. 3, no. 8, p. e2963, 2008.

[12] P.-S. Weng, H.-Y. Tang, P.-C. Ku, and L.-H. Lu, "50 mV-input battery-less boost converter for thermal energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 1031–1041, 2013.

[13] I. Sourikopoulos, S. Hedayat, C. Loyez, F. Danneville, V. Hoel, E. Mercier, and A. Cappy, "A 4-fJ/spike artificial neuron in 65 nm CMOS technology," *Frontiers in neuroscience*, vol. 11, p. 123, 2017.

[14] L. A. P. Melek, A. L. da Silva, M. C. Schneider, and C. Galup-Montoro, "Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 4, pp. 869–878, 2017.

[15] B. L. Dokić, "CMOS regenerative logic circuits," *Microelectronics Journal*, vol. 14, no. 5, pp. 21–30, 1983.

[16] Z. V. Bundalo and B. L. Dokić, "Non-inverting regenerative CMOS logic circuits," *Microelectronics Journal*, vol. 16, no. 5, pp. 5–17, 1985.

[17] M. Nakano, "Schmitt trigger circuit with stable operation," U.S. Patent 4,603,264, Jul. 29, 1986.

[18] D. L. Campbell, "Logic gate with controllable hysteresis and high frequency voltage controlled oscillator," U.S. Patent 5,594,361, Jan. 14, 1997.

[19] R. M. Lall, T. Whitten, and J. Jiang, "High speed Schmitt trigger with low supply voltage," U.S. Patent 6,433,602, Aug. 13, 2002.

[20] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, *Digital integrated circuits*, 2nd ed. Prentice hall Englewood Cliffs, 2002.

[21] E. A. Vittoz, "Weak inversion for ultra low-power and very low-voltage circuits," in *2009 IEEE Asian Solid-State Circuits Conference*. IEEE, 2009, pp. 129–132.

[22] J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 10, pp. 1515–1516, 2000.

[23] M. C. Schneider and C. Galup-Montoro, *CMOS analog design using all-region MOSFET modeling*. Cambridge University Press, 2010.