ISSN 1688-2784

Universidad de la República
Facultad de Ingeniería

On the design of ultra low voltage CMOS oscillators

Tesis presentada a la Facultad de Ingeniería de la Universidad de la República por

Mariana Siniscalchi

en cumplimiento parcial de los requerimientos para la obtención del título de Doctora en Ingeniería Eléctrica.

Directores de Tesis

Carlos Galup ..... Universidade Federal de Santa Catarina
Fernando Silveira ..... Universidad de la República

Tribunal

Andreas Andreou ..... Johns Hopkins University, Estados Unidos
Sylvain Bourdel ..... Université Grenoble Alpes, Francia
Conrado Rossi ..... Universidad de la República
Carlos Galup ..... Universidade Federal de Santa Catarina, Brasil
Fernando Silveira ..... Universidad de la República

Director Académico

Fernando Silveira ..... Universidad de la República

Montevideo
Monday 4th May, 2020

On the design of ultra low voltage CMOS oscillators, Mariana Siniscalchi.

ISSN 1688-2784

This thesis was prepared in LaTeX using the iietesis class (v1.1).
Total number of pages 115.
Compiled on Monday 4th May, 2020.
http://iie.fing.edu.uy/

Why repeat the old errors, if there are so many new errors to commit?

Bertrand Russell

This page is intentionally left blank.

Acknowledgment

First of all, I would like to thank my advisors Prof. Carlos Galup-Montoro and Prof. Fernando Silveira for their support, patience and knowledge.

I am thankful to the members of the committee, Prof. Andreas Andreou, Prof. Sylvain Bourdel and Prof. Conrado Rossi for their kind participation.

I would like to acknowledge the support from grant ANII POS_NAC_2015_1_109743, CAP and CSIC Universidad de la República, the project STIC AmSud O2ERF and the Brazilian research agency Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (CAPES), Finance Code 001, along with MOSIS for providing access to integration.

My sincere thanks also goes to my colleagues from the IIE of Universidad de la República who, in one way or another, are part of this process. Special thanks to Carolina Cabrera, Andrés Seré and Guillermo Antúnez, for their support and insightful suggestions.

Also, I am thankful to my colleagues from the LCI of Universidade Federal de Santa Catarina for making me feel welcome, specially to Daniel Novack for helping me out with some of the measurements and also to Andrés Hurtado, Márcio Schneider, Jefferson Ribeiro and Franciele Norenberg for many useful discussions and their valuable support.

I would also like to thank the people of the RFIC-Lab of Université Grenoble Alpes for receiving me during my stay to work on the project O2ERF.

I am grateful to the director of the Laboratory of UTE, Daniel Slomowitz, and members of his staff for making themselves and their equipment available for the high precision frequency measurements.

Last but not least, I would like to thank my friends and family for their continuous support. Without them, none of this would have been possible. My special thanks goes to Mariana del Castillo, Juliana Viera and Nicolás Gammarano. I am thankful to Nicolás, not only for supporting me through the ups and downs during my studies, but also for many useful discussions and his valuable work.

This page is intentionally left blank.

In memory of my father.

This page is intentionally left blank.

Resumen

Los nodos sensores inalámbricos tienen fuertes requerimientos de bajo consumo de manera de operar con baterías pequeñas o algún mecanismo de cosecha de energía, o ambos. En muchos casos, la cosecha de energía térmica o electroquímica provee tensiones muy bajas del orden de 100 mV o incluso menos. Los sistemas de internet de las cosas incluyen un módulo de reloj que debe estar siempre encendido a efectos de contar el tiempo. Los osciladores a cristal son probadamente útiles como relojes de bajo consumo, y en este contexto la reducción de la tensión es una estrategia conveniente. Por lo tanto, presentamos osciladores a cristal de 32 kHz operando con sólo 60 mV de tensión de alimentación. Dos implementaciones, basadas en el circuito Schmitt trigger para dos cristales diferentes, se diseñan y caracterizan experimentalmente.

Estos osciladores a cristal están basados en la aplicación del Schmitt trigger como amplificador. Se provee una guía para el diseño de este bloque para funcionar como el amplificador de un oscilador a cristal. Adicionalmente se propone un modelo dinámico del Schmitt trigger y los resultados del modelo son comparados con resultados de simulación. Los amplificadores son caracterizados experimentalmente, proveyendo una ganancia de 2.48 V/V con 60 mV de tensión de alimentación. Tal como se pretende en la etapa de diseño, para tensiones mayores a 100 mV aparece el fenómeno de histéresis y el Schmitt trigger comienza a operar como un comparador.

Los Schmitt trigger para operar como amplificadores de los osciladores a cristal son diseñados en un proceso CMOS de 130 nm y ocupan un área de 45 µm x 74 µm y 78 µm x 83 µm, respectivamente. El consumo de potencia de sendos osciladores es 2.26 nW y 15 nW y la estabilidad en temperatura obtenida es de 62 ppm (25-62°C) y 50 ppm (5-62°C), respectivamente. Se midieron la dependencia del consumo de corriente con respecto a la tensión de alimentación, la frequencia de oscilación, el tiempo de arranque y la amplitud de oscilación. La desviación de Allan es 30 ppb en ambos osciladores.

Por otra parte, un oscilador LC controlado por voltaje es diseñado en un proceso CMOS de silicio sobre aislante en deplexión total de 28 nm, para aplicaciones de radiofrecuencia. Se estudia la posibilidad de utilizar en este caso el mismo modelo utilizado para el diseño del Schmitt trigger. Dicho modelo es válido en todas las regiones de inversión y está desarrollado para transistores de tipo sustrato y de canal largo. La arquitectura de transistores nMOS entrelazados es la utilizada para este oscilador. Se estudia el límite teórico para la mínima tensión de alimentación. Los transistores son dimensionados de manera óptima para obtener

el mínimo consumo de potencia posible, utilizando un enfoque de baja tensión y el desempeño del oscilador se obtuvo mediante simulaciones.

Abstract

Wireless sensor nodes require very tight power budgets to operate from either a small battery, some energy harvesting mechanism or both. In many cases, thermal or electrochemical harvesting devices provide very low voltages of the order of 100 mV or even lower. Time-keeping functionality is required in IoT systems and the time-keeping module must be on at all times. Crystal oscillators have proven to be useful for low power time-keeping applications, and in this context supply voltage lowering is a convenient strategy. Therefore, 32 kHz crystal oscillators operating with only 60 mV supply are presented. Two implementations based on a Schmitt trigger circuit for two different crystals were designed and experimentally characterized.

These crystal oscillators are based on the application of a Schmitt trigger as an amplifier. Guidelines for designing this block to be the amplifier of a crystal oscillator are provided. Furthermore, a dynamic model of the Schmitt trigger is proposed and the model results are compared against simulations. The amplifiers were experimentally characterized, providing a gain of 2.48 V/V with a 60 mV power supply. As it was intended in the design stage, for voltages above 100 mV hysteresis appears and the Schmitt trigger starts operating as a comparator.

The Schmitt triggers to operate as amplifiers of the crystal oscillators are designed in a 130 nm CMOS process, requiring an area of 45 µm x 74 µm and 78 µm x 83 µm, respectively. The power consumptions of the crystal oscillators are 2.26 nW and 15 nW and the temperature stabilities attained are 62 ppm (25-62°C) and 50 ppm (5-62°C), respectively. The dependence on the supply voltage of the current consumption, fractional frequency, start-up time and oscillation amplitude were measured. The Allan deviation is 30 ppb for both oscillators.

On the other hand, an LC voltage controlled oscillator (VCO) is designed in 28 nm FD-SOI for RF applications. The possibility of modeling the transistors in the 28 nm FD-SOI technology by means of the all inversion region long channel bulk transistor model used for the Schmitt trigger circuits, is studied. A cross-coupled nMOS architecture is used to build the VCO. The theoretical limit for the minimum supply voltage that enables oscillation is studied. The transistors were optimally sized to aim the minimum power consumption through a low-voltage approach and the performance of the VCO was obtained through simulations.

This page is intentionally left blank.

List of Abbreviations

AC	alternate current
BLE	Bluetooth low-energy
CMOS	complementary metal oxide semiconductor
DC	direct current
FD-SOI	fully depleted silicon on insulator
IoT	internet of things
LC-VCO	LC-tank voltage controlled oscillator
LUT	look up table
MI	moderate inversion
MOSFET	metal oxide semiconductor field effect transistor
nMOS	n-type metal oxide semiconductor
PCB	printed circuit board
PLL	phase locked loop
pMOS	p-type metal oxide semiconductor
RF	radio frequency
SI	strong inversion
SoC	system on chip
UTBB	ultra thin body and buried oxide
WI	weak inversion
WSN	wireless sensor network

This page is intentionally left blank.

List of Symbols

A	voltage gain
A_{Sk}	drain or source diffusion area of transistor k
C'_J	junction capacitance per unit area
C_{Jk}	extrinsic capacitance of the drain or source to bulk junction
C_{jk}	capacitance between nodes j and k
C_m	motional capacitance of the crystal
C'_{ox}	oxide capacitance per unit area
$C_{pk\,ov}$	overlap capacitance at node p of transistor k
f_T	transition frequency
G_m	equivalent transconductance
g_{mb}	bulk transconductance
G_{mcrit}	critical value of the transconductance to enable oscillation
g_{md}	drain transconductance
g_{mg}	gate transconductance
G_{mopt}	transconductance value to achieve the maximum negative resistance
g_{ms}	source transconductance
G_o	equivalent output conductance
I_D	drain current
I_F	forward current
i_f	forward inversion level
I_N	current strength of an nMOS transistor
I_P	current strength of a pMOS transistor
I_k	current strength of transistor k
I_R	reverse current
i_r	reverse inversion level
I_S	specific current
L	transistor channel length
I_{SQ}	specific current of an equivalent square transistor
k	Boltzmann's constant ($= 1.38 \times 10^{-23}$ J/K)
LD	overlapping distance on the channel length direction between the source or drain and the gate

L_m	motional inductance of the crystal
μ	carrier mobility
n	slope factor
ϕ_t	thermal voltage ($= 4kT/q$)
q	electronic charge ($= 1.60 \times 10^{-19}$ C)
Q_B	total bulk charge
Q_D	total drain charge
Q_G	total gate charge
Q'_{ID}	inversion charge per unit area at drain
q'_{ID}	normalized inversion charge density at drain
Q'_{IS}	inversion charge per unit area at source
q'_{IS}	normalized inversion charge density at source
Q_S	total source charge
R_m	motional resistance of the crystal
R_O	output resistance
T	absolute temperature
τ	time constant
V_{BP}	back-plane voltage
V_D	drain-to-bulk voltage
V_{DD}	supply voltage
V_{DDH}	minimum supply voltage to obtain hysteresis
V_G	gate-to-bulk voltage
V_P	pinch-off voltage
V_S	source-to-bulk voltage
V_T	threshold voltage
V_{T0}	zero-bias threshold voltage
W	transistor channel width
Z_{Cr}	crystal impedance
Z_m	motional impedance of the crystal

Contents

Chapter 1

Introduction

Wireless sensor nodes, among other Internet of Things (IoT) elements, require a very tight power budget in order to be powered from either a small battery, some energy harvesting mechanism or both. Applications involving continuous monitoring or idle listening must spend the least energy possible. If so, the battery lifetime would be extended and operation with a harvester only may be possible. In fact, the limited power budget might be the most significant challenge [1].

Voltage scaling has proven effective for energy consumption reduction [2]. Sub-threshold design has been extensively used in power constrained applications, such as time-keeping wrist watches [3]. More recently, near threshold design techniques have been developed and supply voltage has been more aggressively lowered to further reduce power consumption [2]. All kinds of circuits are involved, from a Bluetooth Low-Energy (BLE) receiver front-end operating with 0.18 V [4] to a whole System on Chip (SoC) [5].

However, there are harvesters that provide smaller voltage levels. This is the case of thermoelectric generators [6], which provide a voltage supply in presence of a temperature difference as it is shown in the schematic drawing of Fig. 1.1a. In the IoT applications context, a small thermoelectric generator patch may be worn on the skin and 2 °C, found between the air and the skin, suffice to obtain 150 mV. However, the voltage obtained drops with the temperature difference, compromising the operation of the device powered from this harvester.

Photovoltaic cells arrangements used indoors also provide low voltage levels [7]. For an indoor well illuminated environment, say 200 lux, 0.88 V and 132 µW are extracted. However, if light diminishes to 50 lux, power would drop to less than 50 µW and voltage to 0.3 V. Moreover, each one of these photovoltaic cells spends much more area (19.6 mm × 50 mm) than the aforementioned thermoelectric generator in Fig. 1.1a.

In many cases, thermal or electrochemical harvesting devices provide very low voltages of the order of 100 mV or even lower [8–10]. A startup boost converter is presented in [9] using a thermoelectric generator that provides 50 mV. In [10], energy is harvested from the endocochlear potential, as shown in Fig. 1.1b. This is a 70 to 100 mV electrochemical bio-potential inside the mammalian ear, that provides power within the range from 1.1 to 6.25 nW. In [8], less than 100 mV are

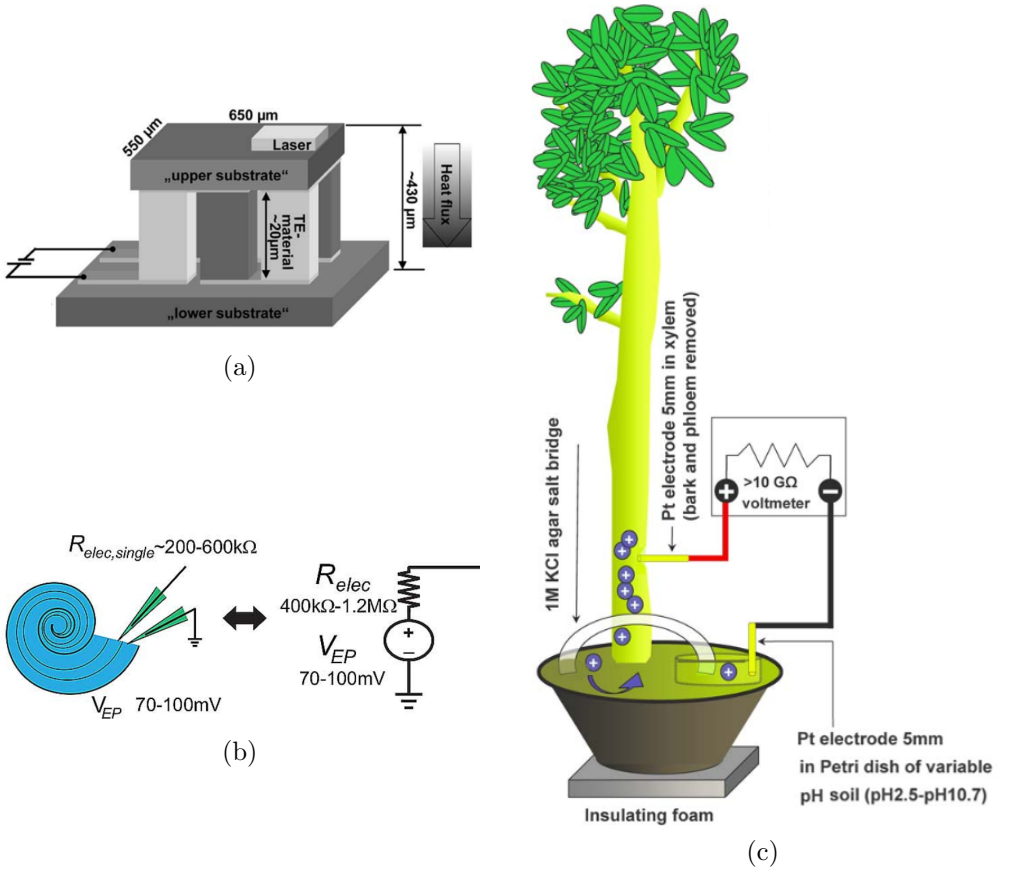


Figure 1.1: (a) Schematic drawing of an application of the Micro-Peltier coolers, taken from [6]. Electrochemical bio-potential examples: schematic drawing of (b) the endocochlear potential as an energy harvesting source, extracted from [10], and (c) the bio-potential between a tree and its soil, taken from [8].

obtained as a result of the pH difference between a tree and its soil. Figure 1.1c shows a schematic diagram on how this voltage difference appears.

Complementary Metal Oxide Semiconductor (CMOS) electronics is possible at such low supply voltages [11, 12], which are well below the supply that minimizes the energy per operation, typically in the range of 200 to 350 mV. The minimum energy per operation point may be the ideal condition for the active operation of a circuit [2], but this is not the case for circuits with long standby times. In effect for such circuits the power spent can be minimized by setting the supply voltage to its lowest possible value in the standby mode [12].

Supply voltage constrained applications are those powered from the aforementioned very low voltage harvesters, given that no higher voltage sources are available. Then, supply voltage reduction techniques should be developed to provide functional circuits within those levels. In particular, for digital circuits, supply voltage reduction beyond the minimum energy per operation point are advantageous and can help to considerably reduce standby power consumption [12]. This is

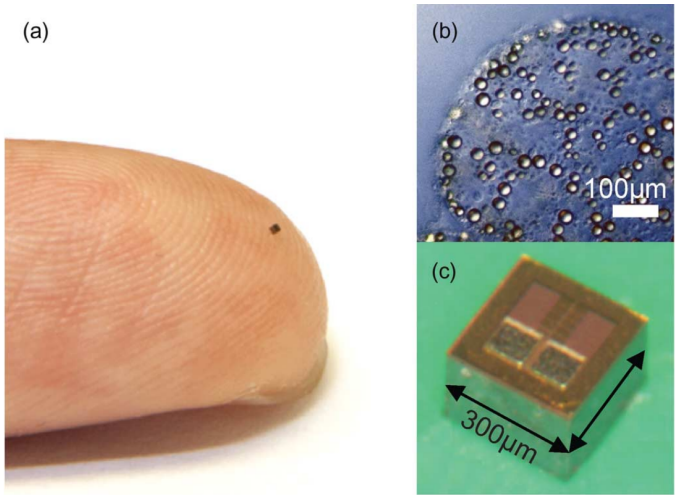


Figure 1.2: (a) Transmitter on fingertip and (b) *Thiomargarita namibiensis*, at the same scale with (c) die photo. Figure taken from [13].

so, even though most efforts are made towards the minimum energy per operation point and near threshold design [2]. In [12], Schmitt trigger gates were proven to be more efficient than CMOS gates for 75 mV supply, with respect to power/delay.

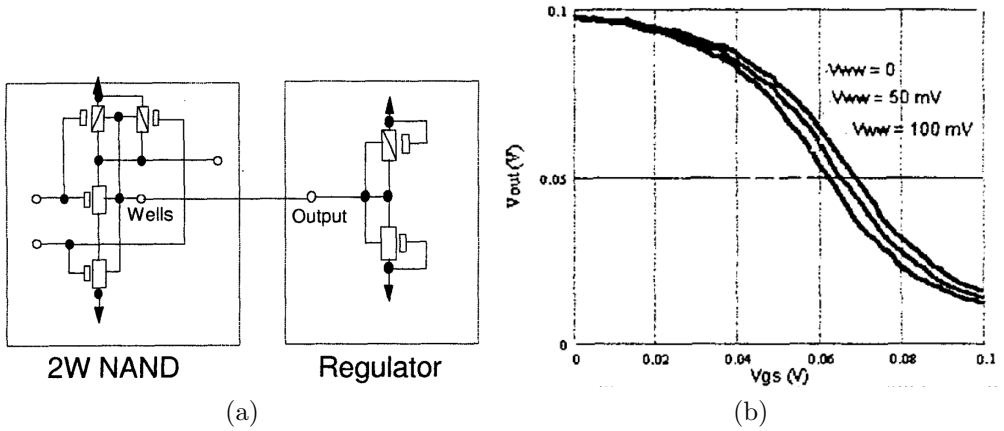
Due to the positive feedback, the Schmitt trigger provides a significant gain for voltages below $4kT/q$, approximately 100 mV at room temperature. This feature could enable CMOS electronics operating from such voltage levels. Practical ultra low voltage levels would be $5kT/q$ for analog RF circuits [13] and $4kT/q$ for digital circuits [14]. In [13], the miniaturization of an RF transmitter compatible with bio-potential energy harvesting sources around $5kT/q$ is addressed. Figure 1.2 shows the SoC on a finger tip, together with a photo of the die and some vacuoles (*Thiomargarita namibiensis*) as a possible source of energy.

To obtain functional digital circuits at ultra low voltage levels, the threshold voltage of nMOS and pMOS devices may be matched by means of a simple regulator circuit [14]. Figure 1.3a shows a NAND gate connected to the regulator circuit. The voltage transfer characteristic of the NAND gate can be modified by adjusting the well bias, as shown in Fig. 1.3b. Additionally, for circuits powered from low voltage energy harvesters, reducing the minimum supply voltage required by the electronics simplifies the design of the voltage step-up converters.

Besides the digital circuits, all kinds of building blocks able to work with such voltage levels are required. Examples of circuits developed to this aim are a 75 mV 71 nW fully-integrated temperature sensor [15] and a 0.18 V 382 µW BLE receiver front-end with 1.33 nW sleep power [4].

Time-keeping functionality is required in IoT systems. Synchronization between nodes in a wireless sensors network (WSN) is vital in order to keep the exchange of coordination messages to the minimum [1]. In addition, the time-keeping module is likely to be always on.

When it comes to ultra low voltage oscillators capable of operating at tens of mV, inductively loaded ring oscillators and Colpitts oscillators may be suita-



(a) (b)

Figure 1.3: Well biasing technique to enable digital circuits at $4kT/q$ supply voltage: (a) circuit schematic showing a NAND and the regulator circuit to bias the wells, and (b) voltage transfer characteristic of circuit in (a). Figures taken from [14].

ble choices for the 100 MHz range [16]. To fulfill the low voltage budget, these oscillators are implemented with zero-VT transistors and high quality factor inductors. The latter might be either external inductors or on chip, area demanding, inductors. Without these, not only the voltage supply and current consumption would have to be increased to enable starting up, but also the performance of the oscillator would worsen.

A relaxation oscillator for time-keeping operating in the Hz-range from 0.3 V to 1.8 V with 3.32 pW has been reported in [17]. Maybe due to the very low power consumption achieved, it exhibits a high frequency spread (8.9 %) and a poor long term stability (<1 000 ppm). In the kHz-range, another relaxation oscillator [18] operates with 0.4 V and 1.14 nW and has 60 Hz variation over the range from 0.4 V to 0.65 V. It accomplishes a frequency stability of 94 ppm/^{o}C and an Allan deviation floor of 58 ppm, which are remarkable considering it being the relaxation type. Nevertheless, RF communications synchronization applications demand better frequency stability and accuracy [1]. A cross-coupled LC-tank Voltage Controlled Oscillator (LC-VCO) with very low phase noise and frequency stability features was presented in [19]. This LC-VCO operates with 0.3 V at 3 579 MHz, but consumes 0.225 mW owing to the high frequency, making it unsuitable for the aforementioned applications.

Crystal oscillators have proven to be useful for low power time-keeping applications, and supply voltage lowering a convenient strategy [3, 20, 21]. Crystal oscillators operating in the range of tens of MHz shall attain µW-power consumption by means of a low supply voltage of 0.7 V in [22] and between 0.3 and 0.5 V in [23, 24].

In [25], a 0.15 V 32 kHz crystal oscillator is presented. A very low power consumption of 1.89 nW and a fine frequency stability performance are accomplished using a self-charging scheme. However, the output waveform is deformed possibly jeopardizing the frequency spectrum of the oscillator. A one-pin oscillator (instead

of two pins) based on the same scheme, but with 0.25 V and 2.89 nW, was reported in [26].

A 32 kHz phase locked loop (PLL) assisted crystal oscillator working within hundreds of mV supply and a remarkable performance is reported in [27], involving additional complex circuits and consequently a large amount of silicon area. Moreover, two different supply sources are required.

Regarding ultra low voltage 32 kHz crystal oscillators, the lowest power consumption is that reported in [28], attaining 0.55 nW by means of downconverting the signal to DC, amplifying in DC and then upconverting the signal to the frequency of the crystal. An excellent phase synchronization is achieved providing excellent frequency stability over temperature and over time. The output waveform is the result of switching DC levels to obtain a four level switched signal, which will have important harmonic content. The output harmonic content would be filtered by the high quality factor of the crystal. Nevertheless, this might be an issue if spectral purity is needed. Other examples in the single digit nW range are those reported in [29], [30] and [31].

This thesis is organized as follows. The Schmitt trigger circuit topology, which is extensively referred to in this thesis, will be presented in Chapter 2. In the first place, the long-channel MOS transistor model used herein and the procedure for the extraction of the parameters of the transistor, are revisited. Then, the small-signal low-frequency model of the Schmitt trigger and its operation as an amplifier for ultra low voltage are also revisited. Finally, a brief comparison between the Schmitt trigger and a CMOS inverter is presented. Chapter 3 is dedicated to the dynamic model of the Schmitt trigger, including the capacitive coefficients due to intrinsic and extrinsic capacitances, the intrinsic transition frequency and the main parameters to describe its operation in the region with hysteresis. The dynamic model is verified through simulations. In Chapter 4, the design of two crystal oscillators is assessed. Firstly, the operation of the Pierce oscillator is revisited. Secondly, the particulars of the design of a Pierce oscillator based on a Schmitt trigger as an amplifier are presented. In Chapter 5, the design and performance of the oscillator are verified through simulations and measurements. Finally, Chapter 6 deals with an LC-VCO for RF applications in a 28 nm Fully Depleted Silicon on Insulator (FD-SOI) technology. First, the model and parameter extraction procedure explained in Chapter 2 are translated to the present circuit and FD-SOI technology. Then, a non-tuneable version of the LC oscillator that operates at the minimum possible supply voltage is studied. The performance of the LC oscillator under this condition is obtained through simulations. Finally, an LC-VCO is optimally designed for the frequency band from 2.4 GHz to 2.5 GHz to minimize the power consumption by means of a low-voltage strategy. The performance of the LC-VCO is obtained through simulations. Finally in Chapter 7 the conclusions of this thesis are drawn.

This page is intentionally left blank.

Chapter 2

Schmitt trigger as an amplifier for ultra low voltage

To design a Schmitt trigger circuit to operate as an amplifier, a small-signal model is used and presented in this chapter. First, a basic all-region MOSFET model is revisited in Section 2.1. Then, expressions for the small-signal transconductances and the capacitive coefficients are provided in Sections 2.2 and 2.3. The equations within the model require the parameters of the technology of use. Thus, a parameter extraction procedure is followed as presented in Section 2.4. The DC transfer characteristic of the Schmitt trigger is subject of Section 2.5, where analytic expressions for obtaining the characteristic are provided. The low-frequency small-signal equivalent model of the Schmitt trigger is derived in Section 2.6 using the MOSFET model aided by the extracted parameters. Finally, the Schmitt trigger is compared to a CMOS inverter to see the benefits of using a Schmitt trigger circuit in ultra low voltage applications through numerical examples.

2.1 Basic all-region MOSFET model

In this section an all-region MOSFET model [32] is briefly reviewed.

The drain current of a long-channel transistor is expressed as the difference between two currents, namely, the forward and reverse currents, I_F and I_R, respectively, as follows

$$I_D = I_F - I_R = I_S(i_f - i_r), \tag{2.1}$$

where I_S (called specific current) is given by

$$I_S = \mu\, n\, C'_{ox}\, \frac{\phi_t^2}{2}\, \frac{W}{L} \tag{2.2}$$

and i_f and i_r are the forward and reverse inversion coefficients, respectively.

In (2.2), μ is the mobility, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, ϕ_t is the thermal voltage and W/L is the aspect ratio.

The specific current is normalized to the aspect ratio, leading to the specific current of an equivalent square transistor I_{SQ}, with $W = L$, giving

$$I_{SQ} = \frac{I_S}{W/L}. \tag{2.3}$$

The forward and reverse currents in (2.1) relate to the normalized inversion charge density at source and drain, q'_{IS} and q'_{ID}, respectively, as follows

$$I_{F(R)} = I_S\,[q'^2_{IS(D)} + 2q'_{IS(D)}], \tag{2.4}$$

where q'_{IS} and q'_{ID} are defined in terms of the inversion charge per unit area Q'_{IS} and Q'_{ID}, such that

$$q'_{IS(D)} = -\frac{Q'_{IS(D)}}{nC'_{ox}\phi_t}. \tag{2.5}$$

The relationship between the terminal voltages V_G, V_S, V_D (all referred to the bulk) and the charge densities is

$$\frac{V_P - V_{S(D)}}{\phi_t} = q'_{IS(D)} - 1 + \ln\left(q'_{IS(D)}\right), \tag{2.6}$$

where the pinch-off voltage V_P can be approximated by

$$V_P \cong \frac{V_G - V_{T0}}{n}, \tag{2.7}$$

being V_{T0} the threshold voltage at $V_S = 0$.

Expressing the inversion coefficients in terms of the normalized inversion charge, results in

$$i_{f(r)} = [q'_{IS(D)} + 1]^2 - 1. \tag{2.8}$$

Note that i_f does not depend on q'_{ID} and i_r does not depend on q'_{IS}.

Thus, (2.6) can be rewritten in terms of the inversion coefficients in (2.8) as follows

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right). \tag{2.9}$$

2.1.1 Weak inversion model of the MOSFET

Deep in weak inversion (WI), $i_{f(r)} \to 0$. In this condition, the square root term in $i_{f(r)}$ becomes negligible and we can approximate the logarithmic term using that $\sqrt{1+x} \approx 1 + \frac{x}{2}$ in (2.9), resulting in

$$\frac{V_P - V_{S(D)}}{\phi_t} = -1 + \ln\left(\frac{i_{f(r)}}{2}\right). \tag{2.10}$$

Substituting (2.10) into (2.1) and using the pinch-off voltage approximation in (2.7), it follows the expression of the drain current I_D for the nMOS transistor operating in WI

$$I_{D\,N} = I_N\, e^{\frac{V_{GB}}{n_N \phi_t}}\left(e^{-\frac{V_{SB}}{\phi_t}} - e^{-\frac{V_{DB}}{\phi_t}}\right), \tag{2.11}$$

where the current scaling factor I_N, which represents the transistor current strength, is given by

$$I_N = 2\, I_{S\,N}\, e^{1-\frac{V_{T0\,N}}{n_N \phi_t}}. \tag{2.12}$$

The expression for the pMOS current is obtained from (2.11) changing V_{SB} by V_{BS}, V_{DB} by V_{BD} and V_{GB} by V_{BG}. The expression for the current strength of the pMOS transistor, I_P, is the same as (2.12), using the pMOS parameters.

2.2 Small-signal transconductances

Provided that the MOSFET is a four terminal device, an increase in the voltage of these terminals translates to an increase in the drain current. Thus,

$$\Delta I_D = g_{mg}\Delta V_G - g_{ms}\Delta V_S + g_{md}\Delta V_D + g_{mb}\Delta V_B \tag{2.13}$$

where

$$g_{mg} = \frac{\partial I_D}{\partial V_G},\ g_{ms} = -\frac{\partial I_D}{\partial V_S},\ g_{md} = \frac{\partial I_D}{\partial V_D},\ g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{2.14}$$

are the gate, source, drain and bulk transconductances, respectively. Figure 2.1 depicts the circuit schematic of this low-frequency small-signal model.

An expression for g_{ms} and g_{md} can be deduced from their definition in (2.14) and from the definition of the drain current in (2.1), giving

$$g_{ms(d)} = -(+)I_S \frac{\partial(i_f - i_r)}{\partial V_{S(D)}} = -I_S \frac{\partial i_{f(r)}}{\partial V_{S(D)}}. \tag{2.15}$$

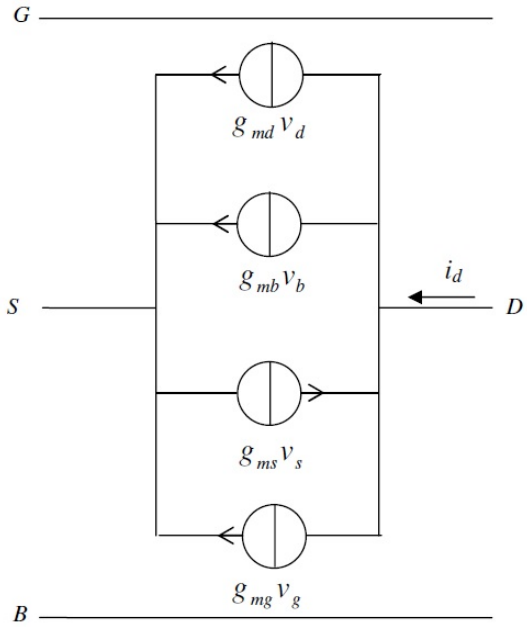


Figure 2.1: Low-frequency small-signal model of the MOSFET. Figure taken from [32].

From (2.9) it can be obtained an expression for the derivative $(\partial i_{f(r)}/\partial V_{S(D)})$. Thus, (2.15) becomes

$$g_{ms(d)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right). \tag{2.16}$$

The expression for g_{mg} can be deduced from its definition in (2.14) and from (2.1), giving

$$g_{mg} = I_S\frac{\partial(i_f - i_r)}{\partial V_G}. \tag{2.17}$$

Noting from (2.9) that

$$\frac{\partial i_{f(r)}}{\partial V_P} = -\frac{\partial i_{f(r)}}{\partial V_{S(D)}}, \tag{2.18}$$

equation (2.17) can be rewritten as

$$g_{mg} = I_S\,\frac{\partial V_P}{\partial V_G}\left(-\frac{\partial i_f}{\partial V_S}+\frac{\partial i_r}{\partial V_D}\right). \tag{2.19}$$

Using the expression for g_{ms} and g_{md} in (2.16), and the definition of V_P in (2.7), g_{mg} reduces to

$$g_{mg} = \frac{g_{ms}-g_{md}}{n}. \tag{2.20}$$

The bulk transconductance g_{mb} can be derived from (2.13) by noting that, if the four terminals of the MOSFET increase the voltage by the same amount, $\Delta I_D = 0$, thus

$$g_{mg} - g_{ms} + g_{md} + g_{mb} = 0. \tag{2.21}$$

From (2.20) and (2.21), g_{mb} reduces to

$$g_{mb} = (n-1)g_{mg}. \tag{2.22}$$

2.3 Capacitive coefficients

All charges Q_j ($j = G$, S, D, B) can be expressed in terms of the instantaneous values of the terminal voltages, by applying the chain rule of differentiation, obtaining an expression for the charging currents as

$$\frac{\partial Q_j}{\partial t} = \frac{\partial Q_j}{\partial V_G}\frac{\partial V_G}{\partial t} + \frac{\partial Q_j}{\partial V_S}\frac{\partial V_S}{\partial t} + \frac{\partial Q_j}{\partial V_D}\frac{\partial V_D}{\partial t} + \frac{\partial Q_j}{\partial V_B}\frac{\partial V_B}{\partial t}. \tag{2.23}$$

The four-by-four matrix of the MOSFET intrinsic capacitances for quasi-static operation is defined by [33]

$$C_{jk} = -\left.\frac{\partial Q_j}{\partial V_k}\right|_0, \quad j \neq k, \tag{2.24}$$

$$C_{jj} = \left.\frac{\partial Q_j}{\partial V_j}\right|_0, \tag{2.25}$$

where Q_j can be any one of the charges Q_S, Q_D, Q_B or Q_G, and V_j and V_k can be any of the voltages V_S, V_D, V_B, and V_G. The notation "0" indicates that the derivatives are calculated at the bias point. C_{jk} determines the current transferred out of node j because of a voltage change on node k, all the other node voltages remaining constant.

Because the MOSFET is an active device, the capacitances C_{jk} are non-reciprocal, that is, in general, $C_{jk} \neq C_{kj}$ for $j \neq k$. Only 9 of the 16 capacitive coefficients are linearly independent, due to charge conservation and the fact that only three voltage differences from four terminal voltages can be chosen independently.

From the expressions for the MOSFET charges, explicit formulas for the capacitive coefficients can be derived from (2.23) and (2.24). Thus,

$$C_{gs} = \frac{2}{3} C_{ox} \frac{1+2\alpha}{(1+\alpha)^2} \frac{q'_{IS}}{1+q'_{IS}}, \tag{2.26a}$$

$$C_{gd} = \frac{2}{3} C_{ox} \frac{\alpha^2+2\alpha}{(1+\alpha)^2} \frac{q'_{ID}}{1+q'_{ID}}, \tag{2.26b}$$

$$C_{bs(d)} = (n-1)\, C_{gs(d)}, \tag{2.26c}$$

$$C_{gb} = C_{bg} = \frac{(n-1)}{n}(C_{ox} - C_{gs} - C_{gd}), \tag{2.26d}$$

$$C_{sd} = -\frac{4}{15} n C_{ox} \frac{\alpha + 3\alpha^2 + \alpha^3}{(1+\alpha)^3} \frac{q'_{ID}}{1+q'_{ID}}, \tag{2.26e}$$

$$C_{ds} = -\frac{4}{15} n C_{ox} \frac{1 + 3\alpha + \alpha^2}{(1+\alpha)^2} \frac{q'_{IS}}{1+q'_{IS}}, \tag{2.26f}$$

$$C_{dg} - C_{gd} = C_m = \frac{C_{sd} - C_{ds}}{n}, \tag{2.26g}$$

where

$$C_{ox} = WLC'_{ox}, \tag{2.27}$$

and

$$\alpha = \frac{q'_{ID} + 1}{q'_{IS} + 1}. \tag{2.28}$$

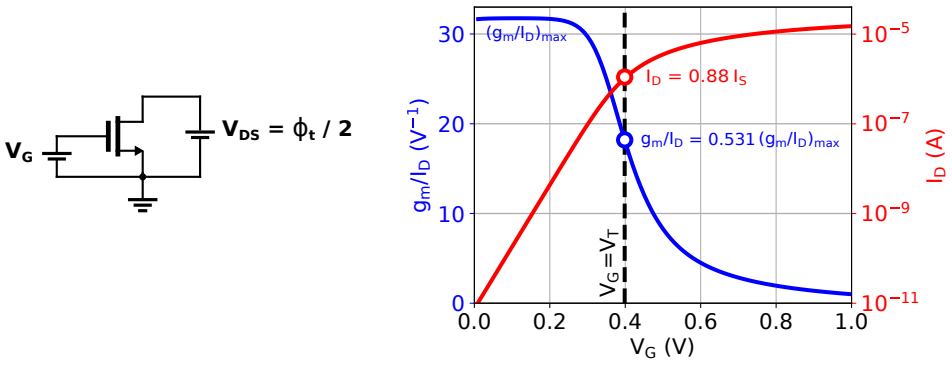
2.4 Parameter extraction

The all-region model in 2.1 is the basic long channel compact model applied to extract the parameters of the transistors.

For parameter extraction, the g_m/I_D based procedure described in [34] is followed, where the authors propose to extract the parameters n, V_{T0} and I_S using $V_S = 0$, $V_D = \phi_t/2$, sweeping V_G (as shown in Fig. 2.2a) and plotting I_D and g_m/I_D with respect to V_G (as shown in Fig. 2.2b).

From (2.20), the g_m/I_D ratio can be expressed as

$$\frac{g_m}{I_D} = \frac{1}{I_D} \frac{\partial I_D}{\partial V_G} = \frac{g_{ms} - g_{md}}{nI_D}. \tag{2.29}$$



(a) (b)

Figure 2.2: (a) Circuit schematic and (b) graphical representation of the g_m/I_D procedure for the extraction of V_T.

Using the expressions for g_{ms} and g_{md} in (2.16), g_m/I_D in (2.29) simplifies to

$$\frac{g_m}{I_D} = \frac{2}{n\phi_t\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)}. \tag{2.30}$$

The extraction of the parameters is then based on the following relationships. The maximum value of g_m/I_D (for $i_f = i_r = 0$) is $1/(n\phi_t)$.

For $V_S = 0$ and $V_G = V_T$ (which implies $V_P = 0$), we obtain $i_f = 3$ from (2.9). For $V_{DS} = \phi_t/2$, $V_S = 0$ and $V_G = V_T$ we obtain $i_r = 2.12$ from (2.9). For these values of i_f and i_r, we have $g_m/I_D = 0.531/(n\phi_t)$ from (2.30) and $I_D = 0.88I_S$ from (2.1).

So the parameters are extracted as follows. First, $n = 1/\left(\phi_t\left(g_m/I_D\right)_{max}\right)$, then V_T such that $g_m/I_D\left(V_G = V_T\right) = 0.531/(n\phi_t)$ is determined and, finally, $I_S = I_D\left(V_G = V_T\right)/0.88$.

Even though an nMOS transistor is used to exemplify the extraction procedure, the parameters of a pMOS transistor are extracted in the same way but with $V_{SD} = \phi_t/2$. Once the extraction is completed, the designer can choose the dimensions of a transistor to match certain parameters. Moreover, by using series and parallel arrangements of unit transistors, one can have an equivalent transistor, build of many transistors in series or in parallel, with the exact same parameters as each of the unit transistors [35].

2.5 DC transfer characteristic of the Schmitt trigger

The Schmitt trigger topology is shown in Fig. 2.3. The bulk of the nMOS and pMOS transistors are connected to ground and V_{DD}, respectively.

In ultra low voltage operation, both nMOS and pMOS are in the WI region. The MOS transistor drain current in WI is given by (2.11) and rewritten here for

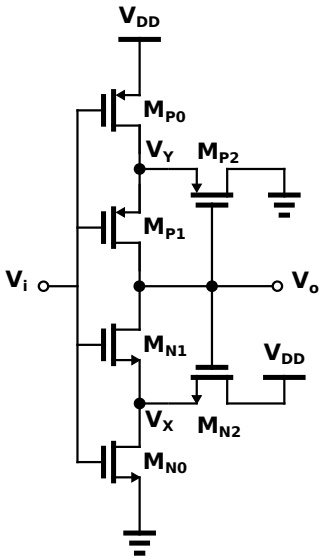


Figure 2.3: Six transistor Schmitt trigger circuit schematic.

convenience. Thus,

$$I_{D\,N} = I_N\, e^{\frac{V_{GB}}{n_N \phi_t}} \left(e^{-\frac{V_{SB}}{\phi_t}} - e^{-\frac{V_{DB}}{\phi_t}} \right), \tag{2.31}$$

where I_N, represents the transistor current strength, and is given in (2.12).

The expression for the pMOS current is obtained from (2.31) changing V_{SB} by V_{BS}, V_{DB} by V_{BD} and V_{GB} by V_{BG}. The expression for the current strength of the pMOS transistor is the same as (2.12), using the pMOS parameters.

In order to design a Schmitt trigger, first the parameters of the transistor are extracted as explained in Section 2.4. The extracted parameters are then replaced in (2.31) to evaluate the drain current of each of the transistors. As a result, the remaining variables are exclusively currents and voltages. Moreover, the transistors may be sized to match certain parameters. The sizing of the transistors is discussed in Section 4.4 applied to the case of a Pierce oscillator using a Schmitt trigger as the inverting amplifier.

All transistors of the Schmitt trigger are composed of parallel arrangements of either nMOS or pMOS unit transistors. Thus, all of the parallel arrangements have the same V_T, I_{SQ} and n as the unit transistor of choice [35]. This strategy significantly simplifies the calculations in circuits with many transistors.

The number of transistors in parallel must be such that every pMOS has the same current strength as its symmetric nMOS, that is, $I_{N0} = I_{P0} = I_0$, $I_{N1} = I_{P1} = I_1$, $I_{N2} = I_{P2} = I_2$ and $n_N = n_P = n$.

Calculating the drain currents of the six transistors in Fig. 2.3 from (2.31), the DC equations for nodes V_X and V_Y are [36]

$$e^{\frac{V_X}{\phi_t}} = \frac{I_0 + I_1 + I_2 e^{\frac{V_O - V_I}{\phi_t}}}{I_0 + I_1 e^{-\frac{V_0}{\phi_t}} + I_2 e^{\frac{V_O - V_I}{\phi_t}} e^{-\frac{V_{DD}}{\phi_t}}}, \tag{2.32}$$

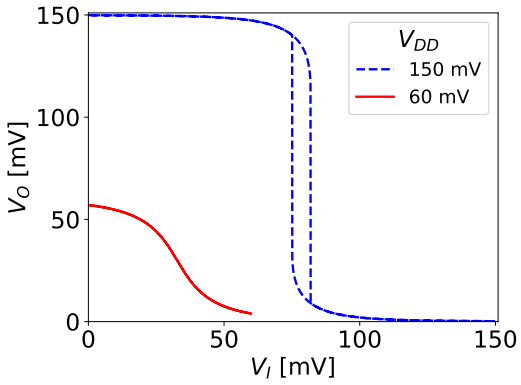


Figure 2.4: Output voltage V_O of the Schmitt trigger obtained from analytical expressions (2.32), (2.33) and (2.34), with $I_1/I_0 = 0.25$ and $I_2/I_0 = 0.5$.

and

$$e^{\frac{V_Y}{\phi_t}} = \frac{I_0\, e^{\frac{V_{DD}}{\phi_t}} + I_1\, e^{\frac{V_O}{\phi_t}} + I_2\, e^{\frac{V_I - V_O}{\phi_t}}}{I_0 + I_1 + I_2\, e^{\frac{V_I - V_O}{\phi_t}}}, \tag{2.33}$$

where $n_N = n_P = 1$ for simplicity. The DC equation for node V_O is given by

$$e^{\frac{V_I - V_X}{\phi_t}} - e^{\frac{V_I - V_O}{\phi_t}} = e^{\frac{V_Y - V_I}{\phi_t}} - e^{\frac{V_O - V_I}{\phi_t}}. \tag{2.34}$$

Figure 2.4 shows the voltage transfer characteristic of the Schmitt trigger, calculated from (2.32), (2.33) and (2.34). For $V_{DD} = 150$ mV the voltage transfer characteristic presents hysteresis, but for $V_{DD} = 60$ mV it does not.

2.6 Low-frequency small signal equivalent model of the Schmitt trigger

The equivalent small-signal model of the Schmitt trigger is depicted in Fig. 2.5. The transconductances present in Fig. 2.5 follow the definition in (2.14) and are evaluated around the operating point $V_I = V_O = V_{DD}/2$, giving

$$g_{mk} = \left.\frac{\partial I_{D\,N}}{\partial V_{GB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{2.35a}$$

$$g_{mdk} = \left.\frac{\partial I_{D\,N}}{\partial V_{DB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{2.35b}$$

$$g_{msk} = -\left.\frac{\partial I_{D\,N}}{\partial V_{SB}}\right|_{V_I = V_O = V_{DD}/2}, \tag{2.35c}$$

where g_{mk}, g_{mdk} and g_{msk}, are the gate, drain and source transconductances of transistor k, respectively. The values of the transconductances, according to (2.35), are given in Table 2.1.

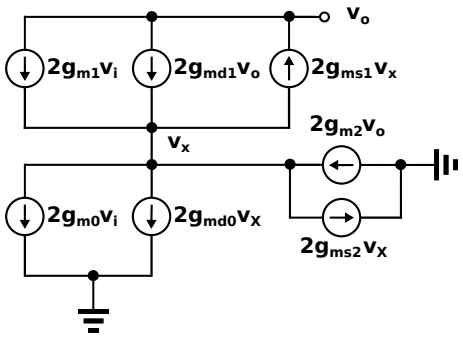


Figure 2.5: Six transistor Schmitt trigger circuit low-frequency small-signal equivalent model for $V_I = V_O = V_{DD}/2$.

Table 2.1: Transconductances of the Schmitt trigger

	g_m	g_{ms}	g_{md}
M_{N0}, M_{P0}	$\frac{I_0}{n\phi_t}\left[\frac{1-e^{-\frac{V_{X0}}{\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$		$\frac{I_0}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$
M_{N1}, M_{P1}	$\frac{I_1}{n\phi_t}\left[\frac{e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{2\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$	$\frac{I_1}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$	$\frac{I_1}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{DD}}{2\phi_t}}}\right]$
M_{N2}, M_{P2}	$\frac{I_2}{n\phi_t}\left[\frac{e^{-\frac{V_{X0}}{\phi_t}}-e^{-\frac{V_{DD}}{\phi_t}}}{e^{-\frac{V_{DD}}{2n\phi_t}}}\right]$	$\frac{I_2}{\phi_t}\left[\frac{e^{\frac{V_{DD}}{2n\phi_t}}}{e^{\frac{V_{X0}}{\phi_t}}}\right]$	

The equivalent small-signal model of the Schmitt trigger in Fig. 2.5, looks like the nMOS network small-signal model, but all transconductance values are doubled.

The Schmitt trigger can be represented by an equivalent transconductance G_m and an equivalent output conductance G_o [37]

$$G_m = \left.\frac{i_o}{v_i}\right|_{V_I=V_O=V_{DD}/2} = -2 \times \frac{g_{m1}(g_{ms2}+g_{md0})+g_{ms1}g_{m0}}{g_{ms1}+g_{ms2}+g_{md0}}, \tag{2.36}$$

and

$$G_o = \left.\frac{i_o}{v_o}\right|_{V_I=V_O=V_{DD}/2} = -2 \times \frac{g_{md1}(g_{ms2}+g_{md0})-g_{ms1}g_{m2}}{g_{ms1}+g_{ms2}+g_{md0}}. \tag{2.37}$$

The equivalent transconductance G_m can be rewritten in terms of the supply

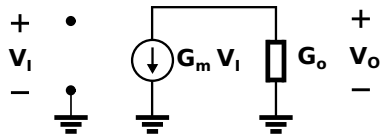


Figure 2.6: Circuit schematic of the small-signal equivalent model of a Schmitt trigger as an amplifier.

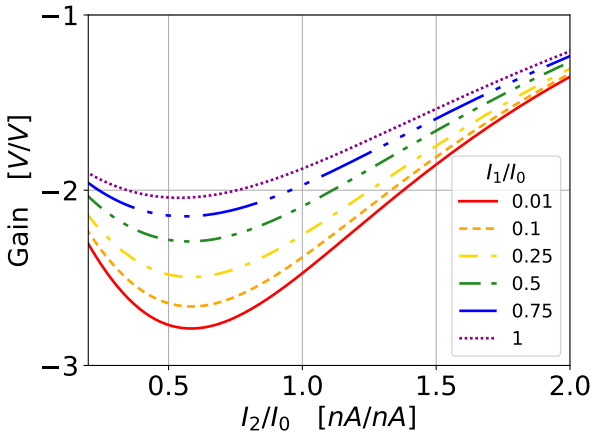


Figure 2.7: Voltage gain as a function of I_1/I_0 and I_2/I_0 given by (2.40), with $n = 1.3$ and $V_{DD} = 60\,mV$, based on [37].

voltage, V_{DD}, and the current strengths, I_0, I_1 and I_2, as follows

$$G_m = \frac{2\,I_1/n}{e^{-V_{DD}/2n\phi_t}}\left[\frac{(I_0+I_2)e^{-V_{DD}/2\phi_t} - I_2 e^{-V_{X0}/\phi_t}}{I_0\,e^{(V_{X0}-V_{DD})/\phi_t} + I_1 + I_2}\right], \tag{2.38}$$

where V_{X0}, the value of V_X at $V_I = V_O = V_{DD}/2$, is such that

$$e^{-V_{X0}/\phi_t} = \frac{I_0 + I_1 e^{-V_{DD}/2\phi_t} + I_2 e^{-V_{DD}/\phi_t}}{I_0 + I_1 + I_2}. \tag{2.39}$$

Figure 2.6 depicts the schematic of the small-signal equivalent model of the Schmitt trigger as an amplifier, with G_m and G_o the equivalent transconductance and output conductance in (2.36) and (2.37), respectively.

Lastly, the Schmitt trigger voltage gain is expressed as

$$A = \frac{v_o}{v_i}\bigg|_{V_I=V_O=V_{DD}/2} = -\frac{G_m}{G_o}. \tag{2.40}$$

The voltage gain A is a function of the supply voltage V_{DD}, the ratios I_1/I_0 and I_2/I_0, and the slope factor of nMOS and pMOS devices n_N and n_P (considered equal for the sake of simplicity, without loss of generality, thus: $n = n_N = n_P$).

Figure 2.7 shows the dependence of the voltage gain on I_2/I_0, for constant values of I_1/I_0 and supply voltage $V_{DD} = 60$ mV. We have chosen this ultra low

voltage to explore the frontier of the design space. A practical ultra low voltage complex circuit should operate with a minimum supply of 100 mV as explained in the introduction. For values of I_2/I_0 close to 0.5, independently of the ratio I_1/I_0, the maximum absolute gain is reached. Therefore, $I_2/I_0 = 0.5$ is chosen. On the other hand, the lower the ratio I_1/I_0, the larger the magnitude of the voltage gain. $I_1/I_0 = 0.25$ is chosen for the sake of layout simplicity. In this case, the voltage gain is $A = -2.48$ V/V.

As a consequence, after V_{DD}, I_1/I_0 and I_2/I_0 have been selected and n is given by the process chosen, G_m and G_o can be expressed only in terms of the current strength I_0.

2.7 Comparison between Schmitt trigger and CMOS inverter

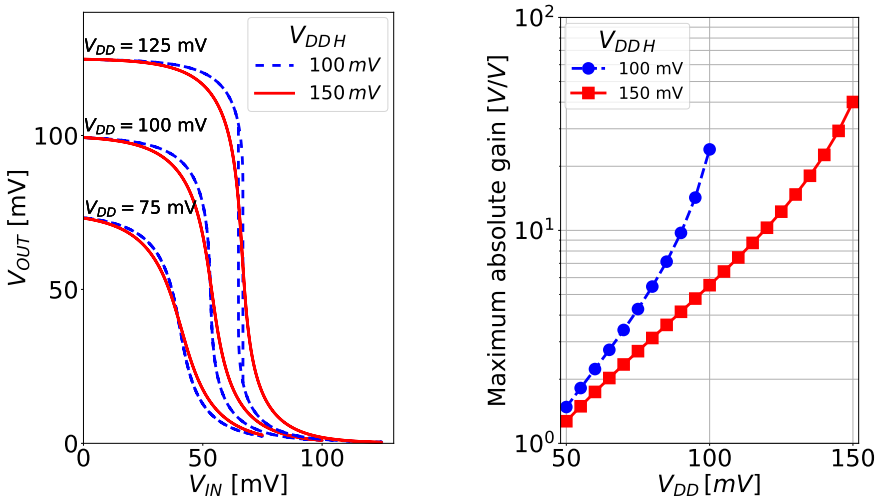
Hysteresis is the most distinguishing characteristic of a Schmitt trigger circuit, when comparing it to a CMOS inverter. As shown in [36], the minimum supply voltage to obtain hysteresis in a Schmitt trigger with balanced pMOS and nMOS subcircuits is given by

$$V_{DDH} \approx 2\phi_t \, ln \left[n \left(1 + \frac{I_0}{I_2} \right) \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0} \right) - \frac{I_1}{I_0} \right]. \tag{2.41}$$

Figures 2.8a and 2.8b show the voltage transfer characteristic and the maximum absolute gain, respectively, of two Schmitt triggers, one with $V_{DDH} = 100$ mV and the other with $V_{DDH} = 150$ mV.

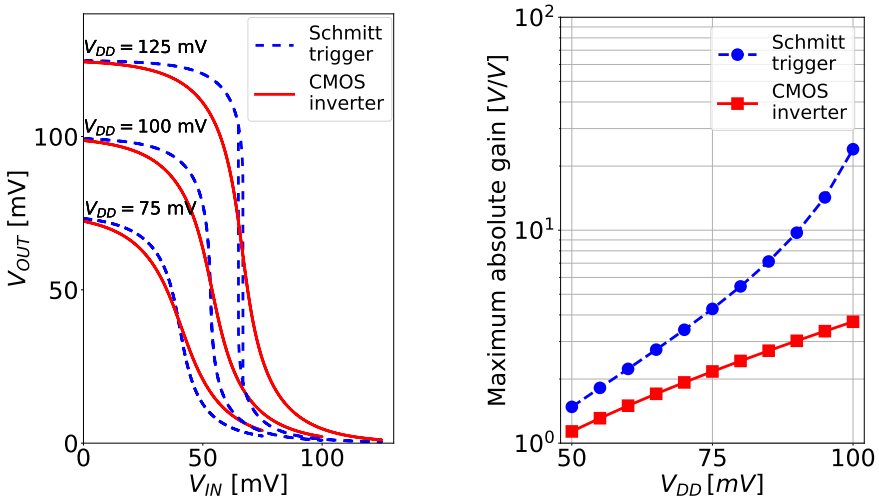
Note that the maximum absolute gain increases until hysteresis appears at a certain level, herein V_{DDH}. It can be seen that, for the same supply voltage V_{DD}, the Schmitt trigger that exhibits hysteresis at a lower voltage consistently has a higher maximum absolute gain. The value of V_{DDH} depends on the values of I_0, I_1 and I_2, and thus is chosen during the design. $I_0 = 70$ nA, $I_1 = 2.8$ nA and $I_2 = 25$ nA give $V_{DDH} = 100$ mV, while $I_0 = 46$ nA, $I_1 = 7.4$ nA and $I_2 = 4.6$ nA give $V_{DDH} = 150$ mV.

On the other hand, Figures 2.9a and 2.9b let us compare the gain of a CMOS inverter to the gain of a Schmitt trigger, as a function of V_{DD}. The Schmitt trigger exhibits a much higher maximum absolute gain. Thus, for a given supply voltage it is possible to design a Schmitt trigger with maximum absolute gain much higher than that of a CMOS inverter.



(a) (b)

Figure 2.8: (a) Voltage transfer characteristic of two Schmitt triggers designed to exhibit hysteresis at different supply voltages, V_{DDH}, and (b) their maximum absolute gain as a function of the supply voltage V_{DD}.



(a) (b)

Figure 2.9: (a) Voltage transfer characteristic of a Schmitt trigger with $V_{DDH} = 100$ mV and of a CMOS inverter and (b) their maximum absolute gain as a function of the supply voltage V_{DD}.

Chapter 3

Schmitt trigger dynamic model

Besides the low-frequency small-signal model presented in Section 2.6, a dynamic model requires insight on the circuit behaviour in the frequency domain. In this chapter, the capacitive coefficients of the transistors are calculated and a model with an equivalent input and output capacitances is proposed. The transition frequency is also derived, completing the model for the Schmitt trigger operating as an amplifier. Afterwards, the key parameters of the operation of the Schmitt trigger with hysteresis are also estimated. These are, the thresholds of the hysteresis and the step response. The model is verified through simulations.

3.1 Capacitive coefficients

Here the capacitive coefficients for the nMOS network only are considered. Later, the results are extended to the entire Schmitt trigger. Figure 3.1 presents the small-signal equivalent model for high-frequency operation, including both transconductances and parasitic capacitances.

In WI the intrinsic capacitances, other than the gate-bulk capacitance C_{gb}, are

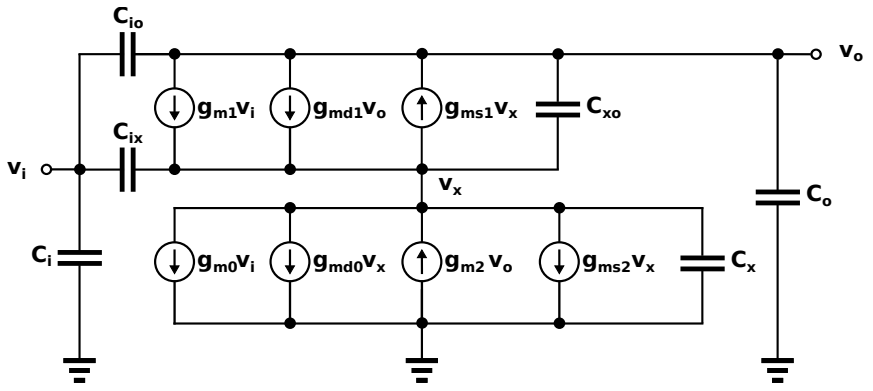


Figure 3.1: nMOS network of the six transistor Schmitt Trigger circuit. High-frequency small-signal equivalent model for $V_I = V_O = V_{DD}/2$, accounting for parasitic capacitances.

negligible. This can be verified by deriving the expressions in WI for the intrinsic capacitances in (2.26a)-(2.26g), as follows. In WI, $\alpha \approx 1$, $1+q'_{IS(D)} \approx 1$, obtaining

$$C_{gs(d)} = \frac{C_{ox}\, q'_{IS(D)}}{2}, \tag{3.1a}$$

$$C_{bs(d)} = \frac{(n-1)\, C_{ox}\, q'_{IS(D)}}{2}, \tag{3.1b}$$

$$C_{sd} = -\frac{n\, C_{ox}\, q'_{ID}}{3}, \tag{3.1c}$$

$$C_{ds} = -\frac{n\, C_{ox}\, q'_{IS}}{3}, \tag{3.1d}$$

$$C_{gb} = C_{bg} = \frac{n-1}{n}(C_{ox} - C_{gs} - C_{gd}), \tag{3.1e}$$

$$C_{dg} = C_{gd} + (C_{sd} - C_{ds})/n, \tag{3.1f}$$

with $q'_{IS(D)}$ much less than one. Consequently, all the intrinsic capacitances are negligible, except for C_{gb} and C_{bg} that can be approximated as

$$C_{gb} = C_{bg} \approx \frac{(n-1)}{n} C_{ox}. \tag{3.2}$$

Thus, the gate to bulk intrinsic capacitance of transistor k is given by

$$C_{gbk} = \left(\frac{n-1}{n}\right) W_k L_k C'_{ox}, \tag{3.3}$$

where W_k and L_k are the width and length of transistor M_{Nk}, respectively.

On the other hand, the overlap and junction extrinsic capacitances are taken into consideration.

Each of the parasitic capacitances contribute to one of the equivalent capacitances in Fig. 3.1, giving

$$C_i = C_{s0\,ov} + C_{gb0} + C_{gb1}, \tag{3.4a}$$

$$C_x = C_{j0} + C_{j1} + C_{j2}, \tag{3.4b}$$

$$C_{ix} = C_{d0\,ov} + C_{s1\,ov}, \tag{3.4c}$$

$$C_o = C_{d2\,ov} + C_{gb2} + C_{j1}, \tag{3.4d}$$

$$C_{io} = C_{d1\,ov}, \tag{3.4e}$$

$$C_{xo} = C_{s2\,ov}, \tag{3.4f}$$

where $C_{pk\,ov}$ is the overlap capacitance at node p of transistor k and C_{Jk} is the extrinsic capacitance within the drain or source to bulk junction.

The extrinsic overlap capacitances of transistor k are expressed as

$$C_{sk\,ov} = C_{dk\,ov} = C'_{ox} W_k LD, \tag{3.5}$$

being LD the overlapping distance.

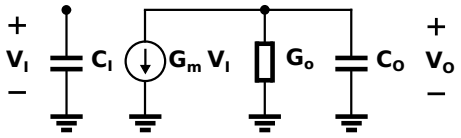


Figure 3.2: Circuit schematic of the dynamic model of a Schmitt trigger as an amplifier.

For the sake of simplicity, the extrinsic junction capacitances are considered to be independent of any voltage variations, this is

$$C_{Jk} = C'_J \times A_{Sk}, \tag{3.6}$$

where C'_J and A_{Sk} are the junction capacitance per unit area and the drain or source diffusion area of transistor k, respectively.

Figure 3.2 depicts the schematic of the dynamic model of the Schmitt trigger as an amplifier, with G_m and G_o the equivalent transconductance and output conductance derived in Section 2.6 in (2.36) and (2.37), respectively. The equivalent input and output capacitances, C_I and C_O, can be expressed taking into consideration the Miller effect [38] as

$$C_I = C_i + C_{io}\left(1 + |A_{io}|\right) + C_{ix}\left(1 + |A_{ix}|\right), \tag{3.7}$$

$$C_O = C_o + C_{io}\left(1 + \frac{1}{|A_{io}|}\right) + C_{xo}\left(1 + \frac{|A_{ix}|}{|A_{io}|}\right), \tag{3.8}$$

where A_{io} and A_{ix} are the low frequency voltage gain between v_o and v_i and between v_x and v_i, respectively. A_{io} and A_{ix} can be expressed as

$$A_{io} = \left.\frac{v_o}{v_i}\right|_{V_I=V_O=V_{DD}/2} = \frac{g_{m1}(g_{ms2} + g_{md0}) + g_{ms1}g_{m0}}{g_{md1}(g_{ms2} + g_{md0}) - g_{ms1}g_{m2}}, \tag{3.9}$$

$$A_{ix} = \left.\frac{v_x}{v_i}\right|_{V_I=V_O=V_{DD}/2} = \frac{g_{m1} - g_{m0}}{g_{ms1} + g_{md0} + g_{ms2} - g_{m2}}, \tag{3.10}$$

being the transconductances those in Table 2.1.

Due to the symmetry of the Schmitt trigger circuit, each capacitive component within the pMOS network is modeled in parallel with the same component in the nMOS network. Thus, the capacitances of the Schmitt trigger shall be computed as those in the nMOS network times $(1 + W_{pMOS}/W_{nMOS})$, provided that the pMOS and nMOS transistors have the same channel length.

In order to verify the model, simulations were run based on the Schmitt trigger circuit designed to work as the inverting amplifier of one of the oscillators presented in Chapter 4. The dimensions of the transistors are shown in Table 3.1 for convenience.

The simulation results are presented in Fig. 3.3 and so are the analytical curves. At $V_{DD} = V_{DDH}$, C_I curve presents a singularity, due to the appearance of hysteresis. An expression for V_{DDH} is provided in (2.41) and the main parameters of the Schmitt trigger with hysteresis are modeled and verified through simulations in Section 3.3.

Table 3.1: Transistor dimensions of the Schmitt trigger circuit.

$L_{N,P}$ $[\mu m]$	W_{N0} $[\mu m]$	W_{P0} $[\mu m]$	W_{N1} $[\mu m]$	W_{P1} $[\mu m]$	W_{N2} $[\mu m]$	W_{P2} $[\mu m]$
1.08	8×5.1	8×53	2×5.1	2×53	4×5.1	4×53

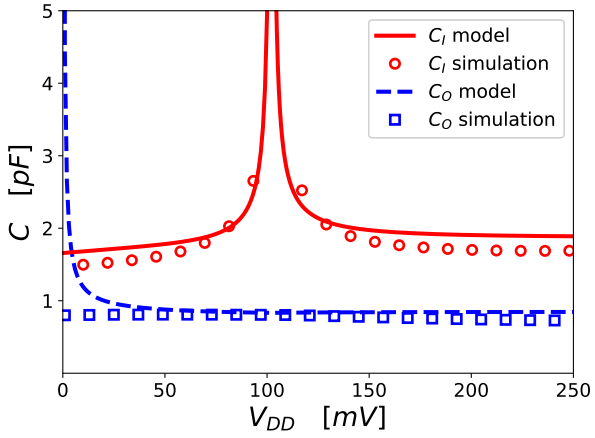


Figure 3.3: Equivalent input and output capacitances as functions of the supply voltage, V_{DD}. The analytic curves follow the equations (3.7) and (3.8) and are contrasted to simulation results.

Furthermore in Fig. 3.3, the simulation results are well predicted by the model, not only in the amplifier region ($V_{DD} < V_{DDH}$), but also in the region with hysteresis ($V_{DD} > V_{DDH}$). This is due to the simulations being AC simulations and the model a linear one.

3.2 Intrinsic transition frequency

The transition frequency of the Schmitt Trigger is defined similarly to that of a single transistor [39]. Firstly, the short-circuit current gain magnitude a_i is defined as the ratio of the amplitude of the small-signal output current to the amplitude of the small-signal input current, this is

$$a_i = \frac{i_{out}}{i_{in}} = \frac{G_m}{2\pi f C_{IT}}, \tag{3.11}$$

being G_m the equivalent transconductance of the Schmitt trigger in (2.36) and C_{IT} the total input capacitance. Note that C_{IT} is simply the sum of all the capacitances in the input node, since a_i is a current gain, in contrast to the voltage gain involved in the calculations of C_I and C_O in Section 3.1. Thus,

$$C_{IT} = C_i + C_{io} + C_{ix}. \tag{3.12}$$

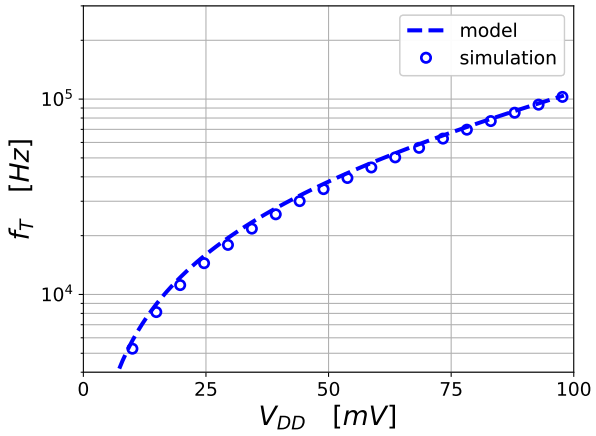


Figure 3.4: Transition frequency as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

The intrinsic transition frequency f_T, is defined as the frequency at which a_i drops to the value of 1. This is

$$f_T = \frac{G_m}{2\pi C_{IT}}, \tag{3.13}$$

where, according to (2.38), G_m can be expressed as

$$G_m = \frac{2\,I_1/n}{e^{-V_{DD}/2n\phi_t}} \left[\frac{(I_0 + I_2)e^{-V_{DD}/2\phi_t} - I_2 e^{-V_{X0}/\phi_t}}{I_0\, e^{(V_{X0}-V_{DD})/\phi_t} + I_1 + I_2} \right]. \tag{3.14}$$

Figure 3.4 shows the simulation results of the transition frequency and the analytic curve provided in (3.13). It is seen that the model fairly predicts the simulation results.

3.3 Schmitt trigger with hysteresis

As explained in Section 2.7, the minimum supply voltage to obtain hysteresis is provided in (2.41) and rewritten here for convenience

$$V_{DDH} \approx 2\phi_t\, ln \left[n \left(1 + \frac{I_0}{I_2}\right) \left(1 + \frac{I_1}{I_0} + \frac{I_2}{I_0}\right) - \frac{I_1}{I_0} \right]. \tag{3.15}$$

The hysteresis width is approximated by [37]

$$V_L \approx \frac{(V_{DD} - 2V_{X0})\left(1 - e^{V_{DD\,H} - V_{DD}}\right)}{2 + \frac{I_0}{I_2} + \frac{I_1}{I_2}}, \tag{3.16}$$

provided that the transistors are in WI region. Owing to the symmetry of the circuit, the input value of the upper and lower thresholds of the hysteresis loop are

$$V_{TH\pm} = \frac{V_{DD}}{2} \pm \frac{V_L}{2}. \tag{3.17}$$

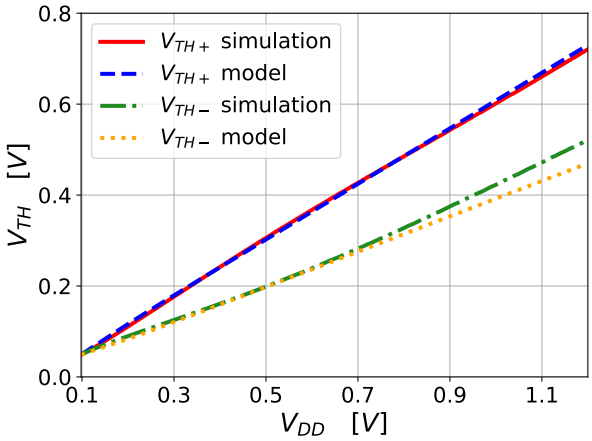


Figure 3.5: Thresholds of the hysteresis as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

Figure 3.5 shows the model results obtained from (3.17) and the simulation results of V_{TH+} and V_{TH-} as a function of the supply voltage.

In the region with hysteresis, the response to a step from V_{DD} to zero is given by

$$v_o(t) = V_{DD}\left(1 - e^{-t/\tau}\right), \tag{3.18}$$

with the time constant

$$\tau = R_O\, C_O \tag{3.19}$$

and the output resistance

$$R_O = \left.\frac{V_O}{I_O}\right|_{V_I=0}. \tag{3.20}$$

The output current I_O is calculated as the difference between the drain currents of transistors M_{N1} and M_{P1}, at $V_I = 0$ V. The drain currents are I_{DN1} and I_{DP1}, respectively, and follow (2.1). The results of the output current predicted by the model are presented in Fig. 3.6, showing that the output current is highly dependent on the output voltage. Therefore, for each value of V_{DD} an approximation of the output current is required to estimate an equivalent resistance R_O and the time constant τ. Thus, the mean value of the output current is chosen to this aim.

Figure 3.7 shows the transient simulation results of the step response for several values of V_{DD}. The time constant τ is extracted from the rise time (between 10% and 90% of the final value V_{DD}) of the step response in Fig. 3.7. It is seen that the rise time decreases with the supply voltage, as expected.

The time constant is calculated following (3.19). Thus, the results predicted by the equations are shown in Fig. 3.8 together with the simulation results.

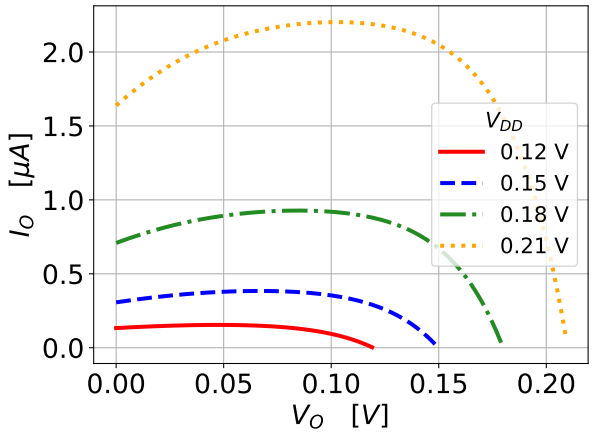


Figure 3.6: Model results of the output current of the Schmitt trigger, I_O, at $V_I = 0$ V, as a function of the output voltage V_O and for several values of supply voltage V_{DD}.

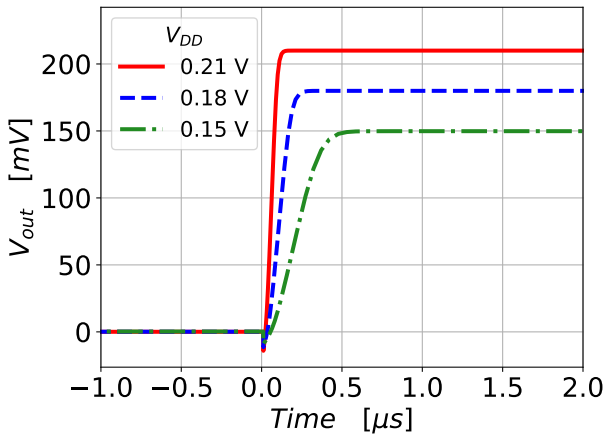


Figure 3.7: Transient simulation results of the step response of the Schmitt trigger with hysteresis for several values of supply voltage V_{DD}.

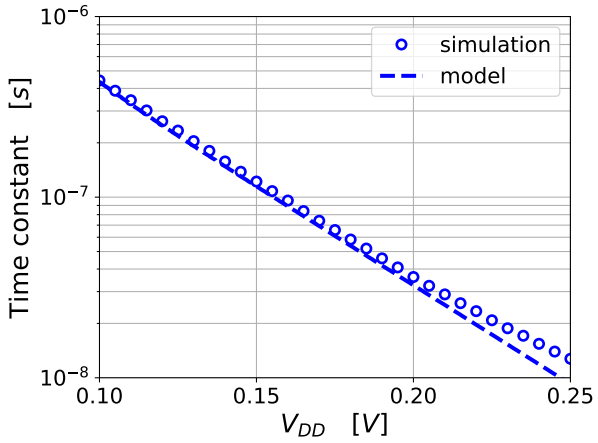


Figure 3.8: Time constant τ as a function of the supply voltage, V_{DD}, estimated analytically and contrasted to simulation results.

Chapter 4

Design of crystal oscillators

In this chapter, the basic concepts to fully understand the operation of the Pierce crystal oscillator are revisited. An amplifier, connected in parallel to a crystal resonator, compensates the losses in the crystal to enable oscillation. Firstly, it is briefly explained how to model the crystal resonator in Section 4.1. Secondly, a linear analysis on how the most simple Pierce circuit works is addressed in Section 4.2. The operation of a Pierce oscillator in a more general form, is presented in Section 4.3. The simplified case of the amplifier being lossless is studied in Section 4.3.1. In the ultra low voltage context, the losses in the amplifier are not negligible. The quantification of these losses and how to deal with them, is subject of Section 4.3.2. The design of two crystal oscillators is presented in Section 4.4, based on our work in [40]. A Schmitt trigger circuit is used as the amplifier of each of the crystal oscillators. The design of the Schmitt trigger circuits is the one explained in Section 2.6.

4.1 Equivalent impedance of the quartz crystal

A quartz crystal can be modeled by means of a motional impedance in parallel with a capacitance [3]. This motional impedance depends on the resonance mode of the crystal resonator. Fig. 4.1a shows the equivalent impedance model, used in the fundamental mode, where R_m, C_m and L_m are the motional resistance, capacitance and inductance, respectively, and C_P is the parallel capacitance.

Thus, the motional impedance of the crystal is given by

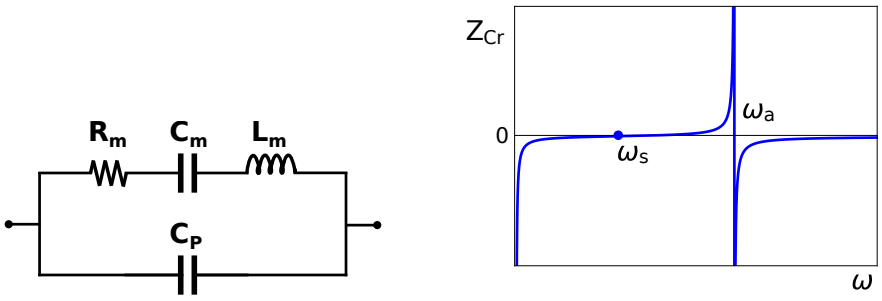
$$Z_m = R_m + j\omega L_m + \frac{1}{j\omega C_m}. \tag{4.1}$$

Neglecting R_m, the equivalent impedance in Fig. 4.1a is such that

$$Z_{Cr} \approx \frac{1}{s}\,\frac{1 + L_m C_m s^2}{L_m C_m C_P s^2 + C_m + C_P}. \tag{4.2}$$

Z_{Cr} in (4.2) has one pole at zero frequency, a double zero at ω_s, with

$$\omega_s = \frac{1}{\sqrt{L_m C_m}}, \tag{4.3}$$



(a) (b)

Figure 4.1: Crystal resonator: (a) circuit schematic of the equivalent impedance model and (b) value of the module of the impedance of the crystal as a function of the frequency ω.

and a double pole at ω_a, with

$$\omega_a = \omega_s \sqrt{1 + \frac{C_m}{C_P}} \approx \omega_s \left(1 + \frac{C_m}{2C_P}\right), \tag{4.4}$$

provided that $C_m/C_P \ll 1$.

Thus, the crystal impedance can be rewritten as follows

$$Z_{Cr} \approx \frac{1}{j\omega C_P} \frac{1 - \frac{\omega^2}{\omega_s^2}}{1 - \frac{\omega^2}{\omega_a^2}}. \tag{4.5}$$

Figure 4.1b shows the dependence of the module of the crystal impedance on frequency.

4.2 Linear analysis of the basic Pierce oscillator

The most basic form of the Pierce oscillator is depicted in Fig. 4.2a, where a single nMOS transistor is used. The biasing circuit is omitted, without losing generality. On the right hand, Fig. 4.2b shows the impedance equivalent model of the circuit in Fig. 4.2a, where Z_m in parallel to C_P represents the crystal equivalent model seen in Section 4.1.

The oscillation condition is given by

$$Z_C + Z_m = 0, \tag{4.6}$$

where the impedance Z_C represents the rest of the circuit, besides motional impedance, as marked in Fig. 4.2b.

To obtain an expression for Z_C it is useful to compute the impedance Z marked in Fig. 4.3a, this is, the transconductance in parallel with C_2. Thus,

$$Z = \frac{g_m + j\omega C_1}{j\omega C_2 j\omega C_1} = \frac{1}{j\omega C_2} + \frac{g_m}{(j\omega)^2 C_1 C_2}. \tag{4.7}$$

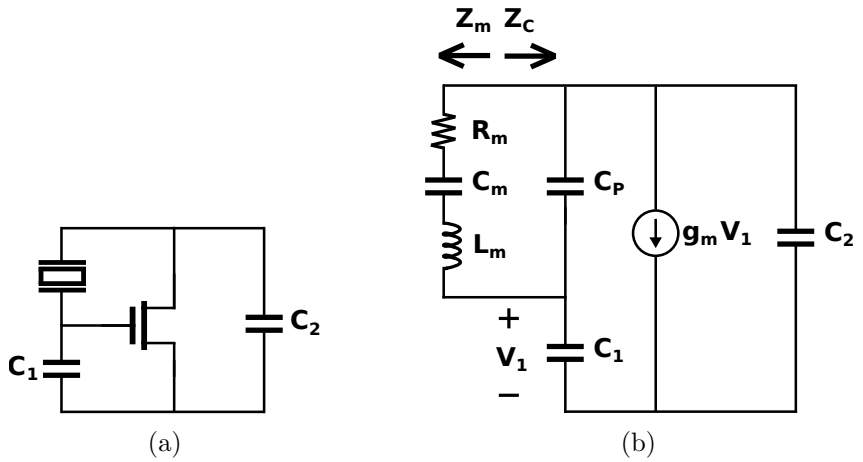


Figure 4.2: Single nMOS Pierce crystal oscillator (a) circuit schematic and (b) impedance equivalent model.

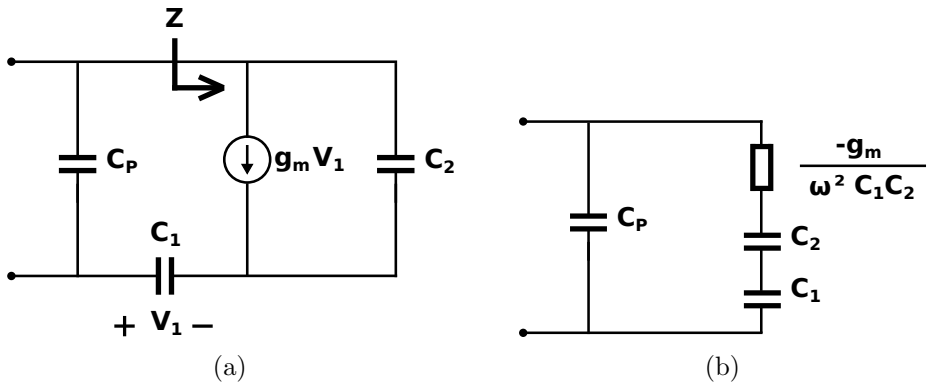


Figure 4.3: Two equivalent circuit schematics representing the same impedance Z_C.

In this way, the circuit schematic in Fig. 4.3a can be redrawn as that depicted in Fig. 4.3b. Thus, the impedance Z_C is given by

$$Z_C = -\frac{g_m + j\omega(C_1 + C_2)}{(C_1C_2 + C_1C_P + C_2C_P)\omega^2 - j\omega g_m C_P}. \tag{4.8}$$

Rearranging (4.8) it is obtained

$$Z_C = -\frac{g_m C_1 C_2 + j[\omega(C_1 + C_2)(C_1C_2 + C_1C_P + C_2C_P) + g_m^2 C_P/\omega]}{\omega^2(C_1C_2 + C_1C_P + C_2C_P)^2 + (g_m C_P)^2}. \tag{4.9}$$

From (4.1) and (4.3), and neglecting R_m, it can be seen that Z_m at the oscillation frequency ω_P is such that

$$Z_m(\omega_P) = \frac{\omega_s^2 - \omega_P^2}{j\omega_s^2\omega_P C_m} \approx \frac{2(\omega_s - \omega_P)}{j\omega_s\omega_P C_m}, \tag{4.10}$$

since $(\omega_s + \omega_P) \approx 2\omega_s$. Then the oscillation condition in (4.6), aided by (4.9) and (4.10), for $g_m \to 0$, reduces to

$$\frac{2(\omega_P - \omega_s)}{C_m \omega_s^2} = \frac{C_1 + C_2}{\omega_s(C_1C_2 + C_1C_P + C_2C_P)}. \tag{4.11}$$

Defining

$$C_L = \frac{C_1C_2}{C_1 + C_2}, \tag{4.12}$$

the oscillation frequency is obtained from (4.11) and (4.12) as

$$\omega_P = \omega_s \left[1 + \frac{C_m}{2(C_P + C_L)}\right]. \tag{4.13}$$

Note that (4.13) is the same result that was obtained in (4.4), by calculating the pole of the impedance of the crystal.

Comparing (4.13) and (4.4), we observe that $\omega_s < \omega_P < \omega_a$. Thus, at the oscillation frequency the impedance of the crystal is inductive, as expected. The impedance of the crystal Z_{Cr} in (4.5) can be obtained at the oscillation frequency, using the expressions for ω_s and ω_a in (4.3) and (4.4), respectively, giving

$$Z_{Cr}(\omega_P) = \frac{1}{j\omega_P C_P} \frac{1 - \left[1 + \frac{C_m}{2(C_P+C_L)}\right]^2}{1 - \frac{\left[1+\frac{C_m}{2(C_P+C_L)}\right]^2}{\left[1+\frac{C_m}{2C_P}\right]^2}} \approx \frac{j}{\omega_s C_L}. \tag{4.14}$$

The critical value of the transconductance to enable oscillation, called g_{mcrit}, is obtained by means of balancing the real parts of Z_C and Z_m when $g_m \to 0$, this is

$$-\operatorname{Re}(Z_C)\big|_{g_m \to 0} = R_m, \tag{4.15}$$

thus, giving

$$g_{mcrit} = \omega_s^2 R_m C_1 C_2 \left(1 + \frac{C_P}{C_L}\right). \tag{4.16}$$

If $C_1 = C_2 = 2 \times C_L$, (4.16) reduces to

$$g_{mcrit} = 4\omega_s^2 R_m (C_L + C_P)^2. \tag{4.17}$$

4.3 Pierce crystal oscillator operation

The schematic of a Pierce oscillator is depicted in Fig. 4.4a, consisting of a quartz crystal connected to an amplifier and two functional capacitors [3]. The amplifier provides the negative resistance required to compensate for the crystal losses, in order for the oscillation to take place.

Figure 4.4b shows the equivalent impedance model of the circuit in Fig. 4.4a. On the left hand side, the motional impedance Z_m, accounts for the motional part of the crystal by means of the series of R_m, C_m and L_m, the crystal motional

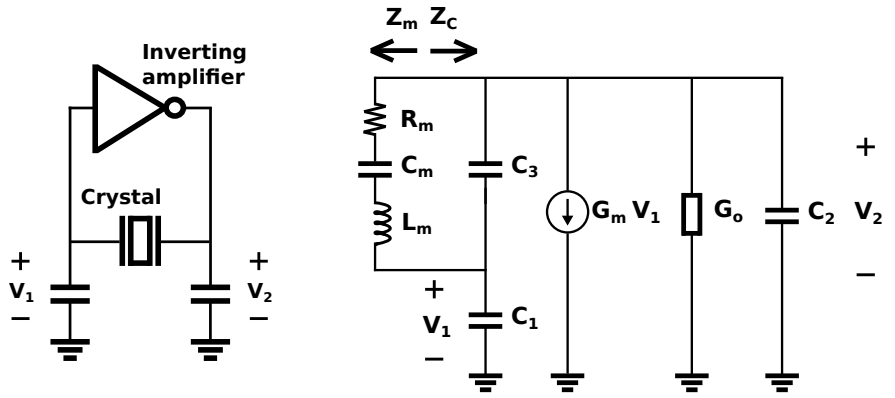


Figure 4.4: Pierce crystal oscillator (a) circuit schematic and (b) impedance equivalent model.

resistance, capacitor and inductor, respectively. On the right hand side, Z_C represents the rest of the circuit impedance for the fundamental frequency, this is, the compact small-signal model of the rest of the circuit connected in parallel to the crystal and also the crystal parallel capacitance C_3. G_m and G_o are the transconductance and the output conductance of the inverting amplifier, respectively. All of the parasitic capacitances within the inverting amplifier as well as the functional capacitors, are grouped in the capacitances C_1 and C_2.

4.3.1 Lossless amplifier

Having a lossless amplifier implies that the conductance G_o in Fig. 4.4b is neglected. According to [3], and by inspection of the schematic in Fig. 4.4b, Z_C can be expressed as

$$Z_C = \frac{Z_1 Z_3 + Z_2 Z_3 + G_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + G_m Z_1 Z_2}, \tag{4.18}$$

being $Z_1 = 1/j\omega C_1$, $Z_2 = 1/(G_o + j\omega C_2)$ and $Z_3 = 1/j\omega C_3$.

The locus of Z_C as a function of G_m is depicted in Fig. 4.5. The imaginary part of Z_C is negative, since it is a purely capacitive impedance. The real part of Z_C is negative, provided that G_m has positive values. The dotted line represents the locus of $-Z_m$, with a constant real part of value $-R_m$. These loci intersect twice, when the critical condition for oscillation is reached at G_{mcrit}, and an unstable solution obtained at G_{mmax} [3]. G_{mopt} is the transconductance value to achieve the maximum negative resistance possible, and can be obtained equating to zero the first derivative of the real part of Z_C. The negative resistance obtained in that case would be $-|R_{n0}|_{max}$.

G_{mcrit} and G_{mmax} are obtained balancing both impedances $-Z_m$ and Z_C real parts, giving [3]

$$G_{mcrit} = \omega^2 C_1 C_2 R_m \left(1 + \frac{C_3}{C_1} + \frac{C_3}{C_2}\right)^2 \tag{4.19}$$

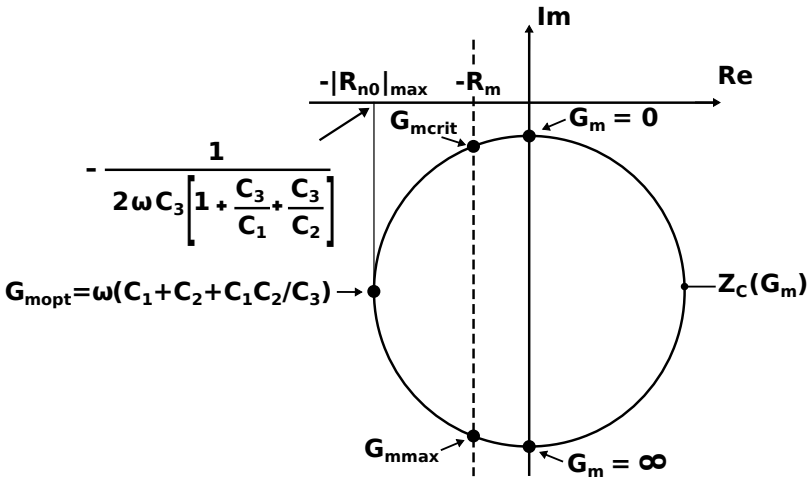


Figure 4.5: Locus of the impedance Z_C as a function of the transconductance G_m for a lossless inverting amplifier and locus of $-Z_m$ (dotted line), being Z_m the motional impendance.

and

$$G_{mmax} = \frac{C_1 C_2}{R_m C_3^2}. \tag{4.20}$$

Equations (4.19) and (4.20) are valid as long as [3]

$$\frac{|R_{n0}|_{max}}{R_m} \gg 1 \tag{4.21}$$

or equivalently

$$2\omega R_m C_3 (1 + C_3/C_1 + C_3/C_2) \ll 1. \tag{4.22}$$

As a rule of thumb [41], the transconductance value is designed to be $3 \times G_{mcrit}$. Afterwards it will be verified that $G_m \ll G_{mopt}$, with

$$G_{mopt} = \omega(C_1 + C_2 + C_1 C_2/C_3), \tag{4.23}$$

in spite of the over estimation of G_m. Also it will be verified that the condition in (4.22) is fulfilled.

4.3.2 Lossy amplifier

The effect of losses in the inverting amplifier is not negligible at low supply voltages, and the transconductance G_m must also compensate these to enable oscillation.

Equations (4.19) and (4.20) are still valid as long as the losses, modeled through G_o, are small. The effect of G_o is accounted for, as seen in Appendix A, as an horizontal displacement in the locus of Z_C, provided that

$${G_o}^2 \ll (\omega C_2)^2. \tag{4.24}$$

Expression (4.24), herein the small losses hypotheses, will be verified after the design is completed in Section 4.4.

Table 4.1: Crystals and Other Discrete Components of the Oscillators.

Parameter	Oscillator A	Oscillator B
Crystal part number	ABS07W-32.768kHz-D1	AB38T-32.768kHz-12.5pF-E-7
$f\,[kHz]$	32.768	32.768
$C_m\,[fF]$	4.68	3.5
$L_m\,[H]$	5 048.571	6 740.193
$R_m\,[k\Omega]$	38.194	15.419
Q	27 214	90 000
$C_L\,[pF]$	3	12.5
$C_1 = C_2\,[pF]$	6	25
$C_3\,[pF]$	1.15	1.60
$R_F\,[G\Omega]$	5	5

This horizontal displacement, ΔR_C, is obtained in (A.9) and rewritten here for convenience

$$\Delta R_C = \frac{G_o}{\omega^2 \left(C_2 + C_3 + \frac{C_2 C_3}{C_1}\right)^2}. \tag{4.25}$$

Thus, from (4.19) and (4.25), the increase in G_{mcrit} needed to compensate losses in G_o is

$$\Delta G_m = \frac{C_1}{C_2} G_o. \tag{4.26}$$

Note that with $C_1 = C_2$, (4.26) simplifies to

$$\Delta G_m = G_o. \tag{4.27}$$

4.4 Design of crystal oscillators based on Schmitt trigger

The design of the crystal oscillators presented herein is based on our work in [40]. Two oscillators, A and B, were designed. Oscillator A includes a crystal suitable for smaller external capacitors. On the other hand oscillator B uses a crystal with a lower motional resistance, R_m, providing a larger quality factor Q.

Table 4.1 summarizes all parameters related to the two crystals, that is, resonance frequency f, motional capacitance C_m, motional inductor L_m, motional resistance R_m, quality factor Q, load capacitance C_L (C_1 in series with C_2) and the parallel capacitance C_3. Here, $C_1 = C_2 = 2 \times C_L$ for simplicity. A feedback resistor R_F is connected in parallel to the crystal for biasing purposes.

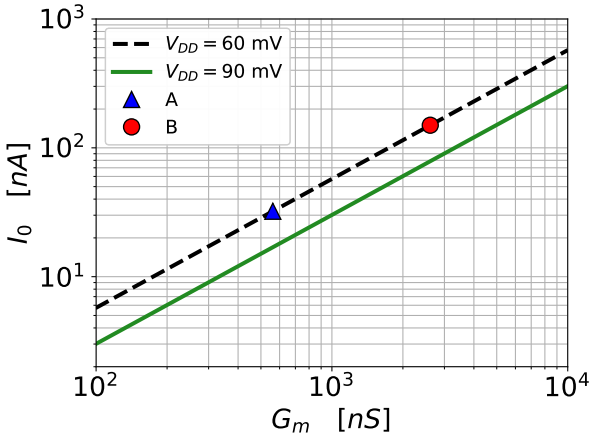


Figure 4.6: The required current strength parameter I_0 as a function of the transconductance G_m in (2.38), for supply voltages 60 mV and 90 mV. G_m also fulfills (4.29) for each oscillator, A or B, with $G_{m\,A}$ = 561 nS (blue triangle) and $G_{m\,B}$ = 2 612 nS (red circle).

A Schmitt trigger is used as the inverting amplifier of the Pierce oscillator. As seen in Section 4.3.1, the transconductance G_m is firstly designed to be $3 \times G_{mcrit}$, with G_{mcrit} that in (4.19). Afterwards in Section 4.3.2, G_m is further increased by the amount ΔG_m in (4.27) to compensate losses in the amplifier. Thus,

$$G_m = 3 \times G_{mcrit} + G_o. \tag{4.28}$$

From (2.40) and (4.28),

$$G_m = \frac{3 \times G_{mcrit}}{1 + 1/A}. \tag{4.29}$$

On the other hand, G_m can be expressed only in terms of the design parameters I_k (with $k = 0, 1, 2$) and V_{DD}, according to (2.38). Figure 4.6 shows the dependence of I_0 on the transconductance G_m, for $I_1/I_0 = 0.25$ and $I_2/I_0 = 0.5$ according to the design in Section 2.6. As a consequence, I_0 is determined for each oscillator, with $G_{m\,A}$ = 561 nS and $G_{m\,B}$ = 2 612 nS according to the values in Table 4.1.

To properly size the transistors, the parameters are extracted following the procedure described in Section 2.4. Figures 4.7, 4.8, and 4.9, show the simulation results, using the PSP model, of the threshold voltage V_{T0}, the slope factor n and the specific current of an equivalent square transistor I_{SQ}.

The transistors are built as parallel arrangements of unit transistors that are long enough to attain a low threshold voltage and a low slope factor. However, the total silicon area increases with the length of the transistors, provided that the current strength I_0 is fixed at this stage. Thus, the channel length is chosen to be $L_{N,\,P} = 1.08\,\mu$m, taking into consideration the results in Figs. 4.7 and 4.8.

The unit nMOS transistor width W_N is selected to obtain a parallel arrangement composed of a reasonable number of unit transistors (less than 20, for the sake of layout simplicity), since all of the parameters, V_{T0}, n and I_{SQ}, are not significantly dependent on W_N. On the other hand, the pMOS transistors are

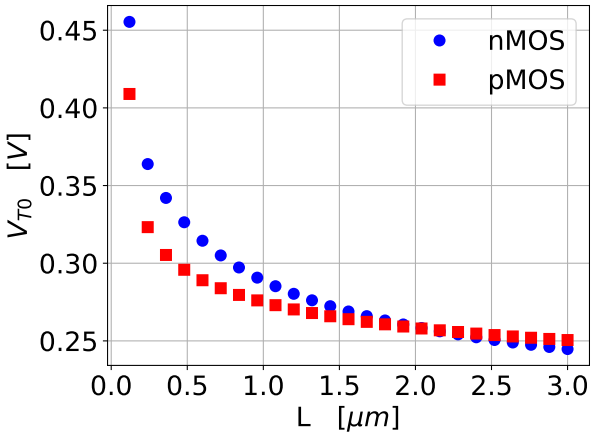


Figure 4.7: Simulation results of the threshold voltage as a function of the channel length of an nMOS and a pMOS transistors. See Section 2.4 for the specifics on the parameter extraction.

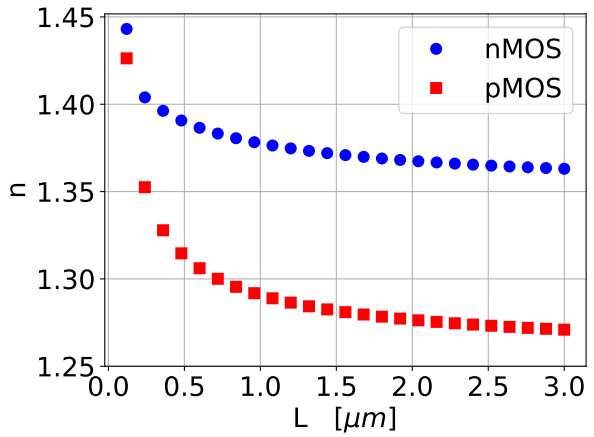


Figure 4.8: Simulation results of the slope factor as a function of the channel length of an nMOS and a pMOS transistors. See Section 2.4 for the specifics on the parameter extraction.

sized such that the current strength in (2.12) is the same as that of the unit nMOS transistor. By inspection of Fig. 4.9, the unit pMOS transistor is chosen to be 10 times wider than the unit nMOS transistor, giving $W_{N\,A} = 5.1\,\mu\text{m}$, $W_{P\,A} = 53\,\mu\text{m}$, $W_{N\,B} = 11\,\mu\text{m}$, $W_{P\,B} = 120\,\mu\text{m}$.

Table 4.2 summarizes all parameters related to both Schmitt trigger circuits, that is, the supply voltage V_{DD}, current strengths I_k (with $k = 0, 1, 2$), current consumption I_{DD}, voltage gain A, transconductance G_m, output conductance G_o and dimensions of all the transistors involved.

Lastly, some assumptions remain to be verified. Equation (4.22), with $C_1 = C_2$, becomes $2\omega R_m C_3(1 + 2C_3/C_1) \ll 1$, which holds for oscillators A and B, given that $0.035 \ll 1$ and $0.011 \ll 1$, respectively. Also in Section 4.3.1 it is stated that, even though G_m is 3 times the critical value, it would still be well below

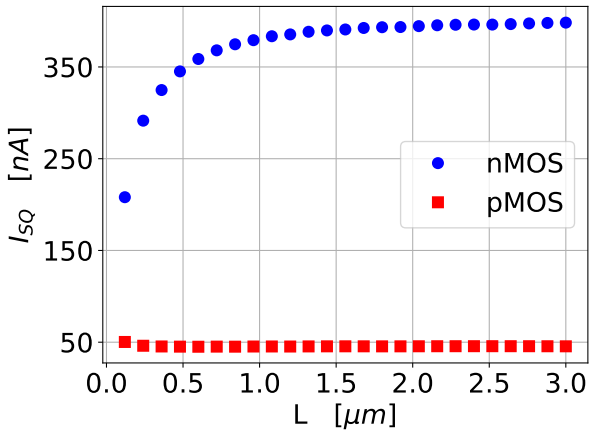


Figure 4.9: Simulation results of the specific current of an equivalent square transistor as a function of the channel length of an nMOS and a pMOS transistors. See Section 2.4 for the specifics on the parameter extraction.

Table 4.2: Operating Point and Transistor Dimensions of both Schmitt trigger Circuits.

	Parameter	A	B
Design parameters	$V_{DD}\,[mV]$	60	60
	$I_0\,[nA]$	32.2	150
	$I_1\,[nA]$	8.05	37.5
	$I_2\,[nA]$	16.1	74.9
Performance parameters	$I_{DD}\,[nA]$	27.7	129
	$G_m\,[nS]$	561	2 612
	$G_o\,[nS]$	226	1 053
	$A\,[V/V]$	-2.48	-2.48
Transistor dimensions	$L_{N,P}\,[\mu m]$	1.08	1.08
	$W_{N0}\,[\mu m]$	8×5.1	16×11
	$W_{P0}\,[\mu m]$	8×53	16×120
	$W_{N1}\,[\mu m]$	2×5.1	4×11
	$W_{P1}\,[\mu m]$	2×53	4×120
	$W_{N2}\,[\mu m]$	4×5.1	8×11
	$W_{P2}\,[\mu m]$	4×53	8×120

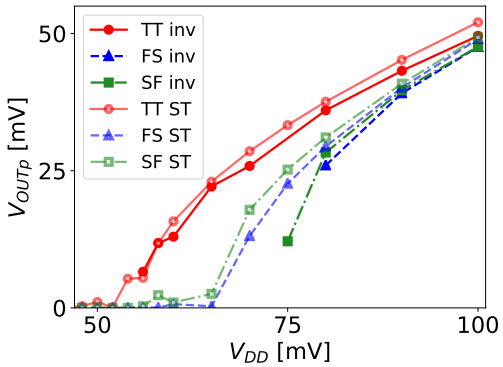


Figure 4.10: Simulation results of the output peak amplitude of an oscillator based on a CMOS inverter and an oscillator based on a Schmitt trigger, versus the supply voltage.

G_{mopt} in (4.23). Since $G_{mopt\,A} = 8\ 915$ nS and $G_{mopt\,B} = 90\ 719$ nS, it holds that $G_m \ll G_{mopt}$. On the other hand, the small losses hypotheses in (4.24) holds for oscillators A and B, provided that for oscillator A

$$G_{oA}{}^2 = 5.12 \times 10^{-14} \ll (\omega C_{2A})^2 = 1.53 \times 10^{-12}$$

and for oscillator B

$$G_{oB}{}^2 = 1.11 \times 10^{-12} \ll (\omega C_{2B})^2 = 2.65 \times 10^{-11}.$$

To complete the understanding on the advantages of using a Schmitt trigger instead of a CMOS inverter, an oscillator based on a CMOS inverter and using the crystal in oscillator A was designed. For comparison purposes the same unit transistors are used and $V_{DD} = 60$ mV. Figure 4.10 shows the simulation results of the output voltage amplitude of the oscillators based on a CMOS inverter and based on a Schmitt trigger. The results in the FS and SF corners show that the CMOS inverter has a lot more variability than the Schmitt trigger. In fact, the oscillator based on a CMOS inverter in the FS corner does not start with less than 80 mV supply and in the SF corner with less than 75 mV supply. Furthermore, the simulation results also show that the standard deviation of the oscillation frequency is 0.16 Hz and 0.53 Hz in the case of the Schmitt trigger and the CMOS inverter, respectively.

The fact that the oscillators in the FS and SF corners do not start, together with the higher standard deviation of the oscillation frequency, make the oscillator based on a CMOS inverter unsuitable at supply voltages as low as 60 mV.

This page is intentionally left blank.

Chapter 5

Results of two crystal oscillators based on Schmitt trigger

The simulation and measurement results of the oscillators designed in Chapter 4, are presented in this chapter. The two oscillators, A and B, are based on a Schmitt trigger circuit operating as an amplifier. A test chip including amplifier circuits A and B was designed and fabricated in a 130 nm technology. A microphotograph of one die is shown in Fig. 5.1. The actual position of these circuits in the die and their dimensions were drawn and superimposed. The layout of each circuit is also depicted. For details on the layout, see Appendix B. The area occupied by circuit A is 44.86 µm × 74.15 µm. Circuit B occupies a larger area (77.90 µm × 82.95 µm), which is related to the need for a higher current drive.

Firstly, the stand-alone amplifier is characterized and the measurement results are compared against simulations. The voltage transfer characteristic of the Schmitt trigger and the gain obtained are presented as functions of the supply voltage. Secondly, the results of the oscillators are presented. The power and current consumption results are shown as functions of the supply voltage and some insight is provided on the dependence of the current consumption on temperature. The results for the start-up time and the minimum supply voltage for the oscillators to start-up, as well as for the output voltage amplitude, are also presented. The oscillation frequency is characterized as a function of the supply voltage and temperature. The time jitter and the Allan deviation results are presented. Finally, the oscillators presented here are compared to prior work.

The results presented herein are based on our work in [40].

5.1 Measurement results of the Schmitt trigger as a stand-alone amplifier

The voltage transfer characteristic of the Schmitt trigger was measured as a function of the supply voltage by means of a semiconductor parameter analyzer (HP4156). Figs. 5.2a and 5.2b, show the voltage transfer characteristic of circuits A and B, respectively, and the simulation results are also shown.

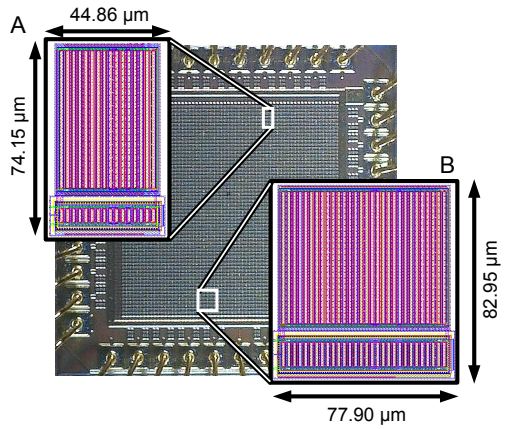


Figure 5.1: Microphotograph of the fabricated integrated circuit, showing circuits A and B, which are the two Schmitt trigger circuits referred to in this theses.

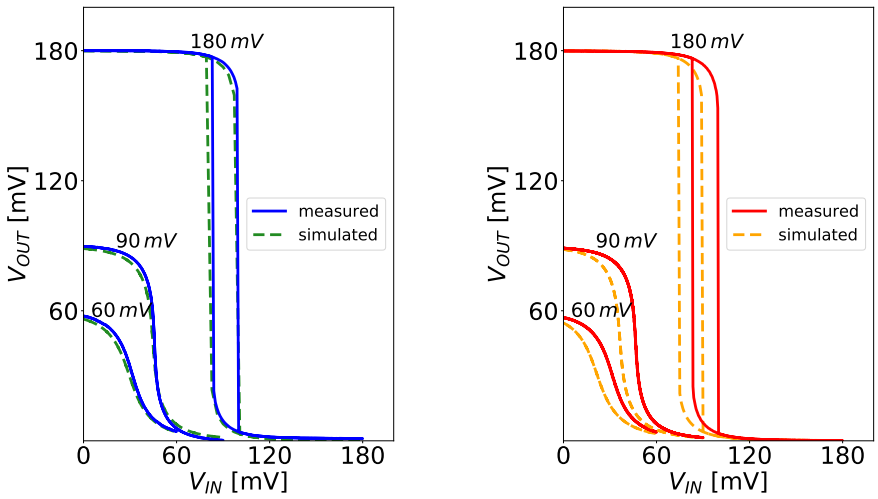
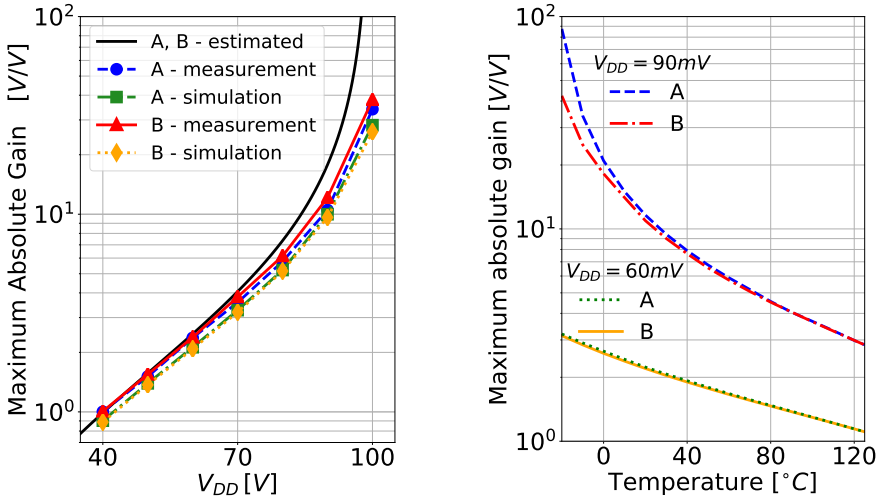


Figure 5.2: Simulation and measurement results of the Schmitt trigger voltage transfer characteristic. Results for different supply voltages are displayed for both circuits, (a) A and (b) B.



(a) (b)

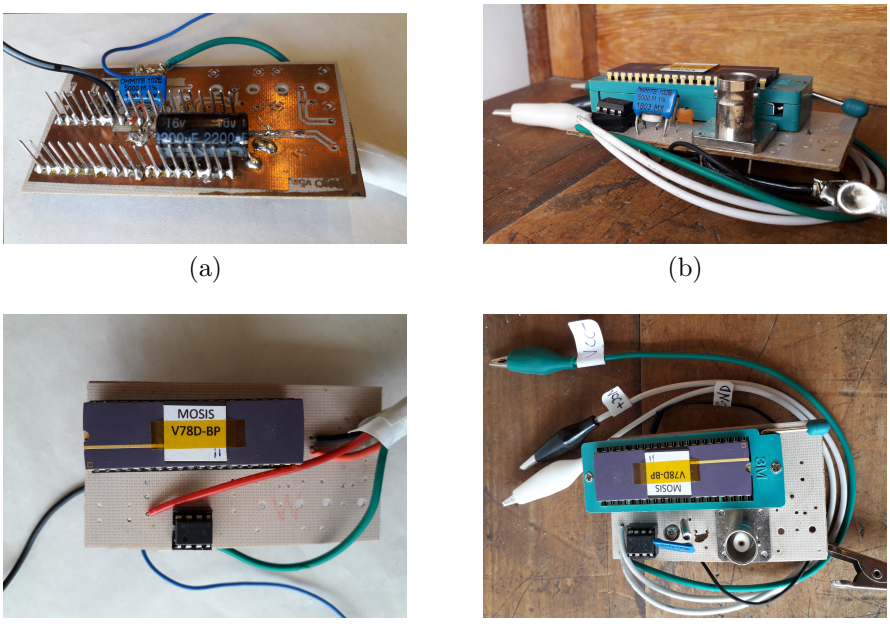
Figure 5.3: Maximum absolute gain of the Schmitt trigger for circuits A and B, showing their dependence on (a) the supply voltage (simulations and measurements) and (b) the temperature (simulations only). For $V_{DD} \geq 100$ mV hysteresis appears, and the circuits no longer work as amplifiers.

The maximum absolute gains for circuits A and B were extracted from the voltage transfer characteristic measurements and simulations, as shown in Fig. 5.3a. The estimated curve was calculated using (2.40), which is why the results are expected to be the same for circuits A and B, since they were designed to achieve the same gain. Accordingly, the simulation results for the two circuits are exactly the same. In the case of the measurements, the results are acceptably close. Note that the predicted gain for $V_{DD} = 40$ mV is unity, thus for $V_{DD} < 40$ mV the maximum absolute voltage gain is less than 1, disabling regeneration. The values for $V_{DD} \geq 100$ mV are not included since hysteresis appears, and these circuits are meant to work as the amplifier of a Pierce oscillator exhibiting no hysteresis.

Figure 5.3b shows the simulation results for the maximum absolute gain over temperature. Since the gain decreases with increasing temperature to well below 2 V/V for a 60 mV supply, the measurement of the frequency of the oscillators as a function of the temperature was taken using a 90 mV supply, in order to arrive at insightful conclusions. These simulations predicted a slightly higher maximum absolute gain for circuit A compared with circuit B, in agreement with the simulation results reported in Fig. 5.3a. This effect becomes more relevant for low temperatures and $V_{DD} = 90$ mV.

5.2 Measurement results of the crystal oscillators

Two printed circuit boards (PCBs) were built in order to fully test both oscillators, one of which is based on circuit A and the other on circuit B. Figures 5.4a and 5.4c



(a) (b)

(c) (d)

Figure 5.4: PCBs to experimentally characterize circuits A and B. (a) bottom view of PCB A, (b) lateral view of PCB B, (c) top view of PCB A, and (d) top view of PCB B.

show the PCB of circuit A. On the other hand, Figs. 5.4b and 5.4d show the PCB of circuit B. Circuit A includes an SMD crystal resonator in the bottom layer, while the crystal in circuit B is through-hole.

The values for the parameters of the crystals, the external capacitances and the feedback resistors, are reported in Table 4.1.

A buffering stage is also included in the PCB and connected at the output using a TL072 operational amplifier, which has a very low input capacitance, to avoid excessively loading the oscillator. The actual capacitors connected to the crystal, the parasitic capacitances and the buffering stage input capacitances must add up to the design values of C_1 and C_2, in order to properly tune the oscillation frequency. Unfortunately, the parasitic capacitances within oscillator A are too large, exceeding the total capacitance needed. As a consequence, the frequency of oscillator A was lower than the nominal resonance frequency of the crystal, which implies a poorer frequency stability. This and other consequences are fully explained in the rest of the chapter and their impact on the performance parameters is quantified. In the case of oscillator B, the oscillation frequency was finely trimmed to the nominal frequency.

To measure the circuits, a Faraday cage is used, as shown in Fig. 5.5a. The measurement setup, shown in Fig. 5.5b, includes two DC voltage sources (HP 3245A, Tektronix PS280) to supply the oscillator and the buffering stage, respectively, an oscilloscope (Tektronix 1001B), a multimeter (Fluke 8846A). Also, another multimeter (Fluke 289) was used to measure temperature.

(a) (b)

Figure 5.5: Measurement setup for power and current consumption, start-up time and voltage amplitude measurements.

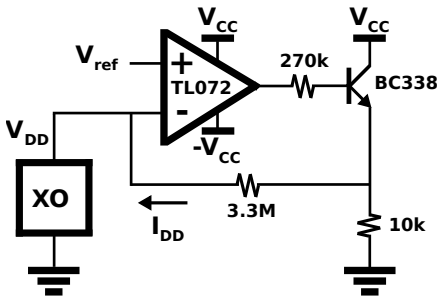


Figure 5.6: Schematic of the auxiliary circuit used for current measurements.

5.2.1 Oscillator power and current consumption

The current delivered to each of the oscillators was measured using a simple auxiliary current-to-voltage converter circuit [42] shown in Fig. 5.6. The results for oscillators A and B are given in Figs. 5.7a and 5.7b, respectively. It can be seen that the current and power consumption increase exponentially with the supply voltage, as expected for WI operation. However, the results for oscillator B deserve further inspection, since the measurement results are not very well predicted by the simulations. To this aim, Monte Carlo simulation results for the current consumption are shown in Figs. 5.8a and 5.8b for both oscillators with 60 mV and 90 mV supplies, respectively. It is seen that oscillator B measured current falls far from the distribution mean value, in agreement with the results presented in Fig. 5.7b. Consistently with results shown in Fig. 5.7a, oscillator A exhibits a measured current closer to the mean value of the distribution.

The variations of the drain currents of the transistors over temperature, as well as the total current consumption over temperature, were simulated. The results

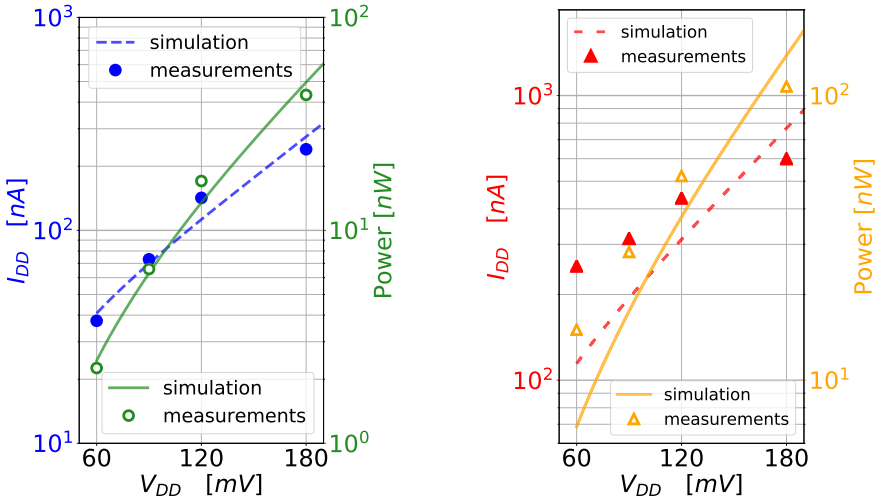


Figure 5.7: Simulation and measurement results of the oscillators (a) A and (b) B, DC current and power consumption against the supply voltage.

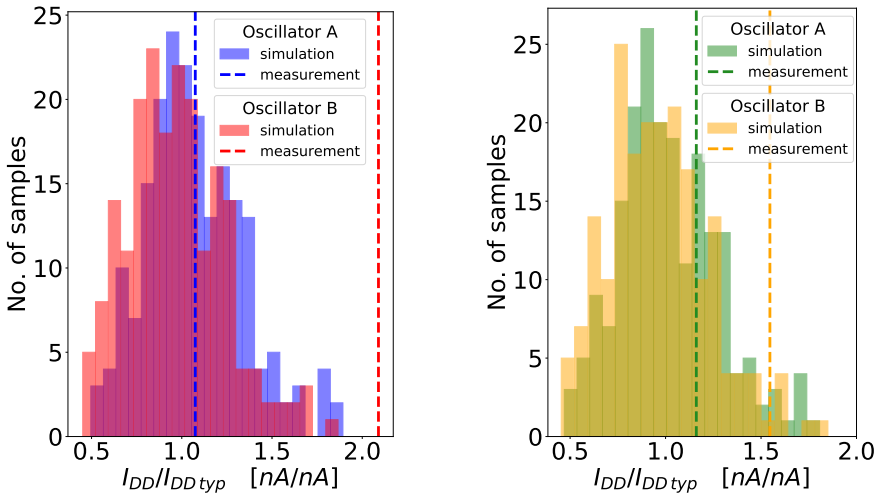


Figure 5.8: Monte Carlo simulation and measurement results for the normalized current consumption of oscillators A and B for (a) 60 mV and (b) 90 mV supplies. The Monte Carlo simulations were run for 200 samples to obtain data for both the mismatch and the process variation.

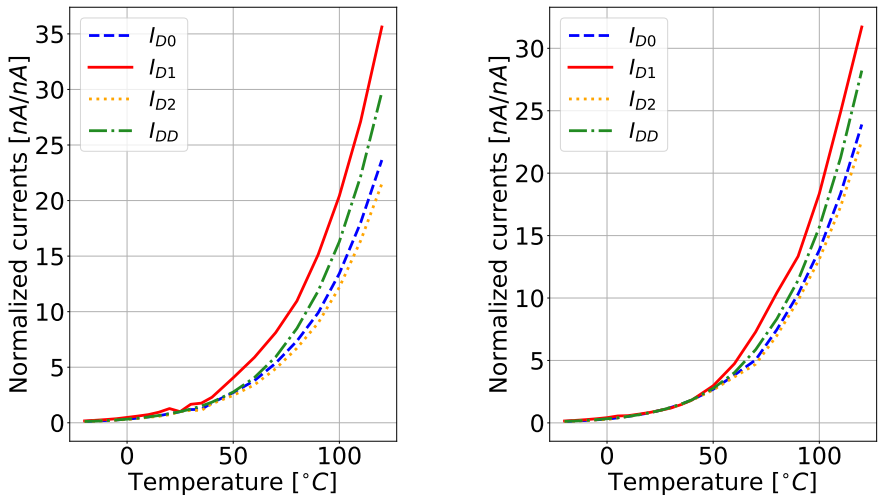


Figure 5.9: Simulation results for the oscillators (a) A and (b) B, DC currents in steady state over temperature. I_{D0}, I_{D1} and I_{D2} are the drain current of transistors M_{N0}, M_{N1} and M_{N2}, respectively, normalized to the value at 25°C and 60 mV supply. I_{DD} is the current consumption of the oscillator in the TT corner, normalized to the value at 25°C and 60 mV supply.

are shown in Figs. 5.9a and 5.9b, for oscillators A and B, respectively. All the currents are normalized to their typical value at 25°C.

Monte Carlo simulations were run to quantify process variations of the drain current through transistors M_{N0}, M_{N1} and M_{N2}. The results are shown in Figs. 5.10a and 5.10b. Besides the fact that the currents in oscillator B have more variability, all the currents in both oscillators may vary between half and twice their nominal value. These variations in the currents are only due to the Schmitt trigger, rather than to the crystal resonator and other components. As a consequence, the frequency stability exhibits variations, and the results are presented in Section 5.2.4.

5.2.2 Oscillator start-up

Figures 5.11a and 5.11b show the start-up transient measurements for oscillators A and B, respectively, for a supply voltage of 60 mV. The start-up time was measured for both oscillators with different values of the supply voltage V_{DD}, and the results are shown in Fig. 5.12a.

In order to determine the minimum supply voltage for which the oscillator starts up, measurements for eight samples were taken and the results are plotted in Fig. 5.12. It can be seen that all oscillators start up and that this occurs for supply voltages below 60 mV. Oscillator B starts-up at a lower supply voltage than oscillator A, which is consistent with the fact that circuit B exhibits a higher maximum absolute gain than circuit A, according to the results shown in Fig. 5.3a.

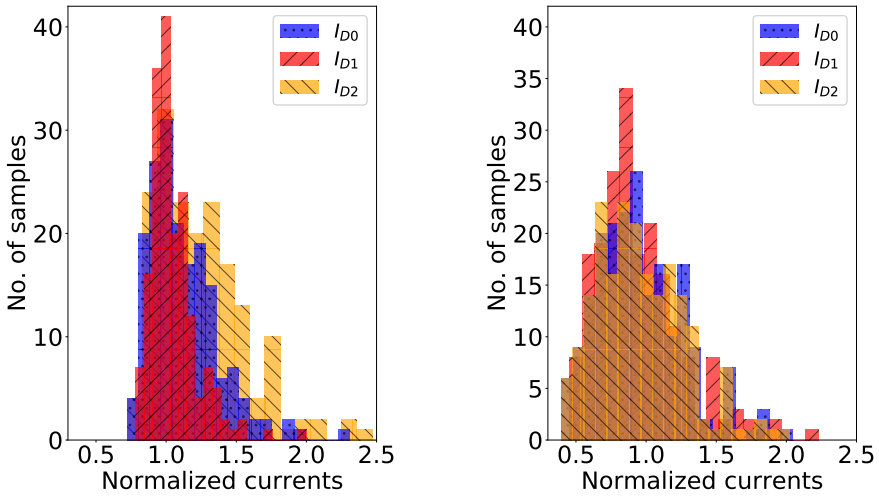


Figure 5.10: Monte Carlo simulation results for the drain current of the transistors M_{N0}, M_{N1} and M_{N2} of oscillators (a) A and (b) B, at 60 mV supply. The Monte Carlo simulations were run for 200 samples to obtain data on both the mismatch and the process variation.

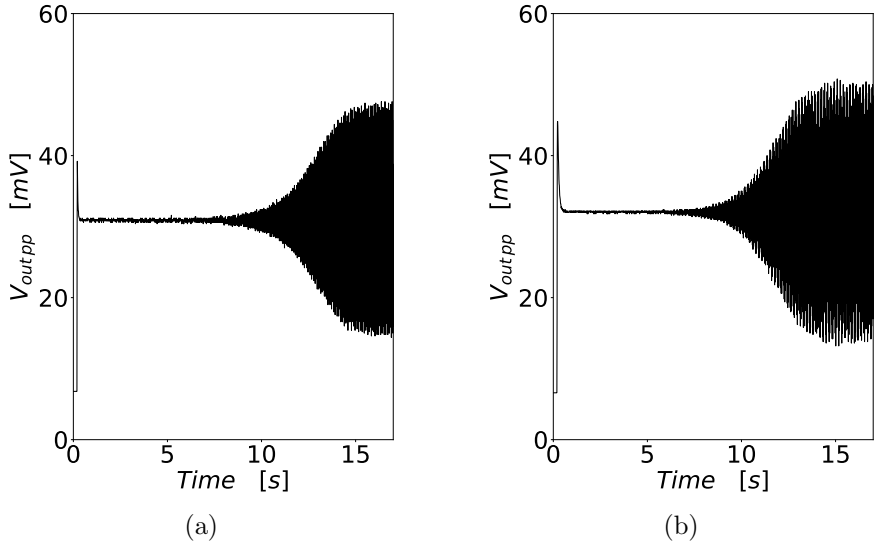
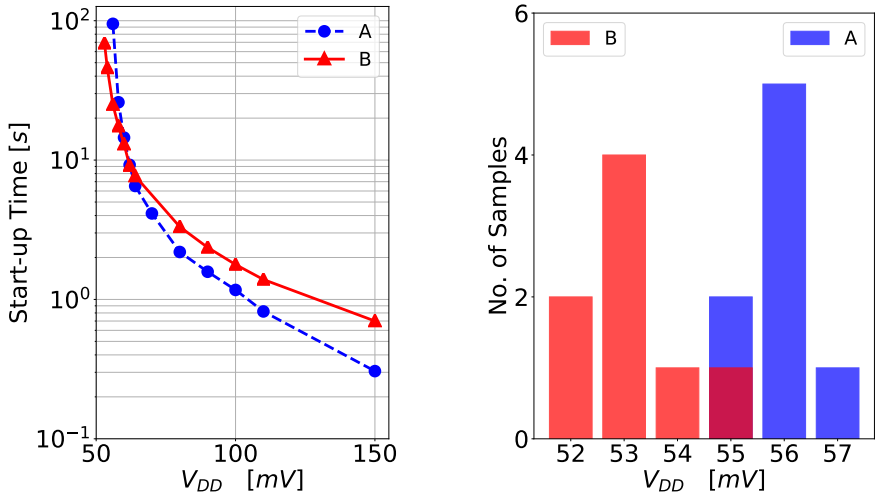


Figure 5.11: Start-up of oscillators (a) A and (b) B, with 60 mV supply.



(a) (b)

Figure 5.12: Measurement results for oscillators A and B: (a) start-up time versus supply voltage and (b) minimum supply voltage for starting up. The start-up time was measured from the instant the DC output voltage reached 90 % of its final value until the instant when the amplitude of the oscillating signal was 90 % of its value at steady state.

The minimum supply voltage varies over temperature, giving a minimum supply to start of 80 mV and 75 mV for oscillators A and B, respectively, at the upper limit of the temperature range measured (62°C).

5.2.3 Oscillator output voltage amplitude

The output voltage amplitude of oscillators A and B at resonance frequency was obtained through Monte Carlo simulations of the mismatch and process variation. The results are presented in Figs. 5.13a and 5.13b for supply voltages of 60 mV and 90 mV, respectively. Oscillation takes place with a yield of 100%, even though for a 60 mV supply the output signal could attain a peak to peak amplitude as small as 3 mV in some cases. Statistically, there is 5% probability that a sample of oscillator A exhibits a peak to peak output voltage smaller than 10 mV and in the case of oscillator B the probability is 9%. As seen in Fig. 5.13b, this effect decreases for a larger supply voltage, where all oscillator A samples attain at least a 39 mV peak and oscillator B samples at least a 36 mV peak.

Figure 5.14 shows the waveforms for the two oscillators with different supply voltages. The blue discontinuous line corresponds to oscillator A and the red continuous line, to oscillator B. For V_{DD} = 120 mV and 180 mV the output waveform is visibly no longer sinusoidal. Furthermore, the harmonic components increase with the supply voltage. It should be noted that for V_{DD} = 110 mV and above the Schmitt trigger exhibits hysteresis and loses the purely amplifying characteristic.

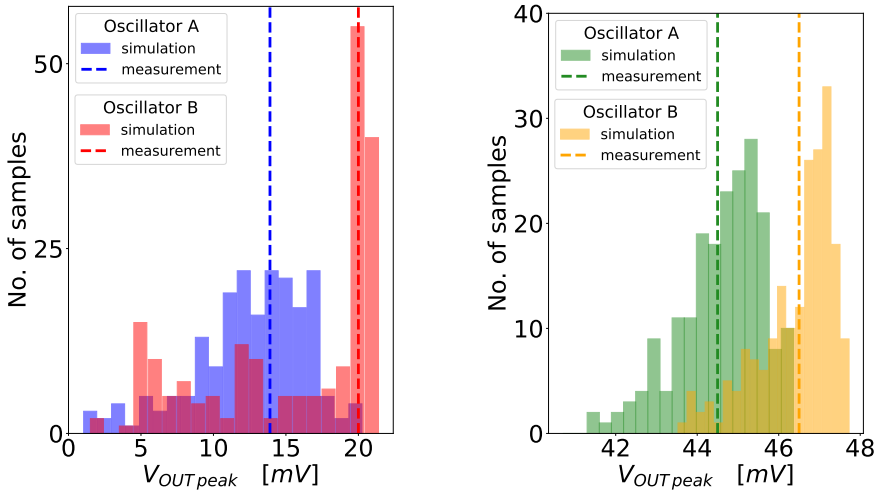


Figure 5.13: Monte Carlo simulation and measurement results for the amplitude of the output voltage of oscillators A and B for (a) 60 mV and (b) 90 mV supplies. The Monte Carlo simulations were run for 200 samples to obtain data on both the mismatch and the process variation.

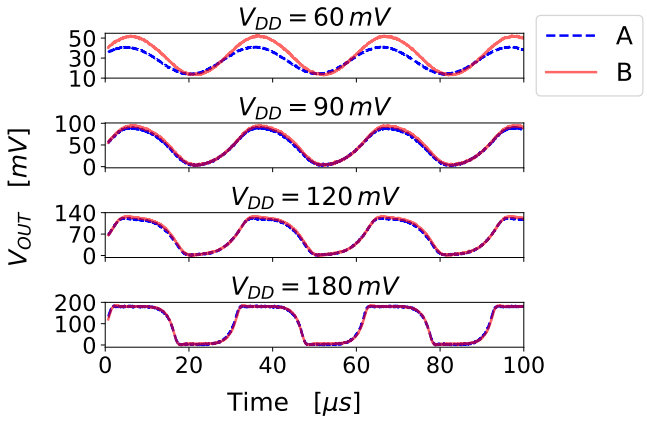


Figure 5.14: Measurement results for the output voltage with different supply voltages, V_{DD}, for oscillators A and B.

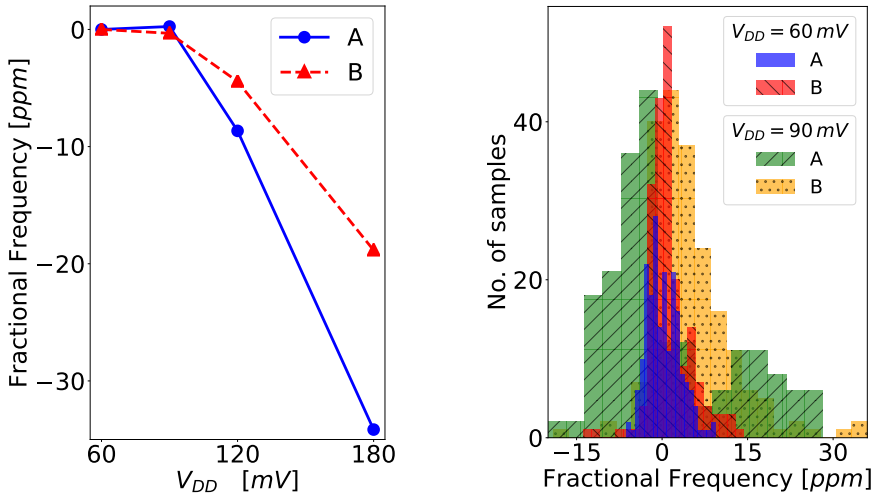


Figure 5.15: (a) Measurement results for the fractional frequency normalized to that obtained with a 60 mV supply for oscillators A and B, and its dependence on the supply voltage. (b) Monte Carlo simulation results for the normalized fractional frequency for oscillators A and B, with either 60 mV or 90 mV supply. Simulations were run for 200 samples to obtain both mismatch and process variation.

5.2.4 Oscillator frequency

The frequency of the oscillators was measured, by means of a frequency counter (Agilent 53230A) linked to a time source (Symmetricom 5071A primary cesium frequency standard). The measurement results for the two oscillators are shown in Fig. 5.15a. The fractional frequency was normalized to the frequency obtained with a 60 mV supply. For oscillators A and B, the fractional frequency varies only 0.251 ppm and 0.328 ppm, within the range from 60 mV to 90 mV supply, respectively. As a consequence, the fractional frequency has little dependence on the supply voltage within the range of interest where there is no hysteresis. As the hysteresis appears the frequency drops.

For reference purposes, the Monte Carlo simulation results are shown in Fig. 5.15b, where the normalized fractional frequency can be observed for both oscillators for supply voltages of 60 mV and 90 mV.

Fig. 5.16 shows the measurement results for the frequency stability for both oscillators operating with a 90 mV supply. Even though the temperature setup used allows for accurate temperature setting and measurement, the heating capability is limited to 62°C. Thus, the temperature was ramped from ambient temperature to 62°C within 4 h and back to ambient temperature over another 4 h, and the frequency was measured at a rate of once per second, obtaining as a result the shaded area in which the actual frequency stability falls. The same procedure was carried out to obtain measurements below ambient temperature. The curves for the typical values of the intrinsic instability of the used crystal resonators are

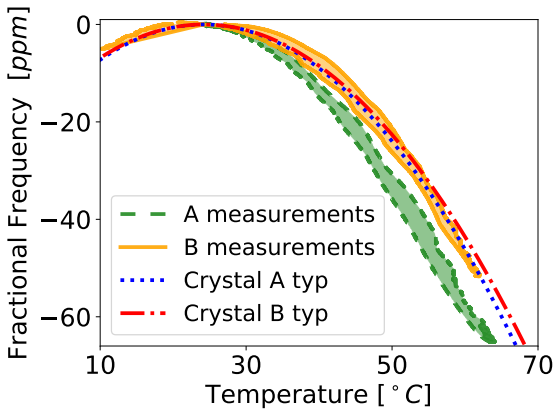


Figure 5.16: Measurement results for the fractional frequency normalized to that obtained at 26°C for circuits A and B with 90 mV supply, and its dependence on temperature compared to typical values of the intrinsic instability of the used crystal resonators (provided in the datasheets).

superimposed for reference. The frequency stability of oscillator B falls within the crystal specifications, indicating that the stability is not altered by the presence of circuit B. In the range of 5-62°C, a stability of 50 ppm is attained. On the other hand, oscillator A exhibits less frequency stability, as expected, due to the poor frequency trimming. In this case, the stability is 62 ppm within the range of 25-62°C.

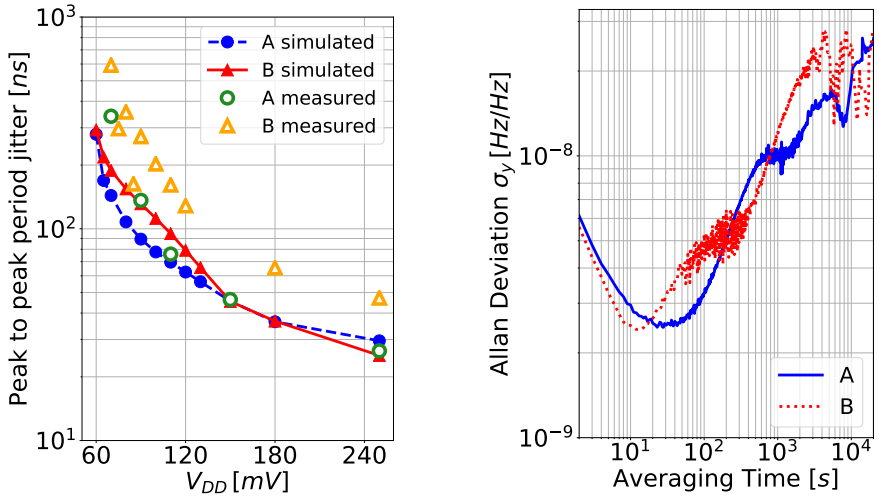
Time jitter was measured using a digital oscilloscope (Tektronix MSO5204). Peak to peak jitter measurements of oscillators A and B are shown next to simulation results in Fig. 5.17a. As the supply voltage increases the jitter decreases, as expected.

Measurement results of the Allan deviation for both oscillators are shown in Fig. 5.17. The measurements were taken with an averaging time of 1 s over 10 h, with a maximum temperature variation of 0.5°C. It can be seen that the Allan deviation is below 30 ppb for both oscillators.

5.2.5 Comparison against state-of-the-art

Table 5.1 summarizes the details for state-of-the-art ultra low voltage crystal oscillators of frequency 32 kHz and compares these to the results of this study.

To the best of our knowledge, the oscillators presented herein are the crystal oscillators for 32 kHz with the lowest operating voltage, working with only 60 mV. The closest prior works in terms of low supply voltage are [27] and [25]. [27] reports a minimum supply voltage of 100 mV in part of oscillator circuit, but requires also a second, higher, supply voltage, from 400 mV on. [25] operates down to 150 mV with a supply voltage drift well above all other reported values, remarkable power consumption, temperature stability and Allan deviation. The power consumption reduction is traded-off with a modification in the oscillator output waveform, which might degrade the frequency spectrum. Furthermore, it



(a) (b)

Figure 5.17: Results for the oscillator performance: (a) simulation and measurement results for time jitter versus supply voltage, and (b) Allan deviation measurements with a supply voltage $V_{DD} = 60$ mV.

needs a conventional crystal oscillator to start-up, requiring more area.

The power consumption of oscillator A is very well suited for ultra low power applications and in line with other state-of-the-art oscillators. Prior works with comparable ultra low power consumption are [28], [29], [25] and [27]. The drawbacks of [25] and [27] have already been discussed. In [28], a power consumption of 0.55 nW is achieved by means of downconverting the signal to DC, amplifying in DC and then upconverting the signal to the frequency of the crystal. An excellent phase synchronization is achieved providing excellent frequency stability over temperature and over time. The output waveform is the result of switching DC levels to obtain a four level switched signal, which will have important harmonic content. The output harmonic content would be filtered by the high quality factor of the crystal. Nevertheless, this might be an issue if spectral purity is needed. [29] reaches a minimum supply voltage of 300 mV while decreasing consumption by means of a sophisticated duty-cycling mechanism. However, a large silicon area is required and the Allan deviation is much larger than that attained in the present work. In order to further reduce the power consumption of a Schmitt trigger-based crystal oscillator, the parasitic capacitances should be lowered using smaller packaging rather than DIP40. Furthermore, a crystal specified for a lower load capacitance would reduce the power consumption. Reduction in packaging capacitances also allows a better tuning of the oscillator frequency in the case of oscillator A.

The approach described herein is also notable for the extremely small silicon area budget, using standard CMOS transistors within a widely used and inexpensive technology. This small area is due to the use of a standalone amplifier, with no calibration or auxiliary circuits needed to improve the power consumption or

frequency stability. Other designs shown in Table 5.1 are several times bigger, even those in more advanced technology nodes.

Table 5.1: Comparison to prior work

	[20]	[25]	[29]	[26]	[27]	[31]	[30]	[28]	This work	
									A	B
Technology	2 µm	28 nm	0.13 µm	0.18 µm	55 nm	40 nm	0.18 µm	65 nm	0.13 µm	0.13 µm
Area (mm^2)	N/A	0.03	0.0625	0.027	0.16	0.07	0.035	0.027	0.0033	0.0065
Frequency (kHz)	32.8	32.768	32.768	32.768	32.768	32.76	32.768	32	32.763	32.768
Crystal total load capacitance (pF)	8.2	N/A	3	N/A	N/A	N/A	2.23	7.5	3	12.5
Supply voltage (V)	0.71 - 1.7	0.15 - 0.5	0.3 - 0.9	0.25 - 0.5	0.1 - 0.5 0.4 - 0.8	0.5	0.4 - 5.5	0.5	0.06 - 0.1	0.06 - 0.1
Supply voltage drift (ppm/V)	N/A	∼83	7	N/A	6.7	1	2.1	13	8.4	11
Power consumption (nW)	23	1.89	1.5	2.89	1.7	47	10 nW@1V	0.55	2.26	15.0
Amplitude of oscillation (mV)	130	150	230	250	100	N/A	90	500	27.5	40
Start-up time	N/A	N/A	31 s	N/A	8 ms	N/A	1 ms	0.2 s	14.5 s	13.0 s
Temperature stability	N/A	48.8 ppm -20∼80°C	-150 ppm 0∼80°C	N/A	109.1 ppm -20∼80°C	0.25 ppm/°C @room temp	120 ppm -40∼85°C	80 ppm -20∼80°C	-62 ppm 25∼62°C	-50 ppm 5∼62°C
Allan deviation	N/A	∼2 ppb	90 ppb	N/A	2.5 ppb	N/A	N/A	14 ppb	30 ppb	30 ppb

The crystal oscillator in [27] is PLL-assisted and requires two different supply voltages. The two operating ranges are reported.
Crystal total load capacitance is the series of C_1 and C_2, including parasitic capacitances.
Amplitude of oscillation is peak to peak.
Amplitude of oscillation and power consumption are reported at the lowest operating supply voltage.
Unless stated otherwise, results are reported at room temperature.

Performance aspects, where other designs in Table 5.1 are better than this work, are start-up time ([27], [30]) and Allan deviation ([25], [27], which drawbacks were previously discussed). Regarding start-up time, [27] and [30] require much higher minimum operating voltage. Furthermore, the start-up time and the Allan deviation in the designs here presented are still within the range achieved or better than other state-of-the art works, as visible in Table 5.1.

Summing up, the designs shown in this work, provide record low operating voltage and a very compact implementation with competitive consumption and precision specifications (temperature stability, long term stability, supply voltage drift).

Chapter 6

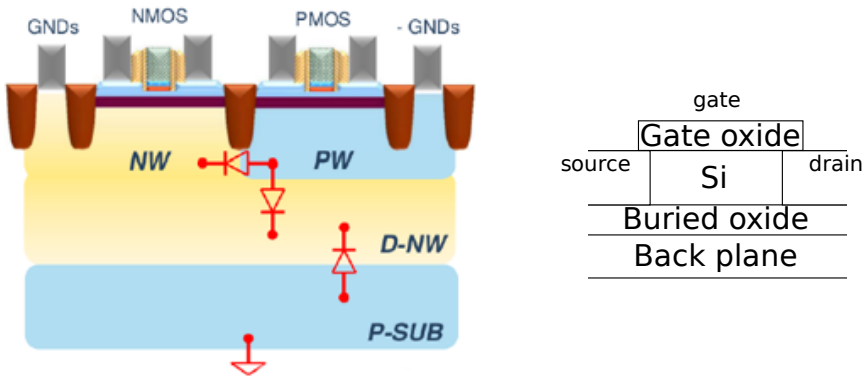
Low power LC voltage controlled oscillator

The LC voltage controlled oscillator (LC-VCO) presented in this chapter is designed using a 28 nm fully depleted silicon on insulator technology (FD-SOI). First, in Section 6.1, it is studied the possibility of using the basic all-region long channel MOSFET model aided with look up tables (LUTs), presented in Sections 2.1 to 2.4, to design the circuit in the 28 nm FD-SOI technology. In Section 6.2, the limit for the minimum supply voltage of an LC oscillator is studied, based on the aforementioned model. Finally, the design of the LC-VCO is presented in Section 6.3, and the simulation results are compared to the state of the art.

6.1 Modeling a nanometer FD-SOI transistor with a basic all-region MOSFET model

The capability to estimate circuit performance and explore the design space in all inversion regions of the MOS transistor is key for gaining insight and optimizing the design of analog and RF circuits. A widespread approach is based on the g_m/I_D method [43, 44]. When aiming at nanometer processes, the transistor characteristics may be captured on look up tables (LUTs) [44, 45]. In this way the complexity of second order modeling effects in nanometer processes, and in particular short channel effects, are dealt with by using different LUTs depending on the target transistor length (or range of lengths) and, in some cases, depending also on the bias drain voltage.

A step further from the pure LUT approach would be to have analytical expressions for the transistor model. In this way analytical derivations can be performed providing further insight and understanding in the design process. However, complete analytical models, including all second order effects, are not suitable for analytical circuit design due to their complexity. Here, an intermediate way is explored. Could the basic model presented in Section 2.1, coupled with a LUT that defines their parameters as a function of the transistor length, be applied to



(a) (b)

Figure 6.1: Cross section of the low V_T devices in the 28 nm FD-SOI technology used showing (a) the connections to the voltage terminals and (b) a diagram of the layers between the front gate and the back plane.

model an advanced nanometer process? Such basic model does not consider effects such as mobility reduction and velocity saturation that will be significant in the strong inversion (SI) region. Nevertheless, considering the very high transition frequency of short channel transistors in a nanometer process, for many analog and RF circuits, even for frequencies up to several GHz, the optimum operating point occurs in the moderate invertion (MI) or even weak inversion (WI) regions [43,44]. This is the case of ultra low power or ultra low voltage circuits, in particular for 2.4 GHz low noise amplifiers in a 90 nm process [46]. Therefore, an analytical model that allows to reasonably fit the transistor characteristics in WI and MI would be enough and useful in several cases.

The nanometer process considered is a fully depleted silicon on insulator (FD-SOI), ultra thin body and buried oxide (UTBB) 28 nm process. There are regular V_T and low V_T devices available. In the ultra low voltage context, the low V_T devices are preferred and are the ones selected here. The profile of the low V_T devices are depicted in Fig. 6.1a and a detailed diagram showing the layers between the front gate and the back plane is depicted in Fig. 6.1b. In Fig. 6.1a, the back plane voltage of the nMOS and the pMOS transistors are connected to ground, but can be connected to any voltage ranging from -0.3 V to 3 V and from -3 V to 0.3 V, respectively. The back plane voltage let the circuit designer tune the threshold voltage of the transistors in a wide range, as it will be seen in the case of the nMOS transistor in Section 6.1.1.

An additional challenge arises, since we will attempt to describe an FD-SOI device with a bulk MOS model. This challenge will be further discussed in Section 6.1.1. On the other hand, FD-SOI largely reduces short channel effects [47], which helps to make viable the approach discussed herein. The device performance for extraction of the model parameters and the assessment of model results is based on simulations performed with the foundry provided model in the Spectre simulator.

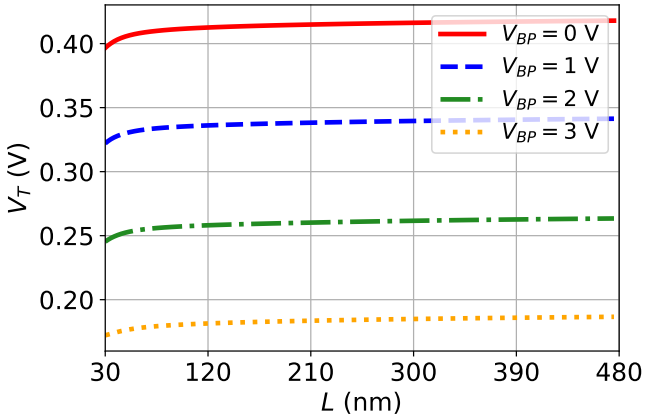


Figure 6.2: Results of the extraction of V_T, according to the g_m/I_D procedure, as a function of the channel length L of an nMOS transistor with a channel width W = 500 nm, for several values of the back-plane voltage V_{BP}.

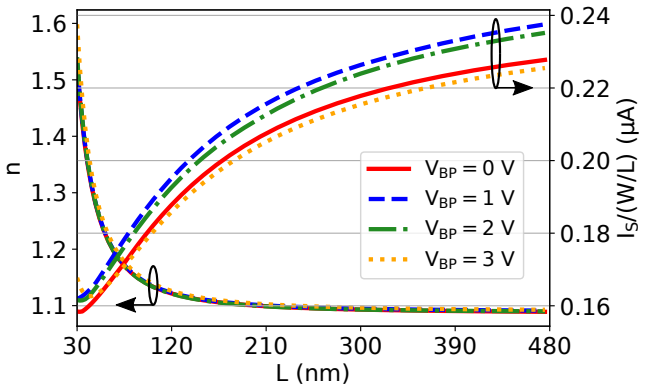


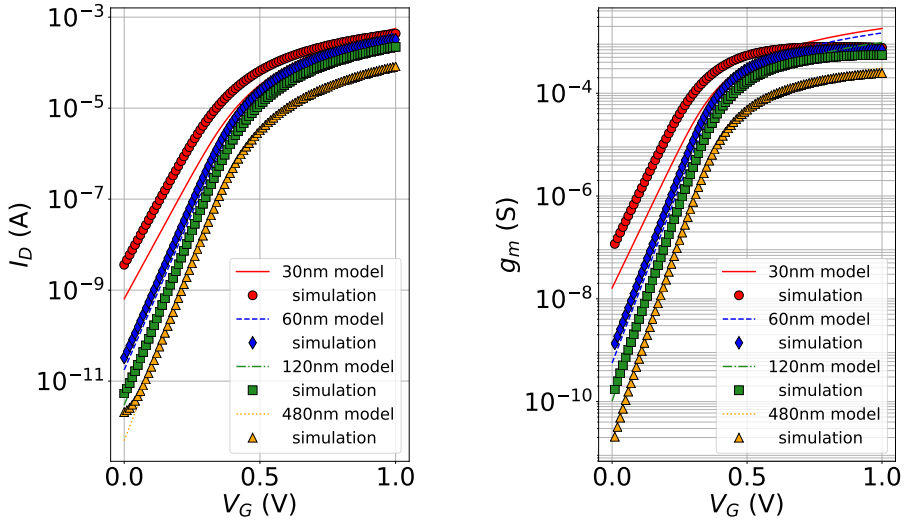
Figure 6.3: Results of the extraction of the normalized I_S and the slope factor n, according to the g_m/I_D procedure, as a function of the channel length L of an nMOS transistor with a channel width W = 500 nm, for several values of the back-plane voltage V_{BP}.

The results presented in Sections 6.1.1 and 6.1.2 are based on our work in [48].

6.1.1 Parameter extraction for FD-SOI nanometer device

In order to apply the bulk MOS transistor model to the FD-SOI device, we will consider the model with $V_S = 0$ (i.e. null source to bulk voltage). Equivalently, we are considering the gate and drain voltage of the FD-SOI transistor referred to the source. The slope factor n, the threshold voltage V_T and the specific current I_S are extracted using the procedure depicted in Section 2 for different values of the channel length (L) and the back plane voltage V_{BP} (also referred to the source). Results, for low V_T transistors, are shown in Figs. 6.2 and 6.3.

It can be seen in Fig. 6.3, that n has little variation with V_{BP}, as has been shown by prior works such as [49, 50], n is very high, up to 1.5, (i.e. the subthreshold



(a) (b)

Figure 6.4: Simulation and model results of (a) I_D and (b) g_m, for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

slope is degraded) for the minimum channel length but n decreases fast as the channel length increases, reaching typical values of FD-SOI of 1.1. The threshold voltage varies with V_{BP}, as expected [47] and has a slight dependence on the channel length, showing the improved (decreased) short channel effects in FD-SOI. Figure 6.3 shows the specific current, given in (2.2), divided by the aspect ratio. There is moderate variation with V_{BP} and a significant dependence on L.

6.1.2 Comparison of the model against simulations

An insightful case with the transistor in saturation, for $V_{DS} = 0.6$ V, was simulated and the results are compared to those obtained with the model. In Section 6.2 where the transistors operate with V_{DS} well below 0.6 V, the parameters that depend on V_{DS} are extracted for a suitable value of this voltage.

Figure 6.4a compares model and simulation for the I_D vs. V_G characteristic for several values of channel length L. Even though the I_D of a minimum channel length transistor (L =30 nm) is not well predicted by the model, it works fine for $L \geq 60$ nm. The same trend occurs with the transconductance in Fig. 6.4b.

Small signal parameters

Figure 6.5 shows g_m/I_D as a function of the normalized drain current. The model fits the simulations for all transistor lengths in all inversion regions except for deep weak inversion and deep strong inversion. The former, with $I_D/(W/L) < 10$ pA, where the leakage current dominates, making this region a very unlikely design choice. The latter, with $g_m/I_D < 6$ V^{-1}, exhibits a difference between the model

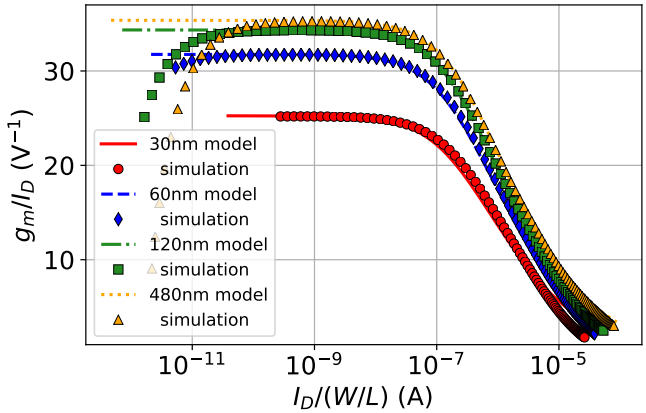


Figure 6.5: Simulation and model results of g_m/I_D for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

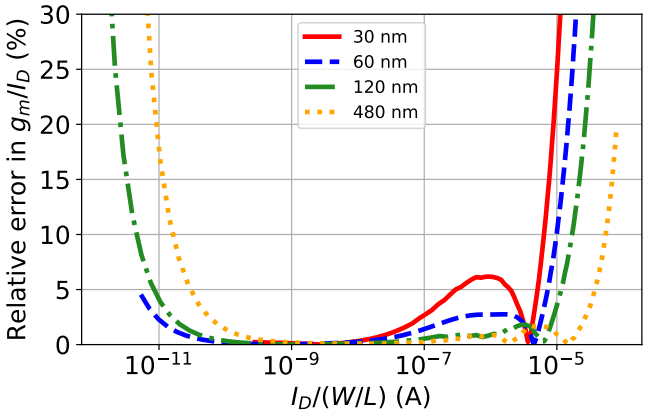


Figure 6.6: Relative error in g_m/I_D, between the model and the simulation results, for several values of L with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

and the simulation due to mobility reduction and velocity saturation.

The relative error in g_m/I_D, between the model and the simulations, is depicted in Fig. 6.6. It can be seen that the model provides a reasonable approximation (relative error less than 7 %) of the g_m/I_D characteristic of the full simulation model in WI and MI, for $g_m/I_D \geq 6$ V^{-1}.

The ratio g_m/I_D proves to be fairly independent of V_{BP}, as has been shown by prior works such as [49, 50], because of its independence on the threshold voltage. The simulation results depicted in Fig. 6.7 are consistent with this.

The considered basic model does not include the second order effects that define the output conductance. Therefore, in the proposed approach the output conductance will be considered fully based on a LUT of the I_D/g_{ds} ratio [44, 45], which can be interpreted as the Early voltage. This LUT will have as inputs L, V_{BP} and g_m/I_D (or alternatively $I_D/(W/L)$). The evolution of the I_D/g_{ds} ratio with L and V_{DS} is shown in Fig. 6.8 for an MI operating point. It can be seen that

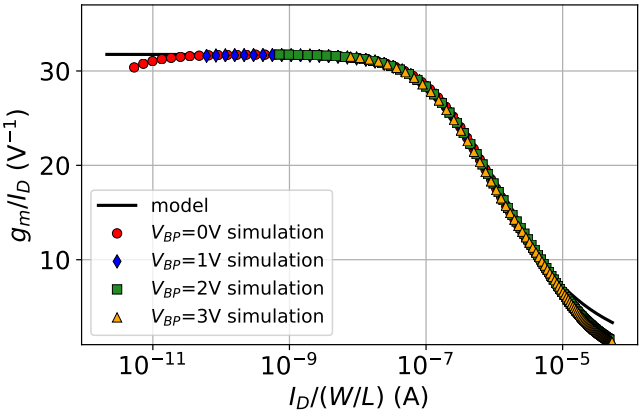


Figure 6.7: Simulation and model results of g_m/I_D for several values of V_{BP}, with $W = 500$ nm, $L = 60$ nm and $V_{DS} = 0.6$ V.

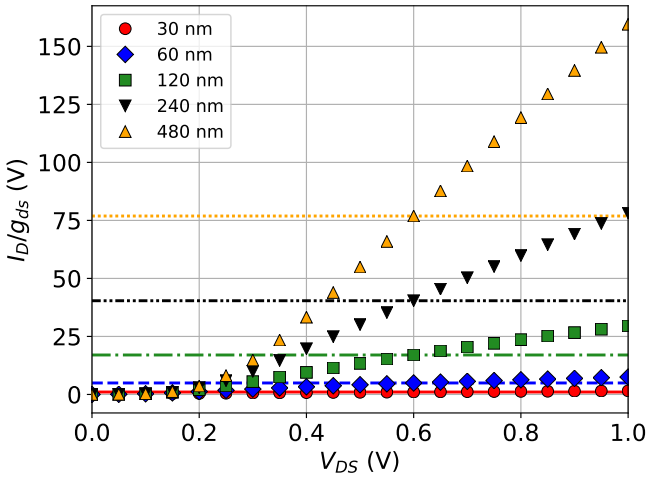
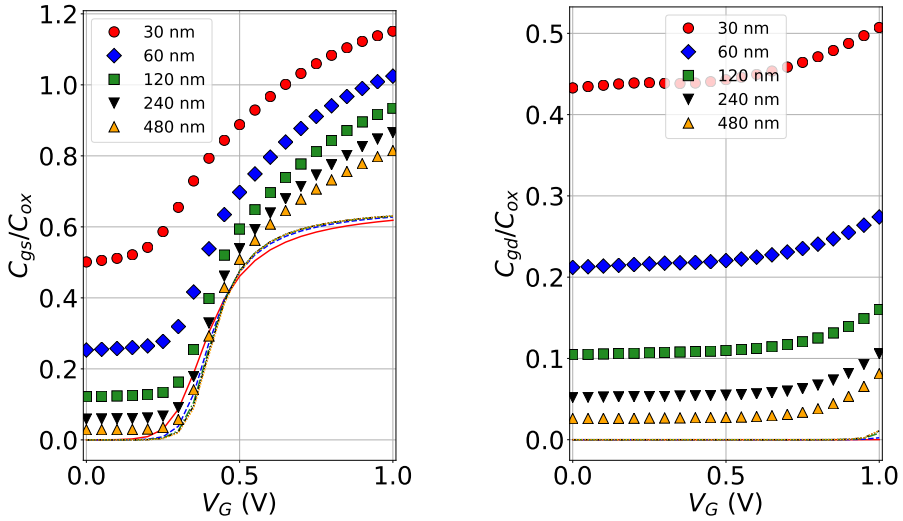


Figure 6.8: Simulation results of the Early voltage for several values of L, with $W = 500$ nm, $g_m/I_D = 15\ V^{-1}$ and $V_{BP} = 0$ V. The horizontal lines are the result of approximating the Early voltage at $V_{DS} = 0.6$ V.

taking a constant Early voltage extracted at a given V_{DS} (e.g. 0.6 V) would be only acceptable if the V_{DS} range is small. Otherwise the LUT should also consider the V_{DS} dependence.

Intrinsic small signal capacitances

In order to assess the performance of the modeling approach regarding the intrinsic small signal capacitances, the main components of the total gate capacitance are considered. These are: gate to source, gate to drain and gate to bulk. In the case of the gate to bulk capacitance of the model, it is associated to the gate to back-plane capacitance of the FD-SOI device. The expressions of these capacitances as



(a) (b)

Figure 6.9: Simulation (markers) and model (lines) results of the normalized intrinsic capacitances (a) C_{gs} and (b) C_{gd} for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

presented in 2.3 as a function of i_r and i_f lead to the results shown in Figs. 6.9a, 6.9b and 6.10a.

Note in Fig. 6.9b that C_{gd} is estimated by the model to be zero in saturation, since the effect of the drain voltage on the transistor charges is neglected in saturation in the basic long channel model. In the simulation results in Fig. 6.9b, it is noticeable that the effect of the drain voltage in saturation is very significant, particularly for shorter channels. This modeling limitation also impacts the other capacitances. This can be seen, either because the part of the channel charge in saturation controlled by the source changes or considering that the three components of the gate capacitance are related by (2.26d), rewritten here for convenience:

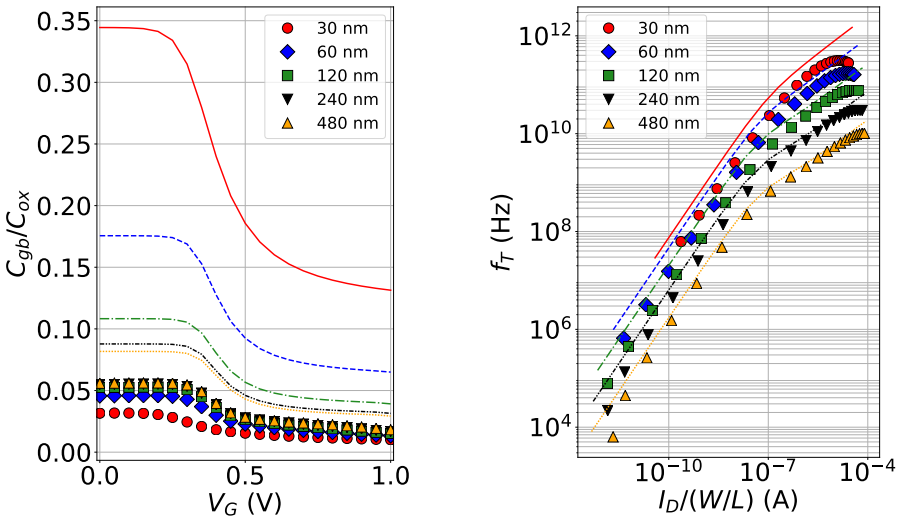
$$C_{gb} = \frac{n-1}{n}(WL\,C'_{ox} - C_{gs} - C_{gd}). \tag{6.1}$$

Furthermore, in this nanometer process, this relationship will be influenced by the change in the inversion charge depth in the Si film with bias voltage [47]. These effects mean a significant intrinsic C_{gd} and modified C_{gs} and C_{gb}. The overall result is that C_{gs} is underestimated and C_{gb} is overestimated.

Figure 6.10b shows the model predicted and simulated transition frequency.

6.2 Study of the minimum operating voltage limit

The minimum possible supply voltage to enable oscillation is studied herein in the case of an LC cross-coupled oscillator. Figure 6.11 shows the circuit schematic of



(a) (b)

Figure 6.10: Simulation (markers) and model (lines) results of (a) the normalized intrinsic capacitance C_{gb} and (b) the transition frequency f_T, for several values of L, with $W = 500$ nm, $V_{DS} = 0.6$ V and $V_{BP} = 0$ V.

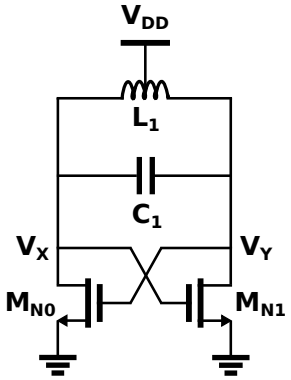


Figure 6.11: Circuit schematic of an LC cross-coupled oscillator.

such oscillator. Each transistor introduces 180° shift, so two transistors suffice for oscillation [51].

This voltage biased topology is more suitable for ultra low voltage operation than a current biased topology, since the transistors in the current mirror would not saturate. In addition, the voltage biased topology is useful in the ultra low voltage context, since the circuit is only connected to the supply voltage, V_{DD}, through the inductor. Therefore, the DC voltage is directly supplied to the transistors and the output may swing well above V_{DD} [52].

Here the oscillator is designed to operate with the least supply voltage. To this aim, the inductor chosen from the library must have the highest quality factor Q. The parasitics of the inductors available in the library are extracted to conveniently

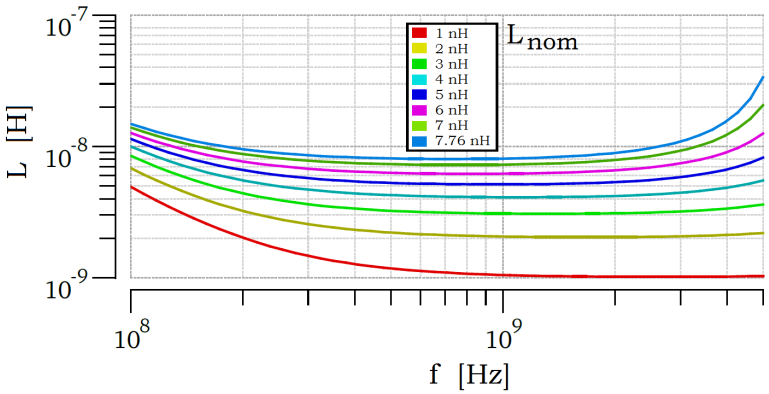


Figure 6.12: Inductance value as a function of frequency of a given inductor in the library with 11 µm coil width.

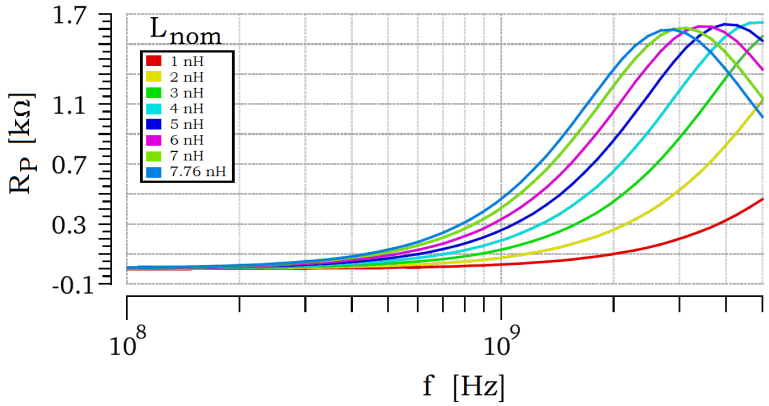


Figure 6.13: Parasitic resistor as a function of frequency of a given inductor of the library with 11 µm coil width.

choose the inductor and the oscillation frequency. The capacitance C_1 must be adjusted to attain that frequency. Finally, the transistors are designed.

6.2.1 Design of the inductor

There are four kinds of inductors available in the library. The achievable inductance values using the single turn coil are in the range from 0.091 nHy to 1.2 nHy, while using the multi turn coils the achievable values are in the range from 0.61 nHy to 7.76 nHy. These two kinds (single and multi turn coils) have their differential and non-differential version. Here the differential multi turn coils are chosen, to use higher values of inductors that achieve a higher Q.

The parameters of the inductors in the library were extracted for several values of the intended nominal inductance. The results are plotted in Figs. 6.12 to 6.14, as a function of frequency.

The maximum value of the quality factor Q increases with frequency, as seen in Fig. 6.14, which is why the oscillation frequency is chosen to be 2.45 GHz.

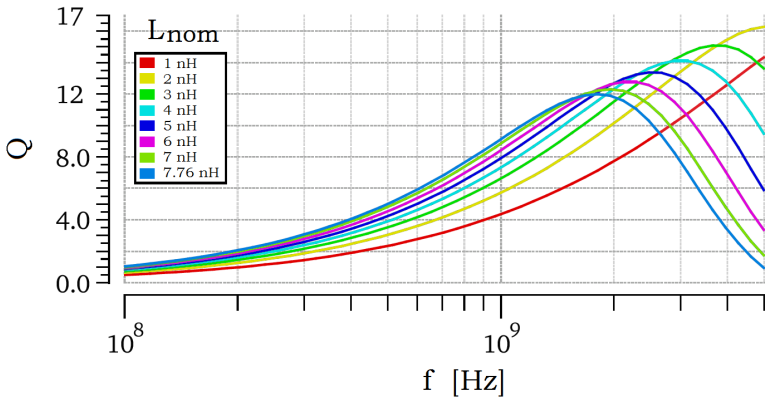


Figure 6.14: Quality factor as a function of frequency of a given inductor of the library with 11 µm coil width.

Consequently, the inductor value will be 6 nHy because it gives maximum Q at 2.45 GHz, with $R_P = 1.3\,\mathrm{k\Omega}$ and $C_P = 0.4$ pF.

The coil width used in these simulations is 11 µm, as stated in the caption of Figs. 6.12 to 6.14. Moreover, the dependence of the coil parameters on its width is negligible, according to simulations (omitted here).

6.2.2 Design of the transistors for minimum supply voltage

The lvtnfet devices are the nMOS transistors of choice, since these have a lower threshold voltage.

To minimize the capacitance contribution, the minimum channel length is used (following some of the suggestions in Section 8.8 of [52]). The width of the transistors must enable start-up for a given supply voltage, V_{DD}. Choosing the minimum width that enables start-up, provides the lowest power oscillator feasible using this topology. Both transistors are implemented as an arrangement of parallel transistors of unit width $W = 160$ nm.

The Barkhausen oscillation condition reduces to

$$g_m \geq \frac{2}{R_P} + g_o, \tag{6.2}$$

where g_m and g_o are the transconductance and the output conductance of either transistor, respectively. Both are calculated around the DC operating point $V_X = V_Y = V_{DD}$.

The output conductance is related to the Early voltage, V_A, giving

$$g_o = \frac{I_D}{V_{DS} + V_A}. \tag{6.3}$$

Then, the oscillation condition simplifies to a condition on the drain current

$$I_D \geq \frac{\frac{2}{R_P}}{\frac{g_m}{I_D} - \frac{1}{V_{DD}+V_A}}. \tag{6.4}$$

Table 6.1: Simulation results of the oscillator for different values of the supply voltage V_{DD}.

V_{DD} (mV)	Fingers	I_D (µA)	V_{xpp}/V_{DD}	Phase noise (dBc/Hz) @ 1 MHz offset
150	2750	53	1.57	-108.2
200	500	42	1.625	-107.6
250	130	44	1.54	-105.2

where $g_m/I_D = 25.8\ \mathrm{V}^{-1}$, according to the extraction for $L = 30$ nm in Fig. 6.5. Besides depending on L, V_A strongly depends on the drain voltage (here $V_{DS} = V_{DD}$) as discussed in Section 6.1.2, which is unknown at this stage. Nevertheless, V_A is approximated by its value at $V_{DD} = 150$ mV, giving $V_A = 85.2$ mV. If the resulting V_{DD} is far from the first estimated value, the value of V_A must be corrected in the loop. Thus, the oscillation condition is $I_D \geq 60\,\mu\mathrm{A}$.

Since in DC $V_{GS} = V_{DS} = V_{DD}$, the drain current depends only on the extracted parameters, W and V_{DD}, following (2.10). Thus, to find the minimum value of V_{DD}, the maximum value of W must be selected, provided that the parasitic capacitances do not disable oscillation. Through simulations, the minimum value of V_{DD} at $f = 2.45$ GHz is found to be 150 mV, where the two nMOS transistors are implemented with a parallel arrangement of 2 750 transistors each (total width 440 µm each). The simulation result of the drain current of each of the equivalent transistors is $I_D = 53\,\mu\mathrm{A}$, which is slightly below but close enough the calculated limit.

The output voltage amplitude at V_X is 236 mV peak to peak (equal to $1.57 \times V_{DD}$).

The oscillation condition does not depend explicitly on the supply voltage, but through the parameters which depend on the voltage biasing. Table 6.1 shows the simulation results of the lowest power oscillator attainable with the nMOS cross-coupled topology, for different values of V_{DD}. The results listed are: the number of transistors in each parallel arrangement (fingers), the drain current of the equivalent transistor, the output swing as a proportion of the supply voltage and the phase noise at 1 MHz offset frequency. For reference, the phase noise required by the IEEE 802.15.4 standard is at least -88 dBc/Hz [53], being in most of cases around -110, -120 dBc/Hz.

Impact of the back-plane voltage on the performance

If the back-plane of the transistors is biased with 3 V, which is the maximum possible value, the minimum supply voltage decreases to $V_{DD} = 50$ mV. Table 6.2 shows the simulation results of the lowest power oscillator with back-plane biasing.

With the back-plane biasing, the parameters of the transistors change. For instance for V_{DD} =150 mV, $g_m/I_D = 14.7\ \mathrm{V}^{-1}$, this is 56 % of its value without back-plane biasing. However, the Early voltage remains almost the same, being $V_A = 150$ mV with back-plane biasing. The variation of g_m/I_D implies a greater

Table 6.2: Simulation results of the oscillator with back-plane biasing for different values of V_{DD}.

V_{DD} (mV)	Fingers	I_D (µA)	V_{xpp}/V_{DD}	Phase noise (dBc/Hz) @ 1 MHz offset
50	703	184	0.830	-94.1
100	118	136	0.922	-102.2
150	47	160	1.07	-103.7
200	26	200	0.985	-104.4

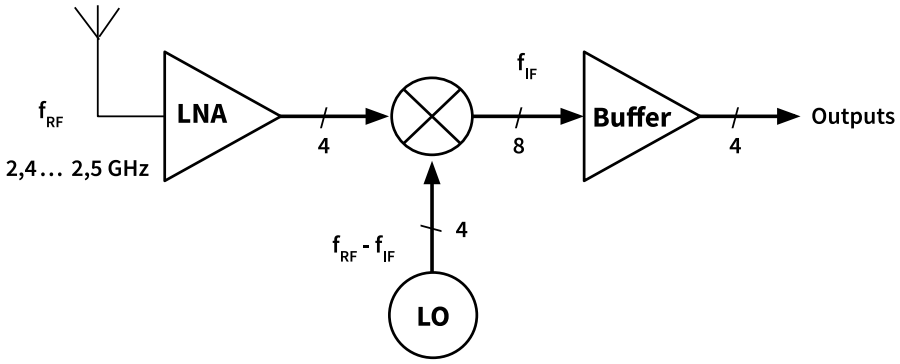


Figure 6.15: Block diagram of the RF receiver.

current is required for oscillation to take place, this is $I_D \geq 107\,\mu A$.

The process variability will be analyzed in the case of the designed VCO in Section 6.3.1.

6.3 Low power voltage controlled oscillator

A voltage controlled oscillator (VCO) is designed to be the local oscillator (LO) of the RF receiver in Figure 6.15.

A four path mixer is used, thus the LO must provide four signals with a 90 °C phase shift from one another. The frequency of these four signals must be tuned in the range from 4.8 GHz to 5.0 GHz with the lowest power consumption possible. Thus, the intermediate frequency f_{IF} is zero. The phase noise should be lower than -88 dBc/Hz at 1 MHz offset frequency, to prove useful according to the standard IEEE 802.15.4.

6.3.1 Design and simulations of the VCO

In the ultra low voltage context, it proves difficult to generate phase and quadrature signals, due to the lack of a well functioning current source, as it is one of the building blocks of this kind of circuits. For this reason, a VCO operating at the

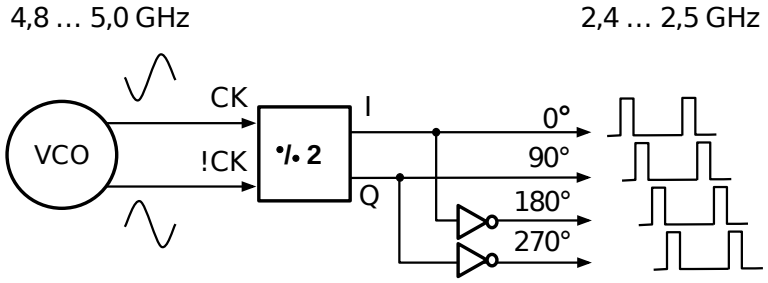


Figure 6.16: Block diagram of the local oscillator, including the VCO and the divider by two, to obtain the four signals with 90 °C phase shift.

double of the nominal frequency will be connected to a divider by two block, to obtain the phase and quadrature signals at the nominal frequency. The block diagram is shown in Fig. 6.16.

The divider by two block is implemented by means of an asynchronous state machine. The logic gates loading the VCO are inverters biased with a supply voltage of 0.5 V and a symmetric back-plane voltage of $V_{BPn} = 2$ V and $V_{BPp} = -2$ V. The low-Vt transistors sizes are: $L = 30$ nm, $W_N = 80$ nm and $W_P = 260$ nm. Even though the back-plane voltages are out of the range defined by the supply voltage of the inverters, the current drawn is very small since the nodes are only capacitively loaded. Thus, these DC voltages can be obtained by means of a voltage step-up.

As a consequence of selecting a higher oscillation frequency, the quality factor of the inductors within the library is higher, according to Fig. 6.14. A higher quality factor enhances the performance of the oscillator. Thus, the inductor of choice to operate at 4.8 GHz to 5 GHz is $L = 4$ nHy, thus, achieving the highest parallel resistance R_P.

The architecture of the VCO is an LC cross-coupled nMOS, as it is the LC oscillator used to discuss the limit for the supply voltage in Section 6.2. Here, a differential varactor is added to tune the oscillation frequency. Figure 6.17 shows the circuit schematic of the VCO.

It is seen from the g_m/I_D results in Fig. 6.5, that the longer the channel length, the higher g_m/I_D in WI region, however increasing the parasitic capacitances. Therefore, the length of the unit transistor is chosen to be 60 nm, as g_m/I_D is already significantly higher than that of a minimum channel length transistor.

In the quest for the minimum supply voltage, the results obtained in Section 6.2 are such that the parasitic capacitances dominate. Moreover, the choice of $L = 60$ nm rather than 30 nm also contributes to increasing the parasitic capacitances. In addition, the VCO is loaded with the divider by two block. Therefore, the tuning range in that case would be very small. It was verified through simulations that the minimum supply voltage to tune the VCO in the range from 4.8 GHz to 5 GHz is $V_{DD} = 250$ mV.

The capacitor C_1 is implemented with a metal over metal (MoM) capacitance available in the library. The varactor C_V is also implemented using a cell from

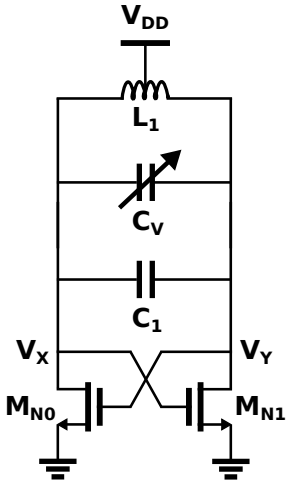


Figure 6.17: Circuit schematic of the LC cross-coupled voltage controlled oscillator.

the library. C_1 and C_V are selected such that the oscillation frequency is 4.8 GHz, the lower limit of the specified range, while the control of the varactor is 0 V. As a result, $C_1 = 4.4$ fF implemented with 10 devices in parallel with 10 fingers of length and width.

Also, C_V must be such that, with a control voltage of at most 1.8 V, the oscillation frequency is 5 GHz, the upper limit of the specified range. As a result, C_V is implemented with 5 fingers of 1.5 µm of length and width, attaining up to 104 fF at a control voltage of 1.8 V. The oscillation frequency is 5 GHz with a control voltage of 0.7 V. The current supplied to the varactor from the 0.7 V source is very small and the variations required are very slow. Thus, it can be handled in the same way as the back-plane voltage supplies.

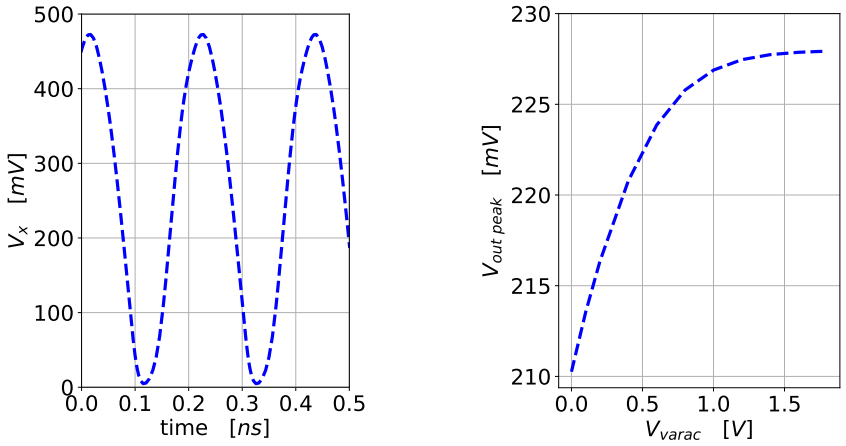
Figure 6.18a shows the transient simulation results of the output voltage at node V_x of the oscillator, with the control voltage of the varactor connected to ground, this is $V_{varac} = 0$ V. The amplitude of the output voltage V_x (which is the same as V_y) is depicted in Fig. 6.18b as a function of V_{varac}. Therefore, 40 mV and 460 mV must be valid low and high input levels of the divider by two block.

The frequency tuning range is depicted in Fig. 6.19a, where it is seen that, by setting $V_{varac} =$ from 0 V to 0.7 V, the oscillation frequency is tuned from 4.8 GHz to 5 GHz. Also, it is seen that frequency is linearly dependent of V_{varac} within the specified tuning range.

Figure 6.20 shows the simulation results of the phase noise of the VCO. The phase noise at 1 MHz offset frequency is presented in Fig. 6.20b, showing that the phase noise is below -90 dBc/Hz in the whole frequency range.

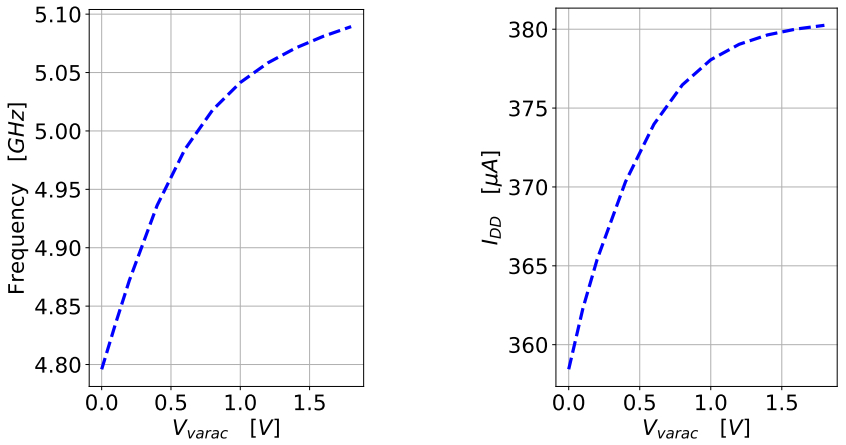
Montecarlo simulations of the VCO

Montecarlo simulations were run to account for process and mismatch variations in all of the circuit components. The results are shown in Fig. 6.21 for $V_{varac} = 0$ V to obtain an oscillation frequency of 4.8 GHz. For $V_{varac} = 0.7$ V to obtain an



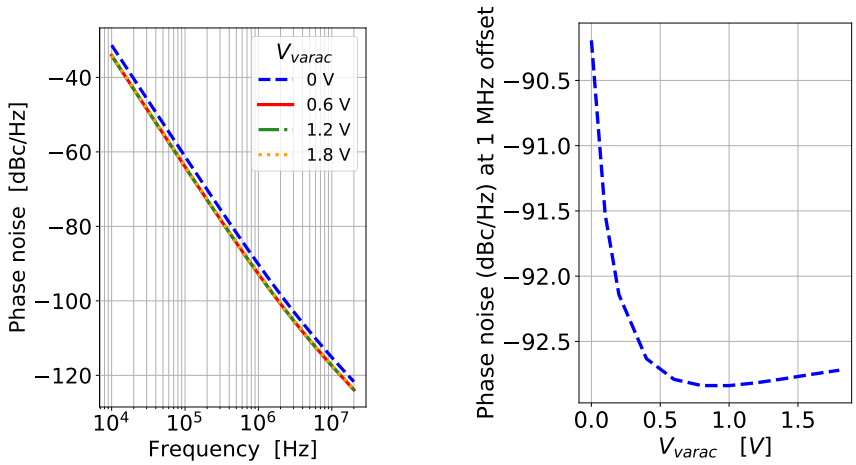
(a) (b)

Figure 6.18: Simulation results of the output voltage of the VCO: (a) transient results for $V_{varac} = 0$ V and (b) amplitude of the output voltage (V_x), as a function of V_{varac}.



(a) (b)

Figure 6.19: Simulation results of (a) the oscillation frequency and (b) the current consumption, as function of V_{varac}.



(a) (b)

Figure 6.20: Simulation results of the phase noise of the VCO (a) over frequency, for several values of the voltage control of the varactor, V_{varac}, and (b) at 1 MHz offset, as a function of V_{varac}.

oscillation frequency of 5 GHz, the results are shown in Fig. 6.22. As expected from the simulations in the typical corner, the performance enhances and the current consumption increases at higher frequencies. However, the current consumption is at most 382 µA in the worst case within the 200 samples at 5 GHz. The amplitude of the output voltage of the VCO is in most of the samples over 200 mV, according to Figs. 6.21a and 6.22a. Therefore, 50 mV and 450 mV must be valid low and high input levels of the divider by two block, respectively.

6.3.2 Comparison of the designed VCO to prior works

Table 6.3 summarizes the key parameters of the two lowest power VCOs in the state of the art to operate at frequencies close to 4 to 5 GHz (to make a fair comparison), these are [54] and [55].

In addition, Table 6.3 includes two low power quadrature VCOs, [56] and [57], which provide phase and quadrature outputs as is the case of the VCO presented herein cascaded with the divider by two block.

The lowest power consumption is that of the VCO presented herein, although the results in [55] are very close. The high power consumption of [56] and [57] is mainly due to the wide tuning range and low phase noise.

On the other hand, the phase noise is very high when compared to the state of the art. Some remarks on how to lower the phase noise are discussed in Section 6.3.3.

The figure of merit (FoM) included in Table 6.3 is defined as follows [51]

$$FoM = \frac{(\text{Tuning Range})^2}{\text{Power Dissipation} \times \text{Phase Noise} \times (\text{Offset Frequency})^2}. \tag{6.5}$$

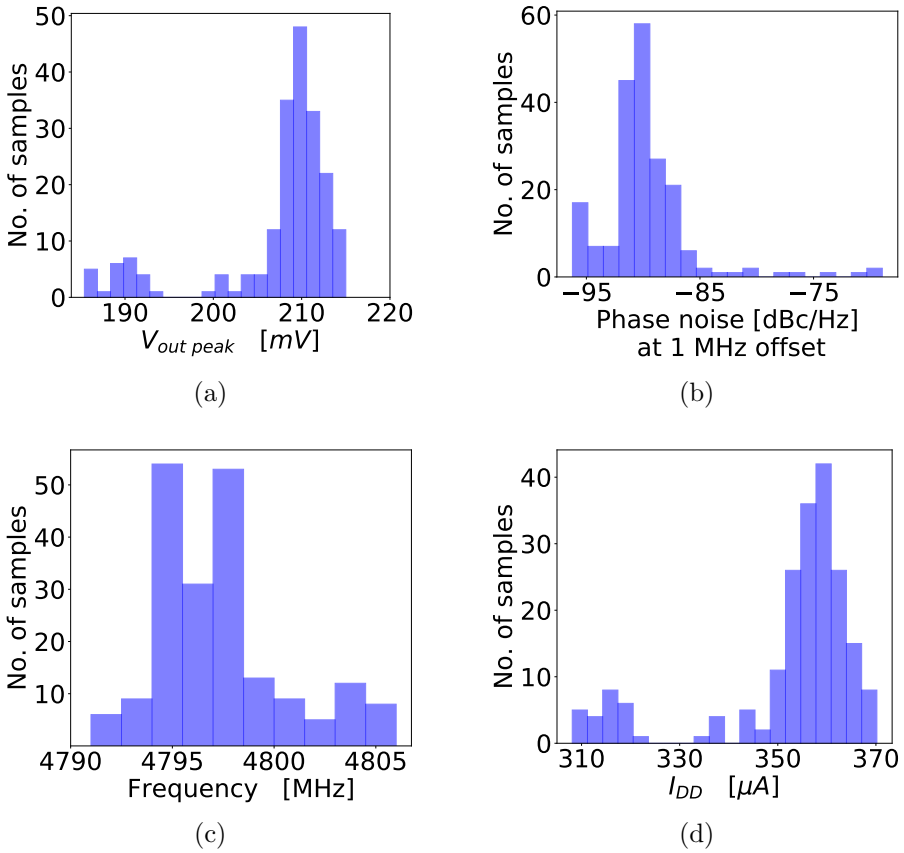


Figure 6.21: Montecarlo simulation results of (a) the amplitude of the output voltage, (b) the phase noise at 1 MHz offset, (c) the oscillation frequency and (d) the current consumption, with $V_{varac} = 0$ V.

Table 6.3: State-of-the art of low-power LC VCOs

	[54]	[55]	[56]	[57]	This work
Frequency (GHz)	5.14-5.44	2.35-2.37	6.98-6.54	1.55-1.67	4.80-5.00
Supply (V)	0.39	0.41	0.35	0.6	0.25
Power (mW)	0.468	0.1	3.4	1.32	0.09
Phase noise (dBc/Hz) at 1 MHz offset	-104.41	-107.2	-108.1	-118.6	-90.2
FoM (dB)	187	173	186	189	177
Process (nm)	130	130	130	40	28

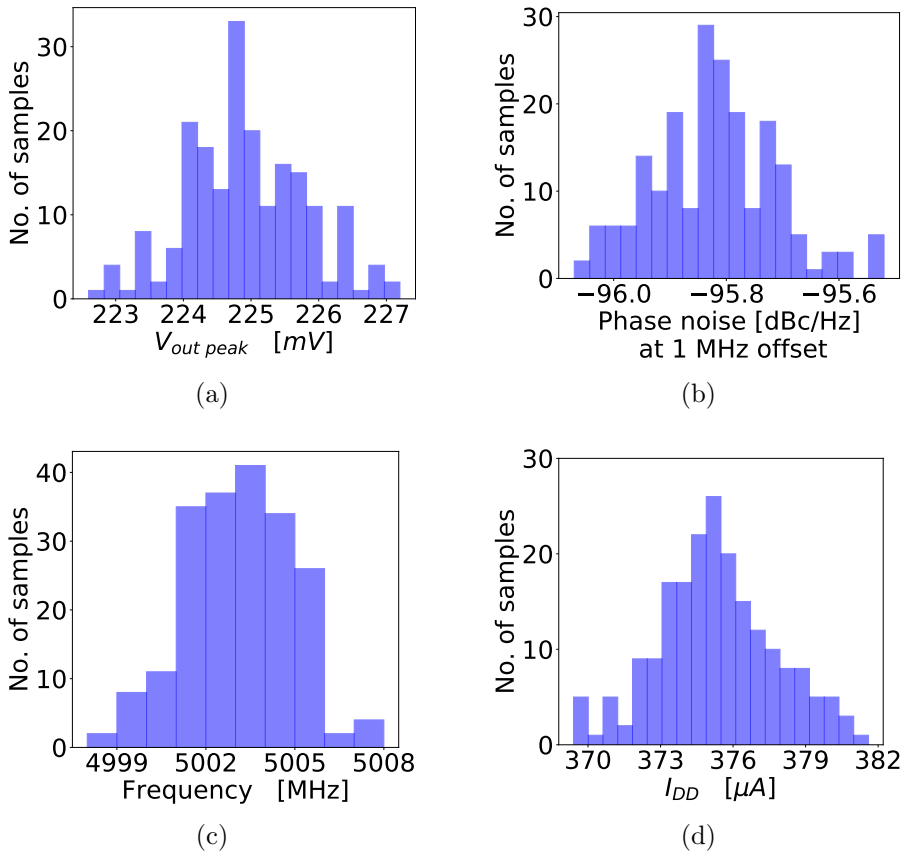


Figure 6.22: Montecarlo simulation results of (a) the amplitude of the output voltage, (b) the phase noise at 1 MHz offset, (c) the oscillation frequency and (d) the current consumption, with $V_{varac} = 0.7$ V.

In spite of the poor phase noise, the FoM of the VCO presented here has a low yet intermediate value, being higher than that of [55].

6.3.3 How to reduce phase noise

As it was seen in Table 6.3, the phase noise of the present work is higher than the VCOs in the state of the art. If the application requires lower phase noise, the circuit design may be modified to this aim in trade of current consumption.

By means of increasing the number of fingers in the nMOS transistors, the phase noise reduces but also the current consumption increases. Moreover, the MoM capacitor must be reduced in order to keep the same oscillation frequency. It was verified through simulations that, to reduce the phase noise by 3 dB in all the tuning range, the number of fingers of the nMOS should be 700 (instead of 500). In addition, to keep the tuning range, the MoM capacitor should have 4 devices in parallel (instead of 10). Figure 6.23 shows the simulation results of this lower phase noise version of the VCO and the VCO considered in Section 6.3.1.

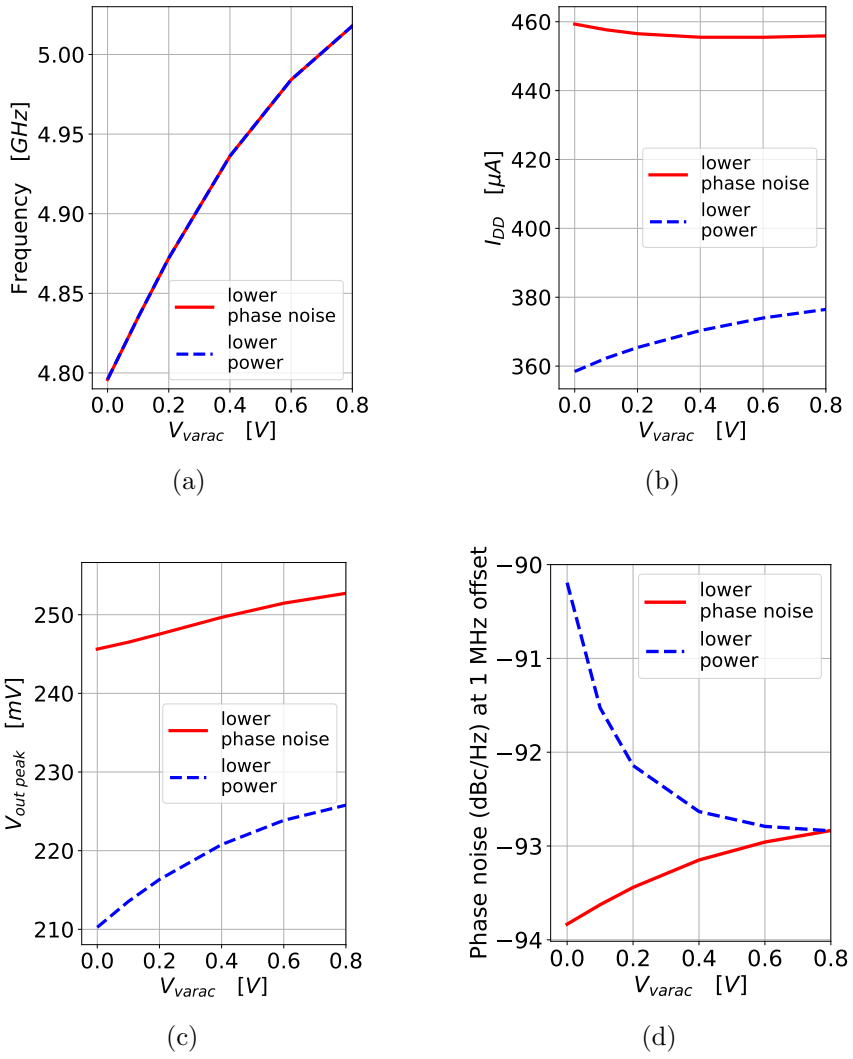


Figure 6.23: Comparison between the low power solution and a lower phase noise solution, through the simulation results of (a) the oscillation frequency, (b) the current consumption, (c) the amplitude of the differential output voltage and (d) the phase noise at 1 MHz offset, in the tuning range.

Figure 6.23c shows that the output voltage amplitude increases, with respect to the VCO presented in Section 6.3.1, which jeopardizes the compatibility with the divider by two block, since the latter has a 0.5 V supply. The phase noise reduction is verified according to Fig. 6.23d.

The tuning range is kept the same, as seen in Fig. 6.23a. As a result of adding fingers to the nMOS transistors, the current consumption increases as seen in Fig. 6.23b. The trend in the current consumption changes consistently with the behaviour of the phase noise in Fig. 6.23d.

It was verified through simulations that further lowering the phase noise is not possible by means of adding more fingers to the transistors. Also, the design space is limited in the direction of adding fingers, since soon the parasitic capacitances dominate and the tuning range starts narrowing.

On the other hand, increasing the supply voltage as a strategy to reduce the phase noise is futile and prohibitively increases the power consumption, according to the study on the minimum supply voltage in Section 6.2. This is the case in [54], where the core circuit topology is the same as the one presented here, and the phase noise obtained is -104.41 dBc/Hz at 1 MHz offset with over 5 times the power consumption.

Therefore, to pursue a qualitatively lower phase noise result as well as a small power budget, a different circuit topology should be used. The cross-coupled topology with a tail current source is the usual choice to reduce phase noise, and is the case of [45] and [55]. However, in the ultra low voltage context a current mirror does not achieve the performance required, since the transistors in the current mirror would not saturate. A tail inductor, connected between the source of the transistors and ground, may be a possible solution.

Chapter 7

Conclusion

An approach to ultra low voltage circuits based on the six transistor Schmitt trigger topology is assessed.

The operation of the Schmitt trigger as an amplifier is studied and guidelines for designing this block to be the amplifier of a crystal oscillator are provided.

It was thoroughly analyzed how the losses of the amplifier should be taken into consideration when designing a Pierce crystal oscillator. The equations to account for these losses, as well as the hypotheses required, are provided.

The design, simulation and measurement results for two crystal oscillators, using a 130 nm bulk CMOS technology, are presented herein. The amplifiers A and B were experimentally characterized, providing a gain of 2.48 V/V with a 60 mV power supply. The oscillators operate with the lowest reported supply voltage of only 60 mV while providing temperature and long-term stability competitive with respect to state-of-the-art ultra low voltage crystal oscillators. Oscillator A exhibits a power consumption in line with the best state-of-the-art oscillators previously reported.

Both oscillators are suitable for operating by means of the ultra low voltage energy harvesting sources described in Chapter 1.

When it comes to operating with less than 100 mV, the Schmitt trigger proves to be very effective and suitable for implementing crystal oscillators. The high gain of the Schmitt trigger, that enables CMOS electronics at such low voltages, entails high current consumption. Thus, the hysteresis voltage must be designed for the particular supply voltage of use in order to be as power efficient as possible.

If higher voltages are available, the CMOS inverter is likely to be a better choice in terms of power efficiency but depends on the application.

A high frequency dynamic model of the Schmitt trigger circuit in WI region is developed. The capacitive coefficients and the main parameters, that describe the operation of the Schmitt trigger with hysteresis, are modeled and verified through simulations. The dynamic model provides insight on the behavior of the circuit with and without hysteresis, as well as the equations to carefully size the transistors according to the specifications required by the targeted application.

The basic, long channel, bulk transistor model applied to design the Schmitt trigger circuits in a 130 nm technology, is also applied to designing an RF oscillator

in a 28 nm FD-SOI technology. Moreover, the parameters of the transistors are extracted using the same procedure and building LUTs in the same way. When applied to 28 nm FD-SOI, the model proved to be a very accurate way of describing the g_m/I_D curve in the MI and WI regions. This was achieved even for minimum length transistors. This approach coupled with an LUT approach for the output conductance provides the main small signal model for design.

In an RF application using the 28 nm FD-SOI technology, as in the case of the Schmitt trigger, this model with LUTs approach proved to be advantageous to understand the trade-offs and the relationships between the variables involved, as well as finding optimums. The theoretical limit for the minimum supply voltage that enables oscillation is studied in the case of a cross-coupled nMOS LC oscillator for 2.4 GHz, by means of the aforementioned model and LUTs approach, with the aid of simulations. Furthermore, it is verified through simulations that the power consumption is effectively lowered by means of using the lowest supply voltage possible, and that the phase noise of the oscillator is not degraded in this scenario.

Finally, a voltage controlled oscillator (VCO) is designed, with the same architecture (cross-coupled nMOS LC), tuneable from 4.8 GHz to 5 GHz and followed by a divider by 2, to obtain a VCO in the 2.4 GHz to 2.5 GHz band. The performance of the VCO is obtained through simulations.

The ultra low voltage approach is the best choice when the available sources to harvest energy are as small as 100 mV. It is important to bear in mind that this approach does not aim for the most power saving solutions but feasible and functional electronics in such a hostile context. If there are higher voltage sources available, such as 0.25 V, power can be saved by means of lowering the voltage supply but to an intermediate extent. This is the case of the VCO presented in Chapter 6.

7.1 Future work

A more compact version of the crystal oscillator could be obtained by means of integrating the feedback resistor and the load capacitances along with the amplifier. The design of the feedback resistor raises a challenging design aspect, since the resistor needs to have a very high yet not precise value. Moreover, it has not been addressed yet, to the best of our knowledge, whether the resistor being as high as possible is in fact convenient. Thus, an interesting future work would be to identify the trade-offs involved in the design of the resistor. As for the integration of the load capacitances, the main challenges are the correct estimation of the parasitic capacitances of the packaging and the adequate design of the PCB to have an overall load capacitance as precise as possible. The load capacitance being precise, has a direct impact on the resulting frequency of the oscillator, because without any off-chip capacitances the tunability is lost.

A small harvester could be built to test the crystal oscillators as a building block of a system. The energy harvesting source could be chosen among the options discussed in Chapter 1. The interface between the harvesting source and the oscillator should be designed to guarantee the operation of the oscillator. In

order to make a practical ultra low power solution, the amplifying stage proceeding the oscillator should be carefully designed.

Regarding the use of the long channel bulk transistor model applied to the 28 nm FD-SOI technology, the intrinsic capacitances remain to be properly modeled. The difference in the geometry of the bulk transistor and the SOI transistor deserve studying whether the model is still useful if the equations of the capacitances are modified to adequate to the physics of the SOI transistor. Bear in mind that there are models specifically for the SOI transistor, so the suggested approach would be to adapt the bulk transistor model without losing the charge based essence that provides, among other things, the fine matching with simulation results in the case of the g_m/I_D curve. If the model requires too many modifications, it would be better to use LUTs for estimating the capacitances for design purposes.

Finally, the voltage controlled oscillator could be built and experimentally tested. To this aim, the interface of the oscillator with the rest of the receiver must be thoroughly simulated. This process might require modifying the design of the oscillator.

This page is intentionally left blank.

Appendix A

Displacement of the locus of the impedance Z_C due to losses in the amplifier

The effect of G_o is accounted for as a displacement in Z_2, ΔZ_2. Thus,

$$Z_2 + \Delta Z_2 = \frac{1}{G_o} + \frac{1}{j\omega C_2}, \tag{A.1}$$

which can be approximated to

$$Z_2 + \Delta Z_2 = Z_2\,(1 + j\alpha)\,, \tag{A.2}$$

with

$$\alpha = \frac{G_o}{\omega C_2} \ll 1. \tag{A.3}$$

Z_C in (4.18) can be rewritten as

$$Z_C = Z_3 \left[1 - \frac{Z_3}{Z_1 + Z_3 + Z_2(1 + G_m Z_1)}\right]. \tag{A.4}$$

The displacement in Z_2 translates to a displacement in Z_C, which can be expressed through (A.4) and (A.2) as

$$Z_C + \Delta Z_C = Z_3 \left[1 - \frac{Z_3}{Z_1 + Z_3 + Z_2(1 + j\alpha)(1 + G_m Z_1)}\right]. \tag{A.5}$$

Thus,

$$\Delta Z_C = Z_3^2 \left[\frac{1}{Z_1 + Z_3 + Z_2(1 + G_m Z_1)} - \frac{1}{Z_1 + Z_3 + Z_2(1 + j\alpha)(1 + G_m Z_1)}\right], \tag{A.6}$$

simplifying to

$$\Delta Z_C = \frac{Z_3^2 Z_2(1 + G_m Z_1) j\alpha}{[Z_1 + Z_2(1 + G_m Z_1) + Z_3]^2}. \tag{A.7}$$

Appendix A. Displacement of the locus of the impedance Z_C due to losses in the amplifier

Replacing α from (A.3), it follows

$$\Delta Z_C = \frac{Z_3^2 Z_2 (1 + G_m Z_1) j G_o / \omega C_2}{[Z_1 + Z_2(1 + G_m Z_1) + Z_3]^2}. \tag{A.8}$$

From(A.8), the displacement ΔZ_C in the locus of Z_C can be obtained for $G_m = 0$, resulting in a purely horizontal shift of the circle in Fig. 4.5.

Substituting in (A.8) the impedances Z_1, Z_2 and Z_3 for their values as functions of C_1, C_2 and C_3, respectively, the horizontal shift ΔR_C is given by

$$\Delta R_C = \Delta Z_C\big|_{G_m=0} = \frac{G_o}{\omega^2 \left(C_2 + C_3 + \frac{C_2 C_3}{C_1}\right)^2}, \tag{A.9}$$

yielding the result in Equation 4.44 in [3].

The approximation of the shift in Z_C by its value at $G_m = 0$ is fulfilled as long as the shift of the circle is small with respect to its radius, this is, $\Delta R_m \ll |R_{n0}|_{max}$.

Appendix B

Schmitt trigger circuit layout

The layouts of the two Schmitt trigger circuits are included in this appendix for reference. Both layouts are built with the same criteria. All the nMOS transistors involved in each Schmitt trigger are built out of parallel arrangements of the same unitary transistor, as required by the design presented in Section 4.4. The unitary transistors are placed such that the currents flow in the same direction. Dummy devices are added in the edges. The pMOS transistors are also built out of parallel arrangements of unitary transistors, and placed in the same manner.

Figures B.1 and B.2 show the circuit layout of Schmitt trigger circuits A and B, respectively.

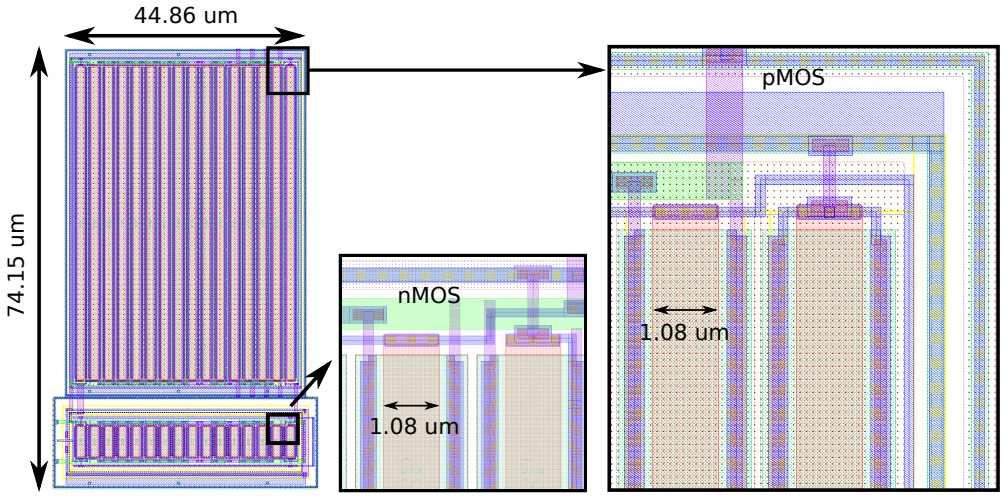


Figure B.1: Layout of circuit A.

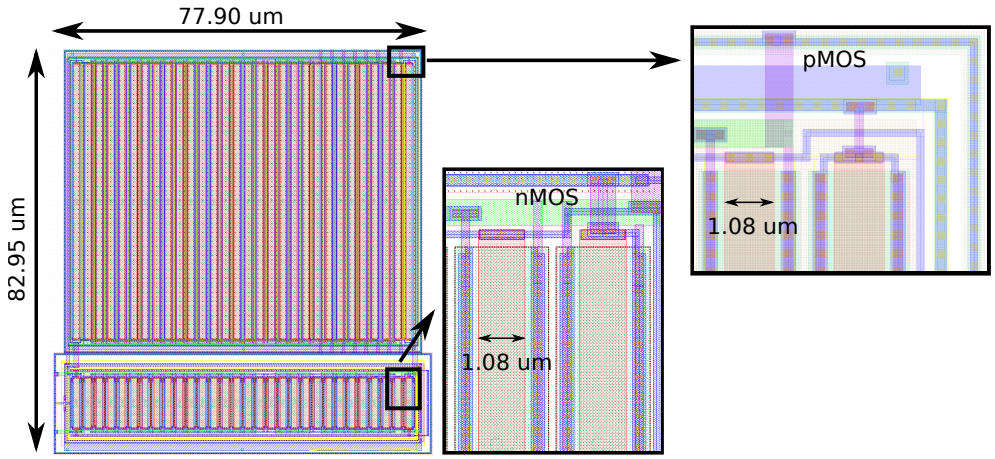


Figure B.2: Layout of circuit B.

Bibliography

[1] D. Yoon, T. Jang, D. Sylvester, and D. Blaauw. A 5.58 nW crystal oscillator using pulsed driver for real-time clocks. *IEEE Journal of Solid-State Circuits*, 51(2):509–522, Feb 2016.

[2] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge. Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits. *Proceedings of the IEEE*, 98(2):253–266, Feb 2010.

[3] Eric Vittoz. *Low-Power Crystal and MEMs Oscillators: The Experience of Watch Developments*. Springer, 2010.

[4] H. Yi, W. Yu, P. Mak, J. Yin, and R. P. Martins. A 0.18-V 382-μW bluetooth low-energy receiver front-end with 1.33-nW sleep power for energy-harvesting applications in 28-nm CMOS. *IEEE Journal of Solid-State Circuits*, 53(6):1618–1627, June 2018.

[5] Y. Pu, C. Shi, G. Samson, D. Park, K. Easton, R. Beraha, A. Newham, M. Lin, V. Rangan, K. Chatha, D. Butterfield, and R. Attar. A 9-mm2 ultra-low-power highly integrated 28-nm CMOS SoC for internet of things. *IEEE Journal of Solid-State Circuits*, 53(3):936–948, March 2018.

[6] H. Bottner, J. Nurnus, A. Gavrikov, G. Kuhner, M. Jagle, C. Kunzel, D. Eberhard, G. Plescher, A. Schubert, and K. Schlereth. New thermoelectric components using microsystem technologies. *Journal of Microelectromechanical Systems*, 13(3):414–420, June 2004.

[7] Alta devices: Single junction gallium arsenide photovoltaic product.

[8] C. J. Love, S. Zhang, and A. Mershin. Source of sustained voltage difference between the xylem of a potted ficus benjamina tree and its soil. *PLoS ONE*, 3(8, e2963), 2008.

[9] P. Weng, H. Tang, P. Ku, and L. Lu. 50 mV-input batteryless boost converter for thermal energy harvesting. *IEEE Journal of Solid-State Circuits*, 48(4):1031–1041, April 2013.

[10] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan. A 1.1 nW energy-harvesting system with 544 pW quiescent power for next-generation implants. *IEEE Journal of Solid-State Circuits*, 49(12):2812–2824, Dec 2014.

[11] N. Lotze and Y. Manoli. A 62 mV 0.13μm CMOS standard-cell-based design technique using Schmitt-trigger logic. *IEEE Journal of Solid-State Circuits*, 47(1):47–60, Jan 2012.

[12] N. Lotze and Y. Manoli. Ultra-sub-threshold operation of always-on digital circuits for IoT applications by use of Schmitt trigger gates. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(11):2920–2933, Nov 2017.

[13] J. Choi, E. Aklimi, C. Shi, D. Tsai, H. Krishnaswamy, and K. L. Shepard. Matching the power, voltage, and size of biological systems: A nW-scale, 0.023-mm^{3}pulsed 33-GHz radio transmitter operating from a 5 kT/q-supply voltage. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(8):1950–1958, Aug 2015.

[14] A. Bryant, J. Brown, P. Cottrell, M. Ketchen, J. Ellis-Monaghan, and E. J. Nowak. Low-power CMOS at Vdd = 4kT/q. In *Device Research Conference. Conference Digest (Cat. No.01TH8561)*, pages 22–23, June 2001.

[15] S. Jeong, Z. Foo, Y. Lee, J. Sim, D. Blaauw, and D. Sylvester. A fully-integrated 71 nW CMOS temperature sensor for low power wireless sensor nodes. *IEEE Journal of Solid-State Circuits*, 49(8):1682–1693, Aug 2014.

[16] M. B. Machado, M. C. Schneider, and C. Galup-Montoro. On the minimum supply voltage for MOSFET oscillators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(2):347–357, Feb 2014.

[17] O. Aiello, P. Crovetti, L. Lin, and M. Alioto. A pW-power Hz-range oscillator operating with a 0.3-1.8-V unregulated supply. *IEEE Journal of Solid-State Circuits*, pages 1–10, 2019.

[18] H. Jiang, P. P. Wang, P. P. Mercier, and D. A. Hall. A 0.4-V 0.93-nW/kHz relaxation oscillator exploiting comparator temperature-dependent delay to achieve 94-ppm/°C stability. *IEEE Journal of Solid-State Circuits*, 53(10):3004–3011, Oct 2018.

[19] S. Jang, C. Huang, C. Hsue, and C. Chang. A 0.3 V cross-coupled VCO using dynamic threshold MOSFET. *IEEE Microwave and Wireless Components Letters*, 20(3):166–168, March 2010.

[20] W. Thommen. An improved low power crystal oscillator. In *Proceedings of the 25th European Solid-State Circuits Conference*, pages 146–149, Sep. 1999.

[21] M. Toki. Low DC-driving-voltage crystal oscillator. In *Proceedings of the 1999 Joint Meeting of the European Frequency and Time Forum and the IEEE International Frequency Control Symposium (Cat. No.99CH36313)*, volume 1, pages 412–415 vol.1, April 1999.

[22] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and M. Takamiya. 93% power reduction by automatic self power gating (ASPG) and multistage inverter for negative resistance (MINR) in 0.7V, 9.2µW, 39MHz crystal oscillator. In *2013 Symposium on VLSI Circuits*, pages C142–C143, June 2013.

[23] K. Lei, P. Mak, and R. P. Martins. A 0.4V 4.8µW 16MHz CMOS crystal oscillator achieving 74-fold startup-time reduction using momentary detuning. In *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–4, May 2017.

[24] K. Lei, P. Mak, M. Law, and R. P. Martins. A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-µW steady-state power. *IEEE Journal of Solid-State Circuits*, 53(9):2624–2635, Sep. 2018.

[25] K. Hsiao. 17.7 a 1.89 nW/0.15 V self-charged XO for real-time clock generation. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 298–299, Feb 2014.

[26] S. Wu and T. Lee. Ultra-low-power one-pin crystal oscillator with self-charged technique. *Electronics Letters*, 52(4):325–327, 2016.

[27] Y. Zeng, T. Jang, Q. Dong, M. Saligane, D. Sylvester, and D. Blaauw. A 1.7 nW PLL-assisted current injected 32 kHz crystal oscillator for IoT. In *2017 Symposium on VLSI Circuits*, pages C68–C69, June 2017.

[28] H. Esmaeelzadeh and S. Pamarti. 18.4 a 0.55nW/0.5V 32kHz crystal oscillator based on a DC-only sustaining amplifier for IoT. In *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*, pages 300–301, Feb 2019.

[29] A. Shrivastava, D. Akella Kamakshi, and B. H. Calhoun. A 1.5 nW, 32.768 kHz XTAL oscillator operational from a 0.3 V supply. *IEEE Journal of Solid-State Circuits*, 51(3):686–696, March 2016.

[30] M. Coustans, F. Krummenacher, M. Kayal, L. Rossi, M. Dellea, Y. Godat, Y. Sierro, and S. DallaPiazza. A 32 kHz crystal oscillator leveraging voltage scaling in an ultra-low power 40 nA real-time clock. In *2018 31st IEEE International System-on-Chip Conference (SOCC)*, pages 308–313, Sep. 2018.

[31] A. Lahiri, P. Badrathwal, N. Jain, and K. Chatterjee. A 0.5 V supply, 49 nW band-gap reference and crystal oscillator in 40 nm CMOS. In *2017 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–4, April 2017.

[32] Márcio Cherem Schneider and Carlos Galup-Montoro. *MOSFET Modeling for Circuit Analysis and Design*. Singapore: World Scientific, 2007.

[33] Márcio Cherem Schneider and Carlos Galup-Montoro. *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge University Press, 2010.

[34] Osmar Franca Siebel, Marcio Cherem Schneider, and Carlos Galup-Montoro. MOSFET threshold voltage: Definition, extraction, and some applications. *Microelectronics Journal*, 43(5):329 – 336, 2012. Special Section NANOTECH 2011.

[35] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss. Series-parallel association of FET's for high gain and high frequency applications. *IEEE Journal of Solid-State Circuits*, 29(9):1094–1101, Sep. 1994.

[36] L. A. Pasini Melek, A. L. da Silva, M. C. Schneider, and C. Galup-Montoro. Analysis and Design of the Classical CMOS Schmitt Trigger in Subthreshold Operation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(4):869–878, April 2017.

[37] L. A. Pasini Melek, M. C. Schneider, and C. Galup-Montoro. Operation of the classical CMOS Schmitt trigger as an ultra-low-voltage amplifier. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65(9):1239–1243, Sep. 2018.

[38] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits*. Oxford University Press 6th Edition, 2010.

[39] Yannis Tsividis and Colin McAndrew. *Operation and Modeling of the MOS Transistor*. Oxford Univ. Press, third edition, 2011.

[40] M. Siniscalchi, F. Silveira, and C. Galup-Montoro. Ultra-low-voltage CMOS crystal oscillators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, pages 1–11, 2020.

[41] Ramón M. Cerda. *Understanding Quartz Crystals and Oscillators*. Artech House, 2014.

[42] M. A. Al-Qutayri, W. J. Tenten, and P. R. Shepherd. A prototype supply current monitor for testing analogue circuits. In *Proceedings. Tenth Annual IEEE International ASIC Conference and Exhibit (Cat. No.97TH8334)*, pages 38–41, Sep. 1997.

[43] Fernando Silveira, Denis Flandre, and Paul GA Jespers. A g_m/i_d based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA. *IEEE Journal of Solid-State Circuits*, 31(9):1314–1319, 1996.

[44] Paul GA Jespers and Boris Murmann. *Systematic Design of Analog CMOS Circuits*. Cambridge University Press, 2017.

[45] R. Fiorelli, E. J. Peralías, and F. Silveira. LC-VCO design optimization methodology based on the g_m/i_d ratio for nanometer CMOS technologies. *IEEE Transactions on Microwave Theory and Techniques*, 59(7):1822–1831, July 2011.

[46] R. Fiorelli, F. Silveira, and E. Peralías. MOST moderate–weak-inversion region as the optimum design zone for CMOS 2.4-GHz CS-LNAs. *IEEE Transactions on Microwave Theory and Techniques*, 62(3):556–566, March 2014.

[47] J. Noel, O. Thomas, M. Jaud, O. Weber, T. Poiroux, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, F. Andrieu, M. Vinet, O. Rozeau, F. Boeuf, O. Faynot, and A. Amara. Multi-V_T UTBB FDSOI device architectures for low-power CMOS circuit. *IEEE Transactions on Electron Devices*, 58(8):2473–2482, Aug 2011.

[48] M. Siniscalchi, N. Gammarano, S. Bourdel, C. Galup-Montoro, and F. Silveira. Modeling a nanometer FD-SOI transistor with a basic all-region MOSFET model. In *2020 Latin American Electron Devices Conference (LAEDC)*, 2020.

[49] V. Kilchytska, M.K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, T. Poiroux, O. Faynot, J.-P. Raskin, and D. Flandre. Ultra-thin body and thin-BOX SOI CMOS technology analog figures of merit. *Solid-State Electronics*, 70:50 – 58, 2012. Selected Full-Length Papers from the EUROSOI 2011 Conference.

[50] S. El Ghouli, D. Rideau, F. Monsieur, P. Scheer, G. Gouget, A. Juge, T. Poiroux, J. Sallese, and C. Lallement. Experimental g_m/I_D invariance assessment for asymmetric double-gate FDSOI MOSFET. *IEEE Transactions on Electron Devices*, 65(1):11–18, Jan 2018.

[51] Behzad Razavi. *RF Microelectronics*. Prentice Hall, Second Edition, 2012.

[52] L. Fanori and P. Andreani. Class-D CMOS oscillators. *IEEE Journal of Solid-State Circuits*, 48(12):3105–3119, Dec 2013.

[53] IEEE standard for low-rate wireless networks. *IEEE Std 802.15.4-2015 (Revision of IEEE Std 802.15.4-2011)*, pages 1–709, April 2016.

[54] I. Ghorbel, F. haddad, W. Rahajandraibe, and M. Loulou. A subthreshold low-power NMOS LC-VCO design for autonomous connected objects. In *2018 30th International Conference on Microelectronics (ICM)*, pages 216–219, Dec 2018.

[55] T. First, A. A. Mariano, P. C. Lacerda, G. Brante, O. C. G. Filho, and B. Leite. 2.4 GHz reconfigurable low voltage and low power VCO dedicated to sensor networks applications. In *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 329–332, Dec 2018.

[56] J. Lou, J. Zhang, Y. Gao, and H. Liu. A ultra-low-voltage 6.9 GHz CMOS quadrature VCO with superharmonic and back-gate coupling. In *The 2012 International Workshop on Microwave and Millimeter Wave Circuits and System Technology*, pages 1–4, April 2012.

[57] X. Ding, J. Wu, and C. Chen. A low-power 0.6-V quadrature VCO with a coupling current reuse technique. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 66(2):202–206, Feb 2019.

List of Tables

This page is intentionally left blank.

List of Figures

This is the last page.
Compiled Monday 4th May, 2020.
http://iie.fing.edu.uy/