frequency-agile transmission, respectively, giving the overall probability to resolve speed $P_1 + P_2$ as function of ε for different values of K.

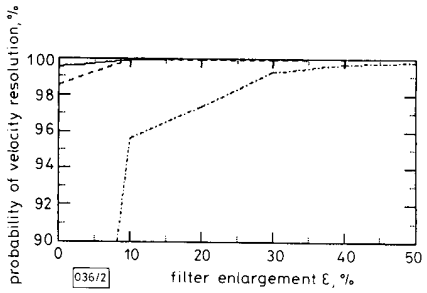

Fig. 2 *Algorithm performance for agile frequency*
——— $K = 3$ – – – – $K = L - 1$ —·—· $K = L$

Conclusions: A two-step procedure has been proposed to extract target speed data in MPRF radars by starting from ambiguous measurements. This approach also assures satisfactory performance for frequency-agile radars. Performance has been assessed through a computer simulation which allowed us to select the best values for Doppler threshold K and filter enlargement ε.

G. ALBANO
S. CACOPARDI
G. FEDELE*

INFO-COM Department
Università degli Studi di Roma 'La Sapienza'
Via Eudossiana 18, 00184 Roma, Italy

* Also with Avionics Department, FIAR SpA, Via Po 162, 00198 Roma, Italy

10th October 1989

References

1 HOVANESSIAN, S. A.: 'An algorithm for calculation of range in a multiple PRF radar', *IEEE Trans.*, 1976, **AES-12**, pp. 287–290
2 SKILLMAN, W. A., and MOONEY, D. H.: 'Multiple high-PRF ranging'. Proc. 5th IRE national convention on military electronics, 1961, pp. 37–40
3 STIMSON, G. W.: 'Introduction to airborne radar'. Hughes Aircraft Company, El Segundo, CA, 1984
4 REDDY, N. S., and SWAMY, M. N.: 'Resolution of range and Doppler ambiguities in medium PRF radars in multiple-target environment', *Signal Process.*, 1986, **11**, pp. 223–236
5 ALBANO, G.: 'Risoluzione delle ambiguità in velocità in un radar aeroportato operante in media frequenza di ripetizione'. Doc. thesis, University of Roma 'La Sapienza', 1988

NEW CMOS OTA FOR FULLY INTEGRATED CONTINUOUS-TIME CIRCUIT APPLICATIONS

Indexing terms: Circuit theory and design, Integrated circuits, Operational transconductance amplifiers, Filters, Amplifiers

A new CMOS circuit is proposed for implementing an operational transconductance amplifier (OTA) based on the square-law characteristic of MOS transistors biased in saturation. Simulation results show that a total harmonic distortion of the output current smaller than 1% for differential input signals up to 3·8 V_{pp} and supply voltages of ±5 V can be obtained.

Introduction: Linear *VI* transconductors are of increasing importance in continuous-time filtering,[1,2] particularly in MOS technology. However, to obtain linearity of the output current with the input voltage, special circuit topologies are required. Many of the good structures presented so far in the literature are based on the circuit shown in Fig. 1.[3–5] Transistors M_1 and M_2 are assumed to be matched devices operating in saturation and in strong inversion. Under these conditions the approximate square-law current/voltage characteristic

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2 \tag{1}$$

is valid for MOS transistors, if the channel-length modulation effect can be neglected (long-channel devices). The differential current $I_0 = I_1 - I_2$ in Fig. 1 can be expressed as[1]

$$I_0 = g_m V \qquad \text{for } |V| \le V_X \quad V = V_1 - V_2 \tag{2}$$

where $g_m = 2\beta V_X$ is the transconductance of the cell and $\beta = \mu_n C_{ox}(W/L)_1$. Therefore, having satisfied the conditions just mentioned, this approach leads to linear OTAs with a large differential input voltage range. The major drawback of the circuit in Fig. 1, however, is the difficulty in implementing the floating constant voltage sources. This letter presents a new solution to this problem which allows large differential input signal amplitudes with very small output harmonic distortion.

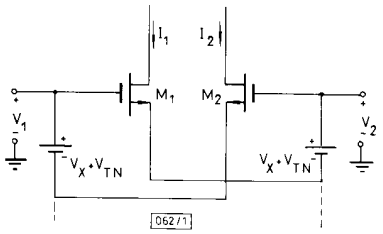

Fig. 1 *Basic cell of OTA*

Convertor realisation: Fig. 2 shows the circuit of the proposed transconductor. The constant voltage-sources are obtained from the gate-to-source voltages of the MOS transistors M_3 and M_4, which are biased in saturation with a constant current I_B. This is achieved in a very simple way: the drain current I_1 (I_2) of the input transistor M_1 (M_2) is mirrored through M_5, M_7, M_{10} and M_{11} (M_6, M_8, M_{13} and M_{14}) and then subtracted at the source node which is common to M_1

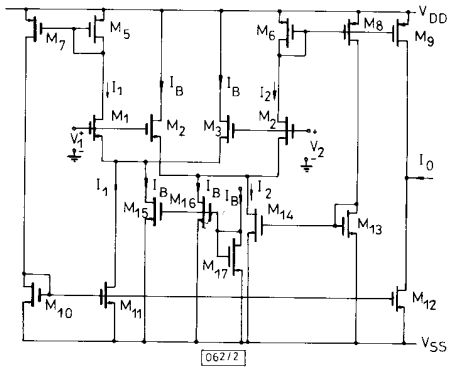

Fig. 2 *CMOS OTA with simple current mirrors*

Parameter	NMOS	PMOS
VTO, V	0·8	−0·8
TOX, $\times 10^{-10}$ m	470	470
UO, cm^2/Vs	600	220
UCRIT, $\times 10^5$ V/cm	0·93	0·85
VMAX, $\times 10^4$ m/s	5	3
NSUB, $\times 10^{15}$ cm^{-3}	6	1·1
GAMMA, $V^{0.5}$	0·43	0·53
NEFF	3·3	3·5

Transistor	W (μm)	L (μm)
M_1, M_2	10	20
M_3, M_4	20	20
M_5–M_9	80	4
M_6–M_{14}	40	4
M_{15}–M_{17}	80	20

and M_3 (M_2 and M_4). Consequently, the current through M_3 (M_4) equals I_B, and V_{GS3} is a constant whose value is given by

$$V_{GS3} = V_X + V_{TN} = (2I_B/\beta_3)^{0.5} + V_{TN} \quad (3)$$

Hence the value of V_X can be adjusted through the value of the bias current I_B. It should be noted that the proposed technique allows control of the transconductance g_m with process and temperature variations, and also provides tuning capability.

The input voltages V_1 and V_2 in the circuit of Fig. 2 must be greater than a minimum value to guarantee that both M_{11} (M_{14}) and M_{15} (M_{16}) are in saturation. Also, the maximum values of these input voltages must be limited to keep M_1 (M_2) in saturation. These two conditions are satisfied, respectively, if

$$V_1 \geq V_X + V_{TN} + V_{SS} + V_X \times \max\left[\left(\frac{\beta_3}{\beta_{16}}\right)^{0.5}, 2\left(\frac{\beta_1}{\beta_{11}}\right)^{0.5}\right] \quad (4)$$

and

$$V_1 \leq V_{DD} + V_{TN} + V_{TP} - 2V_X\left(\frac{\beta_1}{\beta_5}\right)^{0.5} \quad (5)$$

where max (x_1, x_2) denotes the maximum value of the pair (x_1, x_2). Eqns. 2, 4 and 5 clearly show that the increase in the maximum allowable input differential input voltage V_X reduces the common mode input voltage range. This compromise must be kept in mind during the design process.

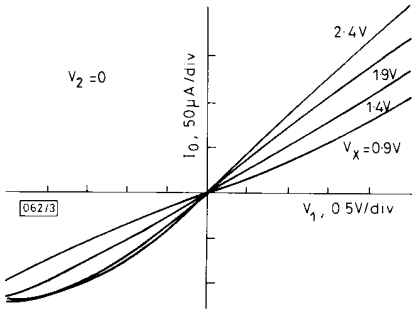

Fig. 3 *DC transfer characteristic of OTA*

Simulation results: The new OTA in Fig. 2 has been simulated using SPICE. For the simulation, the simple current mirrors have been substituted by cascode ones, reducing the errors due to inadequate mirroring. Of course, in this case we have a lower allowable input voltage range, but a smaller total harmonic distortion of the output current. In SPICE circuits simulations we have used $V_{DD} = -V_{SS} = 5$ V and the electrical parameters and the dimensions in Fig. 2. Fig. 3 shows a plot of the DC transfer characteristic of the convertor for various values of the voltage V_X, leading to different transconductance values. It should be noted that, as previously mentioned, the allowable input voltages that assure linearity depend on the value of V_X. Fig. 4 shows a plot of the total harmonic distortion against input peak voltage. The DC level of both the input terminals was necessary to ensure that the NMOS transistors of the current mirrors were biased in the saturation region over the entire input voltage range. Simulation results have shown that the total harmonic distortion can be less than 1% if the peak input differential voltage does not exceed the value of V_X, equal to 1·9 V in this case.

Conclusions: A very simple CMOS circuit has been proposed to implement a linear OTA whose transconductance value can easily be adjusted by controlling the bias current I_B. This circuit also provides a means of obtaining an output current proportional to the square of the input differential voltage.[4] Analysis and simulation results have shown that the proposed circuit can perform as well as or even better than some *VI* convertors presented in the literature. For example, the OTA presented in Reference 3 introduces a more complex circuit to obtain the same transfer function. Also, the allowable

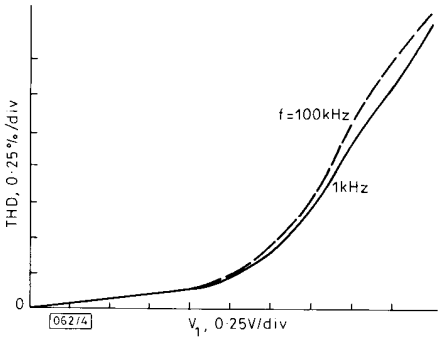

Fig. 4 *Total harmonic distortion of output current against peak input voltage*

V_X = 1·9 V; DC level: $V_1 = V_2$ = 1 V

common mode input voltage range in the convertor suggested here is greater than that presented in Reference 4 for the same manufacturing process. It should be emphasised that a careful layout of the circuit must be planned, to avoid harmonic distortion, especially the second harmonic, due to transistor mismatches.

S. NOCETI FILHO
M. C. SCHNEIDER
R. N. G. ROBERT

Laboratório de Instrumentação Eletrônica—LINSE
Departamento de Engenharia Elétrica
Universidade Federal de Santa Catarina
CP 476, Florianópolis, SC, Brazil

13th October 1989

References

1 GEIGER, R. L., and SÁNCHEZ-SINENCIO, E.: 'Active filter design using operational transconductance amplifiers: a tutorial', *IEEE Circ. & Dev. Mag.*, 1985, **1**, pp. 20–32
2 PARK, C. S., and SCHAUMANN, R.: 'Design of a 4 MHz analog integrated CMOS transconductance-C bandpass filter', *IEEE J. Solid-State Circ.*, 1988, **SC-23**, pp. 987–996
3 NEDUNGADI, A., and VISWANATHAN, T. R.: 'Design of linear CMOS transconductance elements', *IEEE Trans.*, 1984, **CAS-31**, pp. 891–894
4 SEEVINCK, E., and WASSENAAR, R.: 'A versatile CMOS linear transconductor/square-law function circuit', *IEEE J. Solid-State Circ.*, 1987, **SC-22**, pp. 366–377
5 NOCETI FILHO, S., SCHNEIDER, M. C., and ROBERT, R. N. G.: 'A linear differential CMOS $V \times I$ converter'. Tech. report UFSC/EE/TR-003/01-LINSE, 1989

PARTIALLY DOPED GaAs SINGLE-QUANTUM-WELL FET

Indexing terms: Semiconductor devices and materials, FETs, Semiconductor doping, GaAs

We report on 1 μm gate length n^+ AlGaAs/partially doped GaAs/n^+ AlGaAs single-quantum-well (PDSQW) FETs with a high extrinsic peak transconductance of 300 mS/mm. An acceptably high transconductance is maintained over 2·8 V gate-voltage swing. The FETs demonstrate a sharp pinch-off around $V_g = -2$ V, and a full channel current of 820 mA/mm was observed at room temperature. The PDSQW structures exhibit a two-dimensional electron-gas (2DEG) sheet charge density as high as $3{\cdot}4 \times 10^{12}$ cm^{-2} with mobility of 17 000 cm^2/Vs at 77 K. The PDSQW structure combines the advantages of both the conventional single-quantum-well (SQW) structure (high mobility and good carrier confinement) and the doped-channel structure (high carrier density).

Introduction: Selectively doped heterostructure transistors (SDHT) are very attractive for both high-speed digital circuits