Harmonic Distortion Caused by Capacitors Implemented with MOSFET Gates

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***Abstract*—The capacitive gate structures available in digital-oriented CMOS processes are reviewed, with emphasis on their use as linear capacitors. It is shown that the voltage harmonic distortion in MOS gate capacitors biased in either accumulation or strong inversion is almost technology independent. Experimental and analytical results indicate that the total harmonic distortion in an adequately biased (2.5 V) gate capacitor can be kept low (THD < -40 dB for a 3-V voltage swing).**

I. Introduction

FOR economical reasons, it is highly desirable to implement the analog part of a mainly digital system on a chip with standard VLSI processes [1]. Most analog applications require high-quality capacitors, characterized by high specific capacitance, uniformity, and low-voltage and temperature coefficients. Usually, these components are obtained at an extra cost due to the additional process steps necessary to meet these requirements [2], with the double-polysilicon option being the most frequently used.

One promising way to avoid the need for nonstandard processes to implement linear capacitors is to use the MOSFET gate structure, which is the intrinsic element of any MOS technology. Compared with double-poly capacitors, thin oxide capacitors present a larger capacitance per unit area and are expected to have better matching properties [3] (relative mismatches of MOS gate capacitances as low as 0.02% have been reported [4]). By properly biasing this structure, capacitors presenting weak nonlinearities can be realized.

Some authors have described the use of gate capacitors in analog applications as, for example, in transconductance-C (OTA-C) [5], transistor-only [6], [7] and switched-capacitor (SC) [8] filters. Despite the reported use of the gate structure in many analog applications, a more detailed analysis of this capacitor is necessary for the evaluation of the impact of its use in practical filters.

The purpose of this paper is to evaluate the behavior of MOS gates as capacitors. To this end, the capacitive structures available in CMOS technology are reviewed. An accurate model of the gate capacitance together with a numerical analysis and a design-oriented expression of the voltage harmonic distortion are presented. Finally, experimental data measured on an integrated capacitor are shown.

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II. Gate Structures in CMOS Technology

Fig. 1 shows four gate structures that can be employed as capacitors in a p-well CMOS process. The first two (Fig. 1(a) and (b)) must operate in accumulation while the last two must be biased in strong inversion. The device in Fig. 1(a) can act as a floating capacitor. Fig. 1(b) shows an ac grounded capacitor. The device in Fig. 1(c) can be shielded from substrate noise by applying a fixed potential to the well, while the one shown in Fig. 1(d) is a floating capacitor also available in a single-channel technology.

The model of the MOS transistor with $V_{DS} = 0$, valid for low- and medium-frequency operation (Appendix A), is shown in Fig. 2 [9]. Usually, some simple expressions are given for the intrinsic gate capacitance in strong inversion and in accumulation. In strong inversion, for $V_{DS} = 0$:

$$C_{gs} = C_{gd} \cong \tfrac{1}{2} C_{\text{ox}}$$

$$C_{gb} \cong 0 \tag{1a}$$

whereas in accumulation

$$C_{gs} = C_{gd} \cong 0$$

$$C_{gb} \cong C_{ox} \tag{1b}$$

where C_{ox} is the thin oxide intrinsic capacitance.

The other intrinsic capacitances, C_{bs} and C_{bd}, are nonlinear [9] and depend on V_{BS}. For an actual device, the overlap (linear) capacitances are in parallel with C_{gs} and C_{gd} while the junction capacitances are in parallel with C_{bd} and C_{bs}. A third junction capacitance (well to substrate) must be considered if the device is built inside a well.

For the purpose of getting a nearly voltage-independent capacitance, a voltage bias must be provided to the gate terminal to keep the structure in accumulation or strong inversion. This is easy to realize for grounded or virtually grounded capacitors, as shown in Fig. 3 for typical OTA-C and SC integrators, where the natural choice for the top plate is the gate terminal due to its very low parasitic capacitance. The circuits shown in Fig. 3 are differently affected by the parasitic capacitances. In OTA-

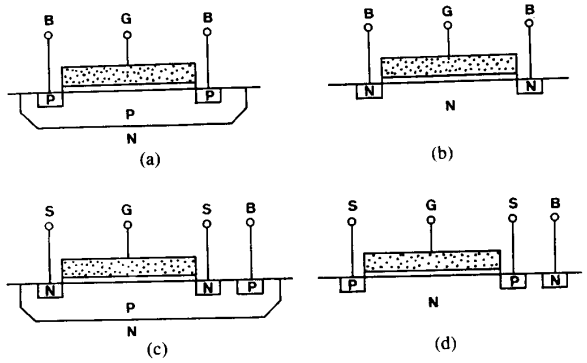


Fig. 1. Gate structures in a p-well CMOS technology.

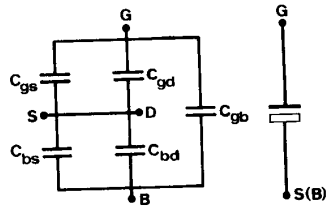


Fig. 2. Intrinsic capacitances of the MOS transistor at $V_{DS} = 0$ and the gate capacitor symbol. The gate is the top plate while the source (bulk) is the bottom plate for strong inversion (accumulation).

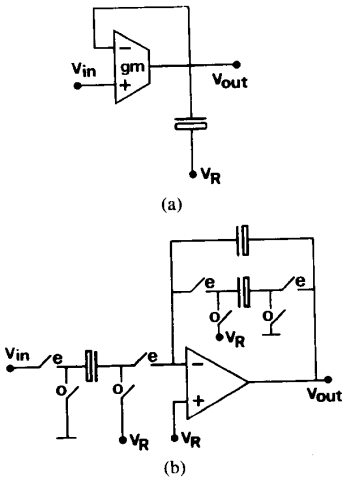


Fig. 3. Bias schemes for a lossy integrator. All capacitors have a dc operating point equal to V_R. (a) OTA-C. (b) Switched capacitor [8].

grounded C filters, the parasitics ($C_{bs} + C_{bd}$) must be bypassed because of their high nonlinearity. This can be accomplished, for instance, using the structure in Fig. 1(c) with S and B connected to V_{SS}. For SC filters, the capacitors can be obtained from the same gate structure (Fig. 1(c)) with the wells tied to V_{SS}, the gates to $V_R (= V_{DD})$, and the sources to the input and output nodes. In this case, capacitances $C_{bs} + C_{bd}$ and C_{gb} will become the bottom- and top-plate parasitic capacitances, respectively. Then, for parasitic-insensitive networks, their values and nonlinearities will not affect the transfer function. Using this biasing scheme for SC filters, properly designed folded-cascode operational amplifiers can provide common-mode input ranges up to V_{DD}.

III. Accurate Model of the Gate Capacitance

Most analytical models of the MOSFET are based on the charge-sheet approximation, in which the thickness of the surface channel (in inversion or accumulation) is neglected [9]. For these models the gate-to-source capacitance C_{gs} in inversion is constant for $V_{DS} = 0$. Therefore, to determine the weak nonlinear behavior of gate capacitors in inversion and accumulation, the simplified models must be abandoned and an approach based on the fundamental equations of the MOS structure has to be followed.

For the three-terminal n-channel MOS structure, the voltage and electrical charge are given by the well-known expressions, valid for nondegenerate silicon [9]:

$$V_{GB} = V_{FB} + \psi_s - Q_c'/C_{ox}' \tag{2}$$

$$Q_c' = -\text{sgn}\,(\psi_s)\, F\sqrt{N_A\phi_t}\left\{\exp\left(\frac{-\psi_s}{\phi_t}\right) + \frac{\psi_s}{\phi_t} - 1 + \exp\left[\frac{\psi_s - (2\phi_F + V_{SB})}{\phi_t}\right]\right\}^{0.5} \tag{3}$$

where ψ_s represents the surface potential, ϕ_F is the Fermi potential, ϕ_t is the thermal voltage, V_{FB} is the flat-band voltage, V_{GB} is the gate-to-bulk voltage, Q_c' is the total semiconductor charge per unit area, and C_{ox}' is the oxide capacitance per unit area. The other variables have their usual meanings [9].

The total small-signal gate capacitance per unit area is given by

$$C_g' = \frac{dQ_G'}{dV_{GB}} = -\frac{dQ_c'}{dV_{GB}} \tag{4}$$

where $C_g' = C_{gs}' + C_{gd}' + C_{gb}'$ (Fig. 2) if $V_{BS} = V_{DS} = 0$.

This capacitance can be interpreted as the series connection of the oxide capacitance C_{ox}' and the semiconductor space-charge capacitance $C_c' = -(dQ_c'/d\psi_s)$, i.e.

$$\frac{1}{C_g'} = \frac{1}{C_{ox}'} + \frac{1}{C_c'}. \tag{5}$$

As previously stated in Section II, the gate structure should be biased in strong inversion or accumulation in order to obtain a nearly voltage-independent capacitance. Hence, the voltage dependence of the gate capacitance in these two regions will be analytically determined for $V_{BS} = V_{DS} = 0$.

A. Accumulation Region

Retaining only the dominant exponential term $e^{-\psi_s/\phi_t}$ in (3), a simple approximation is obtained for the semiconductor charge:

$$Q_c' \cong F\sqrt{N_A\phi_t}\exp\left(\frac{-\psi_s}{2\phi_t}\right). \tag{6a}$$

Consequently

$$Q_c' \cong 2\phi_t \cdot C_c' \tag{6b}$$

and, from (2), it follows that

$$C_c' \cong C_{ox}' \left| \frac{V_{GB} - V_{FB}}{2\phi_t} \right| \tag{6c}$$

where ψ_s has been neglected in the numerator of (6c). Hence, the semiconductor space-charge capacitance depends almost linearly on the gate voltage. Although at a first glance this approximation seems to be crude, an example in Appendix B shows that (6c) gives a good approximation of the semiconductor capacitance. The total gate capacitance is then given by

$$C_g' \cong C_{ox}' \left[1 - \frac{2\phi_t}{|V_{GB} - V_{FB}| + 2\phi_t} \right]. \tag{7}$$

For the analysis of circuits with weak nonlinear components it is useful to obtain the power series expansion of the nonlinear term around a bias voltage V_R. From (5) it follows that

$$C_g' = C_{ox}' \left(1 - \frac{C_{ox}'}{C_c'} + \left(\frac{C_{ox}'}{C_c'} \right)^2 - + \cdots \right). \tag{8}$$

From (6) and (8), writing $V_{GB} = V_R + V$:

$$C_g' \cong C_{ox}' \left(1 - \frac{2\phi_t V}{(V_R - V_{FB})^2} + \frac{2\phi_t V^2}{|V_R - V_{FB}|^3} + \cdots \right). \tag{9}$$

B. Strong Inversion

The total semiconductor charge Q_c' is the sum of the inversion-layer charge and of the depletion-region charge. Assuming that the depletion charge is constant and the inversion charge varies exponentially with the surface potential, it follows that

$$-Q_c' \cong F\sqrt{N_A(2\phi_F)} + F\sqrt{N_A\phi_t}\, e^{(\psi_s - 2\phi_F)/2\phi_t} \tag{10a}$$

which results in

$$-Q_c' \cong F\sqrt{N_A(2\phi_F)} + 2\phi_t \cdot C_c'. \tag{10b}$$

Substituting (10b) in (2)

$$C_c' \cong C_{ox}' \frac{|V_{GB} - V_T|}{2\phi_t} \tag{10c}$$

where ψ_s was assumed to be equal to $2\phi_F$. V_T is the classical strong inversion threshold voltage.

The total gate capacitance is given by

$$C_g' \cong C_{ox}' \left[1 - \frac{2\phi_t}{|V_{GB} - V_T| + 2\phi_t} \right]. \tag{11}$$

Therefore, in strong inversion, a power series analogous to (9) for the gate capacitance is valid if V_{FB} is substituted by V_T. Although the error in this case is usually larger than for accumulation, as shown for the example in Appendix B, the approximation is quite good to model the weak nonlinearities of C_g' in strong inversion.

To conclude this section a comment should be made about the weak nonlinearities of accumulation or strong inversion biased gate capacitors in contrast with their strong nonlinearities in flat-band condition. The voltage coefficient in the latter case is given by [2]

$$V_{cc} = \frac{1}{C_g} \left| \frac{dC_g}{dV_{GB}} \right| = \frac{C_{ox}'^2}{3q\epsilon_{sc}N_A} \tag{12}$$

while the voltage coefficients in accumulation and strong inversion follow immediately from (9):

$$V_{cc} = \frac{2\phi_t}{(V_R - V_{FB})^2} \tag{13a}$$

$$V_{cc} = \frac{2\phi_t}{(V_R - V_T)^2}. \tag{13b}$$

In flat-band condition the voltage coefficient (12) has a strong dependence on the technological parameters C_{ox}' and N_A. On the other hand, in inversion and accumulation, the voltage coefficients (13) are asymptotically independent of technological parameters. For a 5-V technology, for example, typical V_T range from 0.6 to 1.0 V. If a bias voltage equal to 2.5 V is applied to a gate capacitor from a 5-V technology, the voltage capacitance coefficient lies between 14 and 22 kppm/V.

IV. Experimental Results

A test capacitor, made up of 500 thin oxide unit capacitors (Fig. 4) of 40 μm × 40 μm, parallel-connected using metal lines, has been fabricated in a 2-μm CMOS n-well process. The main electrical parameters concerning the available CMOS process are a specific capacitance of 0.86 fF/μm^2, a well doping concentration of 1.9×10^{16} cm^{-3}, and a threshold voltage of -0.6 V for the PMOS transistor.

The experimental CV characteristic of the test structure with source and well short-circuited, together with the theoretical CV characteristic, are shown in Fig. 5. The latter was obtained from the application of the process parameters to expressions (2) to (4). The difference between experimental and theoretical capacitance data in the depletion region (near the minimum of the capacitance curve) is explained by the nonuniform doping profile of the well.

For the purpose of obtaining the ionized impurity profile, the slope of the $1/C_g^2$ versus V_{GB} curve in the depletion region has been determined [10]. This method showed that the well impurity concentration is not constant and reaches a value as low as 2×10^{15} cm^{-3} for a depth of 0.2 μm. Hence, the minimum of the experimental capacitance curve corresponds to an impurity concentration at the depletion edge much lower than the nominal value of the well doping concentration. In spite of this difference, not only the experimental and the theoretical curves nearly

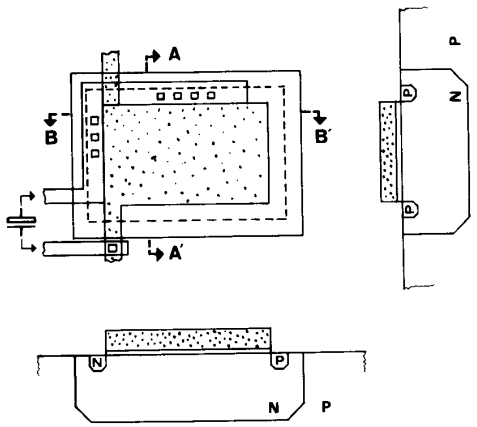


Fig. 4. Unit cell of the test capacitor.

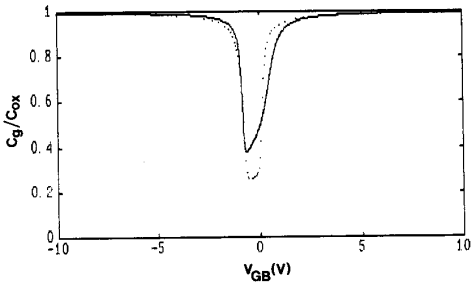


Fig. 5. *CV* characteristic of the test capacitor for $V_{BS} = 0$. —— theoretical, ------- experimental.

coincide in the accumulation and strong inversion regions but also their derivatives fit fairly well, as shown in Fig. 6. This is explained by the fact that in these regions the effect of the doping profile on the total capacitance is small, since the depletion charge variation is deeply overwhelmed by the surface free carrier charge variation [10]. So, the constant doping profile model is accurate in either strong inversion or accumulation.

A spectral analysis of the voltage in the MOS gate capacitor was performed with the integrator of Fig. 7, where the MOS capacitor is driven by a sinusoidal current source. A previous test with a linear capacitor replacing the DUT has pointed to a total harmonic distortion (THD) below −80 dB. Fig. 8 displays the second and third harmonic distortion, experimentally measured, computed from Fourier analysis based on (2) and (3) and computed from:

$$\text{2ND HARM DIST} \cong \frac{\phi_t V_P}{2(V_R - V_{FB})^2} \tag{14a}$$

$$\text{3RD HARM DIST} \cong \frac{\phi_t V_P^2}{6|V_R - V_{FB}|^3} \tag{14b}$$

for accumulation, while

$$\text{2ND HARM DIST} \cong \frac{\phi_t V_P}{2(V_R - V_T)^2} \tag{15a}$$

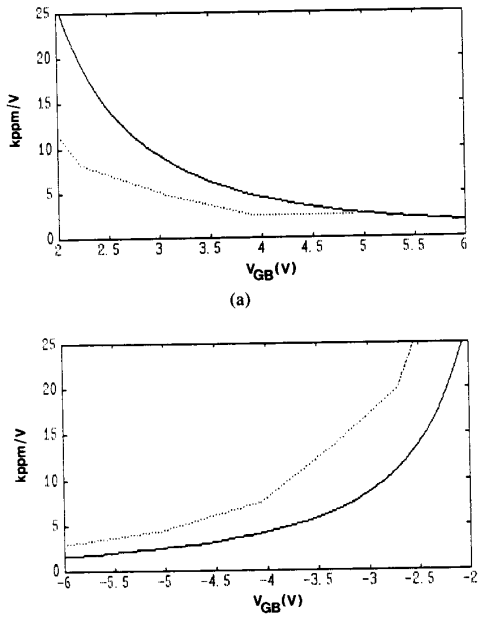


Fig. 6. Voltage coefficient $(1/C_g)(dC_g/dV_{GB})$ of the capacitance for $V_{BS} = 0$: (a) Accumulation. (b) Inversion. —— theoretical, ------ experimental.

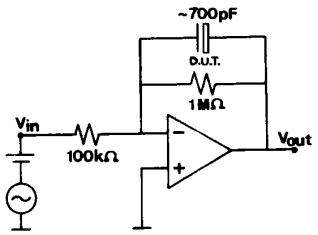


Fig. 7. Circuit for harmonic distortion measurement in the test capacitor.

$$\text{3RD HARM DIST} \cong \frac{\phi_t V_P^2}{6|V_R - V_T|^3} \tag{15b}$$

for strong inversion. In the above formulas, V_R and V_P are the bias and peak values of the gate-to-bulk voltage, respectively. Formulas (14a) and (14b) were derived from (9) and are valid for both N and P substrates, as are expressions (15a) and (15b).

Fig. 9 shows a comparison between experimental and computed THD. It should be noted that for a 2.5-V bias, the peak-to-peak signal in the MOS gate can be about 4 V (in accumulation) and the THD remains below −40 dB. When the signal swing is below 2 V for a capacitor biased at 2.5 V, the high order harmonics are negligible and the THD is approximated by (14a). In this case, fully differential structures are useful for distortion reduction.

V. Conclusions

In spite of being a nonlinear element, the gate structure of the MOS transistor biased in inversion or accumulation

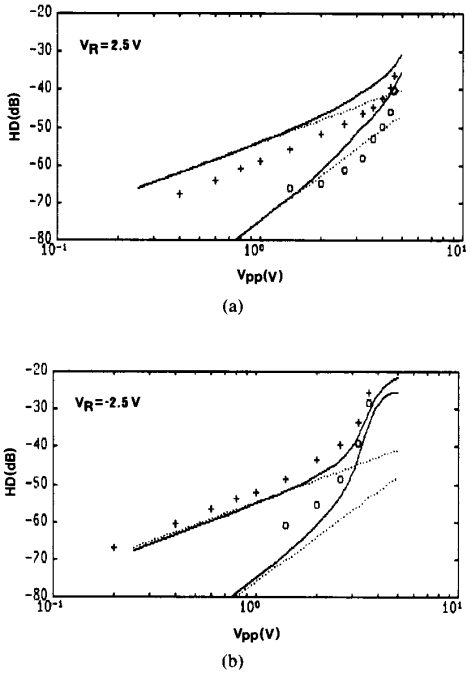


Fig. 8. Second- and third-order capacitor harmonic distortion for a 2.5-kHz input excitation. (a) Accumulation. (b) Inversion. -------- expressions (14) and (15) for the second- and third-order harmonic distortion; —— second- and third-order harmonic distortion computed from (2) and (3) + + + + + experimental second-order harmonic distortion, ○○○○○ experimental third-order harmonic distortion.

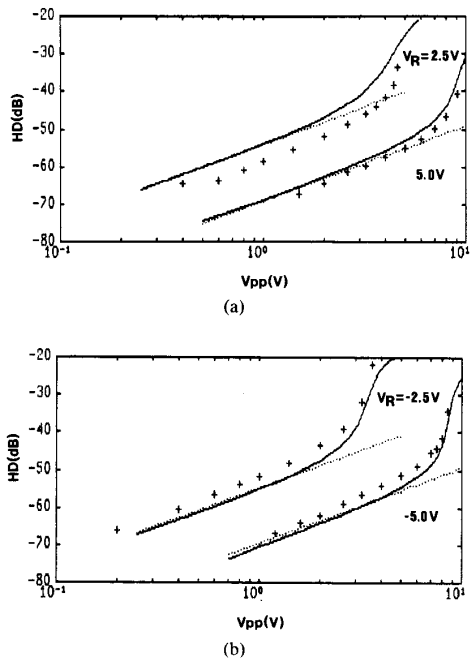


Fig. 9. Harmonic distortion for a 2.5-kHz input excitation. (a) Accumulation. (b) Inversion. -------- expresssions (14a) and (15a) for the second order distortion, —— THD computed from (2) and (3), + + + + + experimental THD.

provides a capacitance with advantages over double-poly capacitors, such as higher capacitance per unit area, better matching, and full compatibility with any digital MOS process.

Harmonic distortion in gate capacitors is almost independent of technology provided they are biased in accumulation or strong inversion. Moreover, the approximate formulas presented for the harmonic distortion can help the circuit designer to predict the maximum voltage swing allowable to maintain the THD at acceptable levels for both single and fully differential structures.

Appendix A
Distributed Model of the MOSFET Gate Capacitor

In the previous analysis, the gate capacitor has been modeled as a lumped element. Practically, the distributed nature of the gate capacitor must be taken into account, since the channel resistance is not equal to zero. Hence, under small-signal operation the gate structure can be modeled as a uniformly distributed RC transmission line. For a gate structure where the drain is open, the equivalent impedance seen from gate and source is equal to [11]

$$Z(s) = \frac{R_t}{\sqrt{s\tau}} \coth \sqrt{s\tau} \tag{16}$$

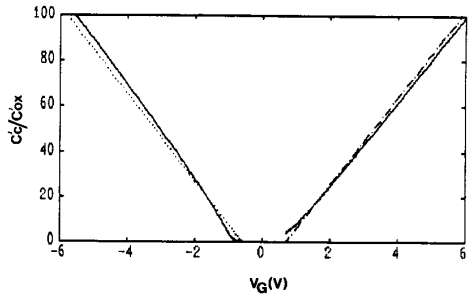
where R_t is the total channel resistance and $\tau = R_t C_t$, where C_t is the total gate capacitance. For the gate structure shown in Fig. 1(c), expression (16) for the gate impedance still holds but with $\tau = R_t C_t/4$ since the drain and source terminals are short-circuited. If the operating frequency is much lower than $1/\tau(\omega \leq 0.2/\tau)$ [12], the transmission line nature of the gate structure in Fig. 1(c) can be modeled with the approximate impedance parameter:

$$Z(s) \cong \frac{1}{sC_t} + \frac{1}{12} R_t. \tag{17}$$

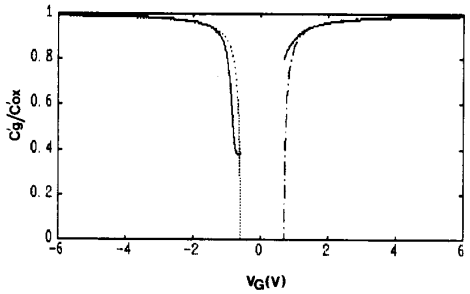
Consequently, under low-frequency operation ($\omega \leq 0.2/\tau$) the MOSFET gate structure behaves like a capacitor with a quality factor $Q \cong 12/(L^2\omega R_s C'_{ox})$, where L is the channel length and R_s is the channel sheet resistance. Therefore, for higher frequency operation, shorter channel capacitors are required in order to avoid excessive phase shift due to their parasitic resistance. The Q factor for the unit capacitor ($L = 40$ μm), biased in accumulation with $V_{GS} = 2.5$ V, is larger than 40 000 for 2.5 kHz, the signal frequency employed for harmonic distortion measurements.

Appendix B
Accuracy of the Linear Approximation of the Semiconductor Capacitance

In order to evaluate the accuracy of approximations (6c) and (10c), the theoretical value of the semiconductor capacitance [9] is plotted for both accumulation and strong inversion regions (Fig. 10(a)), using the electrical param-



(a)



(b)

Fig. 10. (a) Semiconductor capacitance: —— theoretical, ···-··-··- approximated by (6c) (accumulation), ---------- approximated by (10c) (strong inversion). (b) Gate capacitance: —— theoretical, ···-··-··- ···-··· approximated by (7) (accumulation), -------- approximated by (11) (strong inversion).

eters of the available CMOS process. Fig. 10(b) shows the plot of the approximated gate capacitance and its theoretical value. As expected, the approximation presented for the semiconductor capacitance is more accurate for accumulation than for strong inversion, since in the latter case the depletion capacitance has been neglected.

Acknowledgment

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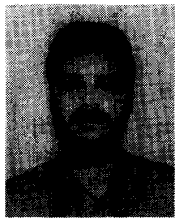

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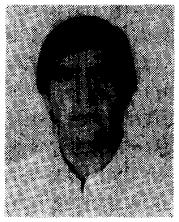

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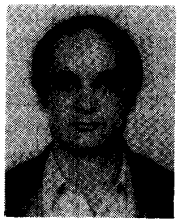
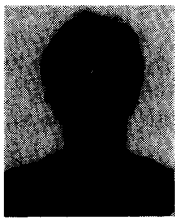


Sidnei Noceti Filho was born in Florianópolis, SC, Brazil, on December 17, 1952. He received the B.E. and M.S. degrees in electrical engineering, both from the Universidade Federal de Santa Catarina (UFSC), Florianópolis, SC, Brazil, in 1975 and 1980, respectively. In 1985 he received the doctoral degree in electrical engineering from the Universidade Federal do Rio de Janeiro, Brazil.

In 1976 he joined the Electrical Engineering Department of UFSC where he has been engaged in education and research on signal processing and circuit analysis and design.



Carlos Galup Montoro (M'89) was born in 1953 in Montevideo, Uruguay. He received the engineer degree from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, in 1979 and the doctor engineer degree in 1982 also from INPG.

From 1982 to 1989 he was at Universidade de São Paulo, São Paulo, Brazil, where he was involved in device modeling and IC design. He joined the Electrical Engineering Department at Universidade Federal de Santa Catarina, Florianópolis, SC, Brazil, in 1990 and is now engaged in education and research.