# Compatibility of switched capacitor filters with VLSI processes

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**Abstract:** This paper demonstrates the compatibility of switched capacitor filters with VLSI processes. Conditions to obtain linear and precise input-to-output voltage relationships in networks containing nonlinear capacitors are derived. Having satisfied these conditions, considerations about the alternatives for capacitor implementations show the realisability of SC filters in any digital MOS process.

## 1 Introduction

Continuous advances in VLSI have resulted in the majority of the presently available integrated circuit technologies being optimised for digital circuits. This fact indicates a clear tendency towards a digital implementation of signal processing systems. On the other hand, analogue circuits will always be required to interface the digital system with the physical world [1]. Therefore, most modern integrated systems are predominantly digital, with the analogue part occupying only a small fraction of the total chip area. In such cases, economy requires that the analogue circuits be fully compatible with a digital process.

The most successful realisations of analogue functions in CMOS technology have been for many years based on the well-established switched capacitor (SC) technique. Switched capacitor systems have been traditionally integrated in nonstandard MOS processes, basically due to the demand for linear capacitors. Attempts have also been made to integrate SC filters with linear capacitors available in standard digital processes [2]. The usual conclusion has been, however, that the price to be paid in silicon real estate was excessive [1, 2].

More recently, a new design technique, called switched current (SI), has been actively pursued. One of the main driving forces behind the development of this new technique has been exactly the consideration that switched capacitors do not fit standard VLSI processing [3–5].

This paper demonstrates the compatibility of SC circuits with VLSI processes. It is shown that, satisfying some trivial requirements, SC circuits containing nonlinear capacitors can realise linear charge processors in exactly the same way SI circuits can be designed as linear current processors. Moreover, it is shown that highly linear and precise SC voltage processors are realisable using any digital MOS technology.

## 2 SC circuits as charge processors

Sampled-data analogue signal processing requires four basic operations: inversion, addition, multiplication and delay. In SI circuits, these operations are accomplished by switched current mirrors [3–8]. These mirrors realise a nonlinear $I$–$V$ conversion followed by an inverse $V$–$I$ conversion, leading to a linear relationship between input and output currents (Fig. 1A) [5]. Obviously, the mirror

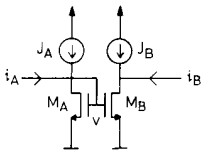


**Fig. 1A** *Current mirror*

concept is not limited to the current variable. In the following, the basic cell of an SC circuit is interpreted as a charge mirror composed of capacitors which can even be nonlinear.

In Fig. 1B, suppose the operational amplifier (op-amp) is ideal. If a charge $q_A$ has been injected into the high

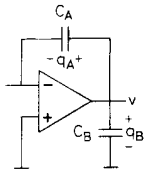


**Fig. 1B** *Charge mirror*

impedance inverting input of the op-amp its relationship with the voltage $v$ at the output terminal is

$$q_A = C_A v = C_{A_0} f_A[v] v \tag{1}$$

In this expression, $f_A[v]$ is a dimensionless function describing the nonlinearity of the capacitor $C_A$ [9]. This

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nonlinearity depends on the structure of the capacitor and can be considered to be equal for capacitors with the same structure and physically close to each other in a chip. The parameter $C_{A_0}$ is the value of the capacitance for a signal voltage $v$ equal to zero, and is proportional to the area of the capacitor.

Using the same notation, the charge in $C_B$ (Fig. 1B) can be written as

$$q_B = C_B v = C_{B_0} f_B[v] v \tag{2}$$

If the nonlinearities of $C_A$ and $C_B$ are equal, then

$$\frac{q_B}{q_A} = \frac{C_{B_0}}{C_{A_0}} = \frac{\text{area } (C_B)}{\text{area } (C_A)} \tag{3}$$

Therefore, under this assumption, the basic block in Fig. 1B performs as a (linear) charge mirror with gain defined by a geometrical ratio and, consequently, independent of the technology.

The building blocks usually employed in SC and SI networks to perform signal processing operations are shown in Fig. 2. In the SC (SI) circuit, each output charge

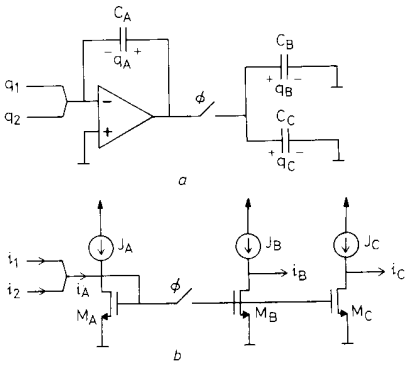


**Fig. 2** *Signal processing building blocks*
*a* SC circuits
*b* SI circuits

(current) is a delayed and scaled image of the sum of the input charges (currents).

From these considerations, it is clear that both SI and SC circuits employing nonlinear elements (transistors in SI circuits and capacitors in SC circuits) can maintain linearity from input to output. If the external quantity is a voltage signal, linear input $V$–$Q$ and output $Q$–$V$ converters are then required for SC circuits, exactly in the same way linear $V$–$I$ and $I$–$V$ converters are required for SI circuits.

## 3 Realisation of linear voltage processors

For analysis, the SC networks are considered to be implemented using ideal op-amps and switches. Also, for simplicity, we consider the class of SC networks satisfying the following topological constraint: after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage.

This topological property is intrinsic to the great majority of stray insensitive SC networks and therefore its assumption does not represent any serious practical limitation.

Consider the third-order SC lowpass filter shown in Fig. 3 [10]. This network clearly satisfies the required topological constraint. For linear capacitors, the function $f[v(\cdot)]$ introduced in eqn. 1 is equal to one. Then, the charge conservation equations (CCEs) at the virtual grounds of the op-amps are

$$\begin{aligned} &-C_{I_0} v_I(nT - T/2) + C_{E_0} v_A(nT) + C_{F_0} v_B(nT) \\ &\quad = -C_{A_0} v_A(nT) + C_{A_0} v_A(nT - T) \end{aligned} \tag{4a}$$

$$\begin{aligned} &-C_{G_0} v_A(nT - T) \\ &\quad = -C_{B_0} v_B(nT) + C_{B_0} v_B(nT - T) \end{aligned} \tag{4b}$$

$$\begin{aligned} &C_{H_0} v_B(nT) + C_{J_0} v_C(nT) \\ &\quad + C_{D_0} v_A(nT) - C_{D_0} v_A(nT - T) \\ &\qquad = -C_{C_0} v_C(nT) + C_{C_0} v_C(nT - T) \end{aligned} \tag{4c}$$

Eqns. 4 can also be written in terms of the charges in the capacitors $C_I$, $C_A$, $C_B$ and $C_C$. This form will be specially useful for the analysis of the more general case of networks containing nonlinear capacitors. Performing the change of variables yields

$$\begin{aligned} &-q_I(nT - T/2) + \frac{C_{E_0}}{C_{A_0}} q_A(nT) + \frac{C_{F_0}}{C_{B_0}} q_B(nT) \\ &\quad = -q_A(nT) + q_A(nT - T) \end{aligned} \tag{5a}$$

$$-\frac{C_{G_0}}{C_{A_0}} q_A(nT - T) = -q_B(nT) + q_B(nT - T) \tag{5b}$$

$$\begin{aligned} &\frac{C_{H_0}}{C_{B_0}} q_B(nT) + \frac{C_{J_0}}{C_{C_0}} q_C(nT) \\ &\quad + \frac{C_{D_0}}{C_{A_0}} q_A(nT) - \frac{C_{D_0}}{C_{A_0}} q_A(nT - T) \\ &\quad = -q_C(nT) + q_C(nT - T) \end{aligned} \tag{5c}$$

At this point, a detailed interpretation of these equations

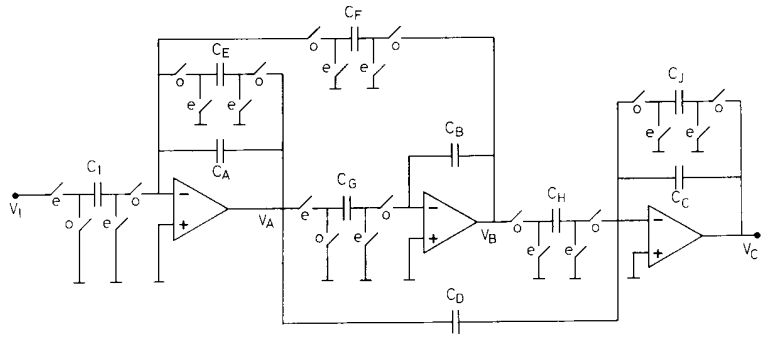


**Fig. 3** *Third-order lowpass SC filter*

is instructive. The various coefficients correspond to the gains of the network charge mirrors, as explained in Section 2. For instance, the charge in capacitor $C_A$ is mirrored to $C_E$, $C_G$ and $C_D$ with gains $C_{E_0}/C_{A_0}$, $C_{G_0}/C_{A_0}$ and $C_{D_0}/C_{A_0}$, respectively. Eqns. 5 are represented by the signal flow graph (SFG) of the $Q$-processor in Fig. 4, where the branch transmittances are proportional to the gains of the charge mirrors. This figure also shows the input $V$–$Q$ and output $Q$–$V$ conversions of the SC filter. To facilitate the visualisation, the charge processing and the conversion roles of the input and output capacitors are explicitly shown.

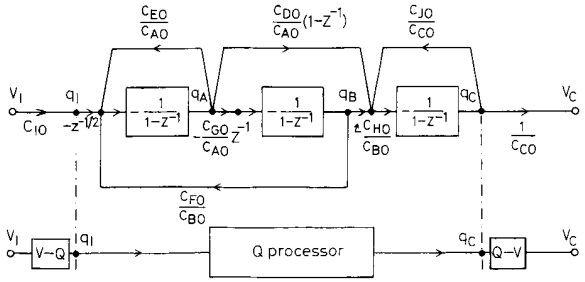


**Fig. 4** *SFG of SC filter in Fig. 3*

Consider now the same network but implemented using nonlinear capacitors. The CCEs at the virtual grounds will then be

$$\begin{aligned}
&-C_{I_0} f_I[v_I(nT - T/2)]v_I(nT - T/2) \\
&\quad + C_{E_0} f_E[v_A(nT)]v_A(nT) + C_{F_0} f_F[v_B(nT)]v_B(nT) \\
&\quad = -C_{A_0} f_A[v_A(nT)]v_A(nT) \\
&\qquad + C_{A_0} f_A[v_A(nT - T)]v_A(nT - T) \qquad (6a)
\end{aligned}$$

$$\begin{aligned}
&-C_{G_0} f_G[v_A(nT - T)]v_A(nT - T) \\
&\quad = -C_{B_0} f_B[v_B(nT)]v_B(nT) \\
&\qquad + C_{B_0} f_B[v_B(nT - T)]v_B(nT - T) \qquad (6b)
\end{aligned}$$

$$\begin{aligned}
&C_{H_0} f_H[v_B(nT)]v_B(nT) + C_{J_0} f_J[v_C(nT)]v_C(nT) \\
&\qquad + C_{D_0} f_D[v_A(nT)]v_A(nT) \\
&\qquad - C_{D_0} f_D[v_A(nT - T)]v_A(nT - T) \\
&\quad = -C_{C_0} f_C[v_C(nT)]v_C(nT) \\
&\qquad + C_{C_0} f_C[v_C(nT - T)]v_C(nT - T) \qquad (6c)
\end{aligned}$$

Assume that all capacitors connected to the same op-amp output have identical nonlinearities, a condition that can be accurately fulfilled in an integrated circuit. In other terms, this condition is equivalent to the implementation of linear charge mirrors. Under this assumption,

$$f_E[\cdot] = f_G[\cdot] = f_D[\cdot] = f_A[\cdot] \qquad (7a)$$

$$f_F[\cdot] = f_H[\cdot] = f_B[\cdot] \qquad (7b)$$

$$f_J[\cdot] = f_C[\cdot] \qquad (7c)$$

and the CCEs (eqns. 6) become

$$\begin{aligned}
&-C_{I_0} f_I[v_I(nT - T/2)]v_I(nT - T/2) \\
&\quad + C_{E_0} f_A[v_A(nT)]v_A(nT) + C_{F_0} f_B[v_B(nT)]v_B(nT) \\
&\quad = -C_{A_0} f_A[v_A(nT)]v_A(nT) \\
&\qquad + C_{A_0} f_A[v_A(nT - T)]v_A(nT - T) \qquad (8a)
\end{aligned}$$

$$\begin{aligned}
&-C_{G_0} f_A[v_A(nT - T)]v_A(nT - T) \\
&\quad = -C_{B_0} f_B[v_B(nT)]v_B(nT) \\
&\qquad + C_{B_0} f_B[v_B(nT - T)]v_B(nT - T) \qquad (8b)
\end{aligned}$$

$$\begin{aligned}
&C_{H_0} f_B[v_B(nT)]v_B(nT) + C_{J_0} f_C[v_C(nT)]v_C(nT) \\
&\qquad + C_{D_0} f_A[v_A(nT)]v_A(nT) \\
&\qquad - C_{D_0} f_A[v_A(nT - T)]v_A(nT - T) \\
&\quad = -C_{C_0} f_C[v_C(nT)]v_C(nT) \\
&\qquad + C_{C_0} f_C[v_C(nT - T)]v_C(nT - T) \qquad (8c)
\end{aligned}$$

Expressing, as for the linear network, the CCEs in terms of the charges in the capacitors $C_I$, $C_A$, $C_B$ and $C_C$,

$$q_I(\cdot) = C_I v_I = C_{I_0} f_I[v_I(\cdot)]v_I(\cdot) \qquad (9a)$$

$$q_A(\cdot) = C_A v_A = C_{A_0} f_A[v_A(\cdot)]v_A(\cdot) \qquad (9b)$$

$$q_B(\cdot) = C_B v_B = C_{B_0} f_B[v_B(\cdot)]v_B(\cdot) \qquad (9c)$$

$$q_C(\cdot) = C_C v_C = C_{C_0} f_C[v_C(\cdot)]v_C(\cdot) \qquad (9d)$$

the same set of linear eqns. 5, relative to the linear network, is obtained. This shows that, provided some simple conditions are satisfied, an SC network containing nonlinear capacitors can realise linear charge processing. Furthermore, the expression of its charge transfer function will be equal to that of the same network with linear capacitors. Another important conclusion is that this charge transfer function is proportional to the voltage transfer function of the linear network. In our example, it can be verified from the SFG of Fig. 4 that

$$\frac{V_C^e(z)}{V_I^o(z)} = \frac{C_{I_0}}{C_{C_0}} \cdot \frac{Q_C^e(z)}{Q_I^o(z)} \qquad (10)$$

Since $Q_I^o(z) = Z\{C_{I_0} f_I[v_I(nT - T/2)]v_I(nT - T/2)\}$ and $Q_C^e(z) = Z\{C_{C_0} f_C[v_C(nT)]v_C(nT)\}$, a linear input-output voltage relationship will exist if $f_C[v_C(\cdot)] = f_I[v_I(\cdot)] = 1$. From eqns. 1 and 7, this condition is satisfied if the capacitors connected to the input and to the output network nodes are linear. With regard to all the remaining capacitors, the only existing requirement is that those connected to the same op-amp output must present equal nonlinearities, which is equivalent to the implementation of linear charge mirrors. Having satisfied these requirements, the right-hand side of eqn. 10 represents also the voltage transfer function of the network employing nonlinear capacitors.

Even though these conclusions have been reached through the analysis of an example, it should be clear that they can be extended to any switched capacitor network satisfying the trivial topological constraint enunciated at the beginning of this section.

Summarising, we state a set of sufficient conditions to implement a linear input-output voltage relationship with a switched capacitor network containing nonlinear capacitors.

*Condition 1:* The network topology must satisfy the constraint that, after the settling time corresponding to each clock phase, the voltage across any capacitor must depend only on a single node voltage.

*Condition 2:* All capacitors connected to the same op-amp output must present identical nonlinearities expressed by the function $f_X[v_X]$, $v_X$ the voltage at the op-amp output node.

*Condition 3:* Only the capacitors connected to the input and output nodes need to be implemented as linear capacitors, regardless of the order or the topology of the network.

## 4 Implementation issues

Switched capacitor filter networks implemented with nonlinear capacitors and satisfying conditions 1 to 3 are actually linear charge processors with linear input $V$–$Q$ and output $Q$–$V$ converters. As far as the charge processing is concerned, precision is guaranteed by the proper implementation of the charge mirrors. This is accomplished by satisfying condition 2 and by geometrically matching the capacitors connected to the same op-amp output.

Regarding voltage processing, eqn. 10 shows that any mismatch between the input and output capacitors will cause only a voltage gain error, which does not usually represent a major drawback. For networks containing more than one input branch, all input capacitors must be matched to ensure the precise realisation of the transmission zeros of the voltage transfer function.

Finally, if the topology chosen for the SC filter has too many capacitors connected to the input and output nodes, the linear $V$–$Q$ and $Q$–$V$ conversions can be realised by using amplifier stages [14] at both ends. This brings the required number of linear capacitors to two or three.

For the implementation of the nonlinear capacitors, the natural choice is to use a MOSFET gate structure. An important feature of this structure is the use of the thin gate oxide as dielectric. Compared with the commonly employed double-poly capacitors, gate capacitors in VLSI processes present a larger capacitance per unit area and are expected to have better matching properties [11, 12]. Moreover, gate capacitors are fully compatible with any digital MOS process, while linear capacitors are costly to implement in VLSI processes [16].

To implement the few required linear capacitors, one possible solution would be the use of external capacitors. If a fully integrated implementation is required, two main alternatives are available. One of them is the use of aluminium-poly [1, 2] or aluminium-aluminium capacitors. Even though these structures present low specific capacitances, they may represent an attractive solution to implement few capacitors [15]. In many practical situations, the total area occupied by capacitors in a filter implemented using one of these structures will be smaller than that which would be required if double-poly capacitors were to be used for the entire filter. For VLSI capacitive structures [16], area savings can be achieved if the internal total capacitance exceeds the input/output capacitance by a factor of ten or more. In this case, the total area savings due to the implementation of the internal capacitors with MOSFET gates overcomes the excess area required for the implementation of the linear input/output capacitors.

The other alternative is to use the MOSFET gate structure in accumulation or inversion [13]. Properly biased, such capacitors may represent both a good choice for many low distortion applications and the best solution in terms of chip area. This alternative is the topic of a current investigation and will be the subject of a future publication.

The compatibility of SC filters with VLSI processes also means its operation from a low voltage power supply. Many modern mixed-mode circuits operate on a single 5 V supply [20–23] and are typically implemented in a 2 $\mu$m (or less) CMOS double-poly processes. The technique proposed enables the integration of such circuits in a 5 V digital process. For a lower supply voltage operation e.g. 3.3 V, circuit techniques have been presented elsewhere [1]. Operational amplifiers, analogue switches and other analogue building blocks for 1 V to 3 V supply voltage operation have been presented [1], showing the feasibility of low voltage operated SC filters.

To conclude this section a comment can be made about the dynamic range of SC filters and how it is related to the thermodynamic limits. As pointed out in Reference 17: 'The reduction on physical size and power dissipation will be limited by the fact that the signals within the filter are represented as energy stored on capacitors. The dynamic range of the filter is related to the ratio of stored energy to thermal energy $kT$ dictating a minimum capacitor size for a given filter dynamic range'. Therefore, the reduction in supply voltage affects in similar ways all the circuits that use capacitors to memorise signals. In fact, it has been demonstrated [18, 19] that for an SC filter the switch noise is only 3 dB higher than the resistor noise generated in the 'equivalent' continuous-time filter.

## 5 Experimental verification

The third-order lowpass SC network in Fig. 5 has been implemented as a discrete prototype, satisfying conditions 1 to 3. The cascade structure has been chosen due to the simplicity of design and large practical applicability. As nonlinear capacitors, the capacitances from gate to the short-circuited source and drain terminals of well-matched Motorola P5N40 power transistors have been used. The maximum value of this nonlinear capacitor measured over the $\pm 5$ V range was 3.3 nF, the same value chosen for the linear unity capacitor. The op-amps used were 741 and the switches were 4066. The voltage reference bias $V_R$ has been employed to allow flexibility on the choice of the operating points of the capacitors [13]. To simulate a very strong nonlinearity, a $V_R = -2$ V has been experimentally determined. Fig. 6 presents the total harmonic distortion measured at the op amp outputs, where at least a 30 dB improvement can be verified from the internal nodes to the output node. Fig. 7 shows the waveforms at an internal node and at the output for a sinusoidal input signal. Obviously, in an integrated circuit implementation, a much better matching of the capacitance nonlinearities will exist compared with the discrete prototype. Therefore it is expected that the output harmonic distortion of integrated SC filters, designed according to the proposed approach, will be

dominated by the nonlinearities of the op-amps and of the switches.

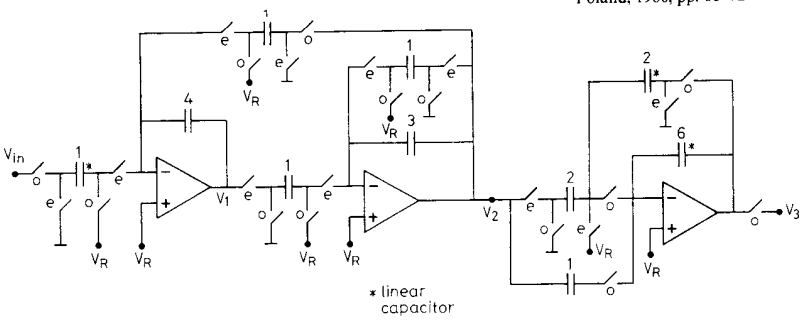


**Fig. 5** *Third-order prototype SC filter*

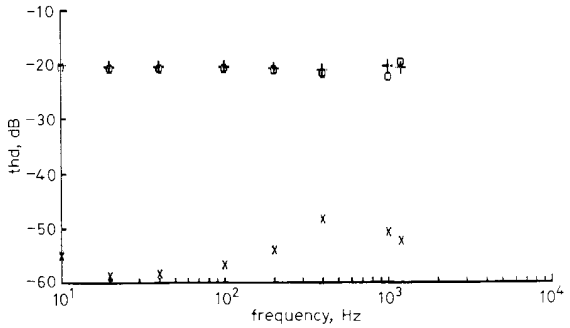


**Fig. 6** *THD at op amp outputs of prototype SC filter*
○ Output 1 + Output 2 × Output 3
$V_R = -2$ V; $V_{in} = 3$ $V_{pp}$

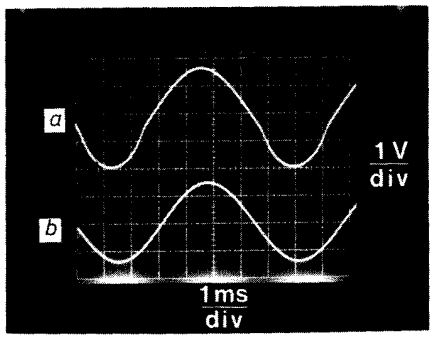


**Fig. 7** *Measured output waveforms*
*a* intermediate node *b* output node

## 6 Conclusions

The full compatibility of switched capacitor filters with VLSI processes has been demonstrated. To this end, the conditions for linear charge and voltage processing have been derived. Considerations about precision of the transfer function coefficients and about alternatives for capacitor implementations show the feasibility of integration of high-precision, low-distortion SC filters in any digital MOS process.

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