An MOS Transistor Model for Analog Circuit Design

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***Abstract*— This paper presents a physically based model for the metal–oxide–semiconductor (MOS) transistor suitable for analysis and design of analog integrated circuits. Static and dynamic characteristics of the MOS field-effect transistor are accurately described by single-piece functions of two saturation currents in all regions of operation. Simple expressions for the transconductance-to-current ratio, the drain-to-source saturation voltage, and the cutoff frequency in terms of the inversion level are given. The design of a common-source amplifier illustrates the application of the proposed model.**

***Index Terms*—Circuit modeling, integrated circuit design, MOS analog integrated circuits, MOS devices.**

I. Introduction

METAL – oxide – semiconductor field-effect-transistor (MOSFET) models for analog integrated circuit (IC) design should consist of simple, continuous, and accurate single-piece expressions valid in the whole inversion regime of operation [1]. These models should verify fundamental properties, such as charge conservation [2] and the MOSFET source-to-drain intrinsic symmetry [3]. Moreover, they have to be technology independent and correctly represent not only the weak and strong inversion regions but also the moderate inversion region, where the MOSFET often operates [4]. Ideally, only a few parameters should be required to describe the model, and a simple and consistent characterization procedure should be devised. Last, analog IC designers need simple expressions to compute transistor dimensions for any current level.

In this work, the model of [5], which satisfies all the above-mentioned requirements, is entirely rewritten in terms of two components of the transistor current: one associated with the source and the other with the drain. In this reformulation, all the static and dynamic characteristics are expressed as functions of these two components of the drain current. Therefore, hand calculations for circuit design can be substantially simplified.

Our model uses the same basic physical variables as the EKV model [3] but avoids the use of nonphysical interpolating curves to bridge the gap between weak and strong inversion. As a consequence, our model allows the calculation of the nonreciprocal capacitances and is charge conserving.

The model presented here does not include short-channel effects or the dependence of the mobility on the transversal field. The inclusion of such effects leads to complicated expressions that are not suitable for discussion in this paper. A computer-implemented version of our MOSFET model that includes short-channel and field-dependent mobility already exists and can be found elsewhere [11].

The basic principles used to derive our MOSFET model are presented in Section II. The expression for the drain current, based on the model of [5], is presented in order to emphasize its decomposition into two components. In Section III, we present the expressions of the MOSFET static and dynamic characteristics in terms of the two components of the drain current. Simulated and measured characteristics are compared. Section IV shows some practical expressions for circuit design. Section V presents the application of our MOSFET model to the design of a common-source amplifier.

II. Fundamentals

The MOSFET model hereinafter is strongly based on two physical features of the MOSFET structure: the charge-sheet model [2], [12] and the incrementally linear relationship between the inversion charge density and the surface potential [5], [6]. Combined, these two approximations allow deriving a MOSFET model entirely formulated in terms of two components of the drain current [3].

In [5], a physics-based model for the MOSFET, valid in the whole inversion regime, has been accomplished. The fundamental approximation of this model is the linear dependence of the inversion charge density on the surface potential ϕ_S [5], [6] for a constant gate-to-bulk voltage V_G over a range of ϕ_S, which encompasses the weak, moderate, and strong inversion regions

$$dQ'_I = nC'_{\rm ox}d\phi_s. \tag{1a}$$

In (1a), $C'_{\rm ox}$ is the oxide capacitance per unit area and n is the slope factor, slightly dependent on the gate voltage, greater than one and usually smaller than two. n is defined [3], [5] by

$$n = \frac{1}{C'_{\rm ox}}\frac{dQ'_I}{d\phi_S}\bigg|_{\phi_S=\phi_0+V_P} = 1+\frac{\gamma}{2\sqrt{\phi_0+V_P}} \tag{1b}$$

where γ is the body effect factor, ϕ_0 is a potential whose value is a few ϕ_t (thermal voltage) above twice the Fermi potential for holes [3], and V_P is the "pinch-off" voltage [3], [5] given

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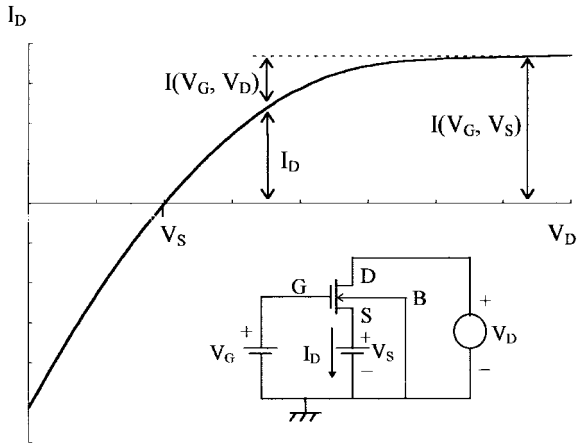

Fig. 1. Output characteristic of a long-channel NMOS transistor for constant V_S and V_G. All voltages are referred to the bulk terminal.

by

$$V_P = \left[\sqrt{V_G - V_{T0} + \left(\sqrt{\phi_0} + \gamma/2\right)^2} - \gamma/2\right]^2 - \phi_0 \cong \frac{V_G - V_{T0}}{n}. \quad (1c)$$

In (1c), V_{T0} is the threshold voltage in equilibrium, corresponding to the value of V_G for which V_P is equal to zero.

The drain current in a long-channel transistor is given by the charge-sheet expression [2]

$$I_D = \mu W\left(-Q'_I\frac{d\phi_S}{dx} + \phi_t\frac{dQ'_I}{dx}\right) \quad (2)$$

where μ is the carrier mobility, W is the channel width, and x is the coordinate along the channel length.

Substituting (1a) into (2) and integrating along the channel length L [5], we obtain

$$I_D = I_F - I_R \quad (3a)$$

$$I_{F(R)} = I(V_G, V_{S(D)}) = \mu n C'_{\rm ox}\frac{W}{L}\frac{\phi_t^2}{2}\left[\left(\frac{Q'_{\rm IS(D)}}{nC'_{\rm ox}\phi_t}\right)^2 - \frac{2Q'_{\rm IS(D)}}{nC'_{\rm ox}\phi_t}\right] \quad (3b)$$

where $I_{F(R)}$ is the forward (reverse) saturation current and $Q'_{\rm IS(D)}$ is the inversion charge density evaluated at the source (drain) end. Therefore, the forward (reverse) saturation component of the current is associated with the source (drain) inversion charge density by a one-to-one relationship.

Equation (3) emphasizes the source–drain symmetry of the MOSFET. To exploit the intrinsic symmetry of the device, voltages are referred to the substrate [3] (Fig. 1). Let us now explain how to determine the forward and reverse components of the drain current from the transistor output characteristic, as the one shown in Fig. 1 for a long-channel MOSFET. Note that there is a region, usually called the saturation region, where the drain current is almost independent of V_D. This means that in this region, $I(V_G, V_D) \ll I(V_G, V_S)$. Therefore, $I(V_G, V_S)$ can be interpreted as the drain current in forward saturation. Similarly, in reverse saturation, I_D is independent of the source voltage. Since the long-channel MOSFET is a symmetric device, the knowledge of the saturation current $I(V_G, V_S)$ for any V_G, V_S allows computing the drain current for any combination of source, drain, and gate voltages.

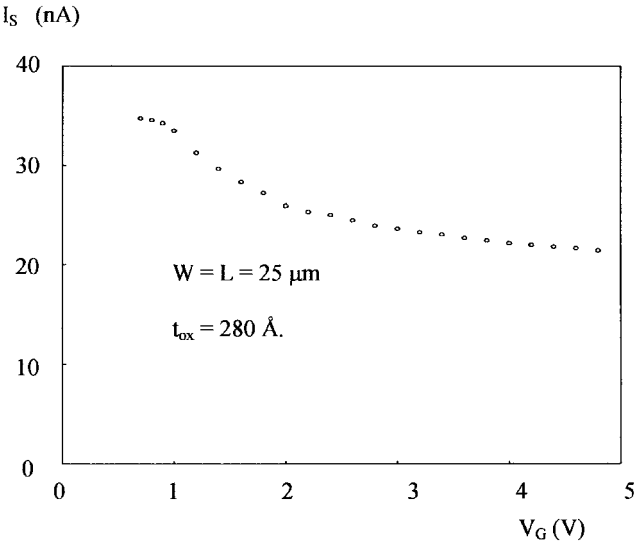

Fig. 2. Measured normalization current for an NMOS transistor ($t_{\rm ox} = 280$ Å and $W = L = 25$ μm).

III. Model Formulation

In this section, we show how to derive continuous, single-piece expressions for the large and small signal characteristics of the MOSFET in terms of the forward and reverse saturation currents. These expressions are very accurate in weak, moderate, and strong inversion.

A. Current Normalization

Expression (3b) can be rewritten in the form

$$-\frac{Q'_{\rm IS(D)}}{nC'_{\rm ox}\phi_t} = \sqrt{1 + i_{f(r)}} - 1 \quad (4a)$$

where

$$i_{f(r)} = \frac{I_{F(R)}}{I_S} = \frac{I\left(V_G, V_{S(D)}\right)}{I_S} \quad (4b)$$

is the forward (reverse) normalized current [3] and

$$I_S = \mu n C'_{\rm ox}\frac{\phi_t^2}{2}\frac{W}{L} \quad (4c)$$

is the normalization current, which is four times smaller than the homonym presented in [3]. The factor $\mu n C'_{\rm ox}\phi_t^2/2$, which is herein denominated the sheet normalization current $I_{S\square}$, is a technological parameter slightly dependent on V_G, through μ and n. Fig. 2 depicts the normalization current of a long-channel MOS transistor versus the gate voltage. The normalization current variation around its average value is about $\pm$30% for a gate voltage ranging from 0.6 to 5 V.

In [3], the forward normalized current i_f is also properly referred to as the inversion coefficient since it indicates the inversion level of the device, which depends on both the gate and source voltages. As a rule of thumb, values of i_f greater than 100 characterize strong inversion. The transistor operates in weak inversion up to $i_f = 1$. Intermediate values of i_f, from 1 to 100, indicate moderate inversion.

TABLE I
EXPRESSIONS FOR THE MOSFET STATIC AND DYNAMIC CHARACTERISTICS

Variable	Expression
I_D	$I_S\,(i_f - i_r)$
Q_I	$-C_{ox} n\phi_t \left[\frac{2}{3}\left(\sqrt{1+i_f}+\sqrt{1+i_r}-\frac{\sqrt{1+i_f}\sqrt{1+i_r}}{\sqrt{1+i_f}+\sqrt{1+i_r}}\right)-1\right]$
Q_B	$-\frac{n-1}{n}Q_I - C_{ox}\frac{\gamma^2}{2(n-1)}$
Q_S	$-C_{ox} n\phi_t \left[\frac{2}{15}\left(\frac{3\left(\sqrt{1+i_f}\right)^3+6(1+i_f)\sqrt{1+i_r}+4\sqrt{1+i_f}(1+i_r)+2\left(\sqrt{1+i_r}\right)^3}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^2}\right)-\frac{1}{2}\right]$
Q_D	$Q_I - Q_S$
$g_{ms(d)}$	$\frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}}-1\right)$
g_{mg}	$\frac{g_{ms}-g_{md}}{n}$
$C_{gs(d)}$	$C_{ox}\frac{2}{3}\left(1-\frac{1}{\sqrt{1+i_{f(r)}}}\right)\left[1-\frac{1+i_{r(f)}}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^2}\right]$
$C_{gb} = C_{bg}$	$\frac{n-1}{n}\left(C_{ox}-C_{gs}-C_{gd}\right)$
$C_{bs(d)}$	$(n-1)C_{gs(d)}$
C_{ss}	$C_{ox}\frac{2}{15}n\left(\sqrt{1+i_f}-1\right)\frac{3(1+i_f)+9\sqrt{1+i_f}\sqrt{1+i_r}+8(1+i_r)}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^3}$
C_{sd}	$-C_{ox}\frac{4}{15}n\left(\sqrt{1+i_r}-1\right)\frac{2+i_f+3\sqrt{1+i_f}\sqrt{1+i_r}+i_r}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^3}$
C_{sg}	$\frac{C_{ss}-C_{sd}}{n}$
C_{sb}	$(n-1)C_{sg}$
V_P-$V_{S(D)}$	$\phi_t\left[\sqrt{1+i_{f(r)}}-\sqrt{1+i_p}+\ln\left(\frac{\sqrt{1+i_{f(r)}}-1}{\sqrt{1+i_p}-1}\right)\right]$

$C_{ox} = WLC'_{ox}$

The source (drain) transconductance, defined as the derivative of the drain current with respect to the source (drain) voltage, can be obtained either by differentiating (3)

$$g_{ms(d)} = -(+)\frac{\partial I_D}{\partial V_{S(D)}} = -\mu\frac{W}{L}\phi_t\frac{\partial Q'_{\mathrm{IS(D)}}}{\partial V_{S(D)}}\left(\frac{Q'_{\mathrm{IS(D)}}}{nC'_{\mathrm{ox}}\phi_t}-1\right) \tag{5a}$$

or from the general expression [3], [5]

$$g_{ms(d)} = -\mu\frac{W}{L}Q'_{\mathrm{IS(D)}}. \tag{5b}$$

The combination of (4a), (5a), and (5b) allows one to express the derivative of the source (drain) inversion charge density with respect to the source (drain) voltage as a function of the forward (reverse) normalized current

$$\frac{\partial Q'_{\mathrm{IS(D)}}}{\partial V_{S(D)}} = nC'_{\mathrm{ox}}\frac{\sqrt{1+i_{f(r)}}-1}{\sqrt{1+i_{f(r)}}}. \tag{5c}$$

In the model of [5], all the static (drain current and total charges) and dynamic [three transconductances and nine independent (trans)capacitances] characteristics of the long-channel MOS transistor are expressed as functions of the source and drain inversion charge densities and their derivatives with respect to the source and drain voltages. Expressions (4a) and (5c) allow rewriting the charge model of [5] in terms of the normalized saturation currents i_f and i_r, as shown in Table I.

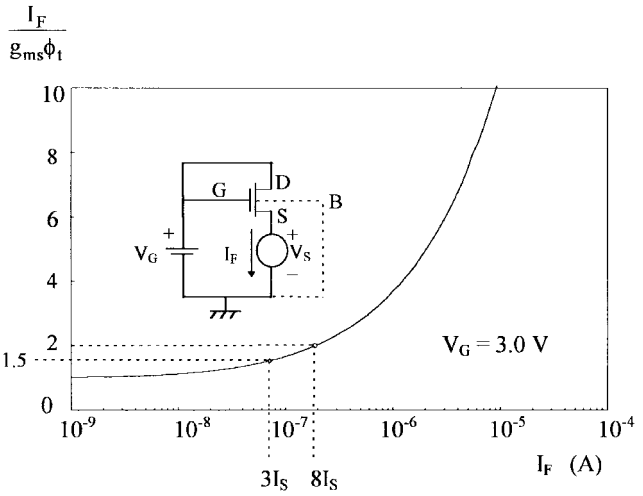

Fig. 3. Determination of the normalization current from the measured current-to-transconductance ratio. (NMOS transistor with $t_{ox} = 280$ Å and $W = L = 25$ μm; $V_G = 3.0$ V.)

Table I synthesizes the overall behavior of a large and long-channel device from weak to strong inversion. It is remarkable that only three parameters (I_S, C_{ox}, and n) are enough to characterize the small-signal parameters of the MOSFET. Short and narrow channel effects can be modeled as in [3]. The current-based expressions in Table I are useful for analysis and design of current-biased circuits, as is the case of almost all the analog circuits.

B. Current-to-Transconductance Ratio

An important design parameter required in analog circuits is the current-to-transconductance ratio [4]. In the following, we will demonstrate that this design parameter can be expressed in terms of a normalized saturation current.

The substitution of (4a) into (5b) allows one to derive the equation for the source (drain) transconductance in Table I. Therefore, the ratio of the drain current in forward (reverse) saturation to the source (drain) transconductance is given by

$$\frac{I_{F(R)}}{\phi_t \cdot g_{ms(d)}} = \frac{\sqrt{1+i_{f(r)}}+1}{2}. \tag{6}$$

Expression (6) is independent of gate voltage, transistor dimensions, technology, and temperature. Therefore, (6) is a universal expression for MOS transistors, as the transconductance-to-current ratio is for bipolar transistors. Expression (6) is a very powerful tool for circuit design since it allows designers to compute the available transconductance-to-current ratio in terms of the inversion level i_f. Moreover, (6) provides a straightforward procedure for extracting the value of the normalization current, the most important parameter in our model. The value 3/2 for the ratio $I_F/(g_{ms}\phi_t)$, for instance, corresponds to $i_f = 3$, that is, $I_S = I_F/3$. This very simple extraction procedure of I_S is illustrated in Fig. 3 for two different values (3/2 and 2) of the current-to-transconductance ratio.

The universality of (6) is confirmed in Fig. 4, where measured and simulated current-to-transconductance ratios are plotted for different gate voltages, technologies, and channel lengths. The accuracy of (6) is excellent for any of these cases.

In general, transistors are driven by the gate rather than by the source. Therefore, the gate transconductance is a more useful definition for design purposes. Fig. 5 shows the ratio of the gate transconductance to current for both long-channel ($L = 8$ μm) and short-channel ($L = 0.8$ μm) MOS transistors from a CMOS technology. The results have been achieved at $V_D = V_G$. According to the curves in Fig. 5, the transconductance-to-current ratio for low and moderate current levels is fairly the same for both devices, while the short-channel MOSFET exhibits lower transconductance-to-current ratio for higher current levels. A discussion on short-channel effects can be found elsewhere [11].

C. Output Characteristics

Since the source (drain) transconductance $g_{ms(d)}$ is the derivative of $-(+)I_{F(R)}$ with respect to $V_{S(D)}$, the relationship between source (drain) voltage and forward (reverse) normalized current (last expression in Table I) is determined by integrating (6). In the last expression of Table I, $V_{S(D)} = V_P$ implies that $i_{f(r)} = i_P$; thus, the assigned value of parameter i_P defines V_P and should be chosen in the transition from weak to strong inversion. In this work, we have adopted $i_P = 3$, which corresponds to the condition at $V_S(D) = V_P$.

The choice of $Q'_{\mathrm{IS(D)}} = -nC'_{ox}\phi_t$ to define the pinchoff voltage is not occasional; rather, this point has been judiciously chosen since it represents the transition from weak inversion, where the transport mechanism is dominated by diffusion, to strong inversion, where the prevailing transport mechanism is drift. Substituting (1a) into (2), one can readily verify that the drift and diffusion components are equal at pinch off.

Fig. 6 shows the measured and simulated "common-gate" characteristics for a saturated ($V_D = V_G$) N-channel (N) MOS transistor of a 0.75-μm technology (oxide thickness of 280 Å) with $L = W = 25$ μm. The simulated curves have been determined from the first and last expressions in Table I (assuming that, in saturation, i_r is equal to zero) and the definitions of i_f and I_S in (4b) and (4c). An excellent matching between the experimental results and the proposed model is observed in all regions of operation.

Since the relationship between bias voltage and the normalized saturation current shown in Table I is not invertible in terms of elementary functions, approximations [11] of this expression where the current is an explicit function of the applied voltages are very useful for transistors driven by voltage signals. The approximation of [11] for the current-to-voltage relationship in a MOSFET can be simplified to $i_{f(r)} = [1 + \ln(1 + e^{(V_P - V_{S(D)})/\phi_t})]^2 - 1$.

The MOSFET output characteristics described by the universal relationship

$$\frac{V_{\mathrm{DS}}}{\phi_t} = \sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right) \tag{7}$$

are readily derived from the last expression in Table I. Expression (7) demonstrates that the normalized output characteristics of a long-channel MOSFET are independent of technology and

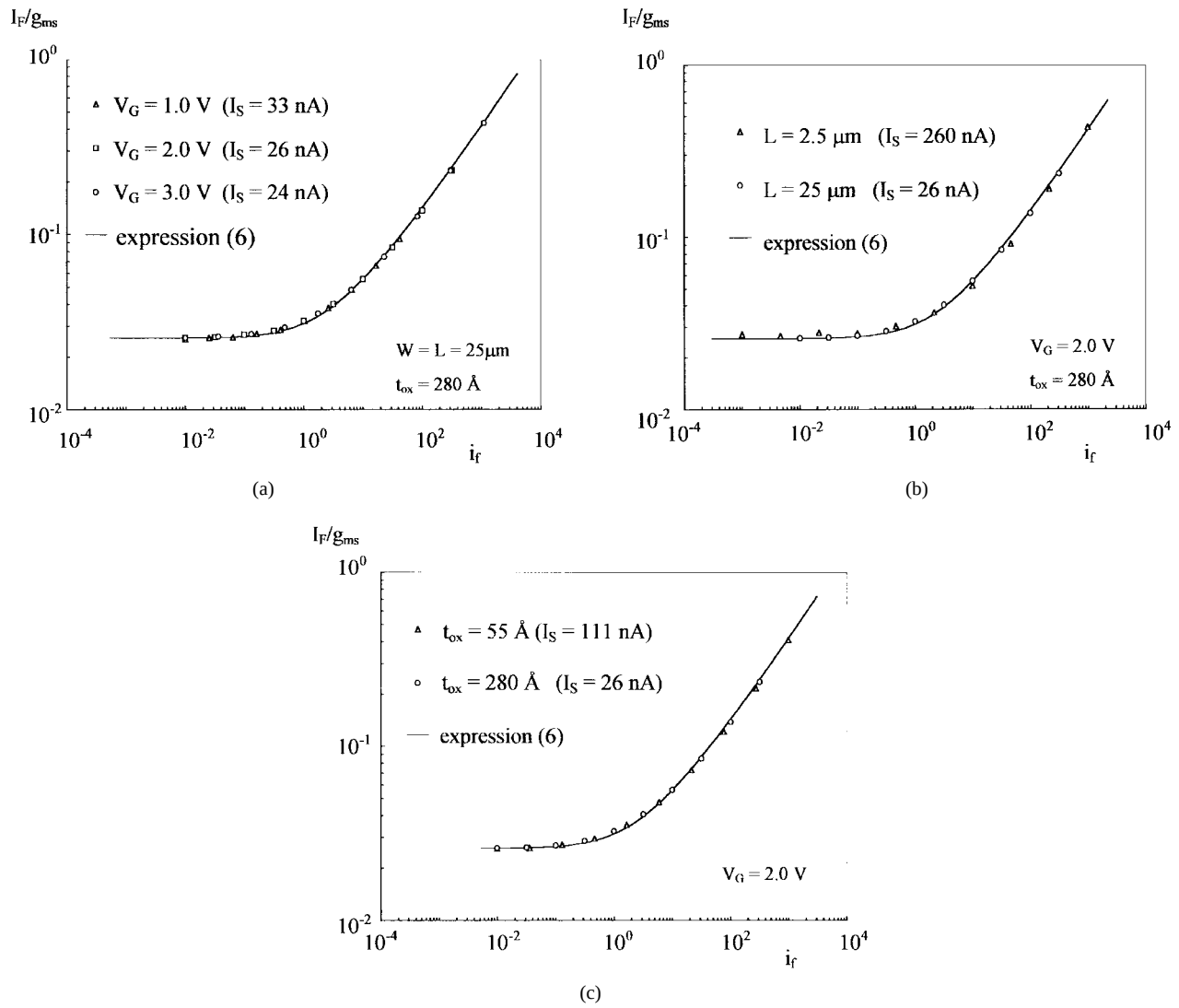

Fig. 4. Forward current-to-transconductance ration (I_F/g_{ms}) versus inversion coefficient of NMOS transistors: (a) biased at different gate voltages, (b) with different channel lengths, and (c) from different technologies.

transistor dimensions, corroborating again the universality and consistency of our model. In Fig. 7, we compare the measured output characteristics, for several gate voltages, and those simulated by (7).

In Fig. 8, we present the theoretical drain-to-source saturation voltage $V_{\rm DSsat}$, defined here as the value of $V_{\rm DS}$ for which the ratio $Q'_{\rm ID}/Q'_{\rm IS} = \varepsilon$, where ε is an arbitrary number much smaller than one. Therefore, from (4a) and (7)

$$V_{\rm DSsat} = \phi_t \left[\ln\left(\frac{1}{\varepsilon}\right) + \sqrt{1+i_f} - 1 \right]. \tag{8}$$

The definition in (8) is extremely useful for circuit design since it gives the boundary between the triode and saturation regions in terms of the inversion level. Note that in weak inversion, $V_{\rm DSsat}$ is independent of the inversion level, while in strong inversion, $V_{\rm DSsat}$ is proportional to the square root of the inversion level. Our definition of saturation is arbitrary but gives designers a very good first-order approximation to the minimum $V_{\rm DS}$ required to keep the MOSFET in the "constant current region."

D. Small Signal Parameters

Table I shows the expressions for the source (g_{ms}), drain (g_{md}), and gate (g_{mg}) transconductances, defined in [3] and [5] as the partial derivatives of $I_D(V_S, V_D, V_G)$ with respect to the source, drain, and gate voltages, respectively. Fig. 9 compares the measured and simulated values of the source and gate transconductances for the same device of Fig. 6, thus demonstrating the satisfactory precision of the proposed model.

The expressions for the ten intrinsic (trans)capacitances listed on Table I are obtained from the differentiation of the inversion (Q_I), depletion (Q_B), source (Q_S), and drain (Q_D) total charges with respect to the terminal voltages. One should recall that only nine of the 16 possible (trans)capacitance definitions are independent [2]. In Fig. 10, we compare some of the intrinsic transcapacitances calculated from the expressions presented in Table I and from the charge-sheet ϕ_S-formulated model of [7], which is already known to fit experiments very well.

It can be noticed that all small-signal parameters in Table I approximate to their well-known asymptotic values in weak

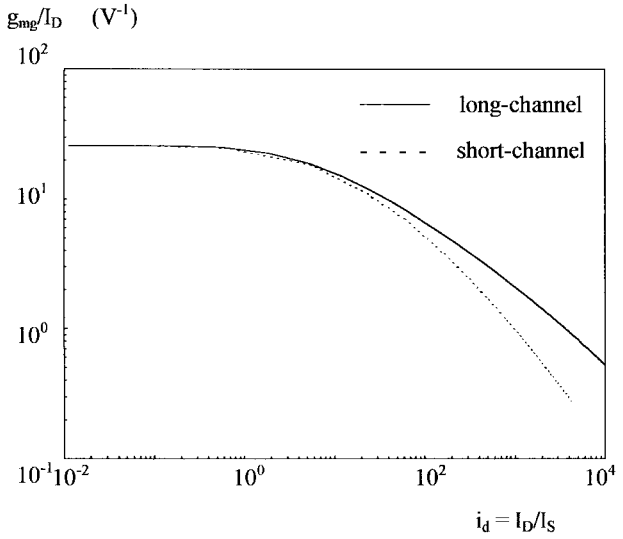

Fig. 5. Simulated gate transconductance-to-current ratio of long- and short-channel MOS transistors in saturation ($V_D = V_G$) versus normalized drain current.

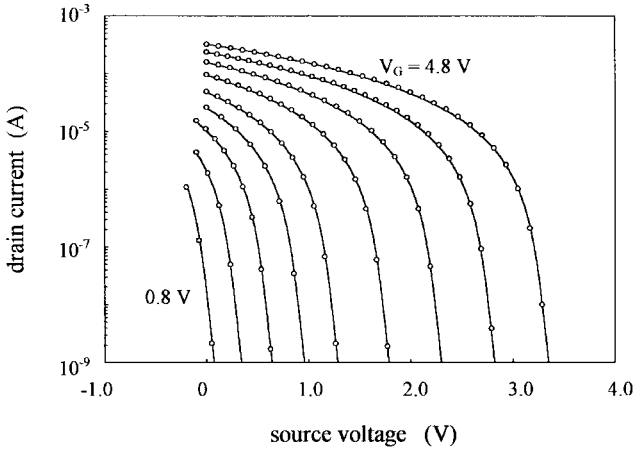

Fig. 6. Common-gate characteristics of an NMOS transistor in saturation, with $t_{ox} = 280$ Å and $W = L = 25$ μm ($V_G = 0.8, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2$, and 4.8 V). (—) simulated curves calculated from Table I; (o) measured curves.

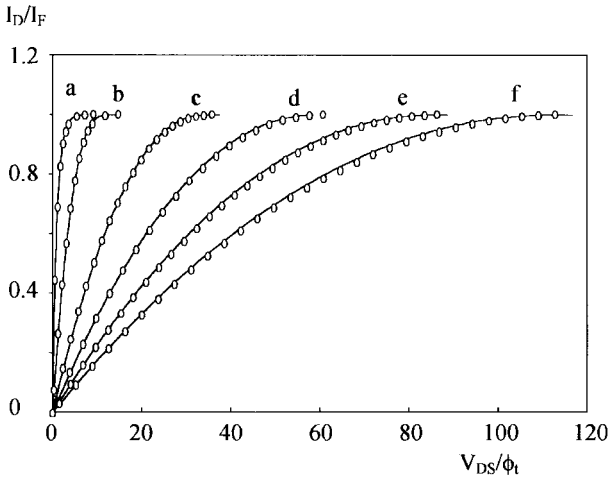

Fig. 7. Normalized output characteristics (NMOS transistor, $t_{ox} = 280$ Å and $W = L = 25$ μm). I_F has been measured for $V_D = V_G$ and $V_S = 0$. **O**: measured data, —: calculated from (7). (a) $i_f = 4.5 \times 10^{-2} (V_G = 0.7$ V). (b) $i_r = 65 (V_G = 1.2$ V). (c) $i_f = 9.5 \times 10^2 (V_G = 2.0$ V). (d) $i_f = 3.1 \times 10^3 (V_G = 2.8$ V). (e) $i_f = 6.8 \times 10^3 (V_G = 3.6$ V). (f) $i_f = 1.2 \times 10^4 (V_G = 4.4$ V).

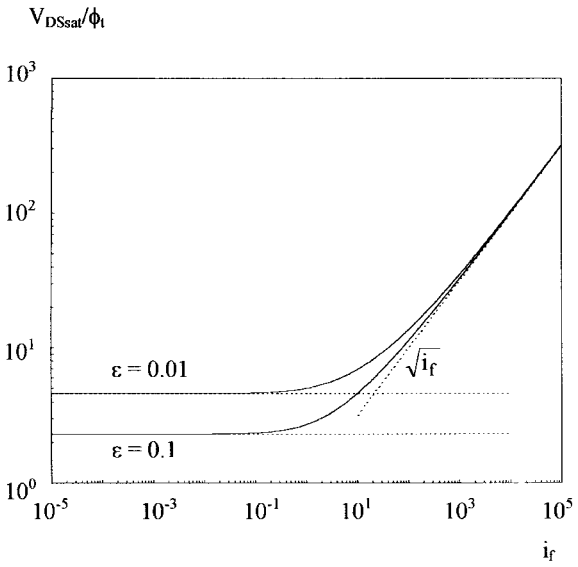

Fig. 8. Saturation drain-to-source voltage computed for $\varepsilon = 0.01$ and $\varepsilon = 0.1$ versus inversion coefficient.

and strong inversion [3]. For instance, deep in weak inversion, that is, for $i_f \ll 1$, $\sqrt{1+i_f}$ can be approximated by $1+i_f/2$. Therefore, g_{ms} (Table I) tends to its expected value, I_F/ϕ_t. On the other hand, in very strong inversion, g_{ms} is proportional to $\sqrt{I_F}$ since i_f is much greater than one.

The small-signal parameters in Table I describe the MOSFET behavior in quasi-static operation, being suitable for low- and medium-frequency analysis. The frequency limits of validity for this quasi-static approach are discussed in the Appendix, where a nonquasi-static model is presented.

IV. Transistor Sizing for Circuit Design

Analog circuit designers need to determine bias current and transistor dimensions in order to satisfy design specifications such as gain and cutoff frequency.

The substitution of (4b) into (6) allows writing

$$I_S = \frac{I_F}{4\dfrac{I_F}{\phi_t g_{ms}}\left(\dfrac{I_F}{\phi_t g_{ms}} - 1\right)}. \tag{9}$$

The substitution of (4c) into (9) allows expressing the transistor aspect ratio (W/L) as

$$\frac{W}{L} = \frac{g_{ms}^2}{2\,\mu n C'_{ox} I_F}\left(\frac{1}{1 - \dfrac{\phi_t g_{ms}}{I_F}}\right). \tag{10a}$$

The term outside the parentheses in the right-hand side of (10a) corresponds to the approximation used to determine the

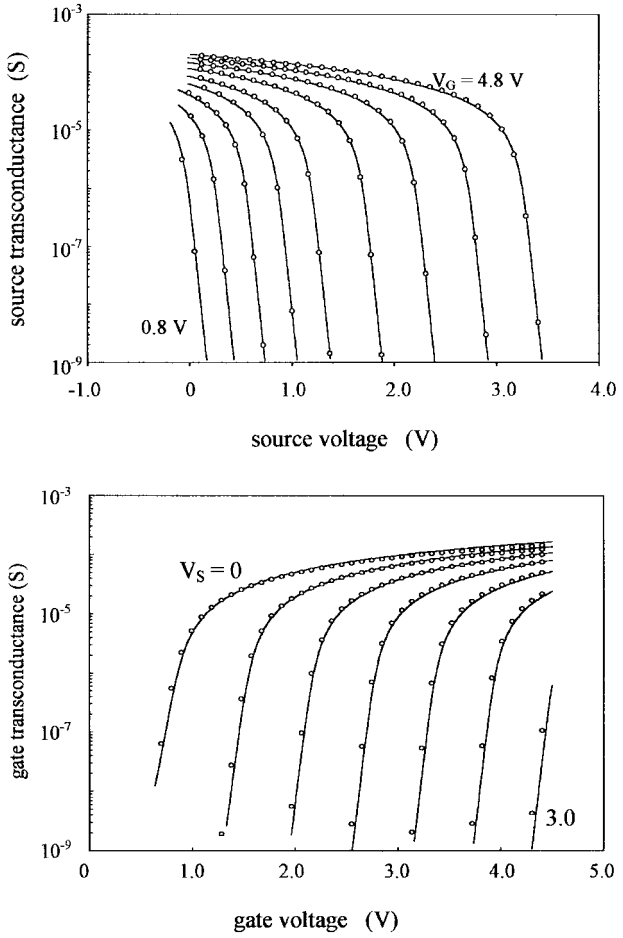

Fig. 9. (a) Source transconductance ($V_G = 0.8$, 1.2, 1.6, 2.0, 2.4, 3.0, 3.6, 4.2, and 4.8 V) and (b) gate transconductance ($V_S = 0$, 0.5, 1.0, 2.0, 2.5, and 3.0 V) of an NMOS transistor with $t_{ox} = 280$ Å and $W = L = 25$ μm. (—) simulated curves calculated from Table I; (o) measured curves.

aspect ratio in the strong inversion region. The factor in parentheses provides a correction in weak and moderate inversion, which allows (10a) to be valid in the entire inversion regime. For $i_f = 100$ (transition from moderate to strong inversion), a significant error of 20% results for the determination of W/L if the term in parentheses in (10a) is not taken into account. An alternative expression for the geometric ratio is obtained by substituting (6) into (10a)

$$\frac{W}{L} = \frac{g_{ms}}{\mu n C'_{ox} \phi_t} \frac{1}{\sqrt{1+i_f}-1}. \tag{10b}$$

Introducing i_f as a design variable is very useful. The designer can readily sketch the area consumption, (10b), and the bias current, (6), in terms of the inversion level and decide on a satisfactory solution to his specific design.

Even though it is possible to choose the inversion level, the designer should be aware of the frequency capability of the transistor, which is most often specified in practice by the intrinsic cutoff frequency f_T. The intrinsic cutoff frequency of an MOS transistor is defined as the frequency value at which the short-circuit current gain in the common-source configuration drops to one [2]. The intrinsic cutoff frequency

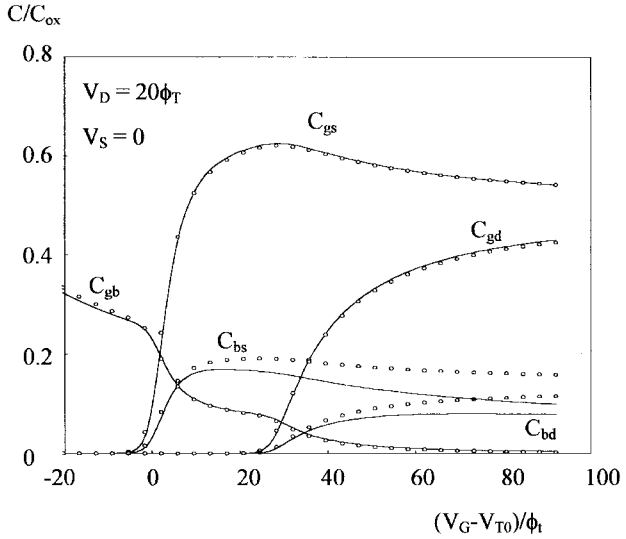

Fig. 10. Intrinsic capacitances simulated from (—) our quasi-static model described in Table I; (o) the ϕ_S-formulated model of [7]. (NMOS transistor with $t_{ox} = 250$ Å, $N_A = 2 \times 10^{22}$ m^{-3} and $V_{T0} = 0.7$ V.)

of a MOSFET in saturation is [2] given by

$$f_T = \frac{g_{mg}}{2\pi(C_{gs}+C_{gb})} = \frac{g_{ms}}{2\pi n(C_{gs}+C_{gb})}. \tag{11a}$$

From the expressions of g_{ms}, C_{gs}, and C_{gb} presented in Table I, f_T can be readily written in terms of the inversion coefficient as

$$f_T = \frac{\mu n \phi_t}{2\pi L^2} \cdot \frac{i_f\left(\sqrt{1+i_f}+1\right)}{(n-1)\left(\sqrt{1+i_f}+1\right)^2 + \frac{2}{3}\left(i_f+\sqrt{1+i_f}-1\right)}. \tag{11b}$$

The first term in the right-hand side of (11b) shows the dependence of f_T on the channel length and on the slope factor and mobility, both slightly dependent on technology and on gate voltage. The second term represents the dependence of the cutoff frequency on the inversion level. Usually, due to the lack of adequate models, designers employ transistors whose f_T is much higher than that required for a specific application, thus leading to an unnecessary increase in power consumption.

Assuming the slope factor n in the denominator of (11b) to be equal to 4/3, a typical value, f_T can be roughly approximated to

$$f_T \cong \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_f}-1\right) \tag{11c}$$

for any inversion level.

Fig. 11 shows the intrinsic cutoff frequency calculated from (11b), for $n = 4/3$ and $n = 5/3$, and from (11c), for a large range of values of the inversion coefficient.

V. Application to the Design of a Common-Source Amplifier

Let us illustrate the application of our model to the design of the basic common-source amplifier in Fig. 12. The

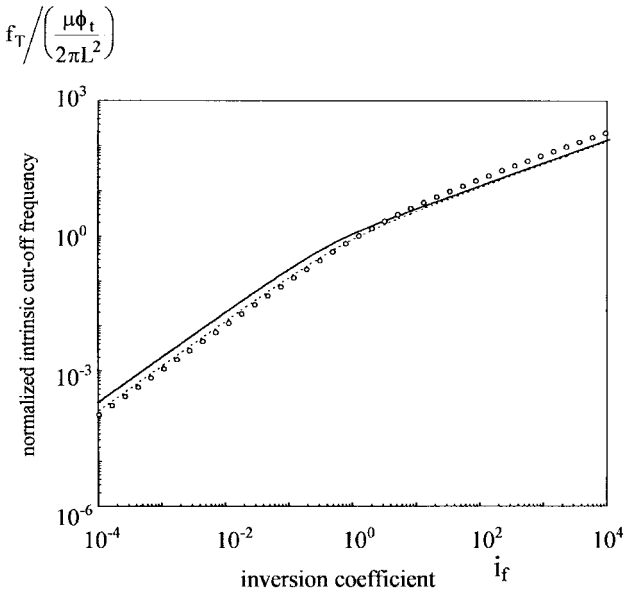

Fig. 11. Normalized intrinsic cutoff frequency. (—) with $n = 4/3$; (– – –) with $n = 5/3$; and (o) expression (11c).

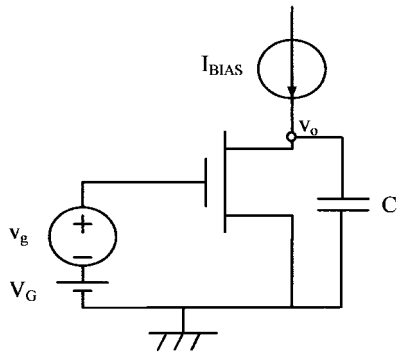

Fig. 12. Basic MOSFET common-source amplifier.

specifications for this design are: a gain-bandwidth product (GBW) equal to 100 MHz and a capacitive load (C) of 10 pF. The channel length of the transistor is equal to 0.75 μm, the minimum allowable value for the technology under consideration (oxide thickness $t_{ox} = 280$ Å). We assume that the electron mobility and the slope factor are equal to 520 cm^2 V/s and 1.25, respectively. One should determine the size of the transistor and the biasing current.

An approximate expression for the GBW of the capacitively loaded amplifier in Fig. 12 is

$$\text{GBW} \cong \frac{g_{mg}}{2\pi C} \cong \frac{g_{ms}}{2\pi n C}. \tag{12}$$

From (12) and the specified values of C and GBW, we obtain $g_{ms} = 7.9$ mS. By introducing this value of g_{ms} into (6) and (10b), we obtain the curves in Fig. 13, which show the required bias current and aspect ratio in terms of the inversion level.

The choice of a value for i_f in the moderate inversion region represents a tradeoff between area and power consumption [4]. Small values of i_f require large aspect ratios, as shown in Fig. 13. Thus, operation in weak inversion is expensive in silicon real estate. On the other hand, operation in strong

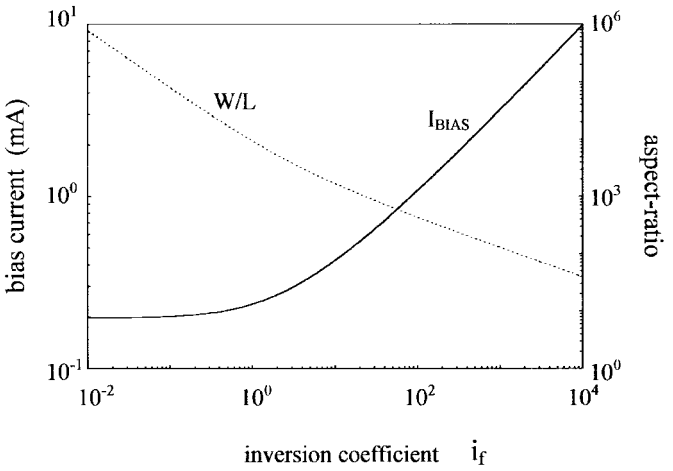

Fig. 13. Bias current and aspect ratio versus inversion coefficient for the design specifications of the common-source amplifier in Section V.

inversion is power consuming owing to the low value of the transconductance-to-current ratio (6), which also results in a small value for the voltage gain.

By assuming that the intrinsic cutoff frequency of the transistor must be greater than, say, three GBW, we can determine a lower limit for the inversion level. In fact, for frequencies above $f_T/3$, the quasi-static considerations in deriving the model of Table I may be no longer valid [2] in moderate and strong inversion. Moreover, the extrinsic capacitance due to drain diffusion can be prohibitively large for low inversion levels (large areas). From (11b), $f_T > 300$ MHz for $i_f > 0.94$. This means that, in this example, the bias current (I_F) should be greater than 244 μA and the aspect ratio (W/L) should be smaller than 9600.

The lower limit for the output voltage can be assumed to be equal to the drain-to-source saturation voltage [8]. From Fig. 8, $V_{\text{DSsat}} = 5\phi_t$ results for $i_f = 0.94$, assuming $\varepsilon = 0.01$.

VI. Conclusions

An accurate MOSFET model valid in weak, moderate, and strong inversion has been presented. All the device characteristics are expressed as single-piece functions of the saturation components of the drain current. A physics-based law for the current-to-transconductance ratio in the MOSFET has been derived and experimentally verified. A compact expression for sizing MOSFET's has been derived from this law. The model presented is a powerful tool that can be used for both hand calculations and computer-assisted analysis and design of MOSFET integrated circuits.

Appendix
Non-Quasi-Static Operation

The small-signal parameters listed in Table I are valid for low and medium frequency analysis. A complete nonquasi-static model, suitable for high-frequency operation, can be derived by taking into account the continuity equation [2], [9]

$$\frac{\partial i_I(x,t)}{\partial x} = W\frac{\partial q_I'(x,t)}{\partial t} \tag{A-1a}$$

TABLE II
EXPRESSIONS FOR THE MOSFET NONQUASI-STATIC MODEL

Variable	Expression
y_{gs}	$-j\omega C_{gs}\frac{1+j\omega\tau_2}{1+j\omega\tau_1}$
y_{gd}	$-j\omega C_{gd}\frac{1+j\omega\tau_3}{1+j\omega\tau_1}$
$y_{gb}=y_{bg}$	$-j\omega C_{gb}\frac{1+j\omega\tau_4}{1+j\omega\tau_1}$
$y_{bs(d)}$	$(n-1)y_{gs(d)}$
y_{ds}	$-\frac{g_{ms}}{1+j\omega\tau_1}$
y_{dd}	$\frac{g_{md}}{1+j\omega\tau_1}-ny_{gd}$
y_{dg}	$-\frac{y_{ds}+y_{dd}}{n}$
τ_1	$-\frac{C_{sd}}{g_{md}}=\frac{L^2}{\mu\phi_t}\frac{4}{15}\frac{2+i_f+3\sqrt{1+i_f}\sqrt{1+i_r}+i_r}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^3}$
$\tau_{2(3)}$	$\frac{L^2}{\mu\phi_t}\frac{1}{15}\frac{2(1+i_{f(r)})+8\sqrt{1+i_f}\sqrt{1+i_r}+5(1+i_{r(f)})}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^2\left(\sqrt{1+i_{f(r)}}+2\sqrt{1+i_{r(f)}}\right)}$
τ_4	$\frac{C_{ox}\tau_1-C_{gs}\tau_2-C_{gd}\tau_3}{C_{ox}-C_{gs}-C_{gd}}$

$C_{ox}=WLC'_{ox}$

where $i_I(x,t)$ is the time-varying inversion channel current, no longer supposed to be constant along the channel length, and q'_I is the time-varying inversion charge density. The time-varying version of (2) together with approximation (1a) leads to

$$i_I(x,t)=-\frac{\mu W}{nC'_{ox}}(q'_I(x,t)-nC'_{ox}\phi_t)\frac{\partial q'_I(x,t)}{\partial x}. \quad \text{(A-1b)}$$

The set of expressions (A-1) can be solved either numerically or by an iterative procedure such as the one proposed in [10] and applied in [9]. The method of [10] allows deriving approximate expressions of the (trans)admittances for any desired order (highest exponent of the frequency in the denominator). For instance, by applying this method to solve (A-1) up to first order, we obtain the nine independent (trans)admittances presented in Table II. The expressions of this table are similar to the corresponding ones derived in [9]. However, the nonquasi-static parameters shown in Table II are expressed in terms of the forward and reverse normalized currents, while the parameters in [9] are functions of the surface potentials at source and drain.

The first-order time constant τ_1, the coefficient of $j\omega$ in the denominator of the transadmittances in Table II, for a saturated MOSFET is given by

$$\tau_1=\frac{L^2}{\mu\phi_t}\frac{4}{15}\frac{2+i_f+3\sqrt{1+i_f}}{\left(\sqrt{1+i_f}+1\right)^3} \quad \text{(A-2)}$$

which can be approximated to

$$\tau_1=\frac{L^2}{\mu\phi_t}\frac{1}{5}\frac{1}{\sqrt{1+i_f}} \quad \text{(A-3)}$$

with maximum deviations of 25 and 20% in strong and in very weak inversion, respectively. Fig. 14 illustrates the variation of the time constant τ_1 in saturation, with the forward normalized current. Since the intrinsic cutoff frequency is proportional to $\sqrt{1+i_f}-1$, the nonquasi-static correction is significant only for moderate and strong inversion. In weak inversion, the quasi-static model presented in Table I predicts dynamic operation with satisfactory precision at frequencies up to the intrinsic cutoff frequency. In moderate and strong inversion, the applicability of the quasi-static model should be restricted

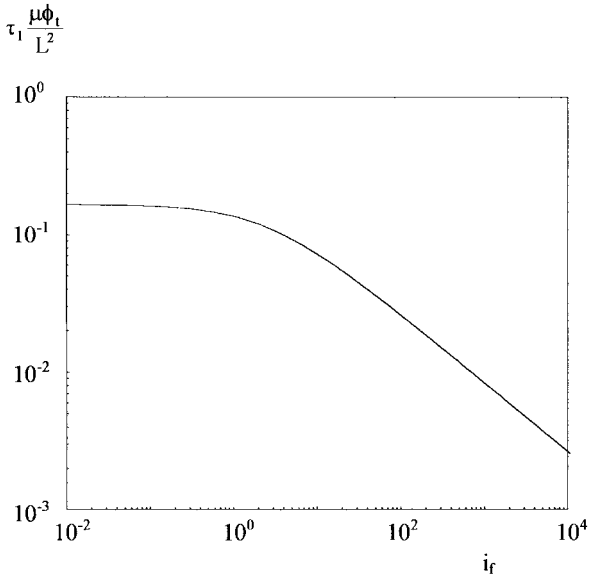

Fig. 14. Normalized first-order time constant τ_1 in saturation.

to frequency values up to one-third of the intrinsic cutoff frequency [2].

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