ured in the same frequency range. The power of the distortion introduced by bandlimiting the modulator output with a digital lowpass filter of bandwidth ω_0 will be smaller than the out-of-band quantisation noise power. As a practical consequence, we may use a lowpass digital filter to decode the output of the modulator provided that that the spectrum of the logarithm of the input signal decays with frequency and that the oversampling ratio is high enough to ensure the required SNR.

For example, the signal:

$$\log[K_1 + K_2 \cdot \sin(\omega \cdot n)] \quad K_1 \geq 1,\ K_2 < 1,\ \omega = \frac{p}{q}\pi \quad (2)$$

where p and q are integers, has a discrete spectrum consisting of tones located at DC, ω and its harmonics. The amplitudes of the harmonics decrease when expressed in logarithmic units. Fig. 2*a* shows the modulus of the first 512 bins of a 32K point FFT of $\log_2 x[n]$, where

$$x[n] = \frac{5}{4} + \frac{3}{8} \cdot \sin\left(\frac{\pi}{512}n\right) \quad (3)$$

We will analyse a single bit version of the modulator, using b = 2 as the logarithm basis. The logarithmic ADC of Fig. 1*b* will encode inputs above one as +1 and inputs below one as −1, regardless of the value of A. This is the equivalent situation to a single bit quantiser that computes the sign of the input magnitude in a conventional sigma-delta modulator. The output of the exponential DAC will map symbol +1 into an electrical magnitude with weight 2^{-A} and symbol −1 into an electrical magnitude with weight 2^{A}.

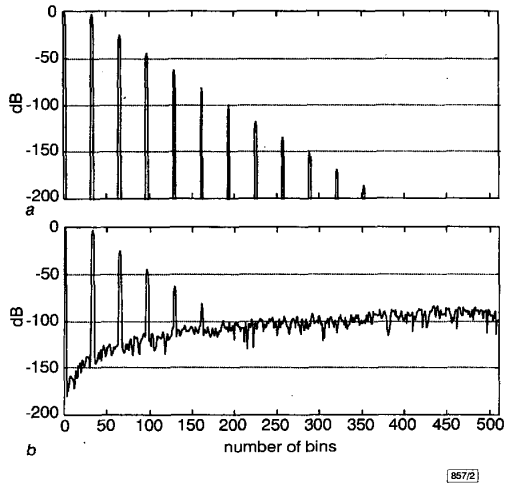

Fig. 2 *Fast Fourier transform plots*

a FFT of $\log_2 x[n]$
b FFT of modulator output

Assuming A = 1, we can use eqn. 3 as a test signal that complies with the stability constraints and the spectral requirements discussed before. Fig. 2*b* shows the equivalent data shown in Fig. 2*a* computed for the output of the modulator. If an oversampling ratio of 256 is used, the SNR achieved is 92dB. The distortion introduced by bandlimiting $\log_2 x[n]$ in eqn. 3 to $\pi/256$ is negligible compared to the out-of-band quantisation noise.

The feedback DAC and multipliers MD_1 and MD_2 may be combined into two gain stages with discrete gain values selected by $y[n]$. In a single-bit, switched-capacitor implementation, the two reciprocal gain values b^{-A} and b^{A} may be implemented by swapping the roles of the feedback and input capacitors in any of the classical switched capacitor gain circuits [5]. The dynamic range of the state variables of the simulation shown in Fig. 2*b* was measured as the ratio between their maximum and minimum values. The dynamic range of the variables designated as $v_1[n]$ and $v_2[n]$ in Fig. 1*b* was 25 and 49dB, respectively.

Any mismatch in the generation of b^{A} and its reciprocal will correspond with gain and offset errors in the feedback path of the equivalent sigma-delta modulator. This situation is equivalent to that of a single-bit sigma-delta modulator in which the two quantisation levels of the feedback DAC are misplaced and add offset to the input signal.

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Sound design of low power nested transconductance-capacitance compensation amplifiers

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An amplifier design approach is presented which is based on an all region MOS transistor model. Low power analogue circuits are designed using the presented approach. For illustrative purposes a nested transconductance-capacitance compensated (NGCC) operational amplifier is designed. Verification was carried out using a CMOS chip prototype which yields an op-amp with 105dB gain, a 1.05MHz gain-bandwidth product, 0.28mW power consumption and 0.137mm² active area for a 2V supply voltage and 10kΩ/20pF load.

Introduction: Low voltage circuits pose serious challenges to designers; in particular, cascoding is no longer a suitable solution for increasing the gain of amplifiers. For high gain amplifiers, multistage cascading along with multiple feedback loops is normally required [1]. In the work described in this Letter, the NGCC topology [2], which is similar to the nested Miller compensation topology [3], was applied to implement high-gain amplifiers.

To reduce power consumption, transistors must operate closer to weak inversion. To achieve this, however, the transistor area needs to be made prohibitively large. A balance between power and area can be obtained under moderate inversion [4].

In this Letter, we discuss how to design analogue circuits using an all region MOS transistor model. For illustration purposes both three- and a four-stage NGCC amplifiers have been designed to operate under moderate inversion by using the transistor model from [5]. With identical performance, our low power amplifiers exhibit a power saving of 80% compared to the op-amp reported in [2], which has been designed to operate under strong inversion.

All region current-based MOSFET model: A current-based MOSFET model, which has a continuous single expression applicable for any region of operation, has been used in the design of our amplifiers; a detailed description of the model can be found in [5]. The main design equations for specific application to amplifiers are as follows [4, 5]:

$$I/\phi_t g_m n = \left(1 + \sqrt{1 + i_f}\right)/2 \quad (1)$$

$$\frac{W}{L} = \frac{g_m}{\mu C_{ox}\phi_t} \frac{1}{\sqrt{1 + i_f} - 1} \quad (2)$$

$$V_{DSSAT} \simeq \phi_t\left[\left(\sqrt{1 + i_f} - 1\right) + 4\right] \quad (3)$$

where n is the slope factor, ϕ_t is the thermal voltage, $i_f = I/I_s$ is the inversion level, while $I_s = \mu n C_{ox} \phi_t^2 W/2L$ is the normalisation current. The other symbols have their usual meanings.

Eqns. 1–3 are valid from weak inversion ($i_f < 1$) up to strong inversion ($i_f \gg 1$) and show that i_f plays a key role in design applications. Given the transistor transconductance, the dimensions can be determined by specifying either the inversion level or the drain current. As can be readily noticed from eqn. 2, the transistor area increases dramatically as the weak inversion region is approached [4].

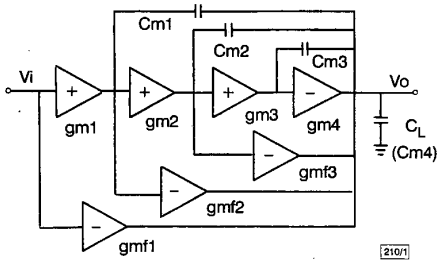

Fig. 1 *Four-stage NGCC amplifier topology*

Implementation of NGCC amplifiers: The architecture of a four-stage NGCC amplifier is shown schematically in Fig. 1. Along with Miller capacitors for pole splitting, additional feedforward stages $g_{mf1}(= g_{m1})$, $g_{mf2}(= g_{m2})$ and $g_{mf3}(= g_{m3})$ are used to cancel out the right half plane zeros introduced by the Miller capacitors. The amplifier transfer function [2] is

$$\frac{V_o(s)}{V_i(s)} = \frac{-A_0}{\left(1 + \frac{A_0 s}{f_1}\right)\left(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3} + \frac{s^3}{f_2 f_3 f_4}\right)} \quad (4)$$

where $A_o = k_1 k_2 k_3 k_4$, $k_i = g_{mi}/g_{oi}$ and $f_i = g_{mi}/C_{mi} \cdot g_{oi}$ is the output conductance of the ith stage and f_1 is the gain bandwidth product. Low values for C_{mi} would not be appropriate; otherwise, the frequency response of the amplifier would become very sensitive to parasitic capacitances and, thus, very unpredictable. High values for C_{mi} would lead to a significant increase in power consumption. Both three- and four-stage amplifiers have been designed to operate under moderate inversion to meet the specifications in Table 1 and a 0.2% settling time $T_s < 1\mu s$.

Table 1: Experimental results of NGCC amplifiers (V_{DD} = 2V, Z_{LOAD} = 10kΩ/20pF)

	Specifications	Three-stage	Four-stage	Four-stage [2]
Power consumption	Minimum	0.26mW	0.28mW	1.4mW
DC gain	≥ 100dB	~96dB	~105dB	~100dB
Gain bandwidth	1.0MHz	1.10MHz	1.05MHz	1.0MHz
Phase margin	> 60°	56.7°	62.0°	58°
THD (1kHz $1V_{p-p}$)		–67.7dB	–67.5dB	–70dB
1% THD input (1kHz)		1.13V	1.1V	–
Active area (relative area)		0.104mm² (1)	0.137mm² (1.32)	0.22mm² (2.11)

The four-stage amplifier is shown in Fig. 2. With the aid of a settling time analysis [2], we chose, $f_2 = 2f_1$, $f_3 = 5f_1$ and $f_4 = 6f_1$. Given $C_{m1} = C_{m2} = C_{m3} = 8$pF, the dimensions and inversion levels of the transistors are summarised in Table 2. The condition $g_{mf2} = g_{m2}$ implies that transistors M6 and M11 should be very closely matched. M5 is the parallel association of two transistors identical to M3; thus $g_{mf1} = g_{m1}$. To avoid large transistor area and save power, the amplifiers were designed to operate under moderate inversion. Choosing $i_f = 6$ ($V_{DSSAT} \simeq 150$mV) for M_{IN1} and M_{IN2}, and substituting this value along with g_{m1} into eqn. 1 gives the drain current. The aspect ratio of M_{IN1} (or M_{IN2}) can be calculated from eqn. 2. For all other PMOS transistors in the current mirrors, we have chosen $i_f = 30$ ($V_{DSSAT} \simeq 220$mV) to enable them to operate closer to strong inversion for better matching. Details of the design of the three-stage amplifier can be found elsewhere [6].

The frequency response of the four-stage amplifier, fabricated in a 1.2μm AMI n-well CMOS process, is shown in Fig. 3. The response of the four-stage low power op-amp to a 100mV step input is shown in Fig. 4. The measured results are summarised in Table 1.

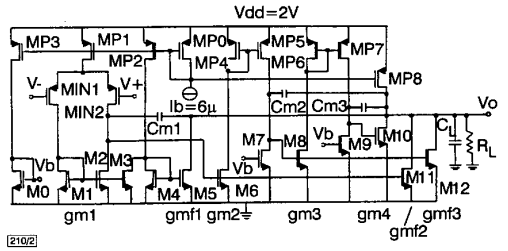

Fig. 2 *Implementation of four-stage NGCC amplifier*

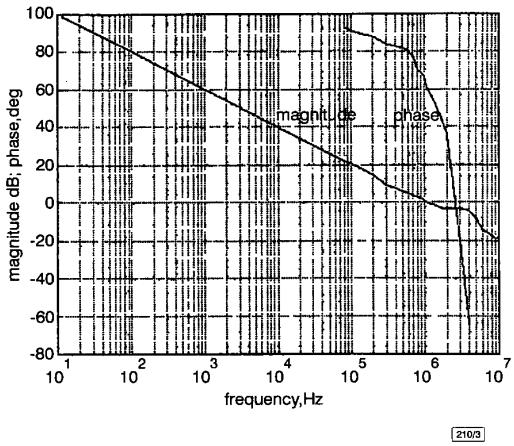

Fig. 3 *Frequency response of the four-stage NGCC amplifier*

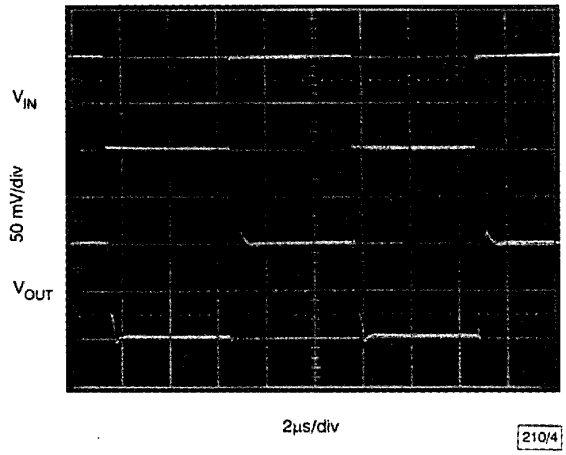

Fig. 4 *Response of unity gain four-stage NGCC amplifier to 100kHz, 100mV step input*

Table 2: Widths and inversion levels of transistors of the four-stage amplifier (L = 1.8μm)

Transistor	W	i_f	Transistor	W	i_f
	μm				
M_1–M_4	4×10.8	6	M_{IN1}, M_{IN2}	8×18	6
M_0, M_5–M_7, M_{11}	8×10.8	6	M_{P0}, M_{P5}	2×18	30
M_8, M_9, M_{12}	20×10.8	6	M_{P6}, M_{P7}	5×18	30
M_{10}	60×10.8	6	M_{P8}	24×18	30

Conclusions: By using an all region MOSFET model, analogue circuits can be optimally designed. In particular, NGCC amplifiers have been designed to operate under moderate inversion yielding

an optimal design. Experimental results have confirmed high accuracy of this model in calculating the transistor dimensions and transconductance. The four-stage amplifier has demonstrated a better overall performance than the three-stage amplifier, but the design of the latter is simpler. With identical or better performance, our low power amplifiers designed to operate at moderate inversion lead to a power saving of 80% compared to the op-amp reported in [2].

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Square wave driver for extremely low resistance and low frequency loads

R.B. Givens

A technique is presented for allowing efficient generation of high currents at low voltage and at frequencies ranging from DC to ~100Hz.

Efforts to generate high currents (of several amps) at a potential of < 1V and at frequencies ranging from DC to ~100Hz inevitably result in power supply systems which are too large, too heavy, and too inefficient for practical battery-powered portable systems. Even for systems where efficiency is not a major concern, the physical size of the transformer becomes impractical as the frequency requirement decreases into the sub-kilohertz range. For the specific case where a high current DC source is required, smaller transformers operating at higher frequencies with subsequent rectification can be used. However, when low output voltages are required, a considerable fraction of the power is lost in the rectifying diodes. In this Letter, a simple and somewhat unconventional technique will be presented which allows efficient generation at high currents, low voltage and at frequencies (square wave) from DC to ~100Hz.

A high current, low voltage, low frequency source became necessary for the construction of a large visual demonstration model of a miniature xylophone magnetometer [1 – 4] recently invented in our laboratory. The transducer in the demonstration magnetometer consists of a 15in long brass bar mounted at the two nodal points expected for its fundamental mechanical mode. An alternating current at the frequency of this resonant mode is then passed through the bar via leads connected at the nodal points causing it to vibrate when in the presence of a magnetic field. It was determined that a supply yielding nominally 8A at 0.2V and 10Hz was required for proper operation. For a portable device that could be carried in a briefcase, the power supply had to be small, lightweight, and powered by a few flashlight cells using no more current than a flashlight bulb.

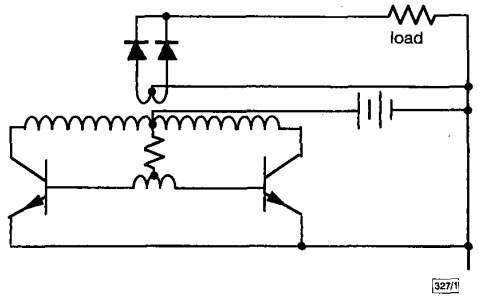

Fig. 1 *Conventional DC-DC converter (simplified)*

In the design presented in Fig. 1, the DC voltage from the battery (9V) is chopped at around 500Hz using a conventional astable oscillator arrangement. As the natural resonance frequency of this oscillator was relatively high, the size and weight of the transformer could be kept correspondingly small. The transformer was wound on a torroid iron core of approximately 1.0in (inner diameter) × 1.25in (outer diameter) × 0.25in and has 280 turns centre-tapped on the primary and eight turns centre-tapped on the secondary for a ratio of 35:1.

This Letter focuses on the way in which the 500Hz output is converted to DC or low frequency AC. Fig. 1 shows a typical (simplified) DC-DC converter with silicon diode rectifiers. At low output voltages (< 1V), the voltage drop across the diodes can result in 50% or more of the power being lost. In Fig. 2, *n*-channel HexFet transistors have been substituted for the traditional silicon rectifiers. Using synchronised rectification (where the HexFets are alternately turned on and off with respect to transformer voltage polarity), the HexFets significantly reduce the power losses associated with the 0.6V dropped across the silicon diodes. For example, for a typical HexFet transistor (IRL3803) with an 'on resistance' of 0.006 Ω, the voltage drop is only 0.06V at 10A. This is easily one tenth of the power lost using a silicon diode. Additional transistors can be added in parallel, if even lower loss is desired.

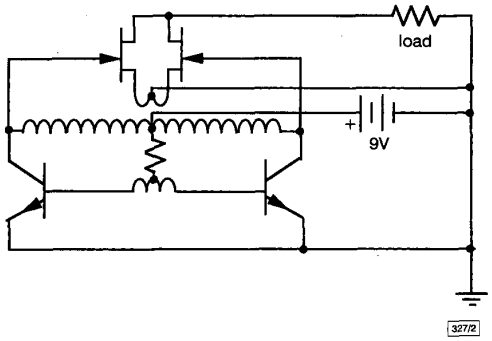

Fig. 2 *Typical synchronous DC-DC converter with rectifier diodes replaced by HexFet transistors*

When the output is 0.5V or less, it is quite easy to change the output polarity of this rectified source by simply inverting the phase of the gate drive going to the two Hexfets. Although somewhat unconventional, this technique takes advantage of the fact that for low voltages (< 0.5V), these transistors can be used reversibly. Therefore, to reverse output polarity, one merely has to reverse the connections between the HexFet gates and the primary winding. This is accomplished manually or as shown in Fig. 3 by using an exclusive OR gate. The output polarity is then determined by applying 1 or 0 to the control input on the exclusive OR. In the demonstration magnetometer described above, a