OPTIMUM DESIGN OF MOS AMPLIFIERS

R. L. Oliveira Pinto, Márcio Cherem Schneider and Carlos Galup-Montoro

Laboratório de Circuitos Integrados (LCI) - Departamento de Engenharia Elétrica - UFSC
C.P. 476 - CEP 88040-900 Florianópolis - SC - Brasil

E-mail: carlos@eel.ufsc.br

Abstract

This paper presents a design procedure for MOS amplifiers based on a universal model of the MOSFET, valid from weak to strong inversion. A set of very simple expressions allows quick design by hand as well as an evaluation of the design in terms of power consumption and silicon real estate. It is shown that in most cases there is an optimum bias in moderate inversion for which the attainable DC gain is maximum. The design and measurements on a common-source amplifier illustrate the appropriateness of the proposed methodology.

1. Introduction

In high frequency analog circuits, MOS transistors are often biased in strong inversion in order to have a high transition frequency f_T [1]. On the other hand, the current efficiency, given by the transconductance over drain current ratio (g_m/I_D), reaches its maximum when MOS transistors operate in weak inversion [2]. Usually, the design trade-off for MOS amplifiers is formulated in terms of the gate voltage overdrive. A classical rule is that a suitable range for analog design is obtained with V_{GS}-$V_{TH}\approx 100,\ldots,500$mV [3, 4]. An alternative formulation is to say that the best compromise between consumption and speed is achieved in moderate inversion [5, 6]. Consequently, conventional MOSFET models developed for either weak inversion or strong inversion are not well suited for optimizing analog design.

In analog circuits, the choice of the channel length of the MOS transistor results from a balance between voltage gain and frequency response. While the transition frequency is maximum for minimum channel length [7], the attainable voltage gain is roughly proportional to the channel length [2].

In this paper we will present a design methodology for MOS amplifiers using the universal MOSFET model developed in [7], which employs the bias current as the key variable. The design procedure proposed in this paper accounts for the specifications of capacitive load (C_L), gain-bandwidth product (GBW), DC voltage gain and voltage swing. It allows the designer to choose the bias current and transistor dimensions from closed expressions. The design approach proposed here, which has been applied to the design of common-source amplifiers, can be extended to more complex topologies such as differential and operational amplifiers.

2. MOSFET MODEL

The following set of equations developed in [7] can be readily used for the design of MOSFETs operating in saturation:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_d}} \qquad (1.a) \qquad i_d = \frac{I_D}{I_S} \qquad (1.b)$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \qquad (1.c)$$

$$f_T \cong \frac{\mu \phi_t}{2\pi L^2} 2\left(\sqrt{1+i_d}-1\right) \qquad (2) \qquad \frac{V_{DSsat}}{\phi_t} \cong \left(\sqrt{1+i_d}-1\right)+4 \qquad (3)$$

(1.a) is a universal relationship for MOSFETs, independent of technology, dimensions and temperature. I_S, the normalization current, depends on both the aspect ratio and technological parameters: mobility μ, oxide capacitance per unit area C'_{ox}, ϕ_t is the thermal voltage and n is the slope factor, which is slightly greater than one [7]. i_d is the normalized drain current or inversion level [7]. The transconductance-to-current ratio of MOSFETs is given by (1.a). Recalling that $\phi_t g_m/I_C=1$ for bipolar transistors, the collector current I_C is uniquely defined for a given g_m. However, in a MOSFET design, the specification of g_m allows the designer to choose from a range of currents, according to (1.a). Equation (2) is an approximation for the

0-7695-0387-X/99 $10.00 © 1999 IEEE

intrinsic cut-off frequency f_T in terms of i_d. An approximate formula for the source-to-drain saturation voltage as a function of the inversion level is shown in (3). The maximum voltage gain achievable with a single transistor is limited by its source to drain conductance. This conductance is approximately proportional to the ratio of the drain current over the channel length [2]. Thus, A_{vo}, the negative of the attainable voltage gain of the common source amplifier can be written as

$$A_{vo} = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D} V_A L \qquad (4)$$

where V_A is the Early voltage per unit length [3]. Here we will suppose that V_A is constant even though it tends to increase somewhat in strong inversion ([2], Chap. 2 in [9]) and is also slightly dependent of L. (1) to (4) constitute a set of fundamental expressions to design MOS amplifiers for inversion levels of practical interest.

The equations above are simple but model the relevant effects for amplifier design. The g_m/I_D ratio is almost independent of the vertical mobility degradation and velocity saturation is not relevant because operation deep in strong inversion is out of the suitable range for analog design. In order to avoid the non-quasi-static effects to have an appreciable influence on the MOSFET dynamic behavior, the maximum value of the operating frequency should be a fraction of the transition frequency. From now on, to prevent the amplifier frequency response from being affected by non-quasi-static effects, we will assume that the transition frequency is at least equal to four times the value of GBW.

3. Optimum Properties of the MOS Amplifier

The methodology presented in [5, 6] to design amplifiers is based on either calculated or measured curves of g_m/I_D in MOSFETs. In the present work we include the voltage gain as an initial specification. Only two technology-dependent parameters are used in our methodology: I_S, the square normalization current (I_S for W=L) and V_A, the Early voltage per unit length.

The channel length required to achieve the voltage gain A_{VO} is readily calculated from (1) and (4):

$$L = \frac{n\phi_t A_{V0}}{V_A} \frac{1+\sqrt{1+i_d}}{2} \qquad (5)$$

Combining (2) and (5) one obtains

$$(A_{V0})^2 f_T = \frac{\mu\phi_t}{2\pi} \left(\frac{V_A}{n\phi_t}\right)^2 . \frac{8(\sqrt{1+i_d}-1)}{(\sqrt{1+i_d}+1)^2} \qquad (6)$$

Expressions (5) and (6) are plotted in Fig. 1. Equation (5) shows the linear dependence of the channel length on the voltage gain, for a constant normalized current. Expression (6) shows that for all transistors of a given technology, the product of the transition frequency f_T and the squared attainable voltage gain $(A_{V0})^2$ is independent of geometry and depends only on the inversion level i_d, attaining a maximum for i_d=8. In other words, for all transistors with the same f_T, the choice of i_d=8 allows us to obtain the maximum gain. Another interesting property of the bias condition i_d=8 follows from (1.a). For i_d=8, the drain current necessary to obtain a given transconductance g_m is the double of the drain current that would be necessary deep in weak inversion (i_d<<1) where the current and, consequently, the power reach their minimum values. Furthermore, the bias condition i_d=8 gives the best solution in terms of area, as long as the effects of the drain parasitic capacitance are not accounted for.

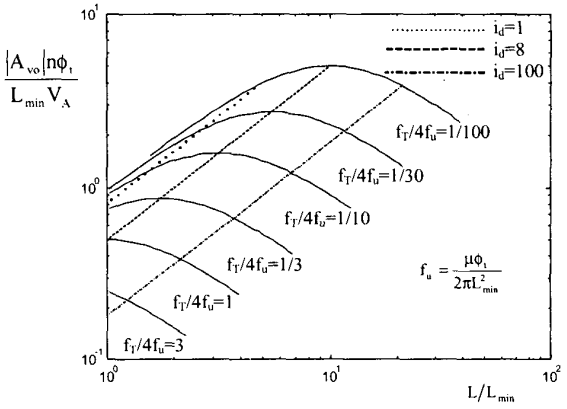

Fig. 1 The relationship between attainable DC gain and channel length, with the inversion level or transition frequency as parameters.

In effect, from (1.a-c) it follows that

$$\frac{W}{L} = \frac{g_m}{\mu C'_{ox}\phi_t} \left(\frac{1}{\sqrt{1+i_d}-1} \right) \qquad (7)$$

while from (5) and (7)

$$WL = \frac{g_m}{\mu C_{ox}\phi_t} \left(\frac{n\phi_t A_{V0}}{V_A}\right)^2 . \frac{1}{\sqrt{1+i_d}-1} \frac{(1+\sqrt{1+i_d})^2}{4} \qquad (8)$$

From (6) and (8) one can notice that, for a given A_{V0}, both the maximum transition frequency and the minimum area are achieved for id=8.

Deep in strong inversion (5) and (6) can be approximated by.

$$L \cong \frac{n\phi_t A_{V0}}{V_A} \frac{\sqrt{i_d}}{2} \qquad (9)$$

$$(A_{V0})^2 f_T \cong \frac{\mu\phi_t}{2\pi} \left(\frac{V_A}{n\phi_t}\right)^2 . \frac{8}{\sqrt{i_d}} \qquad (10)$$

Combining (9) and (10) and assuming $f_T/4$=GBW, one obtains the product of gain and gain-bandwidth product [8] in strong inversion:

$$A_{V0}GBW \cong (\mu V_A)/(2\pi nL) \qquad (11)$$

In (11), the product A_{V0}GBW is inversely proportional to L. This result is in sharp contrast with the product A_{V0}GBW given in [8], which is considered to be independent of L. This difference is explained by the more restrictive hypothesis in our approach. In [8] only the parasitic drain capacitances are considered for the determination of GBW, while in our model the intrinsic transition frequency is taken into account. As it is shown in the next paragraph, usually the parasitic capacitance effect is less restrictive than the transition frequency.

The product of gain and gain-bandwidth at i_d=8 is one half of its value in strong inversion, as can be readily calculated from (5) and (6). From the above properties it is clear that i_d=8 provides an optimum balance between frequency response and voltage gain.

Let us now use Fig. 1 to discuss how to design a single-stage amplifier. Assume the dc gain and gain-bandwidth product to be A_{VO} and GBW. A single-stage amplifier that meets the specs is realizable if the curve f_T=4GBW intersects the horizontal line corresponding to the desired dc gain, A_{VO}. Obviously, if we choose simultaneously high gain (horizontal lines in the uppermost part of the plane) and high GBW (constant f_T curves in the bottom part of the plane) the single-stage solution may not exist. If the design is possible, the optimum (maximum) gain is obtained either for i_d=8 as long as L>L_{min} or setting L= L_{min} when the transition frequency f_T corresponding to i_d=8 is not high enough for the specified GBW.

As an example, consider the design of single stage amplifiers for maximum gain. Assume L_{min}=1μm, μ_n=500cm^2/V.s, V_A=5V/μm, n=1.25, ϕ_t=25mV and GBW's as given in Table I, which shows the results obtained using (2), (3), (5) and (6).

Table I. Basic parameters of single stage amplifiers designed for maximum attainable gain in a 1μm technology.

GBW (MHz)	10	30	100	300	1000	3000
f_t (MHz)	40	120	400	1200	4000	12000
A_{V0} (V/V)	354	206	113	64	27	10
L(μm)	4,4	2,6	1,4	1	1	1
i_d	8	8	8	15	121	970
V_{Dsat} (mv)	150	150	150	175	350	855

4. The Common Source Amplifier

In the ideal common-source amplifier shown in Fig. 2, the transconductance required to achieve the specified gain-bandwidth product (GBW) for a load capacitance equal to C_L is

$$g_m = 2\pi GBW(C_L + W\ C_J') \qquad (12)$$

where C'_J is the parasitic drain capacitance per unit width.

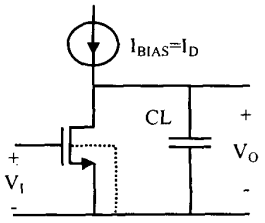

Fig. 2 - Common-source amplifier.

From (2) and (7) we have

$$W = (2g_m)/(2\pi LC'_{ox}f_T) \qquad (13)$$

while from (12) and (13)

$$W = \left(\frac{2C_L}{LC'_{ox}}\frac{GBW}{f_T}\right)\Big/\left(1-\frac{2C'_J}{LC'_{ox}}\frac{GBW}{f_T}\right) \qquad (14)$$

An important figure of merit of transistors is the ratio of the transconductance to the gate area (g_m/WL), which can be denominated area efficiency. This definition is complementary to the definition of current efficiency (g_m/I_D). In our approximated model, the transition frequency and the area efficiency have the same meaning, readily seen in (13).

(14) shows that typically, for L equal to the minimum channel length, f_T should be at least four times higher than GBW to avoid the parasitic diffusion and overlap capacitances of the MOSFET to be of the same order of C_L thus influencing on the determination of the transistor width. It is important to remark that a minimum value of the ratio of the transition frequency to the gain bandwidth product (e.g. 4) has two objectives. The first one is to prevent the non-quasi-static effects (related to L) to affect the frequency response of the amplifier up to GBW. The second one is to avoid the parasitic capacitances (proportional to W) to be comparable to the load capacitance.

5. Experimental Results

Fig. 3 shows the normalized theoretical and measurement-based gain. The measurement-based points have been determined by i_d=1.6, 3.2, 4.8, 6.4, 16, 32, 48, 64, 160, 320, 480 and 640, and are based on experimental results. The maximum of the experimental curves is for i_d=80. The difference between this maximum (i_d=80) and the theoretical value of the i_d for which maximum occurs (i_d=8) is justifing by noting that the Early voltage VA is a slightly increasing function of the normalized current. Therefore, the experimental value of id for which the maximum occurs is higher than the theoretical value.

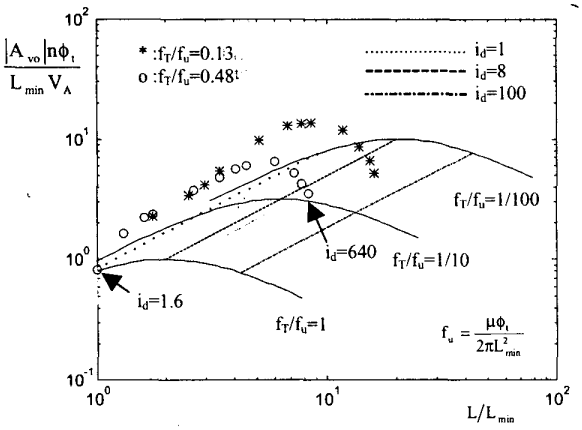

Fig. 3 – Theoretical (full-line) and measurement-based points ('*' and 'o'). L_{min}=1.2μm.

6. Scaling

The continuous increase in circuit density and the trend toward portable equipment, make low voltage/low power design a necessity [9]. The reduction in supply voltage decreases the dynamic power consumption of digital circuits but analog circuits do not benefit from technology scaling in the same way as digital circuits do [10].

Because the threshold voltages are not scaled as much as the supply voltage, MOS transistors in sub-micron technologies cannot operate deep in strong inversion. For digital circuits, the decrease in the transition frequency f_T due to reduction in inversion level at V_G=V_{DD} in scaled technologies is compensated by the reduction of the channel length. On the other hand, analog circuits can benefit from the freedom to choose different aspect ratios for the same specs. Maintaining both constant dynamic range (DNR) and bandwidth while scaling the supply voltage results in a power-dissipation penalty. Consider kT/C noise and the signal power to be proportional to the square of the supply voltage Vdd. If Vdd is reduced by the scaling factor ζ, the capacitance C must by multiplied by ζ^2 in order to keep the DNR constant [10]. To keep the same bandwidth, the transconductance gm must also be multiplied by ζ^2. If the specifications for the scaled technology are still realizable at i_d=8, the drain current I_D must also be multiplied by the scaling factor ζ^2 and the power consumption is increased by the scaling factor ζ. There is a marked contrast between this last result and the one shown in the technical literature [11] where the power consumption is increased by ζ^2, which is a consequence of not changing the aspect ratio of the transistor in the scaled technology. Finally, the technology scaling implies that many designs that today are only possible in strong inversion will migrate to moderate inversion due to the reduction in minimum channel length.

7. Conclusions

A methodology to design MOS amplifiers has been developed. It is supported by a current-based MOSFET model which has accurate and continuous equations from weak inversion to strong inversion. The design approach is suitable for both low power design or for area optimization. We proposed a very simple design which allows maximum gain either with the transistor operating in moderate inversion or using minimum channel length for high frequency amplifiers. The proposed methodology has been applied to the design of a common-source amplifier and corroborated by experimental results.

Acknowledgments

The authors would like to thank the financial support of CNPq and CAPES, from the Brazilian Ministries of Science and Technology and Education.

8. References

[1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 1998 by Cambridge University Press.

[2] E. A. Vittoz, "Micropower Techniques" in *Design of MOS VLSI Circuits for Telecommunications*, J. Franca and Y. Tsividis (eds.), 1993 by Prentice-Hall.

[3] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, 1994 by McGraw-Hill.

[4] B. Razavi, "CMOS Technology Characterization for Analog and RF Design", IEEE JSSC, vol.34, no. 3, pp. 268-276, March 1999.

[5] F. Silveira, D. Flandre and P. G. A. Jespers , " A g_m/I_D Methodology for the Design of CMOS Analog Circuits and its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA"; IEEE JSSC, vol.31, no. 9, pp. 1314-1319, September 1996.

[6] R. L. Oliveira Pinto, A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, 'An Amplifier Design Methodology Derived from a MOSFET Current-Based Model", IEEE ISCAS 98, vol. 1, pp. 301-304, Monterey, CA, USA.

[7] A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design", IEEE JSSC, vol.33, no. 10, pp. 1510-1519, October 1998.

[8] K. Bult, "Basic CMOS techniques" in *Analog VLSI. Signal and Information Processing*, M. Ismail, T. Fiez (eds.), 1994 by McGraw-Hill.

[9] E. Sánchez-Sinencio and A. G. Andreou (eds.), *Low-Voltage/ Low Power Integrated Circuits and Systems*, 1999 by IEEE Press.

[10] R. Castello, F. Montecchi, F. Rezzi, and A. Baschirotto, "Low voltage Analog Filters", IEEE Trans. On CAS-I, vol. 42, no.11, pp.827-839, November 1995.

[11] H. Ng, R. M. Ziazadeh, and D. J. Allstot, "A Multistage Amplifier Technique with Embedded Frequency Compensation", IEEE JSSC, vol.34, no. 3, pp. 339-347, March 1999.