Digitally Programmable Switched-Current FIR Filter for Low-Voltage Applications

F. A. Farag, C. Galup-Montoro, and M. C. Schneider

***Abstract*—In this paper, we describe a switched-current (SI) finite-impulse response (FIR) filter, suitable for equalizer architectures. The basic cell of the FIR filter is the SI sample–hold (S/H) circuit proposed in [1], appropriate for low-voltage operation. The programmability of the FIR filter structure is achieved via MOSFET-only current dividers [2]. The FIR filter has been designed and implemented using a 0.8-μm CMOS process and operates at a power-supply voltage of 2 V.**

***Index Terms*—Low-voltage analog filters, programmable filters, switched-current finite impulse response (FIR) filters.**

I. Introduction

Because many consumer, telecommunication, and computing products are battery-powered, there is a trend toward low-power, low-voltage operated circuits. The switched-current (SI) technique offers advantages over switched-capacitor (SC) circuits in terms of processing technology and power-supply voltage [1], [3], [4]. For both switched-capacitor and conventional switched-current techniques, the conduction gap [5] of the switch shown in Fig. 1 is the most significant obstacle at low-power supply voltage. There are some special techniques to deal with this problem, such as the use of a dedicated process, on-chip generation of a voltage larger than the supply voltage and the switched-op-amp methodology proposed in [5]. However, these techniques add some extra cost to the chip. In the sample-and-hold (S/H) [3] of the conventional SI technique shown in Fig. 2(a), the voltage at the switch terminals is signal-dependent. Thus, as much as SC circuits, conventional SI circuits are subject to the conduction gap. Another circuit technique for SI [1], [4], which is reviewed and employed in this work, overcomes the problem of the conduction gap.

The programmability of conventional SC circuits has been achieved by digitally selecting capacitor arrays [6]. In conventional SI circuits, the programmability has been achieved using either binary-weighted transistors [7] or mask-programming [8] methods. Binary-weighted transistors, as much as capacitor arrays, consume very large area, while mask-programming methods are not suitable for on-line adaptive applications. In this work, MOSFET-only current dividers (MOCD's) are employed to provide the filter with on-line programmability. The MOCD occupies small silicon area and is very simple to program by using digital words.

Following the low-voltage trend, this paper presents a digitally programmable switched-current finite impulse response (FIR) filter that is suitable for low-voltage operation. The paper is organized as follows. The switched-current technique for low-voltage applications is reviewed in Section II. The structure and design of a 4-tap FIR filter based on a circular delay line architecture [9] are presented in Sections III and IV. Section V summarizes the measurement results, and conclusions are given in Section VI.

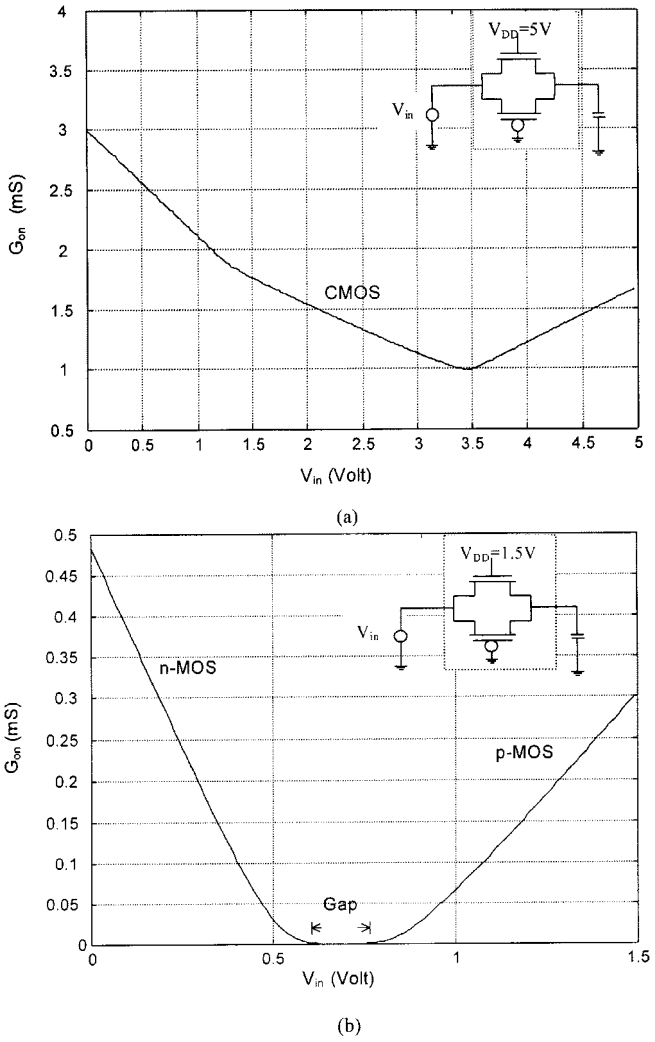

Fig. 1. On-conductance of a CMOS switch for different supply voltages: (a) $V_{\rm DD} = 5$ V and (b) $V_{\rm DD} = 1.5$ V.

II. Low-Voltage Programmable Switched-Current Cell

A. The Sample–Hold Circuit

The S/H circuits shown in Fig. 2 operate as current mirrors when the switches are closed. In the circuit shown in Fig. 2(b),

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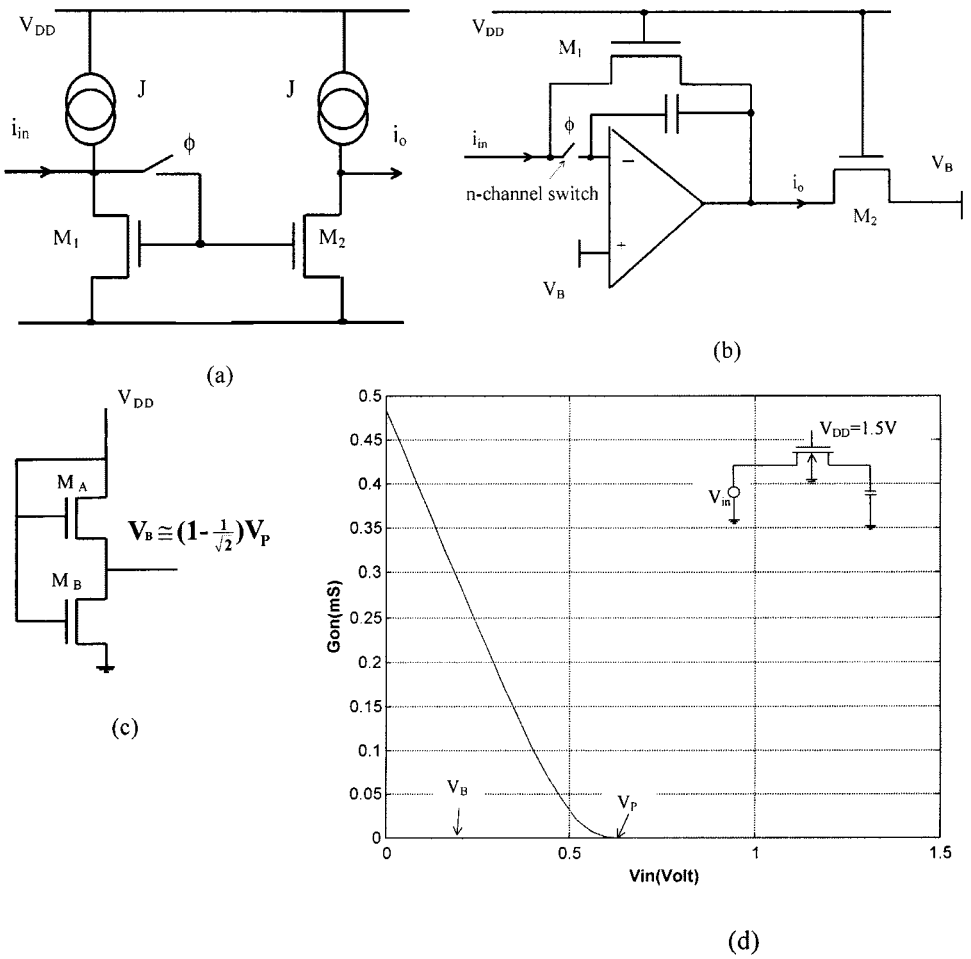

Fig. 2. S/H implementation in SI techniques: (a) the conventional SI technique [3], (b) the SI technique [1] for low supply voltage, (c) bias circuit (M_A and M_B are identical transistors), and (d) on-conductance of the nMOS switch.

assuming the op-amp to be ideal, transistors M_1 and M_2 are both biased with the same set of voltages. Therefore, neglecting transistor mismatch, the output current i_0 is an inverted replica of the input current i_{in}, i.e., $i_o = -Ai_{\mathrm{in}}$, where $A = (W/L)_{M2}/(W/L)_{M1}$.

The S/H circuit shown in Fig. 2(b) operates as follows.

- Track mode: The input current is fed to the cell when the switch is closed. The current is memorized as a voltage across the holding capacitor. It should be emphasized that linear capacitors are not needed to store the data.
- Hold mode: When the switch opens, the voltage is held on the capacitor. The output current is equal to the value on the previous clock phase.

An important property of the S/H shown in Fig. 2(b) is that the switches operate at a constant voltage V_B. Therefore, the conduction gap [5] of the switches at low power-supply voltages is avoided. The dc operating point of the switches causes both the charge injected into the holding capacitor and the settling time [10] of the S/H to be signal-independent.

An appropriate choice of the bias voltage (V_B) allows for both the highest current swing and the conduction gap prevention. Fig. 2(c) illustrates the bias voltage generation [11] circuit, where M_A and M_B are identical transistors. V_B is given [11] by

$$V_B = V_P(1 - 1/\sqrt{2}). \tag{1}$$

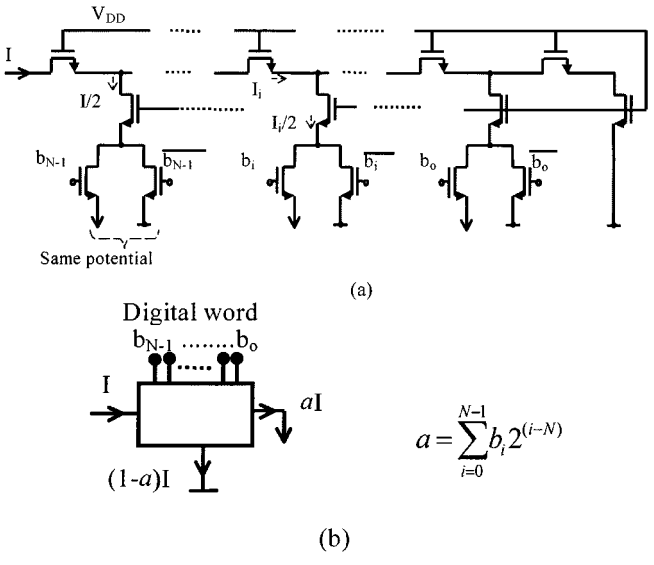

Fig. 3. The MOSFET-only current divider: (a) scheme and (b) symbol.

V_P is the pinchoff voltage [11], [12] given by $V_P \cong (V_{\mathrm{DD}} - V_{\mathrm{TO}})/n$, where V_{TO} is the zero bias threshold voltage and n, the slope factor, is slightly greater than one.

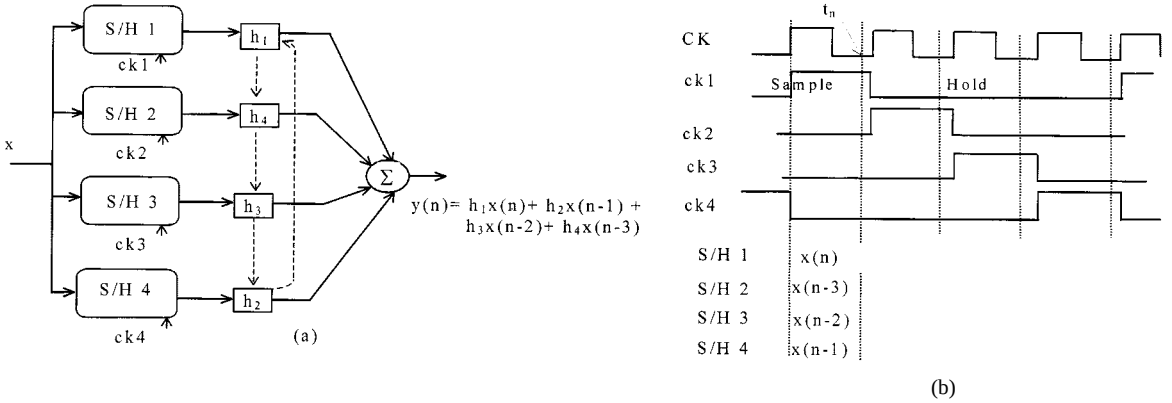

Fig. 4. (a) Circular FIR filter (coefficients during ck1) and (b) clock waveforms.

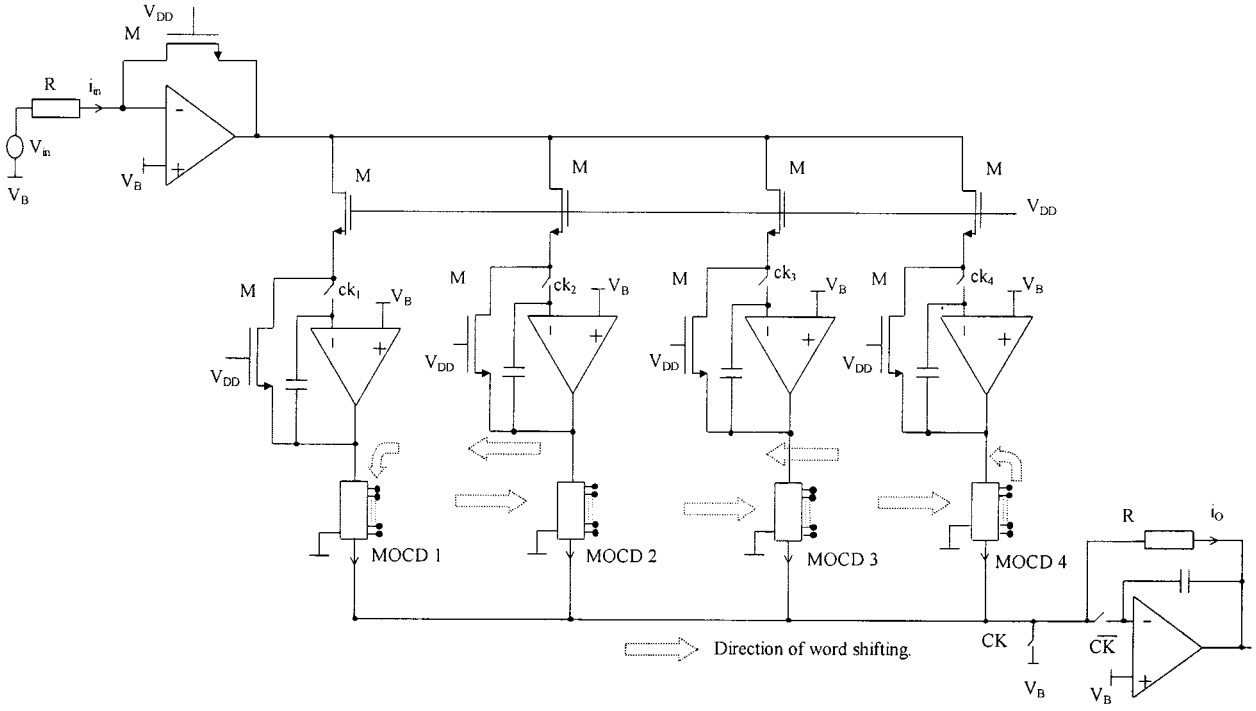

Fig. 5. The 4-tap FIR filter realization in circulating form.

B. The MOCD Structure

The schematic of the MOCD [2] together with its symbol are shown in Fig. 3. The output currents of the MOCD are digitally controlled fractions of the input current. In the SI technique proposed here, the MOCD structure is used as the digitally programmable element. The MOCD has an input impedance independent of the digital word, thus providing a constant load impedance to the op-amps. Without trimming techniques, MOCD's easily achieve 6-bit resolution, which is sufficient in some applications [13].

III. Switched-Current FIR Filter Structure

The circular FIR structure proposed in [9], [14], and [15] has been employed in this work, as shown in Fig. 4. The signal flow through the FIR filter is described as follows.

- During ck1, the S/H 1 is in the sample mode (active), and the other S/H's are in the holding mode. The filter coefficients and the stored signals are distributed as shown in Fig. 4(a) and (b), respectively.
- On ck2, S/H 2 is active, and the stored values of all S/H's but the second are kept unchanged. However, all tap weights must be shifted, as shown in Fig. 4(a), to realize

$$H(z) = h_1 + h_2 z^{-1} + h_3 z^{-2} + h_4 z^{-3}. \tag{2}$$

The circulating process continues on each clock cycle, thus cycling the digital coefficients through all the multipliers. This process simulates a tapped delay line without passing the sampled value into series delay elements on each clock cycle. Consequently, this structure has the advantage of avoiding the propagation of both the offset voltage and noise from each cell to the next (multiple resampling errors).

The S/H circuit and the programmable MOCD presented in Section II have been used for the SI implementation of a 4-tap circular FIR filter, whose scheme is shown in Fig. 5. The input

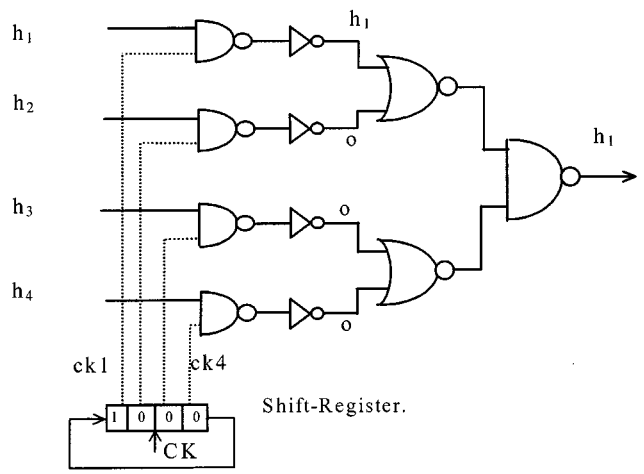

Fig. 6. One-bit circulating circuit.

section realizes a linear voltage-to-current converter, while the output sample–hold circuit performs simultaneously as a summer block and a linear current-to-voltage converter.

IV. Design Considerations

A. The Circulating Coefficients

A rotating switch matrix has been used in [15] to simulate the circulating coefficients. In this work, the circulating process is realized by word shifting. The FIR filter coefficients are shifted using the logic circuit shown in Fig. 6, which presents the circulating scheme for one bit. The digital circuit has been designed using the library from the foundry. The clock phases (ck1,. . ., ck4) have been generated using a circulating shift-register.

B. Considerations About Switching

In our filter, the circulation of the coefficients changes the state (ON/OFF) of some of the MOCD's transistors. Thus, a significant amount of charge can be transferred from the MOCD to the holding capacitor. A simple solution to avoid this charge transfer consists in delaying the clock signal responsible for changing the digital word of the MOCD's with respect to the clock of the last (summing) S/H. In this way, the charge injected by the MOCD is not summed into the holding capacitor.

The circuit shown in Fig. 5 has been designed and simulated with SMASH [16] for a 10-μA input current and 3-/0.8-μm n-channel switches. The ACM MOSFET model [17] has been used for the simulations. Two-stage CMOS op-amps have been designed using the methodology described in [18]. The time delay between the main clock (ck1) and the delayed one ($ck1_s$) was 0.4 ns, which is equivalent to two cascaded logic inverters from the library of the 0.8-μm CMOS technology used in this design.

V. Experimental Results

A 4-tap switched-current FIR filter was fabricated in a double-poly, double-metal 0.8-μm CMOS process. The circuit occupies 4 mm^2 area including bonding pads, while the core area is 1.3 mm^2. A micrograph of the integrated filter is shown in Fig. 7. The frequency response has been measured using

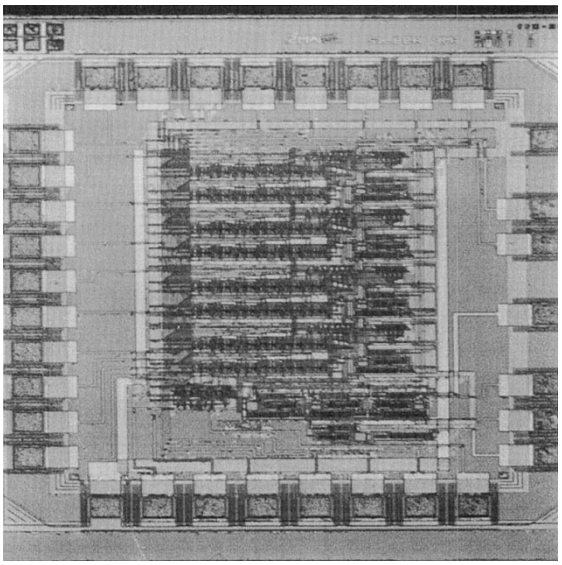

Fig. 7. Chip micrograph.

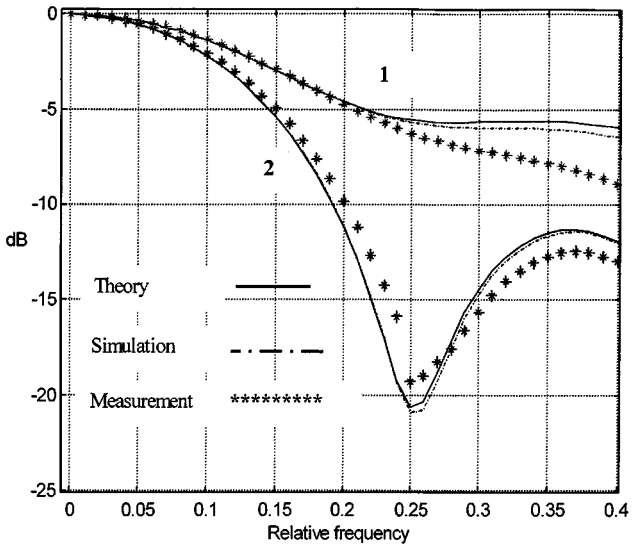

Fig. 8. Measured, simulated, and theoretical frequency response of the 4-tap FIR filter. 1) $h_1 = 3F$, $h_2 = 15$, $h_3 = 0B$, and$h_4 = 06$. 2) $h_1 = 3F$, $h_2 = 36$, $h_3 = 2E$, and$h_4 = 27$.

the 3588-A spectrum analyzer. The supply voltage is 3 V and the sampling frequency is 1 MHz. The measured results for different digital words are depicted in Fig. 8. The figure shows good agreement between theory, simulation, and experimental results. The frequency response of the FIR filter has shown no significant change for supply voltages from 3 down to 2 V. The filter architecture has been digitally programmed without the need for any change in the filter structure. Thus, the proposed FIR filter can be used coupled with an adaptive algorithm.

VI. Conclusion

A digitally programmable switched-current technique suitable for low-voltage applications has been reviewed. In this new SI technique, the problem of low-voltage switches has been overcome. The programmability of the SI circuits has been achieved using the MOCD structure, which allows easily

on-line programming and occupies small silicon area compared to traditional programming methods. A programmable switched-current FIR filter has been designed using the circulating tap technique. A 4-tap FIR filter has been fabricated in 0.8-μm CMOS technology. The applied SI technique is very promising for the implementation of programmable low-voltage FIR filters.

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