Maximizing the Power Conversion Efficiency of Ultra-Low-Voltage CMOS Multi-Stage Rectifiers

Lucas G. de Carli, Yuri Juppa, Adilson J. Cardoso, Carlos Galup-Montoro, and Márcio C. Schneider

***Abstract*—This paper describes an efficient method to explore the design space of AC/DC converters for energy harvesting circuits. A simple analytical model of the rectifier circuit valid down to ultra-low-voltage operation (input voltage below the thermal voltage) is proposed. Based on the Shockley diode equation, the use of an optimization equation that relates the number of stages of the rectifier to the saturation current of the diodes is demonstrated. A set of universal normalized curves to guide the designer regarding the minimum available power from the AC power source is presented. Three rectifiers with different numbers of stages and saturation currents along with matching networks integrated in a 130 nm CMOS technology demonstrated a conversion efficiency of around 10% for an available power of around −20 dBm and DC load voltage and current of 1 V and 1 μA, respectively.**

***Index Terms*—AC-DC converters, energy harvesting, power conversion efficiency, ultra-low-voltage rectifiers, zero-VT transistor.**

I. Introduction

IN THE FUTURE Internet of Things (IoT) most objects will have a wireless connection, leading to a huge number of connected devices [1]. The proliferation of sensors connected to objects will be possible only through the harvesting of energy from the environment, since battery replacement is impractical due to either the enormous number of devices or the difficulty in accessing the node placement. The ubiquity of radiofrequency (RF) signals makes them one of the most important power sources from which sensor networks can be energized. However, the generation of the supply voltage from the RF signal is still an open issue, mainly because of both the very low magnitude of the RF signals and the poor modeling of the rectifier circuits operating with weak signals.

In effect, the classical analysis of voltage multipliers based on the concept of constant voltage drop in the diodes [2] is not suitable for low-input-voltage applications such as wireless sensor networks or RFID tag chips. In these applications, the amplitude of the input voltage is usually within hundreds or even tens of mV [3]–[10]. Consequently, low power consumption, power conversion efficiency, and operation from low voltage power sources are of major relevance for devices that harvest energy from the environment. For ultra-low-voltage (ULV) design, it is mandatory to use the correct physical parameter of the device. For a diode, for example, the saturation current I_S is the appropriate physical parameter and not the threshold (on) voltage, which is meaningless for ULV circuit design.

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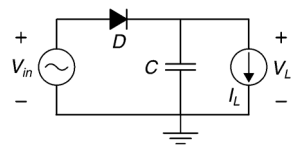


Fig. 1. Single-stage rectifier.

The purpose of this paper is to provide an analysis of rectifiers employed for energy harvesting. The proposed analysis is correct down to input voltages lower than the thermal voltage. Expressions that can be employed to optimize the efficiency of multi-stage rectifiers, which directly affects the energy-harvesting tag range [7], are shown. Rectifier parameters, namely, the diode sizes and the number of stages, can be readily determined by taking into account the load parameters (DC voltage and load current), the source resistance, the matching network parameters (the inductance and its quality factor), and the ideality factor of the diode.

This paper presents a set of analytical results to guide the design of an RF-DC converter. Section II presents the steady-state analysis and a complete circuit model of multi-stage rectifiers. Section III provides the relationship between the number of stages of the voltage multiplier and the diode saturation current for maximum power efficiency. Section IV analyzes the benefits introduced by a matching network. Section V presents the design of three integrated rectifiers as well as experimental results.

II. Steady-State Analysis of the N-Stage Rectifier

The performance of multi-stage rectifiers can be inferred from the analysis of the single-stage rectifier in Fig. 1.

As in [11] and [12], the following assumptions are made: i) the rectifier operates in steady-state; ii) the load current is constant; iii) all diodes are identical; iv) the impedance of the coupling capacitors is negligible at the frequency of analysis; v) the diodes are described by the Shockley equation

$$I_D = I_S \left(e^{\frac{V_D}{n\phi_t}} - 1 \right) \tag{1}$$

where I_S is the saturation current, n is the ideality factor, and ϕ_t is the thermal voltage, approximately equal to 26 mV at room temperature.

A. Output Voltage

In relation to Fig. 1, the average value of the diode current over a complete cycle of the input signal equals the load current,

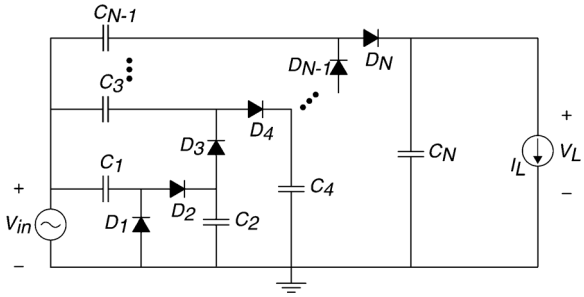


Fig. 2. N-stage voltage rectifier.

i.e.,

$$\frac{1}{2\pi}\int_{-\pi}^{\pi} I_D d\theta = \frac{1}{2\pi}\int_{-\pi}^{\pi} I_S\left(e^{\frac{(V_A\cos\theta - V_L)}{n\phi_t}} - 1\right)d\theta = I_L \quad (2)$$

Assuming that the capacitance in Fig. 1 is sufficiently high to avoid significant changes in the stored charge over a period, i.e., V_L is constant, we have

$$\frac{V_C}{n\phi_t} = \frac{V_L}{n\phi_t} = \ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1 + I_L/I_S}\right] \quad (3)$$

where V_A is the peak of the sine input voltage, and

$$I_0(z) = \frac{1}{2\pi}\int_{-\pi}^{\pi} e^{z\cos\theta}d\theta \quad (4)$$

is the modified Bessel function of the first kind of order zero [13].

The result in (3) can be applied to the N-stage voltage multiplier shown in Fig. 2 if the values for all capacitors C_i are sufficiently large so that the voltages across them can be assumed to be constant. Consequently, for high-frequency analysis all capacitors behave as short-circuits and, therefore, all diodes are in parallel (antiparallel) with the input. Noting that the average current through each diode over a period of the input signal is equal to the load current and using (3) the voltage V_{Ci} stored in each capacitor C_i is a DC voltage given by

$$\frac{V_{Ci}}{n\phi_t} = i\ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1 + I_L/I_S}\right] \quad (5)$$

Thus, the DC output voltage is

$$\frac{V_L}{n\phi_t} = N\ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1 + I_L/I_S}\right] \quad (6)$$

So far both the diode capacitances and the parasitic capacitances of the coupling capacitors are assumed to be negligible. In a true realization, both of them contribute to reducing the effective voltage across the diodes [11], which leads to a decrease in the DC load voltage. However, in the designs to be shown later, the diode capacitances are much smaller than the coupling capacitors. This is because small-area zero-VT transistors were used for the diodes. Also, the use of MIM (metal-insulator-metal) capacitors for the coupling capacitors is appealing since their parasitic capacitances to the substrate are a very small fraction of the main capacitance. In the following, the parasitic capacitances and the diode capacitances will be assumed to be negligible in comparison with the value of the coupling capacitance. Descriptions of the analysis of the effects of parasitic capacitances on the rectifier performance can be found elsewhere [2], [8], [18].

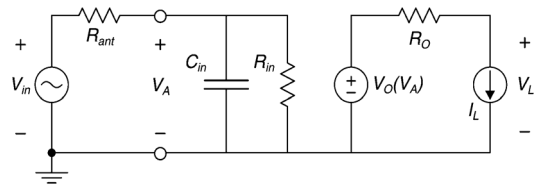


Fig. 3. Model of the N-stage voltage multiplier.

B. Power Conversion Efficiency

The power loss in each diode can be calculated using the fact that the voltage across each diode is

$$V_D = V_A\cos\omega t - V_C \quad (7)$$

with V_C given by (3). Using (7) in the Shockley equation, the average power dissipated in the diode can be found by integrating the instantaneous power over one cycle. The resulting average power loss in the N diodes is given by

$$P_{loss} = -I_L V_L + N(I_L + I_S)V_A\frac{I_1\left(\frac{V_A}{n\phi_t}\right)}{I_0\left(\frac{V_A}{n\phi_t}\right)}$$

$$I_1(z) = \frac{1}{2\pi}\int_{-\pi}^{\pi}\cos\theta e^{z\cos\theta}d\theta \quad (8)$$

where $I_1(z)$ is the modified Bessel function of the first kind of order one [13]. The first term in (8) corresponds to the output power while the second term corresponds to the input power of the voltage multiplier. Note that the result of (8) is similar to that given by expression (13) of reference [11], but here the modified Bessel functions replace the hyperbolic functions of [11].

The PCE of the N-stage rectifier is

$$PCE = \frac{P_{out}}{P_{in}} = \frac{V_L I_L}{P_{loss} + V_L I_L} = \frac{\frac{n\phi_t}{V_A}}{\left(1 + \frac{I_S}{I_L}\right)}\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{I_1\left(\frac{V_A}{n\phi_t}\right)}\ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{1 + I_L/I_S}\right] \quad (9)$$

with P_{loss} given by (8) and V_L given by (6).

C. Voltage Multiplier Model

The rectifier realized through the voltage multiplier is a nonlinear circuit which, for steady-state analysis, can be represented as in Fig. 3, in which a power source is connected to the rectifier input. As it will be shown in Sections III and IV, the electrical model of the voltage multiplier is essential for the design of the converter.

To find the model parameters, assume that the peak value of the sine wave at the rectifier input is V_A.

The equivalent input resistance of the rectifier can be calculated from the input power that enters the voltage multiplier, as in [4], i.e.,

$$R_{in} = \frac{V_A^2}{2P_{in}} = \frac{V_A}{2N(I_L + I_S)}\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{I_1\left(\frac{V_A}{n\phi_t}\right)} \quad (10)$$

For large signals, $z > 5$, $I_0(z)/I_1(z) \simeq 1$ and (10) can be rewritten as

$$R_{in} \simeq \frac{V_A}{2N(I_L + I_S)} \tag{11}$$

whereas for low-level signals, $z < 1$, $I_0(z)/I_1(z) \simeq 2/z$, and (10) simplifies to

$$R_{in} \simeq \frac{n\phi_t}{N(I_L + I_S)} \tag{12}$$

Thus, the input resistance of the rectifier is highly nonlinear, being proportional to the input signal for large values of $V_A/n\phi_t$. For low-level input signals the input resistance of the multi-stage rectifier is equal to the resistance of the parallel combination of N diodes, each one with a resistance whose value is equal to the small-signal resistance of the diode.

The converter input capacitance and output resistance are calculated in Appendix A.

In the sequel, it is assumed that the power source can be represented by an equivalent (peak) voltage V_{ANT} and a series resistance R_{ant}, as shown in Fig. 3.

The available power from the source is given by

$$P_{AV} = \frac{V_{ANT}^2}{8R_{ant}} \tag{13}$$

Assuming that the input capacitance of the rectifier C_{in} has a negligible effect on the power transferred from the source to the rectifier, the KVL for the input circuit in Fig. 3 is

$$V_{ANT} = V_A + R_{ant}\frac{V_A}{R_{in}} = V_A + 2R_{ant}N(I_L + I_S)\frac{I_1\left(\frac{V_A}{n\phi_t}\right)}{I_0\left(\frac{V_A}{n\phi_t}\right)} \tag{14}$$

Assuming V_L, I_L, and $n\phi_t$ as given specifications, one can use (6) to calculate V_A in (14) in terms of N and I_S and plot the required V_{ANT}, or the required available power using (13), in terms of the rectifier parameters, N and I_S. Fig. 4 shows a family of level curves for some values of the available power in terms of the rectifier parameters N and I_S. As it is clear from the figure, there is a minimum available power which satisfies the specifications given in the caption of Fig. 4. This minimum is around -17.7 dBm (17 μW) or, equivalently, $V_{ANT} \approx 82$ mV, which gives an overall conversion efficiency (DC power/RF available power) of the AC/DC converter of around 5.9%. The minimum available power is achieved for $N \approx 86$ and $I_S \approx 3.1$ μA, which corresponds to $V_A \approx 60$ mV and $R_{in} \approx 131$ Ω. Low conversion efficiency is typical of a rectifier operating with ultra-low voltages.

III. Optimization of the Generic N-Stage Rectifier

The following optimization problem is solved next: given V_L, I_L, and $n\phi_t$, determine the number of stages N and the saturation current I_S of the diodes that minimize the available power necessary to meet the output specification. Fig. 5 shows the dependence of both PCE and V_L on the load current for some values of the magnitude of the input signal. Note that the DC output voltage and the load current are normalized to diode parameters $n\phi_t$ and I_S, respectively. As it is clear from Fig. 5, for a fixed input voltage, for instance, $V_A/n\phi_t = 8$, the PCE reaches a maximum of approximately 47%, for a ratio of the load current to saturation current $I_L/I_S \approx 4.5$.

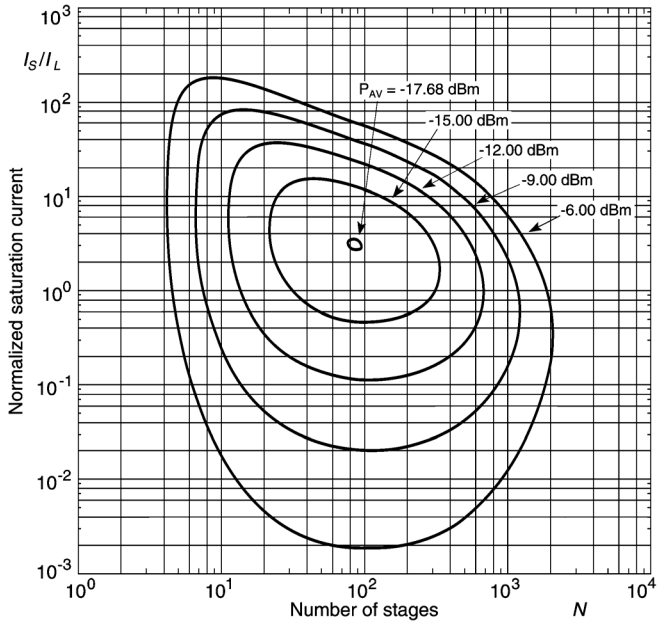


Fig. 4. Required available power in terms of number of stages and normalized diode saturation current calculated from (6), (13) and (14). The design specifications are $V_L = 1$ V, $I_L = 1$ μA, with $R_{ant} = 50$ Ω, $n\phi_t = 36$ mV.

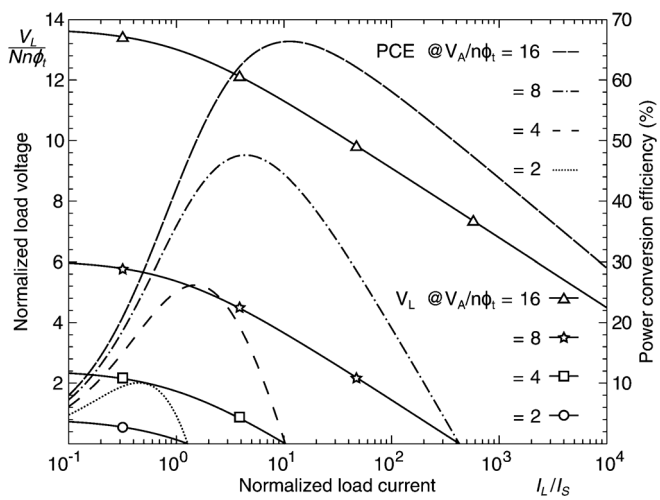


Fig. 5. Normalized load voltage given by (6) and power conversion efficiency of the voltage multiplier, (9), versus normalized load current for values of $V_A/n\phi_t$ of 2, 4, 8, and 16.

The reason for the existence of this optimum value of the PCE for a specific value of the load current can be readily understood. For low saturation current values, the forward voltage drop on the conducting diodes is the most important cause of power dissipation whereas for high values of I_S the reverse diode current is the main cause of the power losses. Thus, there is an optimum value for I_S which minimizes the sum of the forward and reverse losses of the diodes and maximizes the PCE.

The existence of this maximum is essential for the calculation of both the number of stages N and the saturation current I_S of the diodes for an efficient voltage multiplier. For constant input voltage V_A, the derivative of (9) with respect to I_L/I_S gives the following condition for maximum PCE

$$\frac{I_L}{I_S} = \ln\left[\frac{I_0\left(\frac{V_A}{n\phi_t}\right)}{\left(1 + \frac{I_L}{I_S}\right)}\right] \tag{15}$$

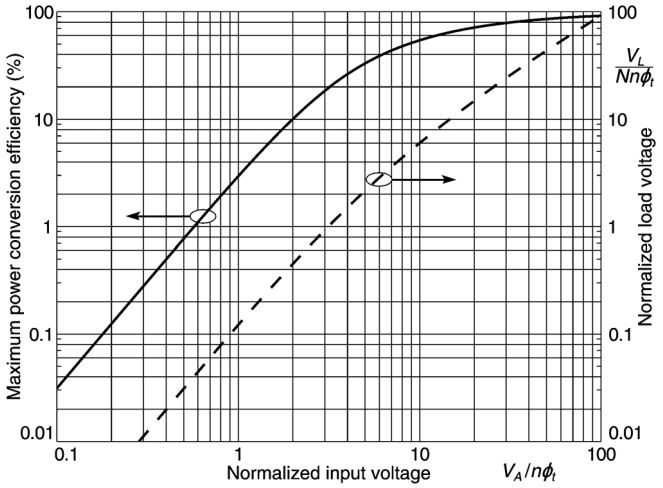


Fig. 6. Maximum power conversion efficiency (PCE) and normalized DC load voltage of the N-stage rectifier versus the magnitude of the normalized input voltage, calculated from (9), (15), and (16).

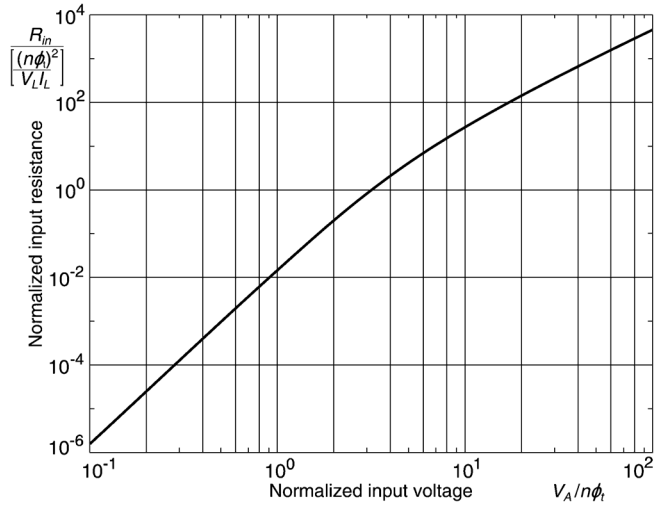


Fig. 7. Normalized input resistance of the optimized voltage multiplier in terms of the normalized input voltage calculated from (10) and (15).

or, equivalently, using (6)

$$\frac{I_L}{I_S} = \frac{V_L}{Nn\phi_t} \tag{16}$$

The result in (16) simply shows that the voltage multiplier achieves its maximum efficiency for a DC load current equal to the diode saturation current times a factor which is the DC load voltage normalized to $Nn\phi_t$. For each specification of the load $(V_L, I_L,)$ and of the ideality factor (n) of the diode there is only one pair of design parameters, namely the number of stages N and the saturation current I_S that maximizes the PCE for a given value of the input voltage V_A.

With (15), we now find the values of I_L/I_S (and $V_L/Nn\phi t$) which maximize the PCE for a given V_A. Using expression (9), along with the result in (15), the maximum PCE for each value of V_A is found. The curves in Fig. 6 summarize the conditions for maximizing the PCE and the corresponding maximum PCE that can be achieved for each input voltage of the multi-stage rectifier.

Note that the maximum PCE was calculated by assuming that the value of V_A can be arbitrarily chosen; however, in the case of a real power source, the voltage at the rectifier input will be dependent on both the power source and the rectifier input impedance.

If the rectifier is designed for maximum PCE, (15) holds and one can write I_L/Is in terms of V_A. Thus, from (10) and (15) we can plot the input resistance R_{in} of the optimized rectifier in terms of V_A, as shown in Fig. 7.

For the sake of illustration, let us consider the case for which $n\phi_t = 36$ mV, $V_L = 1$ V, $I_L = 1$ μA, and $V_A = 60$ mV. The normalized input resistance of the optimized rectifier is, in this case, around of 0.101, which corresponds to $R_{in} \approx 131\ \Omega$.

Under the condition of maximum PCE given by (16), expression (14) can be rewritten as

$$V_{ANT} = V_A + \frac{2R_{ant}V_L I_L}{n\phi_t}\frac{I_S}{I_L}\left(1+\frac{I_S}{I_L}\right)\frac{I_1\left(\frac{V_A}{n\phi_t}\right)}{I_0\left(\frac{V_A}{n\phi_t}\right)} \tag{17}$$

with the relationship between I_S/I_L and V_A given by (15).

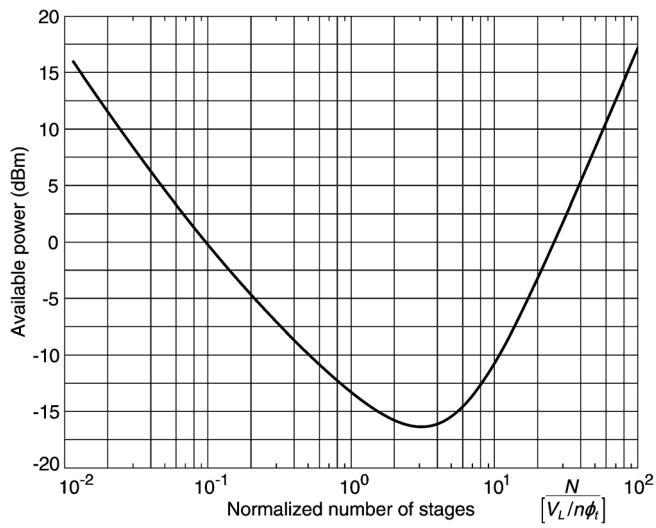


Fig. 8. Required available power in terms of the number of stages N (or diode saturation current I_S) for maximum power conversion efficiency calculated from (13), (15), and (17). The design specs are $V_L = 1$ V, $I_L = 1$ μA, with $R_{ant} = 50\ \Omega$, $n\phi_t = 36$ mV.

The graph in Fig. 8 shows the available power required to reach the specifications ($V_L = 1$ V, $I_L = 1$ μA) for $R_{ant} = 50\ \Omega$ and $n\phi_t = 36$ mV obtained from (13), (15), and (17).

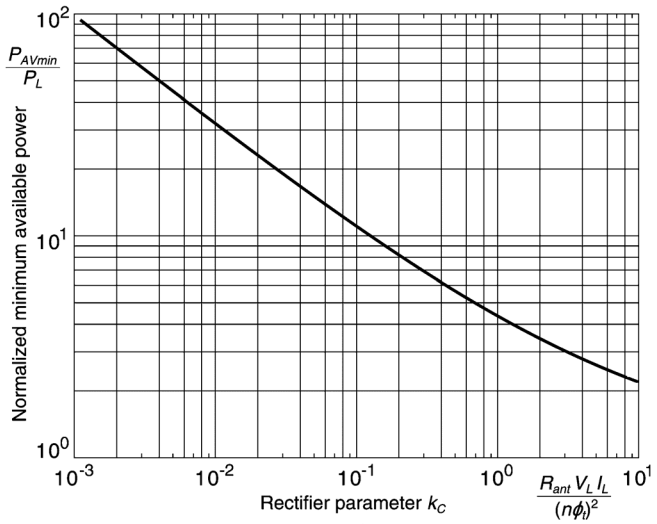
To conclude this section, note that (17) and (15) can be used to find the minimum available power required for a rectifier that complies with the condition for maximum PCE.

In order to generalize the solution to the minimum available power for a given set of rectifier specifications, let us now define the N-stage rectifier parameter k_C [15] as

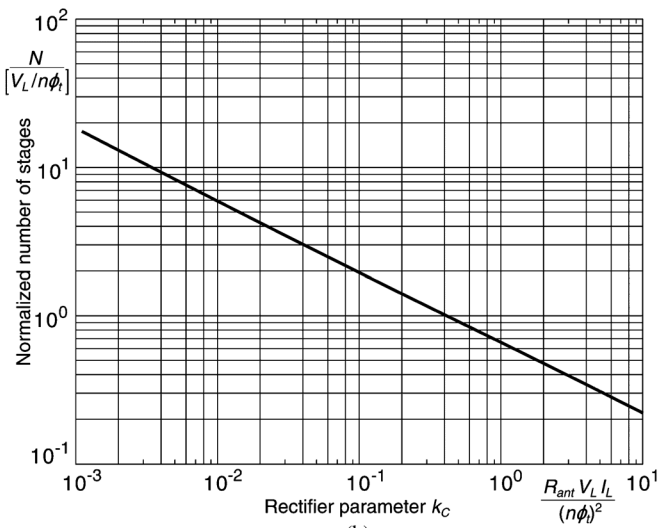
$$k_C = \frac{R_{ant}I_L V_L}{(n\phi_t)^2}$$

Note that k_C represents the main characteristics of the rectifier circuit. It is associated with load requirements (V_L, I_L), together with a Shockley diode characteristic $(n\phi_t)$, and a power source characteristic (R_{ant}).

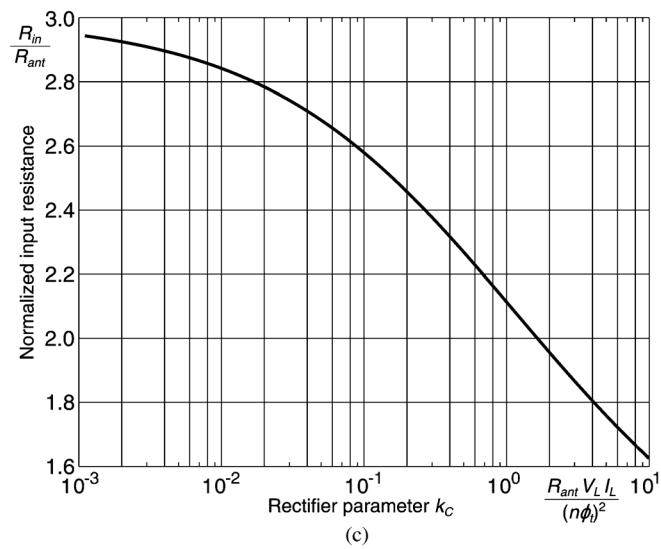
Similarly to the curve of Fig. 8, the minimum available power required as well as the normalized values of the saturation current (or number of stages) for any value of k_C, are shown in Fig. 9 [15].



(a)



(b)



(c)

Fig. 9. (a) Minimum available power normalized to the load power from (13), (15), and (17), (b) normalized number of stages, and (c) normalized input resistance in terms of the rectifier parameter k_C.

For the sake of demonstrating the usefulness of Fig. 9, let us choose the example of a rectifier for which $V_L = 1$ V, $I_L = 1$ μA, with $R_{ant} = 50$ Ω, and $n\phi_t = 36$ mV. This set

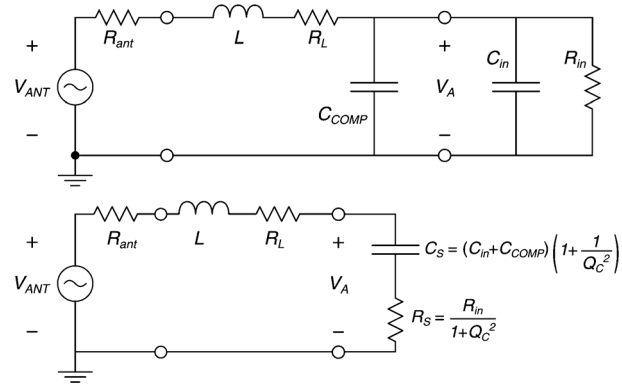


Fig. 10. Model of the N-stage voltage multiplier with impedance matching network.

of parameters gives $k_C \approx 0.039$, which, according to Fig. 9, results in $P_{AVmin}/P_L \approx 16.7$ and $I_S/I_L = Nn\phi_t/V_L \approx 3.1$. Thus, for the data given we have $P_{AVmin} = 16.7$ μW (-17.8 dBm), $I_S \approx 3.1$ μA, and $N \approx 86$. The remaining parameters are $R_{in} \approx 136$ Ω, $V_{ANT} \approx 81.7$ mV, and $V_A \approx 60$ mV. The efficiency of the rectifier can be improved through the insertion of a matching network, as discussed in the next section.

IV. Matching Network

In this study, the output impedance of the RF power source is assumed to be fixed. Thus, the overall efficiency of the AC-DC converter is dependent only on the rectifier PCE and on the power transferred from the source to the rectifier. Since we have previously evaluated the rectifier PCE, the power transfer to the rectifier can now be improved.

The judicious choice of a matching network between the power source and the rectifier leads to an improved converter efficiency due to both an increase in the power transferred to the rectifier and an increase of the rectifier input voltage V_A. As seen in Fig. 6, the PCE of the voltage multiplier increases for higher input voltages. In order to achieve simultaneously a more efficient power transfer from the source to the rectifier and an improvement in the rectifier efficiency, the $L - C_{COMP}$ network shown in Fig. 10 is connected between the source and the rectifier. The series resistance R_L represents the inductor losses. The series inductor resonates out the input capacitance of the rectifier [8], which sometimes includes an additional capacitor (C_{COMP}) for improved matching.

In order to better understand the role of the matching network, the equivalent circuit of the rectifier input is represented as a series association of a resistor (R_S) and a capacitor (C_S). Note that the value of Q_C, the rectifier Q, is given by

$$Q_C = \omega(C_{in} + C_{COMP})R_{in} = \frac{1}{\omega C_S R_S} \tag{18}$$

where ω is the signal frequency. The squared magnitude of the voltage transfer function at resonance ($\omega^2 LC_S = 1$) is

$$\left(\frac{V_A}{V_{ANT}}\right)^2 = \frac{1 + \left(\frac{\omega L}{R_S}\right)^2}{\left[1 + (R_{ant} + R_L)/R_S\right]^2} = \frac{1 + Q_C^2}{\left[1 + (R_{ant} + R_L)/R_S\right]^2} \tag{19}$$

Noting that

$$P_{AV} = \frac{V_{ANT}^2}{8R_{ant}};\ P_{in} = \frac{V_A^2}{2R_{in}};$$
$$R_{in} = R_S\left(1+Q_C^2\right) = R_S\left[1+\frac{(\omega L)^2}{R_S^2}\right] \tag{20}$$

one can find, from (19), that

$$\frac{P_{in}}{P_{AV}} = 4\frac{\frac{R_{ant}}{R_S}}{\left[1+(R_{ant}+R_L)/R_S\right]^2} \tag{21}$$

The maximum power transferred to the rectifier, achieved for $R_S = R_{ant} + R_L$, is given by

$$\left.\frac{P_{in}}{P_{AV}}\right|_{\max} = \frac{1}{1+R_L/R_{ant}} \tag{22}$$

and (19) becomes

$$\frac{V_A}{V_{ANT}} = \frac{1}{2}\sqrt{1+\left[\frac{\omega L}{(R_{ant}+R_L)}\right]^2} \tag{23}$$

The benefits of the inclusion of the matching network can be analyzed as follows. Start with the assumption that the inductor is lossless, i.e., $R_L = 0$. In this case, for $R_S = R_{ant}$ all of the available power is transferred to the rectifier. Additionally, the rectifier input voltage can be increased by using high inductance values, which, in most cases, is not an affordable solution for full integration of the AC/DC converter. For a non-negligible R_L the power transferred to the rectifier input is reduced as long as R_L is a significant fraction of the source resistance R_{ant}. Summarizing, a high inductance value is beneficial to the increase in V_A, the input voltage of the rectifier, but it can have a deleterious effect on the input power of the rectifier due to the inductor losses.

The simulation of the Q-factors of some inductors of a 0.13 μm technology for the operating frequency of 900 MHz indicated that the inductors present a Q-factor in the range of 7 to 12. The reactance and the Q-factor of the 41 nH inductor at 900 MHz are 232 Ω and 11, respectively, which implies a series resistance of 21 Ω.

Let us now resort to the previous design ($V_L = 1$ V, $I_L = 1$ μA, $R_{ant} = 50$ Ω, $n\phi_t = 36$ mV, which give $k_C \approx 0.039$) to show the usefulness of the matching network. If no matching network is used, we find from Fig. 9 that the available power required is around 16.7 μW, $N \approx 86$ and $I_S \approx 3.1$ μA.

By using the 41 nH inductor ($R_L = 21$ Ω) we find that, under matching conditions, $R_S = R_{ant} + R_L = 71$ Ω, $P_{in}/P_{AV} \approx 0.7$ from (22), and $V_A/V_{ANT} = 1.71$ from (23). The value of R_{in} is calculated from

$$R_{in} = R_S\left[1+\frac{(\omega L)^2}{R_S^2}\right] = 71\left[1+\frac{232^2}{71^2}\right] \approx 830\ \Omega$$

The normalized value of R_{in} is given by

$$\frac{R_{in}}{\left[\frac{(n\phi_t)^2}{(V_L I_L)}\right]} = \frac{830\ \Omega}{1296\ \Omega} \approx 0.64$$

From Fig. 7, which gives the normalized input resistance of the optimized voltage multiplier in terms of the normalized input voltage, it is found that $V_A/(n\phi_t) \approx 2.8$. For this value of $V_A/(n\phi_t)$, Fig. 6 shows that the maximum PCE is equal to around 16.5%, with $N \approx 35$ and $I_S \approx 1.25$ μA. Since $P_{in}/P_{AV} \approx 0.7$, the overall converter efficiency η is

$$\eta = \frac{P_L}{P_{AV}} = \frac{P_L}{P_{in}}\frac{P_{in}}{P_{AV}} \approx 16.5\% \times 0.7 = 11.5\%$$

or, equivalently, the required available power is 8.7 μW, which is less than one-half of the available power without a matching network. Using the Friis formula [16] for the far field, a comparison of the above results shows that the range is augmented by a factor of around 43% due to the insertion of the matching network.

To conclude this section, it should be noted that the total capacitance at the rectifier input is

$$C_{in}+C_{COMP} = \frac{C_S}{1+1/Q_C^2} = \frac{1}{\omega^2 L}\frac{1}{1+R_S^2/(\omega L)^2} \approx 0.7\ \text{pF}$$

The compensation capacitance can be calculated after the evaluation of the rectifier capacitance $C_{in} \approx NC_D$, where C_D is the average diode capacitance.

V. Experimental Results

Notable results for the AC-DC converter obtained in our experiments are those related to the design of the voltage multiplier and the matching network. A signal generator with an output impedance (R_{ant}) of 50 Ω was used for the measurements. Readers interested in the co-design of a CMOS rectifier and antenna are referred to [17].

The strategy to design the rectifiers was based on both the inclusion of a matching network to increase the power transfer from the source to the voltage multiplier and the use of the condition in relationship (16), which maximizes the PCE. Although higher inductance values can be employed, for the purposes of this study the inductances were limited to the range of 10 nH–60 nH. The reasons for this are twofold. Firstly, the quality factors of inductances outside this range at the operating frequency of 900 MHz are relatively low for the technology of choice. Secondly, the silicon real-estate for realizing large inductances increases more than linearly with the inductance.

The optimization process applied to find an appropriate number of stages and the value of the diode saturation current for the rectifier was started from a simple assumption: the equivalent series resistance $R_S = R_{ant} + R_L$, which is the condition required to maximize the power transferred from the source to the rectifier. Our choice for one of the designs was $L = 38$ nH, which corresponds to a reactance of $X_L = 215$ Ω and to a series resistance of $R_L = 20$ Ω. Using the relationship between the equivalent series resistance and the input resistance of the rectifier yields

$$R_{in} = R_S\left[1+\frac{(\omega L)^2}{R_S^2}\right] = 70\left[1+\frac{215^2}{70^2}\right] = 730\ \Omega$$

The normalized value of R_{in} is

$$\frac{R_{in}}{\left[\frac{(n\phi_t)^2}{(V_L I_L)}\right]} = \frac{730}{\frac{36^2}{1}} = 0.56$$

For the normalized value of R_{in}, it is found from Fig. 7 that $V_A/n\phi_t \approx 2.66$ or, equivalently, $V_A \approx 96$ mV. Using Fig. 6, the maximum PCE for this input voltage is around 15.5%, which is achieved for $I_L/I_S = V_L/Nn\phi_t \approx 0.75$; for the design specifications this corresponds to $N \approx 37$ and $I_S \approx 1.33$ μA.

TABLE I
RELEVANT DESIGN PARAMETERS OF THE INTEGRATED RECTIFIERS. THE DESIGN SPECIFICATIONS ARE $V_L = 1$ V, $I_L = 1$ μA, $R_{ant} = 50\ \Omega$, $n\phi_t = 36$ mV

N	L (Q)	C_{COMP}	I_S (nA)	W (μm)	L (μm)
18	42 nH ($\approx$ 10)	190 fF	650	4	0.5
24	38 nH ($\approx$ 10)	150 fF	780	4.8	0.5
36	42 nH ($\approx$ 10)	0	1300	7.8	0.5

Theoretically, the overall efficiency of the AC-DC converter is $\eta = PCE \cdot P_{in}/P_{AV} \approx 15.5\% \cdot 50/(50+20) \approx 11.1\%$.

After this initial guess, some fine tuning through simulation was used to find the maximum converter efficiency. We finally arrived at the values of $N \approx 24$ and $I_S \approx 780$ nA, which, according to Fig. 6, result in $V_A/n\phi_t \approx 3.2$ and $PCE \approx 20\%$. From Fig. 7, $V_A/n\phi_t \approx 3.2$ results in a normalized value of the rectifier input resistance of approximately 1.0, which gives $R_{in} \approx 1296\ \Omega$. Finally, using the relationship between the input resistance and the equivalent series resistance, it is found that $R_S \approx 37\ \Omega$. Therefore, the ratio P_{in}/P_{AV}, according to (21), is approximately 0.65. Consequently, the overall efficiency of the AC-DC converter is $\eta \approx 20\% \cdot 0.65 = 13\%$.

Three different rectifiers were integrated in a 130 nm CMOS technology. Relevant data on the three designs are shown in Table I. The intended voltage, V_L, and current, I_L, at the load are 1 V and 1 μA, respectively. Owing to their high drive capability at low voltages [12], zero-VT transistors (bulk connected to the most negative voltage) were used for the diodes (their width W and length L are given in Table I).

MIM capacitors, when needed, were used for the compensation (C_{COMP}) capacitors. The parasitic capacitances of MIM capacitors (on the topmost metal levels) to the substrate are typically a few percent of the main capacitance. For all three cases, the total input capacitance ($C_C + C_{COMP}$) of the voltage multiplier is around 0.8 pF.

Fig. 11 shows measurements taken for 9 samples of the 24-stage voltage multiplier for $P_{AV} = -20$ dBm. The average DC value of the output for an AC signal at 900 MHz is around 920 mV. It should be noted that a limiter composed of a stack of five off-the-shelf diodes was connected to the output to avoid excessive overvoltage. The limiter is responsible for a small reduction in the converter efficiency.

Measurements taken on the three rectifiers described in Table I showed that their responses at the nominal frequency of 900 MHz are quite close to each other (Fig. 12), which means that the design is not very sensitive to the number of stages N, provided that N is close to the optimum value ($N_{optimum} = 24$ in this example) and the diodes are resized to keep the efficiency high.

The 24-stage rectifier presents the best performance of the three circuits. In order to meet the output specifications ($V_L = 1$ V, $I_L = 1$ μA), the average value of the available power is -19.6 dBm. This corresponds to an overall converter efficiency $\eta = 9.1\%$, against the theoretical value of 13% previously calculated in this section.

The input impedance of the 24-stage converter measured for $P_{AV} = -19.8$ dBm (DC output voltage = 1 V) at 900 MHz equals (50 + j 12.7) Ω, which is close to the nominal theoretical value of 60 Ω ($R_S + R_L \approx 40\ \Omega + 20\ \Omega$). The imaginary part not equal to zero indicates that a fraction of the 38 nH inductance equal to 2.26 nH is not compensated by the capacitive input of the rectifier.

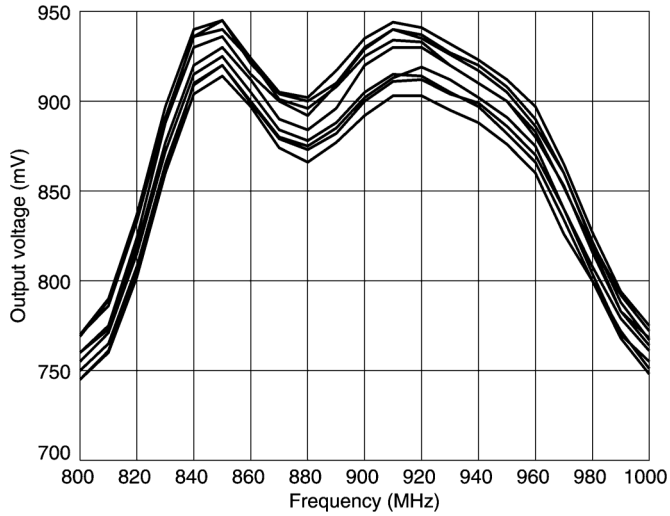


Fig. 11. DC voltage at the multiplier output versus input signal frequency ($P_{AV} = -20$ dBm). Measurements were taken for 9 samples of the 24-stage rectifier for a load resistance of 1 MΩ.

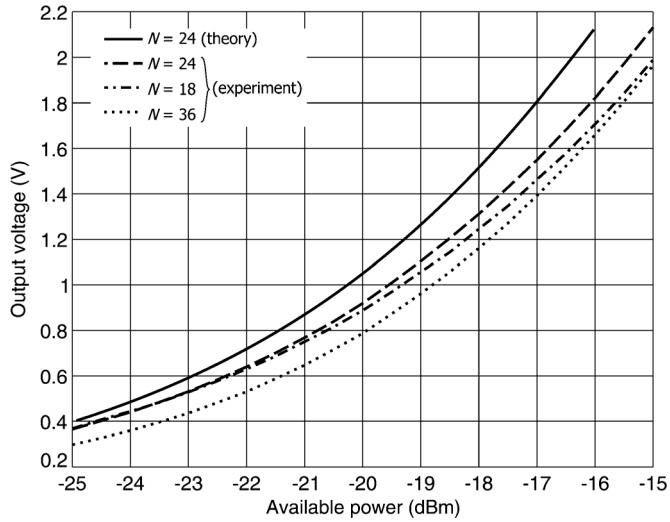


Fig. 12. Experimental average (taken over 9 samples of each voltage multiplier) DC voltage at the multiplier output versus available power at the input. Measurements were taken with a load resistance of 1 MΩ. The solid line indicates the theoretical values of the output voltage calculated for $N = 24$, using nominal parameters of the technology.

Fig. 13 shows a micrograph of the 24-stage rectifier, which occupies an area (excluding the measurement pads) of around 0.25 mm^2.

VI. CONCLUSIONS

A general analysis of the AC-DC converter powered by an RF signal and composed of a matching network and a voltage multiplier has been presented. A universal method for the optimization of the power conversion efficiency (PCE) for specified load voltage, load current, and source impedance has been described. The essence of this method is the use of the Shockley equation to represent the I-V characteristic of the diode. Using both a PCE-optimized rectifier along with a matching network, we have proposed an efficient method to explore the space of possible designs for multi-stage rectifiers. Starting from the model derived in this study along with the results of the PCE and

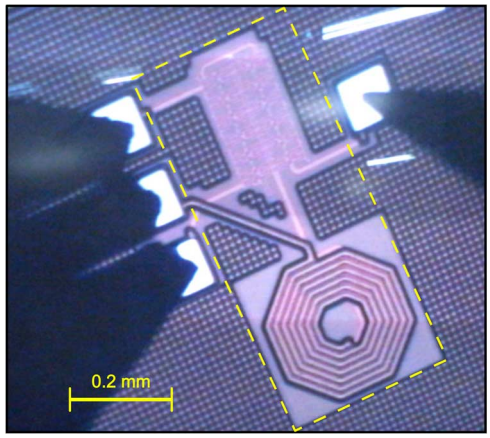


Fig. 13. Micrograph of the 24-stage AC-DC converter.

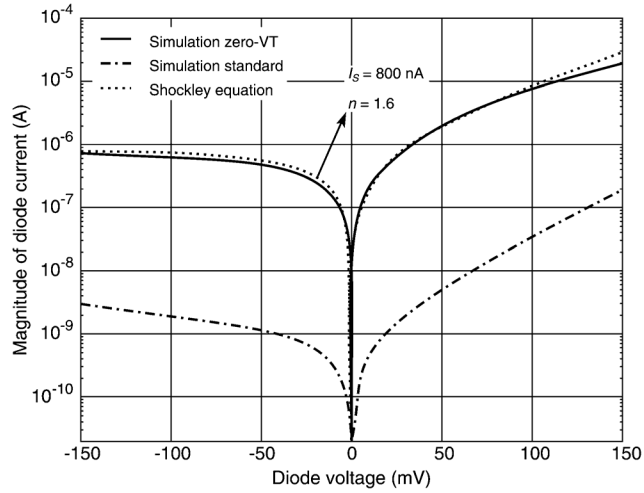


Fig. 14. Simulated I_D vs. V_D characteristics of the standard and zero-VT transistors available in the 130 nm technology, both connected as diodes ($V_D = V_G$, $V_S = V_B = 0$) with $W = L = 4.2\ \mu\text{m}/420$ nm. The dashed line represents the Shockley equation for $n = 1.6$ and a saturation current of 800 nA.

matching network analysis, three rectifiers designed in a 130 nm technology were able to meet the desired specifications, load voltage and current of 1 V and 1 μA, respectively, from an input power of around -20 dBm with an overall efficiency of 10%. The experimental results obtained for the 18-stage, 24-stage, and 36-stage rectifiers are quite close to each other. This confirms that there is a broad minimum for the required available power which satisfies the converter specifications. To finish, it should be emphasized that the analysis and graphs presented in this paper constitute a powerful design tool for energy harvesters powered by RF signals.

Appendix A
Input Capacitance and Output Resistance of the Rectifier

Assuming, as before, that the coupling capacitances C_i, $i = 1,\ N$ are much higher than the diode capacitances, the input capacitance C_{in} is approximately equal to NC_D, where C_D is the average diode capacitance [4].

The values of V_o and R_o calculated from (6) are

$$\frac{V_o}{n\phi_t} = \frac{V_L}{n\phi_t}\bigg|_{I_L=0} = N \ln\left[I_0\left(\frac{V_A}{n\phi_t}\right)\right] \tag{24}$$

and

$$R_O = \frac{V_O - V_L}{I_L} = \frac{Nn\phi_t}{I_S}\frac{\ln[1 + I_L/I_S]}{\frac{I_L}{I_S}} \tag{25}$$

For the optimized rectifier, the output resistance becomes

$$R_O = \frac{V_L}{I_L}\frac{\ln[1 + I_L/I_S]}{\frac{I_L}{I_S}} \tag{26}$$

It is interesting to note that, for $V_A/n\phi_t \ll 1$, $I_L/I_S \ll 1$. Thus, the output resistance becomes equal to V_L/I_L.

Appendix B
Rectifier Diodes

Schottky diodes, low-VT or zero-VT (native) transistors connected as diodes are generally employed for the AC-DC conversion of energy harvesters. In the experiments reported in this paper diode-connected zero-VT transistors were used for the diodes of the rectifier. The main reason for this choice is that these transistors have a much higher current drive capability as compared to standard or low-VT transistors with the same gate area. The consequent small capacitance of the diodes is advantageous since it avoids the deterioration of the performance observed when the diode capacitances are a significant fraction of the coupling capacitances.

For the sake of comparison, the DC characteristics of both a zero-VT transistor and a standard transistor connected as a diode are shown in Fig. 14. The saturation current of the zero-VT transistor is more than two orders of magnitude higher than that of the conventional transistor available in the IBM 130 nm process for the same gate area. Fig. 14 shows the approximation of the I-V characteristics of the diode-connected zero-VT transistor by the Shockley equation in the range of $-150\ \text{mV} < V_D < 150\ \text{mV}$. In this voltage range the approximation of the I-V characteristic of a zero-VT transistor by the Shockley equation is acceptable. It should be mentioned here that the voltage drop across the diode varies between $V_A - V_L/N$ and $-V_A - V_L/N$, with V_L/N given by (6). If the available power is of the order of -16 dBm or less, $V_{ANT} < 50$ mV (for $R_{ant} = 50\ \Omega$). Typically, the value of V_A will not exceed 3 V_{ANT} in an integrated circuit implementation. This means that the forward voltage across the diode will not exceed a certain value (e.g., 150 mV) whereas the reverse voltage will not exceed a somewhat larger value (e.g., 250 mV). As can be seen in the graph, the reverse current of the diode-connected zero-VT transistor does not change to a significant extent for reverse voltages higher than 100 mV. Thus, the Shockley equation provides a good approximation of the I-V characteristics of the diode-connected device for the usual range of voltages across the diodes of the rectifier.

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