Inadequacy of the Classical Formulation of the CMOS Schmitt Trigger

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Summary
The classical CMOS Schmitt trigger (ST) circuit operating in strong inversion has been used as a basic building block in electronics since the seventies. However, no appropriate analytical models for determining the hysteresis threshold voltages have been presented. In this paper, we review the classical CMOS ST formulation for operation in strong inversion and introduce a new model for calculating the hysteresis window. In order to validate the approximations employed in this work, we measured the hysteresis curve for several combinations of transistors available in the popular off-the-shelf CD4007 and resorted to simulation in a 180 nm technology for the specific purpose of measuring the ST window in terms of the transistors aspect ratios. Numerical, experimental and simulation results corroborate the approximations employed in this research to derive simple expressions for the hysteresis threshold voltages.

KEYWORDS
CMOS Schmitt trigger, CMOS inverter, MOSFET model, strong inversion, hysteresis width.

1 | INTRODUCTION

The classical CMOS ST shown in Figure 1 is one of the most basic building blocks for electronic circuits. It can be used for applications such as noise reduction, pulse-width preserving, pulse stretching, conversion of continuous wave to square wave and relaxation oscillators [1]. The classical CMOS ST was patented in 1975 [2], but accurate approximations for the ST high and low threshold voltages for all ratios of feedback are still lacking, which is not the case for ST circuits based on either bipolar transistors or operational amplifiers [3] .

Several authors [4]-[7] presented expressions for calculating the threshold voltages of the CMOS ST decades ago. Although the expressions for the threshold voltages appear to be good approximations for strong positive feedback (wide hysteresis window), they totally fail for weak feedback (narrow hysteresis window). As pointed out in [8], sometimes it is important to include a narrow hysteresis window to a comparator in order to avoid inappropriate output changes of the comparator due to interference signals of very-high frequency. Another important application of comparators of narrow hysteresis is that of ripple-based control of DC-DC converters [9], [10].

Due to the lack of a good model to determine the hysteresis window, several designers have either resorted to intensive simulation [10], [11] to find out the appropriate size of the ST transistors or proposed ST architectures [12], [13] that are amenable to adjustment. In fact, designers of integrated circuits still struggle to place correctly the thresholds of the CMOS ST, in spite of its use in present-day applications [14]. On the other hand, recent work [15]-[18] on the ST has been focused on the weak inversion region, but there is only one study [18] that provides equations developed for the forward and reverse threshold voltages.

In this paper, we revisit the equations of the classical CMOS Schmitt trigger in strong inversion. The main motivation for this study was to provide the readers with approximations that are good enough to determine the transistor parameters (current scaling factors) for the intended hysteresis width, independent of its size.

Regarding the organization of this paper, Section 2 revisits the usual model of the classical CMOS ST circuit and points out some shortcomings of the existing expressions for calculating the hysteresis threshold voltages. A more general analysis for determining the ST threshold voltages follows in Section 3, where the voltage transfer characteristic of the ST, for both rising and falling inputs, is described. Asymptotic values of the hysteresis window for both strong and weak feedback are given. Section 4 recalls an accurate strong inversion model of the MOS transistor and develops accurate expressions for the high and low threshold voltages of the ST inverter. Finally, Section 5 reports experimental and simulation results for different feedback strengths.

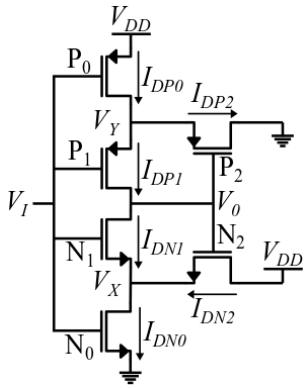

Figure 1: Classical CMOS Schmitt-trigger circuit [1].

2 | REVISITING THE CLASSICAL MODELS OF THE ST IN STRONG INVERSION

For a first order analysis of the ST we use the simplest model of the MOS transistor [19], [20] in strong inversion, given by

$$I_{DNi} = \beta_{Ni}[(V_G - V_{TN} - V_S)^2 - (V_G - V_{TN} - V_D)^2] \tag{1a}$$

and

$$I_{DPi} = \beta_{Pi}[(-V_G + V_{TP} + V_S)^2 - (-V_G + V_{TP} + V_D)^2] \tag{1b}$$

where, V_S, V_D, and V_G are the source, drain, and gate voltages, respectively. $V_{TN} > 0$ and $V_{TP} < 0$ are the threshold voltages of the n- and p-channel transistors, respectively. It is of paramount importance to base the analysis of the CMOS Schmitt trigger on a MOSFET model such as that of equations (1a) and (1b), which preserves the symmetry between source and drain. Indeed, the symmetry property is essential for the correct simulation of the series association of MOS transistors [21].

In the simplified analysis that follows, for the sake of simplicity we have assumed that the transistor strengths, or transconductance parameters, given by

$$\beta_{Ni} = \frac{\mu_N C_{ox}}{2}\left(\frac{W}{L}\right)_{Ni} \qquad \beta_{Pi} = \frac{\mu_P C_{ox}}{2}\left(\frac{W}{L}\right)_{Pi} \tag{1c}$$

are the same for the P and N networks, *i.e.*, $\beta_{N0}=\beta_{P0}=\beta_0$, $\beta_{N1}=\beta_{P1}=\beta_1$, and $\beta_{N2}=\beta_{P2}=\beta_2$.

The symbols in (1c) have their usual meanings [8].

In order to get an insight into the first order behavior of the ST circuit, we initially resorted to numerical calculations of equations (1a) – (1b), along with the Kirchhoff current law for each node. By proceeding in this way, we were able to have full control of the equation parameters and check the validity of the approximations that we have used for developing an analytical model. Also, the information about the number of iterations, the region of operation of each transistor and the plots of the drain currents of transistors N_1 and P_1 led to important conclusions about the circuit behavior.

The numerical simulation of the effect of the feedback strength in the ST circuit can be seen in Figure 2, which shows the cases of strong, moderate, weak, and no (standard CMOS inverter) feedback. For the numerical calculation the input voltage was swept from 0 V to V_{DD}= 1 V in steps of 1 mV (or even less in some cases). For each new value of the input voltage, the initial condition for the output voltage V_O is its value found in the previous step. The same procedure was applied to descending values of the input voltage, from V_{DD} to 0 V.

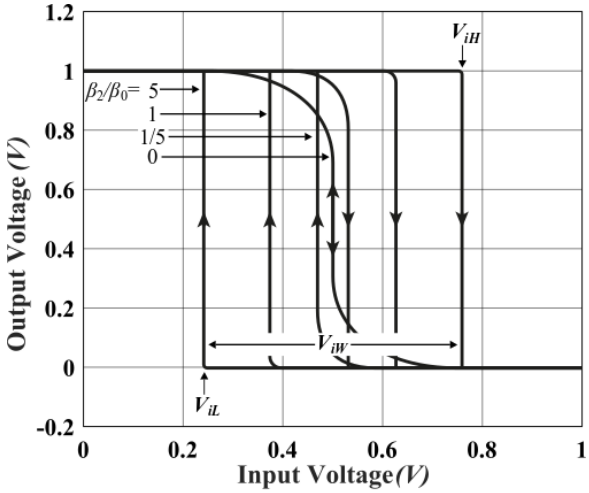

Figure 2: Voltage transfer curves (VTCs) of the standard inverter (β2/β0 =0) and STs with weak feedback (β2/β0=1/5), moderate feedback (β2/β0 =1) and strong feedback (β2/β0 =5), for β0 = β1, VTN=|VTP|= 0.2 V, VDD=1 V.

The case of a wide hysteresis loop is appropriately modeled [5]-[7] by

$$V_{iH} = \frac{V_{TN}+V_{DD}\sqrt{\frac{\beta_2}{\beta_0}}}{1+\sqrt{\frac{\beta_2}{\beta_0}}} \tag{2a}$$

$$V_{iL} = \frac{V_{TP}+V_{DD}}{1+\sqrt{\frac{\beta_2}{\beta_0}}} \tag{2b}$$

$$V_{iW} = V_{iH} - V_{iL} \tag{2c}$$

V_{iH} and V_{iL} are the high and low threshold voltages of the Schmitt trigger, respectively, and V_{iw} is the hysteresis window. The meaning of wide hysteresis loop, which is not clear in the technical literature, will be clarified in Section 3.

It is easy to show that equations (2a)-(2c) are meaningless in the case of small feedback ratios. In fact, for very weak feedback, $\beta_2/\beta_0 \ll 1$, the formulas in (2) reduce to $V_{iH}=V_{TN}<V_{DD}+V_{TP}=V_{iL}$. In order to avoid V_{iH} to be less than V_{iL}, we must have, from equations (2)

$$\frac{\beta_2}{\beta_0} > \left(\frac{V_{EFF}}{V_{DD}}\right)^2 \tag{2d}$$

$$V_{EFF} = V_{DD} - V_{TN} + V_{TP} \tag{2e}$$

Here, V_{EFF} is the *effective supply voltage*. As we shall see, this is an important parameter for the characterization of the Schmitt trigger. Thus, the use of equations (2a) and (2b) for moderate and weak feedback factors β_2/β_0 can lead to a negative hysteresis width or, equivalently, an anticlockwise hysteresis inverter.

A general formula for the calculation of the hysteresis window $V_{iW.}$ was proposed in [4]. For the case of P and N networks with equal transconductance parameters, and with $\beta_0=\beta_1$, equation (16) of reference [4] is written as

$$V_{iW} = \frac{V_{DD}+\frac{V_{TP}-V_{TN}}{2}}{1+\sqrt{\frac{\beta_0}{\beta_2}}} \tag{3}$$

In order to check whether the approximations of references [4] - [6] for the hysteresis width are appropriate, Figure 3 shows plots of the approximations together with a numerical simulation that employs the transistor equations (1a) – (1b).

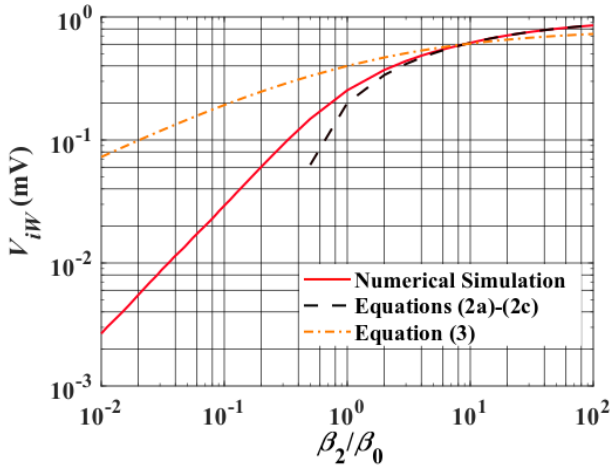

Figure 3: Hysteresis width versus feedback ratio β2/β0 of the ST in Figure 1 for VTN=|VTP|= 0.2 V, VDD=1 V, and β0=β1.

For the data of Figure 3, V_{EFF}= 0.6 V; thus, the hysteresis width given by equations (2a) - (2c) becomes equal to zero for a feedback ratio $\beta_2/\beta_0=(V_{EFF}/V_{DD})^2$ =0.36. This is the reason for truncating the curve corresponding to equations (2a) - (2c) for values of feedback ratio less than 0.36. On the other hand, as will be demonstrated in Section 3, those equations are exact for $\beta_2/\beta_0>(V_{EFF}/V_{TP})^2$, *i.e.* $\beta_2/\beta_0>9$ in the case of Figure 3. The coincidence of the numerical results with equations (2a) - (2c) is quite clear for $\beta_2/\beta_0>9$. Finally, equation (3) (equation (16) of [4]) is not an adequate approximation, since it gives very poor results for the case of weak feedback factors ($\beta_2/\beta_0<1$).

The next section is devoted to a simplified analysis of the ST.

3 | DC Transfer Characteristic of the Schmitt Trigger

For the ongoing analysis, the voltage transfer characteristic (VTC) is divided into regions according to the conducting state of the transistors, as shown in Figure 4. Regions I, II, IV, and V are valid for both rising and falling input voltages. Regions III and VI are associated with a rising and a falling input, respectively.

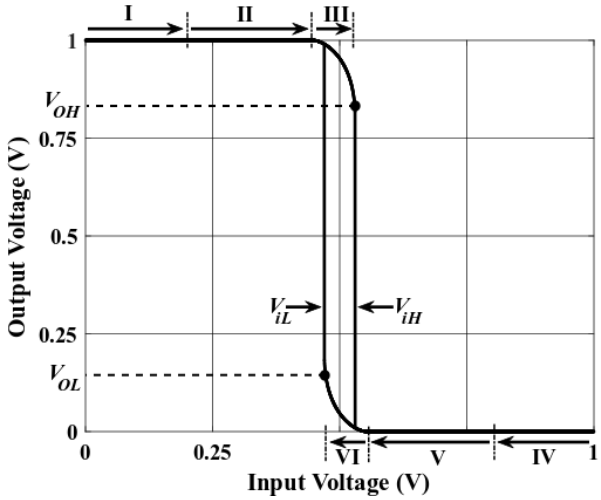

Figure 4: VTC of the ST in Figure 1 for VTN=|VTP|= 0.2 V, VDD=1 V, and β0=β1=5β2.

In region I neither of the n-channel transistors conducts. In region II, both N_0 and N_2 conduct, whereas N_1 is off. Finally, in region III the three n-channel transistors conduct. Figure 5 shows the states of the transistors of the N-network for regions I, II, and III. Regions IV, V, and VI, defined according to the conduction state of the PMOS transistors, are analogous to regions I, II and III, respectively.

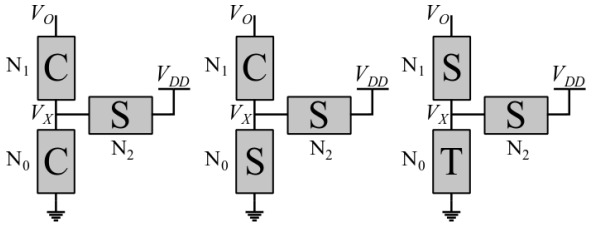

Figure 5: Left to right: State of the transistors of the N-network for increasing input voltage, for regions I, II, and III, respectively. C, S, and T stand for cutoff, saturation, and triode regions, respectively.

The description of regions I to VI of the graph in Figure 4 is given by the following conditions.

(a) Rising input $V_I : 0 \rightarrow V_{DD}$

Region I: $0 < V_I < V_{TN}$: N_0, N_1, and P_2 - cutoff, P_0 and P_1 - triode, N_2 - verge of conduction.
The calculation of V_X is shown below.

$$I_{DN2} = \beta_2(V_{DD} - V_{TN} - V_X)^2 = 0 \Rightarrow$$
$$V_X = V_{DD} - V_{TN}; \quad V_O = V_{DD} \tag{4}$$

Region II: N_1 and P_2 - cutoff, P_0 and P_1 - triode, N_0 and N_2 - saturation.
The value of V_X in Region II is found as follows:

$$I_{DN2} = I_{DN0} \Rightarrow \beta_2(V_{DD} - V_{TN} - V_X)^2 = \beta_0(V_I - V_{TN})^2 \Rightarrow$$
$$V_X = V_{DD} - V_{TN} - \sqrt{\frac{\beta_0}{\beta_2}}(V_I - V_{TN}); \quad V_O = V_{DD} \tag{5}$$

Thus, the cutoff of transistor N_1 implies that $(V_I - V_{TN}) < V_X$ or, equivalently,

$$V_I < \frac{V_{TN} + V_{DD}\sqrt{\frac{\beta_2}{\beta_0}}}{1+\sqrt{\frac{\beta_2}{\beta_0}}} \tag{6}$$

Region III: $\frac{\left(V_{TN} + V_{DD}\sqrt{\frac{\beta_2}{\beta_0}}\right)}{1+\sqrt{\frac{\beta_2}{\beta_0}}} \leq V_I \leq V_{iH}$: N_0 - triode, N_1 and N_2 - saturation, P_2 - cutoff, P_0 and P_1 – triode.

Before describing the equations of the ST for region III, we first determine the condition under which the high threshold voltage V_{iH} occurs in region II, *i.e.* the width of region III tends towards zero or, equivalently, V_{OH} tends towards V_{DD}. This limit condition can be readily found out by noting that, when V_{OH} tends towards V_{DD}, transistors P_1 and N_1 never conduct simultaneously, *i.e.*

$$V_{iH} = V_{DD} + V_{TP}$$

Equating the higher and lower limits of region III we find that

$$\frac{\left(V_{TN}+V_{DD}\sqrt{\frac{\beta_2}{\beta_0}\Big|_{lim}}\right)}{1+\sqrt{\frac{\beta_2}{\beta_0}\Big|_{lim}}} = V_{DD} + V_{TP} \rightarrow \frac{\beta_2}{\beta_0}\Big|_{lim} = \left(\frac{V_{EFF}}{V_{TP}}\right)^2 \tag{7}$$

Thus, the classical equations (2a) - (2b) are exact only for

$$\frac{\beta_2}{\beta_0} > \left(\frac{V_{EFF}}{V_{TP}}\right)^2$$

In other words, the circuit will show a wide hysteresis loop if the inequality above holds, whereas $\beta_2/\beta_0<1$ is characteristic of a narrow hysteresis loop. In Section 4 we describe how V_{iH} can be accurately determined for the case in which the feedback factor is less than the limit given above.

For weak feedback, we can obtain very directly the main results of Section 4 by taking advantage of the closeness between the VTC of the ST and that of the inverter. In order to simplify the equations, we start with the case for which $V_{TN}<<V_{DD}$ and $|V_{TP}|<<V_{DD}$. Thus, we will determine V_{iH} under the hypothesis $V_I=V_{iH}=V_O$.

Once again, we will assume that the NMOS and PMOS networks have the same transconductance parameters. The KCL for node V_X in Figure 1, with V_I equal to the high threshold voltage, is

$$\beta_0[(V_{iH} - V_{TN})^2 - (V_{iH} - V_{TN} - V_X)^2] = \beta_1(V_{iH} - V_{TN} - V_X)^2 + \beta_2(V_{iH} - V_{TN} - V_X)^2 \tag{8}$$

Thus,

$$(V_{iH} - V_{TN} - V_X)^2 = \frac{(V_{iH}-V_{TN})^2}{1+\frac{\beta_1+\beta_2}{\beta_0}} \tag{9}$$

If $\beta_2/\beta_0 <<1$ the P network is approximately equivalent to the series association of P_0 and P_1 [21]; thus, the DC equation of the output node is

$$I_{DN1} = \frac{\beta_1(V_{iH}-V_{TN})^2}{1+\frac{\beta_1+\beta_2}{\beta_0}} = I_{DP1} \cong \frac{\beta_1\beta_0}{\beta_0+\beta_1}(V_{DD} - V_{iH} + V_{TP})^2 \tag{10}$$

From (10) we deduce the value of the high threshold voltage of the ST circuit as

$$V_{iH} = V_{TN} + \frac{V_{EFF}}{1+\sqrt{\frac{\beta_0+\beta_1}{\beta_0+\beta_1+\beta_2}}} \tag{11}$$

Since $\beta_2/\beta_0 <<1$, a first-order approximation of the square root in the denominator of (11) leads to

$$V_{iH} = \frac{V_{DD}+V_{TN}+V_{TP}}{2} + \frac{1}{8}\frac{\beta_2}{\beta_0+\beta_1}V_{EFF} \tag{12}$$

where the first term in (12) is the inverter threshold voltage.

(b) Falling input $V_I : V_{DD} \rightarrow 0$

For a descending input voltage, an analogous analysis gives

$$V_{iL} = \frac{V_{DD}+V_{TN}+V_{TP}}{2} - \frac{1}{8}\frac{\beta_2}{\beta_0+\beta_1}V_{EFF} \tag{13}$$

Thus, a rough approximation of the hysteresis width for weak feedback is

$$V_{iW} = V_{iH} - V_{iL} = \frac{1}{4}\frac{\beta_2}{\beta_0+\beta_1}V_{EFF} \tag{14}$$

The accurate approximation of V_{iW}, demonstrated in the Section 4 for V_{TN}=-V_{TP} and slope factors n_N=n_P=1, is

$$V_{iW} = V_{iH} - V_{iL} = \frac{\beta_2}{4\beta_0}\left(\sqrt{\frac{\beta_0}{\beta_0+\beta_1}} + 2\frac{V_{TN}}{V_{EFF}}\right)^2 V_{EFF} \tag{15}$$

which also gives a linear dependence of the hysteresis width on the current strength β_2. Figure 6 presents a plot of equation (15) together with numerical simulations using equations (1a) and (1b). Note that equation (15) provides a very good approximation of the hysteresis widths for$\beta_2/\beta_0<1$.

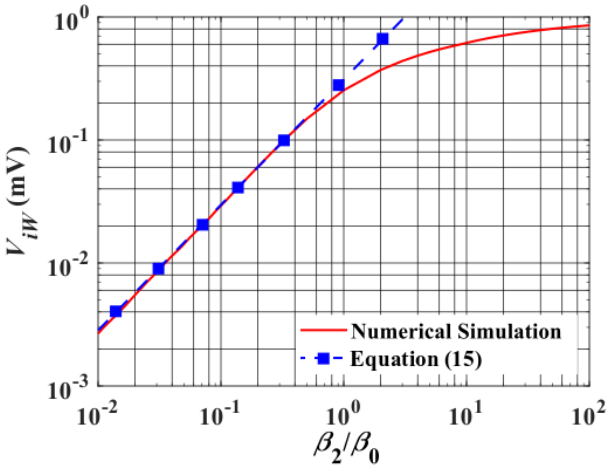

Figure 6: Hysteresis width versus feedback ratio β_2/β_0 of the ST in Figure 1 for V_{TN}=|V_{TP}|= 0.2 V, V_{DD}=1 V, and β_0=β_1.

A comment is now in order. When narrow hysteresis comparators are needed, the classical expressions of equations (2a) and (2b) in this paper fail to help designers. Note that the feedback strength is dependent not only on the β's ratio, but also on the ratio of the MOSFET threshold voltages to the effective supply voltage V_{EFF}.

Before going to experimental and simulation results, the next section shows a more accurate and detailed analysis for determining the high and low threshold voltages of the Schmitt trigger.

4 | EQUATIONS FOR THE DETERMINATION OF THE HIGH AND LOW THRESHOLD VOLTAGES V_{IH} AND V_{IL}

The I-V equations for strong inversion operation of the NMOS and PMOS transistors shown in Figure 7, can be written as in equations (16) and (17), and Table 1, where s and d are binary values defined in the first column of Table 1.

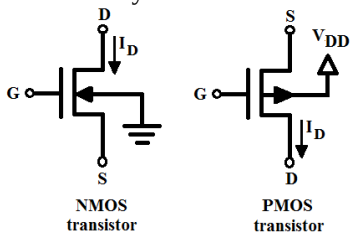

Figure 7: Symbols for the terminals of the NMOS and PMOS transistors.

$$I_{DN} = \beta_N n_N \left[s\left(\frac{V_G - V_{TN}}{n_N} - V_S\right)^2 - d\left(\frac{V_G - V_{TN}}{n_N} - V_D\right)^2 \right] \quad (16)$$

$$I_{DP} = \beta_P n_P \left[s\left(\frac{V_{DD} - V_G + V_{TP}}{n_P} - (V_{DD} - V_S)\right)^2 - d\left(\frac{V_{DD} - V_G + V_{TP}}{n_P} - (V_{DD} - V_D)\right)^2 \right] \quad (17)$$

Table 1: Conditions under which the mos transistors operate in the regimes of cutoff, triode, or saturation.

Region	Source bias	Drain bias
	NMOS transistor	
Triode (s=d=1)	$V_G - V_{TN} - n_N V_S > 0$	$V_G - V_{TN} - n_N V_D > 0$
Saturation (s=1, d=0)	$V_G - V_{TN} - n_N V_S > 0$	$V_G - V_{TN} - n_N V_D \leq 0$
Cutoff (s=d=0)	$V_G - V_{TN} - n_N V_S \leq 0$	$V_G - V_{TN} - n_N V_D \leq 0$
	PMOS transistor	
Triode (s=d=1)	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_S) > 0$	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_D) > 0$
Saturation (s=1, d=0)	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_S) > 0$	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_D) \leq 0$
Cutoff (s=d=0)	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_S) \leq 0$	$V_{DD} - V_G + V_{TP} - n_P(V_{DD} - V_D) \leq 0$

Now, let us make use of both Figure 1 and Figure 2 to explain how to determine the high and low threshold voltages of the Schmitt trigger. First, examining the circuit of Figure 1, the ST circuit reduces to the conventional CMOS inverter if transistors N_2 and P_2 are removed, thus leading to the hysteresis-less curve in Figure 2. The value of V_{OH} for the inverter is the output voltage on the edge of saturation of the PMOS transistor [22]. For high values of β_2/β_0, Figure 2 shows that V_{OH} tends towards V_{DD}.

In other words, the infinite gain of the standard inverter (β_2=0) is confined to the region V_I-V_{TN}<V_O<V_I-V_{TP}. Thus, for the inverter, the maximum value (V_{OH}) of V_O at which the inverter is in the saturation region is V_{OH}= V_I-V_{TP}. On the other hand, when the positive feedback provided by transistor N_2 is very strong, *i.e.*

$$\frac{\beta_2}{\beta_0} > \left(\frac{V_{EFF}}{V_{TP}}\right)^2 \rightarrow V_{OH} = V_{DD}$$

In order to develop an analytical model, we have approximated the value of V_{OH} as a weighted sum of V_{DD} and the output voltage of the inverter on the edge of saturation of the PMOS transistor, as given below

$$V_{OH} = \frac{\beta_2}{\beta_0+\beta_2} V_{DD} + \frac{\beta_0}{\beta_0+\beta_2} V_{SD,satP} \tag{18}$$

where

$$V_{SD,satP} = V_{DD} - \frac{V_{DD}+V_{TP}-V_{iH}}{n_P} \tag{19}$$

and V_{iH} represents the upper threshold voltage. Combining (18) and (19) and denoting α=1/(1+β_0/β_2), we find that

$$V_{OH} = V_{DD} - \frac{(1-\alpha)(V_{DD}+V_{TP}-V_{iH})}{n_P} = V_{DD} - \frac{(1-\alpha)H}{n_P} \tag{20}$$

where $H = V_{DD} + V_{TP} - V_{iH}$.

For V_I=V_{iH} and V_O=V_{OH} the following conditions hold: N_0 - triode, N_1 and N_2 - saturation, P_2 - cutoff, P_0 and P_1 – triode.

Equation (21) describes the current through the (equivalent) series association of transistors P_1 and P_2. Note that the currents through N_1 and N_2 in (22) are independent of the drain voltages. The application of KCL to node V_X yields (23).

Using the approximation of (20) for V_{OH} and the equality I_{DN1}=I_{DP1}, after lengthy algebra, we find (24). This equation gives the high threshold voltage V_{iH}.

$$I_{DP1} = I_{DP0} = n_P \frac{\beta_0\beta_1}{\beta_0+\beta_1}\left[\left(\frac{V_{DD}-V_{iH}+V_{TP}}{n_P}\right)^2 - \left(\frac{V_{DD}-V_{iH}+V_{TP}}{n_P} - (V_{DD}-V_{OH})\right)^2\right] \tag{21}$$

$$I_{DN0} = n_N\beta_0\left[\left(\frac{V_{iH}-V_{TN}}{n_N}\right)^2 - \left(\frac{V_{IH}-V_{TN}}{n_N} - V_X\right)^2\right]; I_{DN1} = n_N\beta_1\left(\frac{V_{iH}-V_{TN}}{n_N} - V_X\right)^2; I_{DN2} = n_N\beta_2\left(\frac{V_{OH}-V_{TN}}{n_N} - V_X\right)^2 \tag{22}$$

$$I_{DN0} = I_{DN1} + I_{DN2} \tag{23}$$

$$\frac{n_N}{n_P}H^2[1-\alpha^2] + \frac{\beta_2}{\beta_0}\left[H\left(1+\sqrt{\frac{n_N}{n_P}\frac{\beta_0}{\beta_0+\beta_1}[1-\alpha^2]} - \frac{(1-\alpha)}{n_P}\right) - V_{TP}\right]^2 = (V_{EFF}-H)^2 \tag{24}$$

The low threshold voltage V_{iL} of the ST can be derived similarly to V_{iH}. In order to save space, the equations and algebra that led to the result for V_{iL} in (25) are not transcribed here.

$$\frac{n_P}{n_N}L^2[1-\alpha^2] + \frac{\beta_2}{\beta_0}\left[L\left(1+\sqrt{\frac{n_P}{n_N}\frac{\beta_0}{\beta_0+\beta_1}[1-\alpha^2]} - \frac{(1-\alpha)}{n_N}\right) + V_{TN}\right]^2 = (V_{EFF}-L)^2 \tag{25}$$

where $L = V_{iL} - V_{TN}$.

It is important to notice that applying a very strong feedback to (24) and (25), *i.e.* $\alpha \rightarrow 1$, leads directly to equations (2a) - (2b), as already discussed in Section 2. To obtain more practical analytical equations for the weak feedback cases, further algebra is necessary.

Now, for very weak feedback, *i.e.* $\alpha \rightarrow 0$, (24) can be rewritten as

$$V_{iH} \cong \frac{V_{DD}+V_{TP}+V_{TN}}{2} + \frac{V_{EFF}}{8}\frac{\beta_2}{\beta_0}\left(a - \frac{2V_{TP}}{V_{EFF}}\right)^2 \tag{26}$$

$$V_{EFF} = V_{DD} + V_{TP} - V_{TN}\ ;\ \ a = \frac{n_N\sqrt{\frac{\beta_0}{\beta_0+\beta_1}}+n_P-1}{n_P}$$

while (25) as

$$V_{iL} \cong \frac{V_{DD}+V_{TP}+V_{TN}}{2} - \frac{V_{EFF}}{8}\frac{\beta_2}{\beta_0}\left(b - \frac{2V_{TN}}{V_{EFF}}\right)^2 \tag{27}$$

$$b = \frac{n_P\sqrt{\frac{\beta_0}{\beta_0+\beta_1}}+n_N-1}{n_N}$$

Finally, the difference between (26) and (27) leads to,

$$V_{iW} = V_{iH} - V_{iL} = \frac{V_{EFF}}{4}\frac{\beta_2}{\beta_0}\left[\left(a - \frac{2V_{TP}}{V_{EFF}}\right)^2 - \left(b - \frac{2V_{TN}}{V_{EFF}}\right)^2\right] \quad (28)$$

For $n_N = n_P = 1$ and $V_{TN} = -V_{TP}$, (27) can be further simplified to

$$V_{iW} = V_{iH} - V_{iL} = V_{EFF}\frac{\beta_2}{4\beta_0}\left(\sqrt{\frac{\beta_0}{\beta_0+\beta_1}} + 2\frac{V_{TN}}{V_{EFF}}\right)^2 \quad (29)$$

5 | EXPERIMENTAL AND SIMULATION RESULTS

For the experimental validation of the results reported herein, samples of the popular CD4007, which contains 3 NMOS and 3 PMOS transistors, were used.

The transistor parameters, namely the threshold voltages and the specific currents, were extracted according to the g_m/I_D methodology described in Figure 4 of reference [23], while the values for the slope factors n_N and n_P were determined using the method described on pages 463-464 of reference [20]. Table 2 shows the parameters extracted for both types of transistors.

Table 2: EXTRACTED PARAMETERS OF THE NMOS AND PMOS TRANSISTORS OF THE CD4007.

NMOS			**PMOS**		
V_{TN}	1.41	V	V_{TP}	-1.27	V
β_N*	1.1	mA/V^2	β_P*	0.85	mA/V^2
n_N (V_{GB}=3V)	1.71	-	n_P (V_{GB}=-3V)	1.13	-
n_N (V_{GB}=5V)	1.54	-	n_P (V_{GB}=-5V)	1.09	-
n_N (V_{GB}=7V)	1.46	-	n_P (V_{GB}=-7V)	1.07	-

*The values for β_N and β_P were extracted from the values for the correlated specific currents I_{SN} and I_{SP} [20].

For the sake of simplicity, equal values of β_N and β_P were used for the calculation of the ST threshold voltages. In order to emulate different feedback factors, series and parallel associations of transistors [21] were employed, as shown in Figure 8.

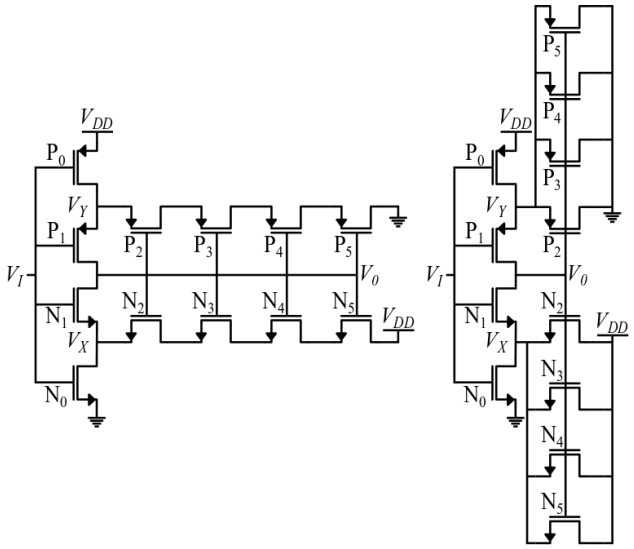

Figure 8: Series and parallel associations of transistors to obtain feedback factors β_2/β_0 of 1/4 (left) and 4/1 (right).

Figure 9 shows the hysteresis width obtained either experimentally or by the difference between the values of V_{iH} and V_{iL} calculated using equations (24) and (25), which are valid for any feedback ratio. It can be readily seen that the experimental and analytical approaches provide similar values, especially for feedback ratios close to 1. For 10V and 15 V supplies, the experimental measurements and the analytical curves are in very close agreement for $\beta_2/\beta_0 \geq 1$. On the other hand, the proximity of the experimental points from the analytical curves is not as good for weak feedback. These deviations, for $\beta_2/\beta_0<1$, can be explained by means of some simplifying assumptions employed to determine the values of V_{iH} and V_{iL}. Firstly, the p- and n-networks were assumed to have the same strength, which is not true, especially around the ST threshold points. Secondly, identical transistors were assumed to have the same transconductance parameters, but this assumption does not hold in the practical case, since transistors with different gate voltages (the gate voltage of the feedback transistors is different from that of the input transistors) have differences in their mobility as well in their slope factor. The feedback ratio range of the experimental circuit was no further increased due to the use of discrete components and the difficulty in finding matched transistors.

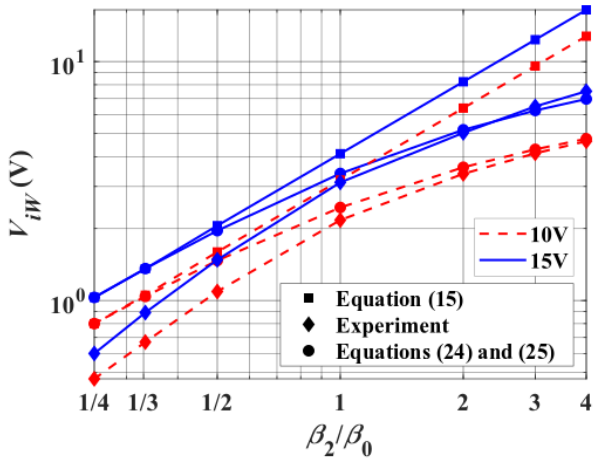

Figure 9: Calculated and experimental results of STs built with samples of the off-the-shelf CD4007. Solid and dashed lines represent values for 15V and 10V, respectively. Closed circles are calculated values from equations (24) and (25), squares are calculated values from equation (15), while diamonds represent experimental results.

We have run simulations of STs with high voltage (5V) thick gate devices of a 180 nm technology of the Silterra D18V process. The approximate parameters of the transistors required as inputs for the ST model developed herein are presented in Table 3. Note that the p-channel transistors are 2 times wider than the n-channel transistors to equalize the transconductance parameters of the NMOS and PMOS networks. For the simulations, all the transistors, except N2 and P2, have the fixed dimensions given in Table 3. The feedback transistors N2 and P2 are either composed of series-connected unit transistors, for feedback factors of less than unity, or a parallel association of unit transistors for feedback ratios of more than unity.

Table 3: APPROXIMATE PARAMETERS OF THE NMOS AND PMOS TRANSISTORS OF A 180 nm TECHNOLOGY

NMOS			**PMOS**		
V_{TN}	0.814	V	V_{TP}	-0.725	V
n_N	1.61	–	n_P	1.58	–
W_N	4	µm	W_P	8	µm
L_N	0.6	µm	L_P	0.6	µm

Figure 10 shows a comparison, for 3.3V and 5V supplies, of the hysteresis widths determined either from simulation or using the model developed herein. It can be noted that the model we have developed is a good approximation of the results provided by the simulation. It is interesting to note that, for high feedback factors, the hysteresis width is an increasing function of the supply voltage.

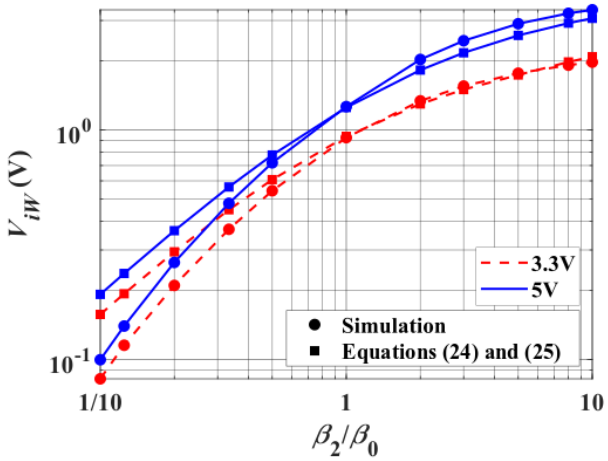

Figure 10: Hysteresis width in terms of the feedback factor obtained either through the model using approximations (24) and (25) (closed circles) or simulation (squares) of STs built with high voltage (5V) thick gate unit transistors of a 180 nm CMOS technology. Solid and dashed lines represent values for 5V and 3.3V, respectively.

6 | SUMMARY

We have shown, for the first time, the limit of validity of the classical equations (2a) – (2b) used for calculation of the hysteresis width in the classical CMOS Schmitt trigger. These commonly used expressions, although having been cited by numerous authors, seldom serves as a starting point of a design, except for wide hysteresis width. We have developed a model based on a simple approximation for both the output voltages at the trip points that allows the calculation of the high and low threshold voltages of the classical CMOS Schmitt trigger in strong inversion, for any feedback factor. We have also presented a very simple formula for the calculation of the trip points in terms of the main transistor parameters and supply voltage for the case of weak feedback. Circuit designers now have a more accurate model for determining the hysteresis thresholds.

Data sharing not applicable to this article as no datasets were generated or analysed during the current study

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