A 2-nW 1.1-V Self-Biased Current Reference in CMOS Technology

Edgar Mauricio Camacho-Galeano, Carlos Galup-Montoro, *Member, IEEE*, and Márcio Cherem Schneider, *Member, IEEE*

***Abstract*—This paper presents the design of an ultra-low-power self-biased 400-pA current source. We propose the use of a very simple topology along with a design methodology based on the concept of inversion level. An efficient design methodology has resulted in a cell area around 0.045 mm^2 in the AMI 1.5-μm CMOS technology and power consumption around 2 nW for 1.2-V supply. Simulated and experimental results validate the design and show that the current source can operate at supply voltages down to 1.1 V with a good regulation ($<$ 6%/V variation of the supply voltage) in a 1.5-μm technology.**

***Index Terms*—CMOS analog integrated circuit, current source, low voltage, proportional to absolute temperature (PTAT) voltage.**

I. Introduction

IT IS well known that the performance of nonlinear analog components depends strongly on the current flowing through them. Therefore, current references are essential blocks for properly biasing analog components of integrated circuits. In the selection of current references, efficient, simple, and easy-to-design structures are highly desirable [4], [6], [8].

Methodologies for CMOS analog design based on the concept of the inversion level [7], [10] have been shown to provide a robust alternative for high performance in very-low-power [5] and low-voltage circuits [4]. In this methodology, the MOSFET is biased at a current that depends on technological parameters. Analog circuits based on such a design technique require a current reference to be generated on-chip or, in other words, the design calls for a self-biased current source (SBCS) operating at the nominal inversion level. An important benefit of the generation of on-chip current references is the avoidance of extra pads to communicate with the external environment [1].

Several SBCS circuits are found in the literature [1]–[7], but none of them has proved to be suitable for extremely low-power applications. Papers [1]–[3] present current references based on the properties of the MOSFET biased in strong inversion, which exhibit relatively high current consumption, on the order of microamperes. The current references of articles [2] and [3] are not appropriate for low supply voltage since they use stacked transistors biased in strong inversion. The SBCS in [6] is dependent on the thermal voltage and on a resistance value that would require a very large silicon area for currents in the picoampere and nanoampere range. The large current gains required for the current mirrors to implement the SBCS presented in [7] degrade its power efficiency. Common to both current references of [8] and [9] are the generation of a proportional to absolute temperature (PTAT) voltage, the use of some current mirrors with gain higher than one, and the operation of some transistors in strong inversion. The use of non unity-gain current mirrors results in power consumption higher than using unity-gain current mirrors. Moreover, operation of transistors in strong inversion requires higher supply voltages to turn on the current source.

The SBCS we propose here shares some similarities with the circuits proposed in [7]–[9], namely: 1) a PTAT voltage derived from MOSFETs biased in weak inversion; 2) an output current proportional to the MOSFET specific current [10]. However, our SBCS circuit uses MOSFETs only, operating in either weak inversion or moderate inversion. As a result, the SBCS in this study is able to operate at lower supply voltages and consumes less power than all the previously reported SBCS since we employ unity-gain current mirrors. Our current reference can operate down to 1.1-V supply voltage in 1.5-μm CMOS technology (or 0.7-V supply in sub-0.18-μm technologies) and exhibits low sensitivity to supply voltage.

The paper is organized as follows. In Section II, the advanced compact MOSFET (ACM) model [10] and the concept of inversion level are summarized. We develop the basic design equations for the SBCS in Section III. Section IV introduces the low-voltage SBCS. The design methodology of the current reference is formulated in Section V. As a design example, a very low power SBCS is implemented in the AMI 1.5-μm CMOS process and the associated simulation and experimental results are presented in Section VI. Finally, concluding comments are presented in Section VII.

II. ACM Model

In the design methodology for the SBCS, we have employed ACM, a current-based MOSFET model that uses the concept of inversion level [10]. According to the ACM model, the drain current can be split into the forward (I_F) and reverse (I_R) currents

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{1}$$

$$I_S = I_{\mathrm{SQ}}\left(\frac{W}{L}\right) = I_{\mathrm{SQ}}\,(S) \tag{2}$$

$$I_{\mathrm{SQ}} = \mu C'_{\mathrm{ox}} n \frac{\phi_t^2}{2}. \tag{3}$$

Manuscript received April 2, 2004; revised July 22, 2004. This work was supported in part by CNPq and CAPES (research agencies of the Brazilian government). This paper was recommended by Associate Editor B. Zhao.

The authors are with the Electrical Engineering Department, Federal University of Santa Catarina, CEP 88040 900 Florianópolis, Brazil (e-mail: maoedgar@eel.ufsc.br; carlos@eel.ufsc.br, marcio@eel.ufsc.br).

Digital Object Identifier 10.1109/TCSII.2004.842059

1057-7130/$20.00 © 2005 IEEE

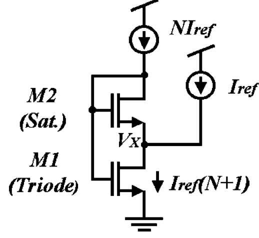

Fig. 1. Schematic of the SCM.

I_F (I_R) depends on the gate and source (drain) voltages. In forward saturation, $I_F \gg I_R$; consequently, $I_D \cong I_F = I_S i_f$. I_S is the normalization (specific) current and I_{SQ} is the sheet specific current (I_S for $W = L$), $i_f(i_r)$ is the forward (reverse) inversion level, and μ, C'_{ox}, n, ϕ_t, and $W/L = S$ are the mobility, gate oxide capacitance/area, slope factor, thermal voltage, and the transistor aspect ratio, respectively. The relationship between current and voltage [10] is given by

$$\frac{V_P - V_{S_{(D)}}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \quad (4)$$

where $V_P \cong (V_G - V_{TO})/n$ is the pinch-off voltage and V_{TO} is the zero bias threshold voltage. More details regarding (1)–(4) can be found in [10]. The sheet specific currents for the AMI 1.5-μm technology are approximately $I_{SQN} = 28$ nA and $I_{SQP} = 10$ nA calculated assuming $n = 1.2$ for n- and p-channel devices, respectively, while $V_{TP} = -0.9$ V and $V_{TN} = 0.6$ V.

The SBCS circuit proposed here is an extractor of the normalization (specific) current I_{SQ} [7] optimized for low-voltage and very low power applications.

III. Design Equations

The core of the SBCS is the self-cascode MOSFET (SCM) shown in Fig. 1. The V–I characteristic of the SCM is very appropriate for building low-voltage analog blocks such as current references and sub-100-mV PTAT voltage [5]–[9].

The design equations (7)–(9) that describe the V-I characteristic of the SCM have been deduced using (1)–(4) and the schematic in Fig. 1. According to (1), the drain currents of M_1 and M_2 can be expressed as functions of the forward and reverse inversion levels. Since M_2 is saturated, then

$$I_{D_2} \cong I_{F2} = I_{S2} i_{f2} \quad (5)$$

and for M_1, in the triode region

$$I_{D1} = I_{F1} - I_{R1} = I_{S1}(i_{f1} - i_{r_1}) = I_{ref}\,(N + 1). \quad (6)$$

Since $V_{P1} = V_{P2} = V_P$ and $V_{D1} = V_{S2}$, then $i_{r1} = i_{f2}$; thus, from (5) and (6), we can find the relationship

$$i_{f1} = i_{f2}\left[1 + \frac{S_2}{S_1}\left(1 + \frac{1}{N}\right)\right]. \quad (7)$$

The application of (4) to node V_X for M_2 results in

$$\frac{V_P - V_X}{\phi_t} + 1 = \left(\sqrt{1 + i_{f2}} - 1\right) + \ln\left(\sqrt{1 + i_{f2}} - 1\right) \quad (8)$$

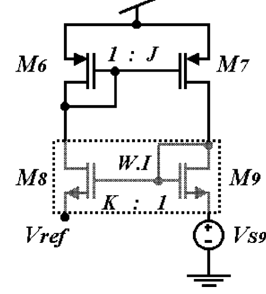

Fig. 2. SBS.

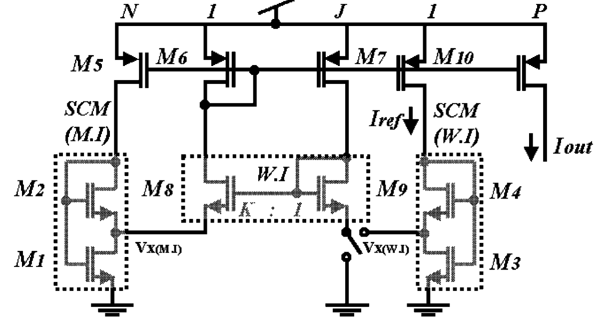

Fig. 3. SBCS circuit.

while, for the source of M_1, expression (4) gives

$$\frac{V_P}{\phi_t} + 1 = \left(\sqrt{1 + i_{f1}} - 1\right) + \ln\left(\sqrt{1 + i_{f1}} - 1\right). \quad (9)$$

Equations (7)–(9) with three unknowns (V_P, i_{f1}, i_{f2}) have been instrumental in the development of the design methodology of the SBCS. If we assume that a voltage generator sets V_X at a given value and a pMOS current mirror defines N, the inversion levels i_{f1} and i_{f2} as well as the current flowing through M_1 and M_2 are readily determined. In the following, we show an implementation of a reference voltage for V_X.

The self-biased structure (SBS) in Fig. 2 can be used to generate V_X at the intermediate node of the SCM [6]. V_{ref} can be calculated using (4) and assuming M_8-M_9 to be operating in weak inversion saturation. Noting that $V_{P8} = V_{P9}$, $I_{D8} = I_{D9}/J$, and $V_{ref} = V_{S8}$, then

$$V_{ref} = V_{S9} + \phi_t \ln(JK) \quad (10)$$

where $J = S_7/S_6$ and $K = S_8/S_9$. In our circuit topology, V_{S9} can be either zero or a PTAT voltage generated by means of a second SCM operating in weak inversion, as shown in Fig. 3. The application of expressions (7)–(9) to the SCM M_3-M_4 operating in weak inversion gives

$$V_{S9} = \phi_t \ln\left[1 + (1 + J)\frac{S_4}{S_3}\right]. \quad (11)$$

Both PTAT voltage references expressed by (10) and (11) are relatively immune to supply voltage as well as to technological parameters provided the transistors operate in weak inversion. In weak inversion, the SCM M_3-M_4 generates a sub-100-mV PTAT reference independent of current level and technology.

IV. Proposed Low-Voltage SBCS

A simple version of our SBCS circuit is shown in Fig. 3, where V_{S9} can be either zero or $V_{X(WI)}$. This power-efficient SBCS replaces the resistor given in [6] with an SCM operating in moderate inversion to achieve the requirements of low voltage operation.

The circuit shown in Fig. 3 operates as follows. When both M_8 and M_9 are biased in weak inversion there is a PTAT voltage shift ($KJ > 1$) between the two MOS devices. If the switch is connected to ground, the PTAT voltage is given by (10), with $V_{S9} = 0$. This simple topology is stable for $KJ > 1$ and is very accurate for $KJ > 10$ [9].

If the switch is connected to M_3-M_4, then V_{S9} is given by (11). This second implementation results in improved symmetry (for $K = J = 1$) and matching of the structure.

V. Design Methodology

The design specifications of the current reference are usually the minimum supply voltage ($V_{DD\,\min}$), power dissipation, silicon area, and sensitivities, in addition to I_{ref}, the value of the current itself. The design methodology can be applied to either the simple topology (switch connected to ground) or the symmetric topology (switch connected to node $V_{X(WI)}$) in Fig. 3. The only difference between these two topologies as regards design methodology is the way how the voltage $V_{X(MI)}$ is generated.

The minimum supply voltage, which is determined by the constraints imposed by the two leftmost branches in Fig. 3, can be written as

$$V_{DD} \geq \max\{|V_{\text{DSsat},P}|+V_{\text{GS},M1}, |V_{\text{GS},P}|+V_{\text{DSsat},M8}+V_X\} \tag{12.a}$$

where $V_{\text{DSsat},M8} \cong 100$ mV since M_8 operates in weak inversion. The p-channel transistors are sized to operate in weak inversion, with an inversion level close to 1 or smaller; therefore, $|V_{\text{DSsat},P}| \cong 100$ mV and $V_{\text{GS},P} \cong V_{\text{TP}}$ or less. V_X is chosen to be less than 100 mV while M_2 is sized so as to operate in moderate inversion, with i_{f2} within the range 3 to 8. This choice of i_{f2} has two purposes: 1) M_2 should not be operating in weak inversion in order to reduce the sensitivity of the reference current to both mismatch and supply voltage; 2) the selected inversion level of M_2 should have a relatively small value in moderate inversion so that its gate-to-source voltage is only slightly higher than the threshold voltage. Since, in this case, $V_X < 100$ mV and i_{f2} is within the range 3 to 8, then $V_{\text{GS},M1} = V_{\text{GS},M2} \cong V_{\text{TN}} + 100$ mV. Hence, we can use the first-order approximation for (12.a)

$$V_{DD} \geq \max\{|V_{\text{TP}}|, V_{\text{TN}}\} + 200\text{ mV} \tag{12.b}$$

to calculate the minimum supply voltage. Although expression (12.b) is a rough approximation, it is very useful for predicting the minimum supply voltage required to turn on the current reference circuit.

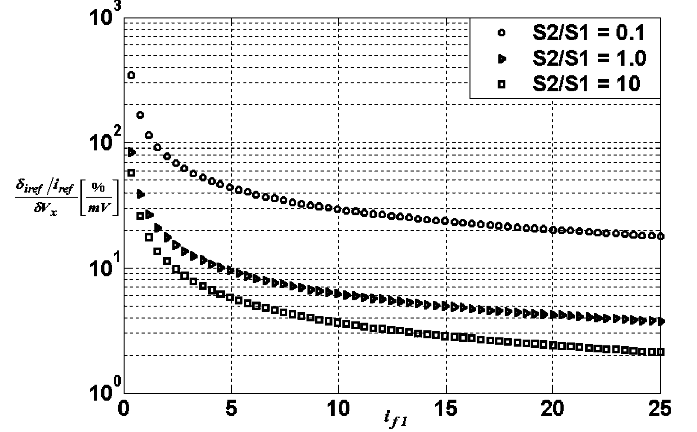

Fig. 4. Relative sensitivity of the reference current versus i_{f1}.

Expressions (7)–(9), together with

$$\frac{\delta i_{\text{ref}}}{i_{\text{ref}}} = 2\frac{\delta V_X}{\phi_t}\left[\sqrt{1+i_{f1}} - \sqrt{1+\frac{i_{f1}}{\left(1+\frac{2S_2}{S_1}\right)}}\right]^{-1} \tag{13}$$

which gives the sensitivity of the reference current to V_X, form the basis of our design methodology. To derive (13), we have assumed a deviation in $V_{X(\text{M.I.})}$ equal to δV_X and that equal currents flow through M_5 and M_6 ($N = 1$).

The graphical representation of (13) is shown in Fig. 4 for three different S_2/S_1 ratios.

One can readily notice that the sensitivity of the reference current to V_X is extremely high for low inversion levels ($i_{f1} \to 0$). If $i_{f1} < 3$, for instance, the reference current changes by more than 10%/mV variation in V_X. The regulation of the current with respect to supply voltage can be demonstrated to be inversely proportional to the factor in square brackets given in expression (13). Therefore, in order to minimize the dependence of I_{ref} on both mismatch and V_{DD} one should avoid operation of M_2 at low inversion levels. The sensitivity of the current to the power supply is mostly associated with the Early effect of M_7 and M_8. The Early effect can be reduced using long channel transistors. However, this demands a large silicon area. One approach to obtaining long channel lengths with moderate area is the trapezoidal transistor proposed in [12]. We have employed trapezoidal transistors for implementing M_8 and M_9 as well as the pMOS transistors.

In our design methodology, we have designed M_2 to operate in moderate inversion with $i_{f2} = 3$ or, equivalently, $V_P = V_{x(M.I)}$ [see (8)], and $J = 1$. Using the simple topology ($V_{S9} = 0$) for a given K factor, we can readily calculate i_{f1} from (8) and (9) by solving

$$1 + \ln(K) = \sqrt{1+i_{f1}} - 1 + \ln\left(\sqrt{1+i_{f1}} - 1\right) \tag{14.a}$$

for i_{f1}. Once i_{f1} has been calculated for a given K, one can calculate S_2/S_1 from (7), which, for $i_{f2} = 3$, yields

$$\frac{S_2}{S_1} = \frac{i_{f1} - 3}{3\left(1+\frac{1}{N}\right)}. \tag{14.b}$$

TABLE I
SUMMARY OF SIMULATIONS AND EXPERIMENTS

Parameter	Simple topology, K=9		Symmetric topology, K=1		Unit
	Simulation	Experiment	Simulation	Experiment	
V_{DDmin}	1.1	1.1	1.1	1.1	V
Power (at 1.1V)	1.5	1.5	2.0	2.0	nW
V_{ref} sensitivity to V_{DD}	0.9	1.6	0.7	1.3	%/V
V_{ref} sensitivity to T	+0.32	X	+0.32	X	%/°C
I_{ref} sensitivity to V_{DD}	4.7	6.2	3.5	6.0	%/V
I_{ref} sensitivity to T	+0.047	0.3	+0.047	0.25	%/°C

X – not measured

TABLE II
TRANSISTOR SIZES FOR THE SYMMETRIC TOPOLOGY

Transistor	W [μm]	L [μm]	i_f
M_1	4	18x60*	10.2
M_2	4	15x60	3
M_3	10	10	0.032
M_4	4x10	10	0.004
$M_{5\text{-}7,\,10}$ &	4	16	0.16
$M_{8\text{-}9}$ &	10	10	0.016

& Trapezoidal transistors were implemented. The dimensions of the transistor connected to the source are W and L as given in Table II while the one connected to the drain is sized 5W and L.
* Series association of 18 transistors having W=4μm and L=60μm.

From

$$i_{f2} = \frac{I_{D2}}{(I_{SQ}S_2)} = \frac{NI_{\rm ref}}{(I_{SQ}S_2)} \tag{14.c}$$

we find $S_2 = NI_{\rm ref}/3I_{\rm SQ}$.

For $JI_{\rm ref} \ll I_{\rm SQ}$, $S_9 = J$ keeps M_9 in weak inversion and the factor N defines a tradeoff between power consumption and area. The aspect ratio (S_P) of the pMOS transistors M_5-M_7 and M_{10} is calculated using (2) and the appropriate inversion level, which is usually less than 1 for low-voltage applications.

For the design of the symmetric topology, we have used the same methodology but with $K = 1$, and S_3, S_4 calculated from (11) for a given V_{S9}.

VI. RESULTS

The circuit topologies with the switch connected either to ground or to the $V_{X(W.I.)}$ node in Fig. 3 have been designed for the AMI 1.5-μm CMOS technology. A comparison of post layout simulation using the BSIM 3v3 model and experimental results is given in Table I for $I_{\rm ref} = 400$ pA, $N = J = 1$, $S_9 = 1$, and $S_2/S_1 = 1.2$. The transistor dimensions for the symmetric topology are presented in Table II.

The experimental results show that the sensitivity of the reference current to the supply is relatively low and quite acceptable for most applications. Two major factors are primarily responsible for the discrepancies between the simulated and experimental results for both the current and voltage regulation namely, poor modeling of the MOSFET output conductance in the BSIM 3v3 model and leakage through the protection diodes of the I/O pads.

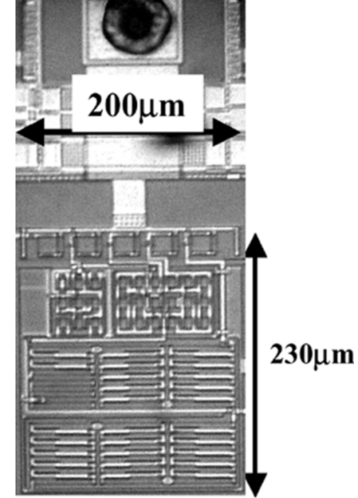

Fig. 5. Micrograph of the symmetric topology of the current reference.

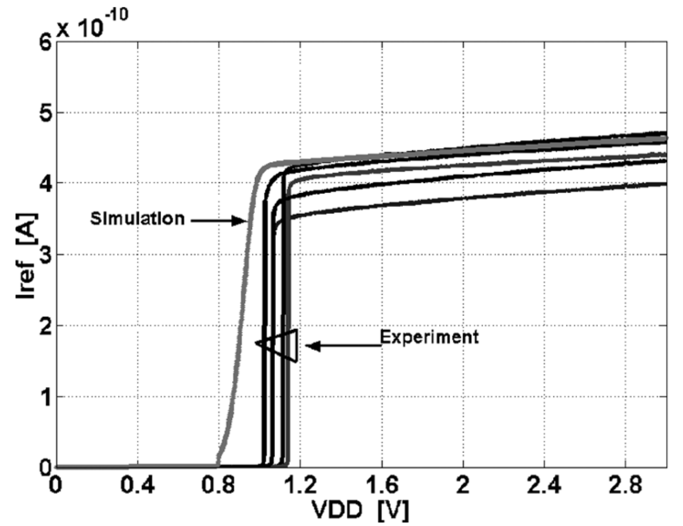

Fig. 6. Current reference against supply voltage for the symmetric topology ($K = 1$).

The area of the core cell of the symmetric SBCS shown in Fig. 5 is around 230×200 μm^2.

Simulation and experimental results for the reference current are compared in Fig. 6 for five samples of the circuit. These results validate the design and show that the current source can operate at voltages down to the value resulting from (12.b) (in the technology used for the current reference, $V_{\rm TP} = -0.9$ V and $V_{\rm TN} = 0.6$ V). As can be observed in Fig. 6, the variation of the reference current around the nominal value is relatively low. The average current reference obtained from two sets of five samples with two different layouts is 410 pA with a maximum deviation of $\pm 10\%$ at 1.2 V supply.

Fig. 7 shows the approximate PTAT dependence of the current reference, which can be explained using (3). For the temperature range of the measurements, the mobility is inversely proportional to the absolute temperature. For temperatures close to 60° or higher, the leakage current through the protection diode of the current pad becomes on the order of the reference current and, thus, the current measured is much higher than expected.

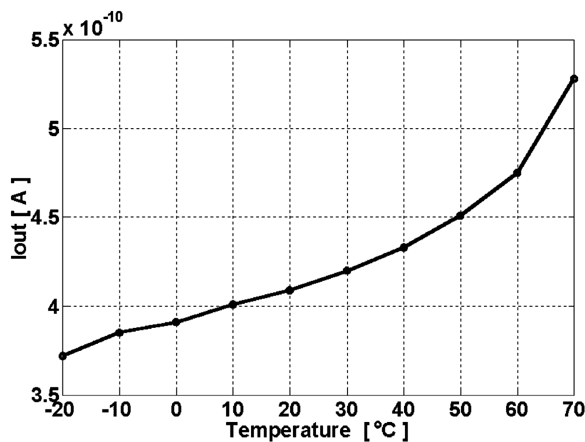

Fig. 7. Dependence of current reference on temperature.

VII. Summary and Conclusion

A low-voltage low-power self-biased current-source has been proposed. Design equations based on the ACM model have been provided. The proposed circuits are process-independent and reproducible in any standard CMOS technology. Simulation and experimental results have shown that the SBCS provides ultra-low-power operation, low sensitivity to changes in the supply voltage, small silicon area and can operate at power-supply voltages down to 1.1 V in a 1.5-μm technology. The SBCS and design methodology proposed here were demonstrated to be particularly suited to very-low-power low-voltage applications, offering the potential to operate at supply voltages down to 0.7 V in a 0.18-μm CMOS technology due to operation of all transistors in either moderate or weak inversion.

Acknowledgment

MOSIS is gratefully acknowledged for providing access to integration. The authors also thank Prof. C. Reis, UNICAMP, and his team for the thermal characterization of the current source.

References

[1] S. Tang, S. Narendra, and V. De, "Temperature and process invariant MOS-based reference current generation circuits for sub-1 V operation," in *Proc. ISLPED'03*, pp. 199–204.

[2] W. M. Sansen, F. O. Eynde, and M. Steyaert, "A CMOS temperature-compensated current reference," *IEEE J. Solid-State Circuits*, vol. 23, pp. 821–824, Jun. 1988.

[3] C.-H. Lee and H.-J. Park, "All-CMOS temperature independent current reference," *Electron. Lett.*, vol. 32, no. 14, pp. 1280–1281, 1996.

[4] S. Yan and E. Sánchez-Sinencio, "Low voltage analog circuit design techniques: A tutorial," *IEICE Trans. Fund.*, vol. E83-A, no. 2, pp. 1–17, Feb. 2000.

[5] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.

[6] E. Vittoz and J. Fellrath, "CMOS analog circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. SC-12, no. 6, pp. 224–231, Jun. 1977.

[7] E. A. Vittoz and C. C. Enz, "CMOS low-power analog circuit design," in *Proc. Int. Symp. Circuits Syst. (ISCAS'96)*, 1996, pp. 79–133.

[8] H. J. Oguey and D. Aebischer, "CMOS current reference without resistance," *IEEE J. Solid-State Circuits*, vol. SC-32, no. 7, pp. 1132–1135, Jul. 1997.

[9] F. Serra-Graells and J. L. Huertas, "Sub-1-V CMOS proportional-to-absolute temperature references," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 84–88, Jan. 2003.

[10] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[11] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 10, pp. 1433–1440, Oct. 1989.

[12] C. Galup-Montoro, M. C. Schneider, and I. J. B. Loss, "Series-parallel association of FETs for high gain and high frequency applications," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1094–1101, Sep. 1994.