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CMOS Amplifiers and Schmitt Triggers for Ultra-Low-Voltage Applications

Dissertação submetida ao Programa de Pós-Graduação em Engenharia Elétrica da Universidade Federal de Santa Catarina para a obtenção do título de Mestre em Engenharia Elétrica.
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Florianópolis

2019

Ficha de identificação da obra elaborada pelo autor,
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Fernandes, Thiago Darós
CMOS amplifiers and Schmitt triggers for ultra low-voltage applications / Thiago Darós Fernandes ; orientador, Marcio Cherem Schneider, coorientador, Djones Vinicius Lettnin, 2019.
76 p.

Dissertação (mestrado) - Universidade Federal de Santa Catarina, Centro Tecnológico, Programa de Pós Graduação em Engenharia Elétrica, Florianópolis, 2019.

Inclui referências.

1. Engenharia Elétrica. 2. CMOS. 3. ultra low voltage. 4. Schmitt trigger. 5. hysteresis. I. Cherem Schneider, Marcio. II. Lettnin, Djones Vinicius. III. Universidade Federal de Santa Catarina. Programa de Pós-Graduação em Engenharia Elétrica. IV. Título.

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Esta Dissertação foi julgada adequada para obtenção do título de Mestre em Engenharia Elétrica e aprovada em sua forma final pelo Programa de Pós-Graduação em Engenharia Elétrica.

Florianópolis, 11 de junho de 2019.

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RESUMO

A colheita de energia do ambiente é uma escolha comum para se operar dispositivos situados em locais inacessíveis, mas esta alternativa exige que estes equipamentos arranquem com fontes de tensão e potências muito baixas. Com a redução de tensão, os transistores CMOS são sujeitos a operar no modo *subthreshold* e na região linear, o que reduz ganho e degrada os níveis lógicos de circuitos digitais. Para mitigar esses efeitos, quatro alternativas ao inversor CMOS são revisadas e comparadas através de soluções numéricas e simulação: o *classical Schmitt trigger*, o *three-inverter Schmitt trigger* (TI-ST), o *dynamic leakage-suppresion logic* (DLS) e o *stacked-inverter gate* (SIG). Demonstrou-se numericamente que o SIG possui uma tensão de alimentação para ganho unitário menor que o inversor tradicional, diminuindo o valor para $V_{DD} \approx 30$ mV a 300 K. Também foi demonstrado, pela primeira vez, que o TI-ST apresenta histerese a partir de uma tensão de alimentação de $V_{DD} = 36$ mV a temperatura ambiente. As células *classical Schmitt Trigger* e TI-ST foram fabricadas e medidas. A tensão mínima mensurada para o aparecimento da histerese no TI-ST foi de $V_{DD} = 48.5$ mV para um dado projeto.

Palavras-chave: CMOS, ultra baixa tensão, Schmitt Trigger, histerese.

RESUMO EXPANDIDO

Introdução

A colheita de energia do ambiente é uma escolha comum para se operar dispositivos situados em locais inacessíveis, mas esta alternativa exige que estes equipamentos arranquem com fontes de tensão e potências muito baixas. Com a redução de tensão, os transistores CMOS são sujeitos a operar no modo *subthreshold* e na região linear, o que reduz ganho e degrada os níveis lógicos de circuitos digitais. Uma desvantagem de operar em tensões baixas é a redução do ganho de tensão que, conjuntamente com níveis lógicos mais deteriorados, reduz drasticamente a margem de ruído estática (SNM).

Objetivos

O circuito *Schmitt trigger* (ST) foi utilizado em circuitos de ultra baixa tensão como um elemento que provém histerese, um amplificador ou como um bloco básico de lógica e memória. Os circuitos Schmitt trigger usam realimentação positiva para aumentar o ganho de tensão e melhorar a regeneração de sinal de circuitos lógicos. Este trabalho tem como objetivo procurar por arquiteturas simples de circuitos CMOS que operem a partir de fontes de tensão ultra-baixas, da ordem de 60 mV, para tanto operarem em aplicações de lógica, amplificadores ou Schmitt triggers. Durante a revisão bibliográfica, quatro arquiteturas de células inversoras foram apresentadas com seus resultados, o *classical Schmitt trigger*, o *three-inverter Schmitt trigger* (TI-ST), o *dynamic leakage-suppresion logic* (DLS) e o *stacked-inverter gate*

(SIG). Esses resultados apresentados sobre lógica de baixa tensão demonstram a falta de elementos consistentes de comparação. Por esse motivo, esse trabalho procura se colocar como uma análise comparativa, para ajudar os projetistas a escolherem a célula lógica padrão mais adequada. Não menos importante, é a análise de circuitos de ultra baixa tensão para a geração de laços de histerese.

Metodologia

A propriedade regenerativa de uma porta lógica é importante para garantir níveis lógicos bem definidos de acordo com a métrica de margem de ruído estático. Através da conexão de duas células idênticas em paralelo, tal como num *latch*, é possível medir a SNM através da figura borboleta, bem como o quão próximo aos limites da fonte de tensão os níveis lógicos se encontram. As células propostas foram analisadas através do uso do modelo UICM considerando condições ideias de funcionamento e modelos simplificados de inversão fraca. O *classical inverter* é uma célula básica tradicional para testes e comparação de performance. O TI-ST, o qual é baseado no inversor básico, é capaz de prover histerese de uma tensão de alimentação coincidente com a tensão de alimentação do inversor necessária para ganho unitário. Contudo, para tensões maiores, a histerese cresce excessivamente até um ponto no qual a célula trava em um nível lógico arbitrário, que nenhuma entrada de tensão nos limites da fonte de alimentação pode alterar. O DLS é construído utilizando menos transistores e, de acordo dom a referência, apresenta uma fuga de corrente menor que o inversor clássico, porém tem ganho inferior e níveis lógicos mais deteriorados. O SIG apresenta a menor tensão de

alimentação para ganho unitário de todas as células analisadas neste trabalho. Ele não apresenta histerese, mesmo para tensões mais altas, por não possuir laço de realimentação positiva. Apesar de todos as vantagens apresentadas pelas topologias alternativas, o inversor básico ainda utiliza menos silício em sua fabricação e, por essa razão, possui capacitância de entrada inferior.

Resultados e Discussão

Três circuitos foram descritos analiticamente. O SIG demonstrou numericamente quebrar novamente a barreira do ganho unitário, baixando o valor para $V_{DD} \approx 30$ mV. Também apresentou níveis lógicos mais próximos as fontes de alimentação que o *classical Schmitt trigger*. Finalmente, nós demonstramos pela primeira vez que o TI-ST provém histerese a partir de tensões de alimentação muito baixas, quando comparado a outras topologias de ST. Teoricamente, o TI-ST pode apresentar histerese a partir de tensões de alimentação iguais ao limite de Meindl de $2\phi_t \ln 2$. O circuito TI-ST pode ser melhor empregado quando há a necessidade de projeto de se obter uma quantidade considerável de histerese, enquanto o SIG tem vantagens em termos de ganho e regeneração de níveis lógicos. O *classical Schmitt trigger* fica em uma classe intermediária. O DLS não demonstrou superioridade em termos de ganho e regeneração lógica, por este motivo, seus resultados foram omitidos. Uma análise aprofundada em consumo de potência pode revelar vantagens no seu uso para evitar o consumo estático de potência, como citado pelos autores.

Considerações Finais

Apesar da redução na performance de velocidade quando comparadas ao inversor, as células analisadas neste trabalho podem ser vantajosamente empregadas em circuitos de ultra baixa tensão para melhorar as margens de ruído estática. Com o aumento na demanda para circuitos altamente eficientes operando a partir de fontes de alimentação muito baixas, eles podem representar uma escolha interessante para viabilizar circuitos de lógica e memória, e elementos úteis para gerar histerese com tensões muito baixas.

Palavras-chave: CMOS, ultra baixa tensão, Schmitt Trigger, histerese.

ABSTRACT

Harvesting energy from the surroundings is a common choice to operate devices that are in inaccessible environments, but this alternative requires the electronics to start up from very low supply voltages and very low power. As voltage decreases, CMOS transistors are subjected to operate in the subthreshold mode and in the linear region, which reduces gain and degrades the logic levels. In order to mitigate these effects, four alternatives to the CMOS inverter are revised and compared through numerical solutions and simulation: the classic Schmitt trigger, the three-inverter Schmitt trigger (TI-ST), the dynamic leakage-suppression inverter and the stacked. We demonstrate numerically that the stacked inverters have a lower power supply voltage for unity gain than that of the standard inverter, lowering the value to $V_{DD} \approx 30$ mV at 300 K. We also demonstrate, for the first time, that the TI-ST provides hysteresis from a supply voltage of $V_{DD} = 36$ mV at room temperature. Cells classical Schmitt trigger and TI-ST were fabricated and measured. The measured minimum supply voltage for the appearance of hysteresis in the TI-ST was $V_{DD} = 48.5$ mV for a given design.

Key-words: CMOS, ultra low voltage, Schmitt trigger, hysteresis.

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND ACRONYMS

AC	Alternating Current
BJT	Bipolar-Junction Transistor
CMOS	Complementary MOS
DC	Direct Current
DLS	Dynamic Leakage-Suppression
IoT	Internet of Things
MOS	Metal-Oxide-Semiconductor
MOSFET	MOS Field Effect Transistor
MPW	Multi-Project Wafer
NMOS	N-Channel MOS
PDP	Power-Delay-Product
PMOS	P-Channel MOS
RO	Ring Oscillator
SIG	Stacked-Inverter Gate
SNM	Static Noise Margin
SRAM	Static Random Access Memory

ST	Schmitt Trigger
TI-ST	Three-Inverter Schmitt Trigger
UICM	Unified Current-Control Model
VTC	Voltage Transfer Characteristic

LIST OF SYMBOLS

μ	Mean
μ_n	Electron mobility
ϕ_t	Thermal voltage
σ	Standard deviation
A_V	Voltage gain
C'_{ox}	Oxide capacitance per unit area
g_{mb}	Bulk transconductance
g_{md}	Drain transconductance
g_{ms}	Source transconductance
g_m	Gate transconductance
I	Transistor strength
I_{SH}	Sheet normaliztion current
I_D	Drain current
I_F	Forward current
i_f	Normalized forward current
I_N	Transistor scale factor
I_R	Reverse current

i_r	Normalized reverse current
I_S	Normalization current
J	Design factor (I_2/I_1)
K	Design factor (I_0/I_1)
L	Transistor channel length
n	Slope factor
$V_{DD_{min}}$	Minimum voltage supply for unity gain
V_{DD}	Power supply voltage
V_{DDH}	Minimum voltage supply for hysteresis
V_H	High latch stable point
V_L	Low latch stable point
V_{T0}	Threshold voltage
V_W	Hysteresis loop width
V_D	Drain voltage
V_G	Gate voltage
V_I	Input voltage
V_O	Output voltage
V_P	Pinch-off voltage
V_S	Source voltage
W	Transistor channel width

CONTENTS

1 INTRODUCTION

In 2017, Brazil's economical year finished with a U$29.7 billion net export deficit on electrical materials, components and goods, which where responsible for 19.7% of the total imports [1]. The semiconductor area alone has imported U$4.7 billion and was the most imported product in the electrical industry in 2018, with a 8% growth. It is expected that this demand keeps on rising due to the IoT (Internet of Things) trend and its by-products.

The last two decades brought a huge rise in low voltage research. This is presented in Bell's Law, which states that every ten years a new computer class arises [2]. The device segment of low voltage was formerly composed of portable computers and it is currently represented by wireless sensor networks and energy harvesting devices, that will be innovations of the current and next decades. Some examples of applications that are seldom provided with high power supply voltages are biomedical sensors, environmental monitors and wearables. Moreover, running in low voltage forces the MOS devices to operate in subthreshold domain, providing a boost in energy efficiency that may make feasible these power scarce devices.

1.1 Motivation

The early digital integrated circuits were made of bipolar-junction transistors (BJT), and due to its intrinsic behavior, a logic gate required a static current to maintain a certain logic level. Likewise, the first MOSFET circuits employed depletion

mode NMOS as pull-up devices, which have a threshold voltage lower than zero. The static current is also high, leading to a logic with a high static current consumption. CMOS circuits were revolutionary as they did not have virtually any static current consumption to preserve logic levels.

In the hunt for more efficient circuits, the usual idea is to think of reducing the dynamic power right away, and that was true for many years. To keep the frequencies in the Gigahertz domain and, at the same time, decrease the power consumption, the technology has scaled down many orders of magnitude through miniaturization, lowering the logic gates input capacitance. The faster devices made feasible high frequency processors, but they brought a heat density problem, as power dissipation is limited. This issue could be solved by a voltage supply reduction while keeping speed performance, since a reduction in power supply results in a quadratic improvement in power savings [3].

As voltages decreases, CMOS transistors are subjected to operate in the subthreshold mode, which brings a new perspective for power consumption. Secondary effects once ignored become more relevant, henceforth putting the static current dissipation in the spotlight. Logic levels are not well regenerated by gates when working in subthreshold, because transistors do not operate so close to ideal switches, thus holding off the logic state from supply voltage rails level and conducting current even in the OFF state.

A disadvantage of low voltage logic is the intrinsic voltage gain reduction that, along with poorer logic levels, dramatically reduces the static noise margin (SNM) of a logic gate. Figure 1 shows the measured behavior of a classic CMOS inverter with

the gain and logic levels degradation.

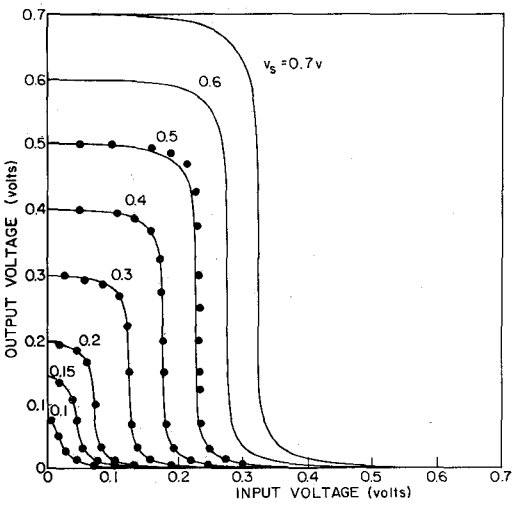

Figure 1 – Voltage transfer characteristics for a CMOS inverter for several supply voltages. Source: Swanson e Meindl[4], 1972.

The Schmitt trigger (ST) circuit has been used in ultra-low-voltage circuits as an element to provide hysteresis, as an amplifier, or as a block for logic and memory [5, 6, 7]. Schmitt trigger circuits use positive feedback to increase voltage gain and improve signal regeneration.

This work has as objective to search for simple architectures of CMOS circuits that operate from ultra low supply voltages of the order of 60 mV, for either serve as logic, amplifier, or Schmitt trigger applications.

1.2 Chapter Organization

In Chapter 2, we review the basic CMOS inverter characteristics for ultra low supply voltages and present recent research that shows improvements regarding gain and voltage regeneration over the traditional CMOS logic inverter. Four circuits that recently showed interesting results are going to be presented.

Chapter 3 presents an analytic study about the four cells, to establish a theoretical basis for this as well as future works.

In Chapter 4, the previous analytic results are compared to simulations and some measurements are presented.

Chapter 5 discusses the previous results and summarizes the outcomes of this research.

2 REVIEW OF TECHNICAL LITERATURE

Several works have presented solutions on how to deal with low voltage design challenges. Some of them will be reviewed here, not necessarily in chronological order, but rather first the theoretical evidence followed by applications that reach new limits.

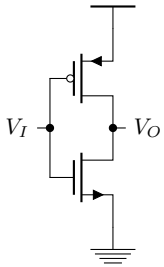

Figure 2 – Classical CMOS inverter.

In [8] the authors derived an important result, shown in Figure 1, for low voltage CMOS logic. By analyzing the classical CMOS inverter, as in Figure 2, operating in weak inversion, the minimum supply voltage required for unity gain, for balanced NMOS and PMOS transistors having slope factors equal to unity, is given by (2.1), where ϕ_t is the thermal voltage (25.9 mV at

27°C), resulting in a minimum supply voltage of around 36 mV.

$$V_{DD_{min}} = 2\phi_t \ln 2 \tag{2.1}$$

The unity gain is an important metric for logic gates because it defines a threshold for regenerative logic, and also, can be used to benchmark and compare different logic inverter cells. But a gain slightly higher than unity is not necessarily enough, since noise is inherent to the nature of electronics devices. For this reason, Static Noise Magin (SNM) is preferred for performing design comparisons. A practical way to measure a gate performance is to connect itself as a latch [9], as it is equivalent to an infinitely long chain of gates, to estimate the worst-case static noise margin.

A paper by Melek et al.[10] brought the minimum supply voltage limit down, as compared to the CMOS inverter, through the use of positive feedback. The circuit employed by the team is referred to as the classical Schmitt trigger, which is shown in Figure 3. By analyzing the small-signal gain of a classical Schmitt trigger, optimized for maximum voltage gain, the authors presented relation (2.2), which gives a supply voltage of 31.5 mV for unity gain at ambient temperature.

$$V_{DD_{min}} = 2\phi_t \ln\left(\frac{8+\sqrt{73}}{9}\right) \tag{2.2}$$

In [5] the authors show expressions that describe the DC transfer function of the classical ST. One of the results is related to the supply voltage at which the ST switches from the amplifier mode to the hysteretic mode. The theoretical minimum supply voltage, given by (2.3), gives the transition between these two

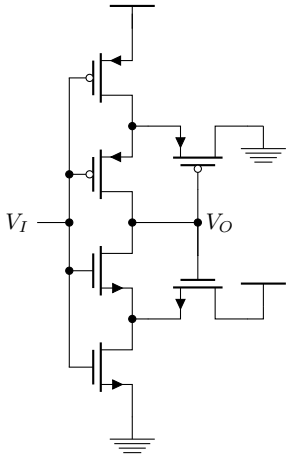

Figure 3 – Classical Schmitt trigger.

operating modes. In practical structures, the measured values are usually higher than 100 mV.

$$V_{DDH} = 2\phi_t \ln\left(2+\sqrt{5}\right) = 75\text{mV at } 300\text{K} \qquad (2.3)$$

A standard cell library based on the classical Schmitt trigger operating at 62 mV was presented in [7]. In this work, the authors emphasize the improvements on the on-to-off current ratio by running an ST-based 8×8 bit multiplier. Kulkarni et al.[6] presented in 2007 a fully functional ST-based static random access memory (SRAM), which offers improvements, in terms of both robustness and static noise margin, over those based on standard CMOS inverters.

Due to higher gain and better signal regeneration, the classical Schmitt trigger can also be used to achieve the Barkhausen

criterion at lower voltages in ring oscillators and simultaneously be combined with other low voltage techniques, like body biasing [11].

The dynamic leakage-suppression (DLS) logic is an alternative implementation of positive feedback, presented in Figure 4. It presents a low leakage performance and has been used to build a picowatt ARM core with a minimum supply voltage of 160 mV [12].

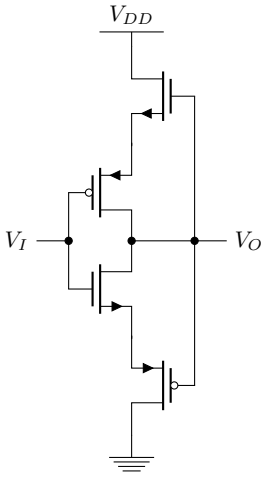

Figure 4 – Dynamic leakage-suppression logic inverter.

Figure 5 shows an ST implementation first presented by Dokic [13], more commonly seen as a non-inverter ST [14, 15, 16, 17] and also common in textbooks [18], but unexplored in the low voltage context. It consists of a CMOS inverter followed by a latch that will further be referred to as a three-inverter ST (TI-ST).

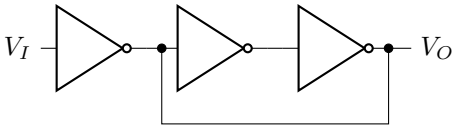

Figure 5 – Three-inverter Schmitt trigger block diagram.

In 2018, a circuit composed of unbalanced inverters without positive feedback, referred to as stacked inverters or redundant inverters, showed advantage over the CMOS inverter as regards voltage gain [19, 20]. It consists of an inverter with rails supplied by other unbalanced inverters, as shown in Figure 6. By applying this technique to build ring oscillators, the authors could measure a oscillation in stacked inverters running from a 45 mV supply. It will be herein referred to as stacked-inverter gate (SIG).

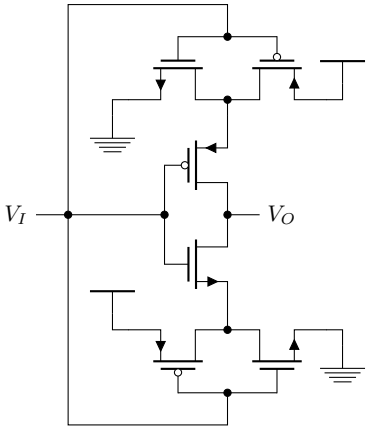

Figure 6 – Stacked inverters schematic.

The recent research results on low-voltage logic present

lack of consistent comparison elements. For this reason, this work seeks to pose itself as a comparative analysis, in order to help designers to choose the most suitable standard logic cell. Not less important is the analysis of ultra-low-voltage circuits for the generation of hysteresis loops.

3 A BRIEF ANALYSIS OF BASIC BUILDING BLOCKS

This chapter presents the analyses of the cells presented in Chapter 2 using both the UICM model and numerical simulation.

3.1 Voltage Transfer Characteristic and Output Voltage Swing

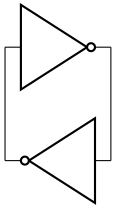

Figure 7 – Basic Latch.

The regenerative property of a gate is important to guarantee well defined logic levels according to the static noise margin metric. By connecting two identical cells as a latch, as depicted in Figure 7, it is possible to measure the SNM through the Butterfly plot, which is shown in Figure 8.

The two stable points, V_H and V_L, are indicated in Figure 8 as black dots. The solution to analytically identify them can be obtained by finding the crossing points of its inverse function, but this leads to a more complex result. Another approach to

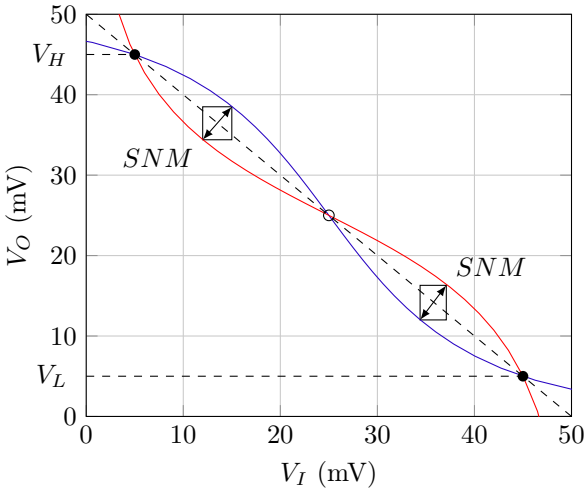

Figure 8 – Butterfly plot for demonstrating the latch stable points.

find V_H and V_L is to use the fact that the function is odd around $V_{DD}/2$ and draw the dashed line $V_O = V_{DD} - V_I$ to input in the VTC equations of each cell.

In an inverter operating at high supply voltages, the latch stable points, V_H and V_L, are equal to the rail voltages. In the same way as the gain, the latch stable points affect the SNM and are going to be used as a performance metric.

3.2 CMOS Inverter

Despite being well-known, the CMOS inverter analysis will be presented here to expose the use of the UICM model as a straightforward method to describe the circuit's behavior.

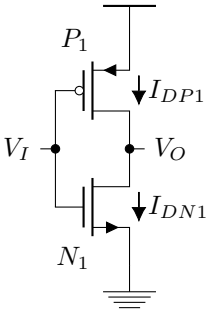

Figure 9 – Classical CMOS inverter.

The nodal current equation for V_O is:

$$I_{DP_1} = I_{DN_1} \tag{3.1}$$

Applying (A.6), the currents of each transistor can be written as

$$I_{DN_1} = I_{N1} \mathrm{e}^{\frac{V_I}{n\phi_t}} \left(1 - \mathrm{e}^{\frac{-V_O}{\phi_t}}\right) \tag{3.2}$$

$$I_{DP_1} = I_{P1} \mathrm{e}^{\frac{V_{DD}-V_I}{n\phi_t}} \left(1 - \mathrm{e}^{-\frac{V_{DD}-V_O}{\phi_t}}\right) \tag{3.3}$$

Combining equations (3.2) and (3.3) with (3.1) results in an equation that describes the transfer function of the circuit in weak inversion mode (3.4).

$$I_{N1} \mathrm{e}^{\frac{V_I}{n\phi_t}} \left(1 - \mathrm{e}^{\frac{-V_O}{\phi_t}}\right) = I_{P1} \mathrm{e}^{\frac{V_{DD}-V_I}{n\phi_t}} \left(1 - \mathrm{e}^{-\frac{V_{DD}-V_O}{\phi_t}}\right) \tag{3.4}$$

Figure 10 shows the voltage transfer characteristic of the inverter. For reference, a dashed line of unity gain is also plotted. Note that, in this case, the latch stable points deviate from the rails 10% of V_{DD}.

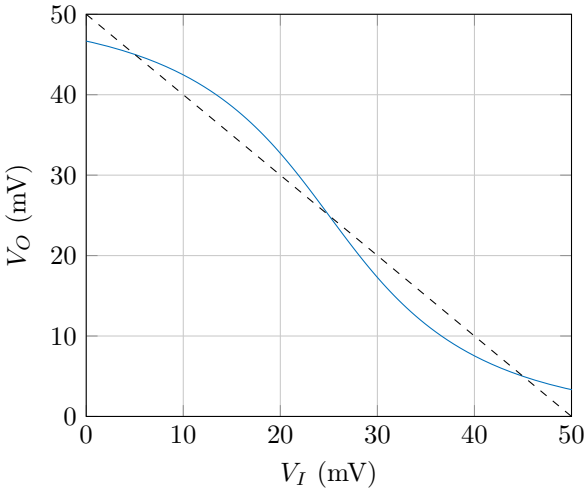

Figure 10 – Inverter VTC curve ($V_{DD} = 50$ mV, $I_{N1} = I_{P1} = 1$ nA, $n = 1$).

3.2.1 Small-signal Analysis

Using the MOSFET small-signal model, the voltage gain is

$$\frac{v_O}{v_I} = -\frac{g_{m_{N1}} + g_{m_{P1}}}{g_{md_{N1}} + g_{md_{P1}}} = -\frac{g_m}{g_{md}} \tag{3.5}$$

for balanced P and N transistors.

The gain is then estimated by calculating the transconductances for a DC operating point $V_I = V_O = V_{DD}/2$

$$A_V = \left.\frac{v_O}{v_I}\right|_{V_I = V_O = \frac{V_{DD}}{2}} = -\frac{\mathrm{e}^{\frac{V_{DD}}{2\phi_t}} - 1}{n} \tag{3.6}$$

For $n = 1$, the supply voltage required for having $A_V =$

-1 is

$$e^{\frac{V_{DD}}{2\phi_t}} = 2 \tag{3.7}$$

which gives the value of (2.1) for the minimum supply voltage for unity gain.

3.3 Classical CMOS Schmitt Trigger

The classical CMOS Schmitt trigger is depicted in Figure 11. Its operation in weak inversion is studied in Melek et al. [21] and demands an extensive algebra that will be omitted here. The positive feedback loop is established by N_2 and P_2 in a common drain amplifier configuration from V_O to V_X and V_Y together with N_1 and P_1 in a common gate amplifier configuration from V_X and V_Y to V_O.

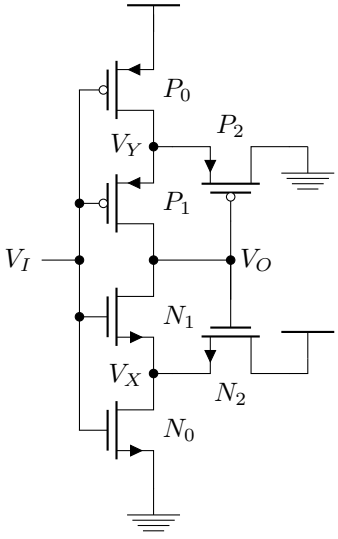

Figure 11 – Classical Schmitt trigger.

For simplifying reasons, the authors of [5] assume that the P- and N- networks are balanced, i. e.

$$I_{N0} = I_{P0} = I_0 \qquad I_{N1} = I_{P1} = I_1 \qquad I_{N2} = I_{P2} = I_2 \tag{3.8}$$

Balanced P- and N- networks will be assumed from now on, except where otherwise noted.

Reference [21] demonstrates that the best design to achieve maximum gain is to make $I_1/I_0 \to 0$ and $I_2/I_0 \to 1/3$ at minimum unity gain voltage of 31.5 mV. Since these values are not feasible, an arbitrary reasonable ratio of $I_2/I_0 = 1/2$ and $I_1/I_0 = 1/2$ will be used. With the goal of iso-area comparison between the cells, from now on, all of the circuits are going to have a $K = I_0/I_1 = 2$ ratio.

Figure 12 shows the voltage transfer characteristic of the classical ST inverter. When compared to the inverter curve, it is noticeable that the gain is increased and also, the latch points are closer to the rails.

3.3.1 Minimum V_{DD} for the appearance of hysteresis

A simple method for finding the minimum supply voltage (V_{DDH}) such that the circuit exhibits hysteresis is through the small-signal equation singularity, that will be addressed in Section 3.4. In Melek et al. [5] the authors presented this methodology and came out with the result presented in (3.9)

$$V_{DDH} \approx 2\phi_t \ln\left(2 + \frac{I_2}{I_0} + \frac{I_0}{I_2} + \frac{I_1}{I_2}\right) \tag{3.9}$$

By applying the optimum boundary conditions for the

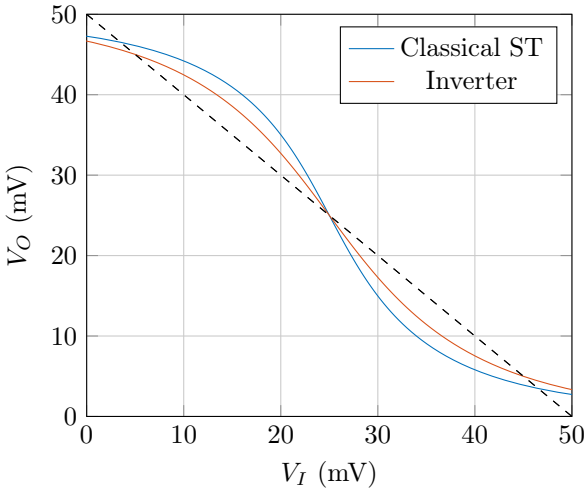

Figure 12 – Classical ST and inverter VTC curves ($V_{DD} = 50$ mV, $K = 2$, $I_0/I_2 = 1$, $n = 1$).

lower voltage supply for hysteresis, the minimum theoretical V_{DDH} of 75 mV is presented, as in (2.3).

3.4 Three-Inverter Schmitt Trigger (TI-ST)

The three-inverter Schmitt trigger architecture consists of a cascade of three CMOS inverter blocks, as shown in Figure 5. Figure 13 shows the schematic to be analyzed.

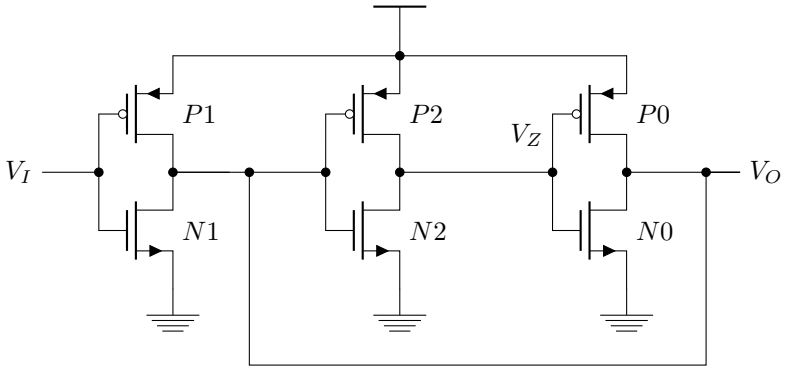

Figure 13 – Three-inverter Schmitt trigger schematic.

Equations (3.10) and (3.11) are obtained by applying (A.6) to the circuit, assuming $n = 1$ and P transistors having the same strength as the N transistors. They describe the transfer function $V_O \times V_I$ of the circuit, although not explicitly. The equations for nodes V_O and V_Z are, respectively

$$\begin{aligned} &I_1(\mathrm{e}^{\frac{V_I}{\phi_t}} - \mathrm{e}^{\frac{V_I - V_O}{\phi_t}}) + I_0(\mathrm{e}^{\frac{V_Z}{\phi_t}} - \mathrm{e}^{\frac{V_Z - V_O}{\phi_t}}) = \\ &I_1(\mathrm{e}^{\frac{V_{DD} - V_I}{\phi_t}} - \mathrm{e}^{\frac{V_O - V_I}{\phi_t}}) + I_0(\mathrm{e}^{\frac{V_{DD} - V_Z}{\phi_t}} - \mathrm{e}^{\frac{V_O - V_Z}{\phi_t}}) \end{aligned} \tag{3.10}$$

$$\mathrm{e}^{\frac{V_O}{\phi_t}} - \mathrm{e}^{\frac{V_O - V_Z}{\phi_t}} = \mathrm{e}^{\frac{V_{DD} - V_O}{\phi_t}} - \mathrm{e}^{\frac{V_Z - V_O}{\phi_t}} \tag{3.11}$$

Figure 14 shows the voltage transfer characteristic of the TI-ST. Even at a supply voltage as low as 50 mV, the TI-ST presents hysteresis; that is why the curve is "Z" shaped. The positive gain in the middle region, which is not feasible experimentally, is called "metastable region". In practice, when V_I varies, V_O should face two distincts infinite gain thresholds. We also define the scale factors ratios as $I_0/I_1 = K$ and $I_2/I_1 = J$ that are useful as design parameters.

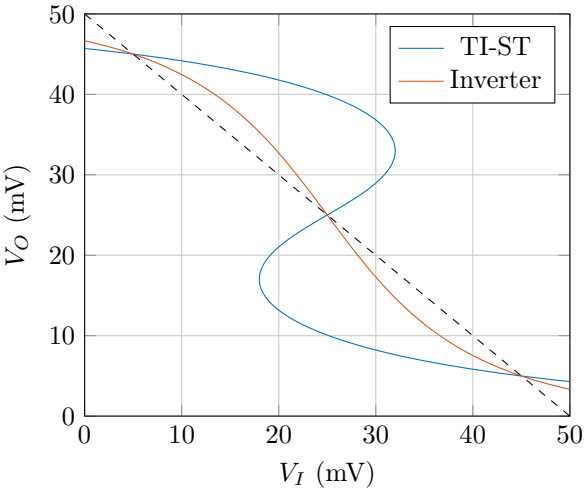

Figure 14 – TI-ST and inverter VTC curves ($V_{DD} = 50$ mV, $K = 2$, $n = 1$).

It should be noted that the scale factor J does not affect the voltage transfer characteristic at low frequencies. This is explained by the fact that inverter 2 drives a nodal capacitance only.

3.4.1 Small-Signal Analysis

The small-signal behavior of the circuit is described by the model in Figure 15. For the sake of simplicity, we assume that the P transistors are well balanced with the N transistors.

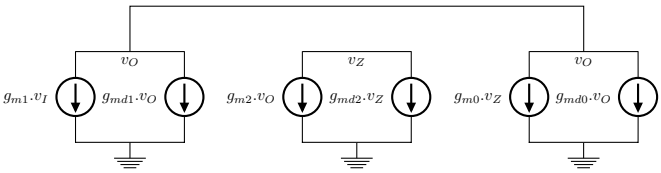

Figure 15 – TI-ST small-signal model.

The application of Kirchhoff currents law to the circuit of Figure 15 gives

$$g_{m1}.v_I + g_{md1}.v_O + g_{m0}.v_Z + g_{md0}.v_O = 0 \tag{3.12}$$

$$g_{m2}.v_O + g_{md2}.v_Z = 0 \tag{3.13}$$

Thus, combining 3.12 and 3.13 and applying the scale factors K and J:

$$\begin{aligned} \left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} &= -\frac{g_{m1}}{g_{md1}}\frac{1}{1-\frac{g_{m2}}{g_{md2}}\frac{g_{m0}}{g_{md1}}+\frac{g_{md0}}{g_{md1}}} \\ &= -\frac{g_m}{g_{md}}\frac{1}{1-K\frac{g_m^2}{g_{md}^2}+K} \end{aligned} \tag{3.14}$$

This result can be further simplified by using the previous CMOS inverter gain $A_V = -g_m/g_{md}$ of (3.5).

$$\left.\frac{v_O}{v_I}\right|_{V_O=V_I=\frac{V_{DD}}{2}} = A_V \frac{1}{1 - KA_V^2 + K} = \frac{A_V}{1 + K(1 - A_V^2)} \quad (3.15)$$

Equation (3.15) describes the small-signal gain of the TI-ST. Its dependence on the supply voltage, given by (3.6), assuming equal transistors ($K = J = 1$), $n = 1$ and 300K, is shown in Figure 16. The discontinuous part, in which the gain changes sign, represents the supply voltage which gives infinity gain or, in other terms, the minimum V_{DD} for the appearance of hysteresis. The positive gain is associated with the metastable segment of the hysteresis loop, which, in [5], has been used to give a rough approximation of the hysteresis width.

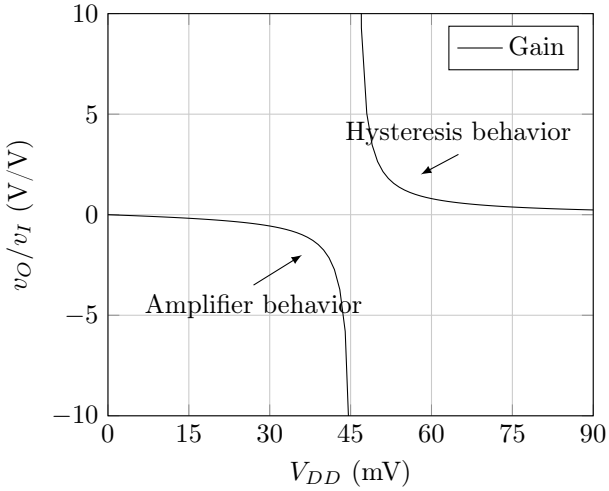

Figure 16 – TI-ST gain with $K = 1$.

3.4.2 Minimum V_{DD} for the appearance of hysteresis

For the purpose of finding the discontinuous transition between the amplification and hysteretic modes, a $v_O/v_I = \infty$ boundary condition is applied to (3.15) [5], yielding

$$1 + K.(1 - A_V^2) = 0 \tag{3.16}$$

Applying the inverter gain equation for $V_{DD}/2$, (3.6), yields (3.17).

$$V_{DDH} = 2\phi_t \ln\left(1 + n\sqrt{\frac{1+K}{K}}\right) \tag{3.17}$$

Here, V_{DDH} is the minimum V_{DD} for the appearance of hysteresis. Figure 17 shows the dependence of V_{DDH} on K, for two values of n. Theoretically, for $n = 1$, $K = 3$ is sufficient to reach infinity gain at $V_{DD} \approx 40$mV.

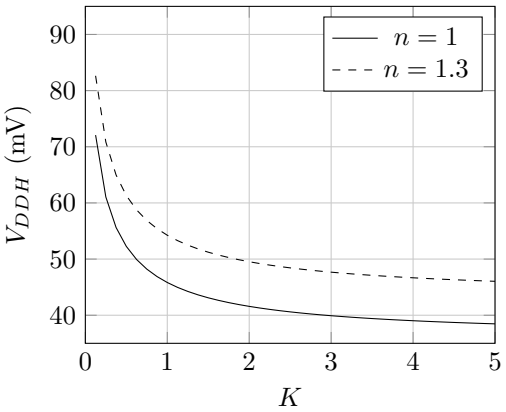

Figure 17 – Minimum V_{DD} required for infinity gain at $27°C$ versus scale factor K

With $n = 1$ and $K >> 1$, (3.17) reduces to $V_{DDH} \approx 2\phi_t . \ln(2)$; hence, the TI-ST is able to exhibit hysteresis for a supply voltage as low as the fundamental limit of unity gain for the CMOS inverter. Figure 18 demonstrates the shape of the VTC curve next to the asymptotic value of $V_{DD} = 36$ mV.

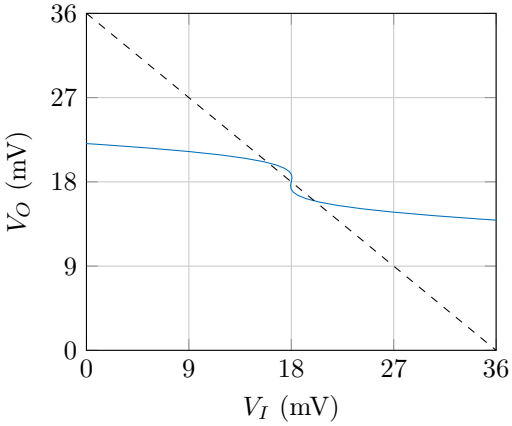

Figure 18 – TI-ST VTC curve at $V_{DD} = 36$ mV with $K = 100$.

3.5 Dynamic Leakage-Suppression Logic

The DLS inverter was proposed in [12], in order to reduce the consumption of a logic circuit in ultra low voltage operation. It is characterized by its positive feedback loop and a mixed network that can make the layout of logic cells a bit more troublesome, as well as its analysis. Figure 19 shows the schematic.

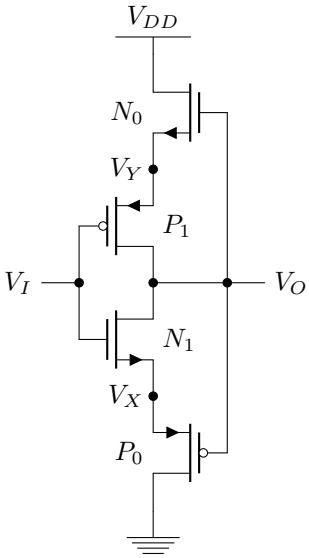

Figure 19 – Dynamic leakage-suppression inverter schematic.

Figure 20 shows the voltage transfer characteristic of the DLS inverter. It is noticeable that the DLS has a gain similar to the inverter cell and worse logic levels.

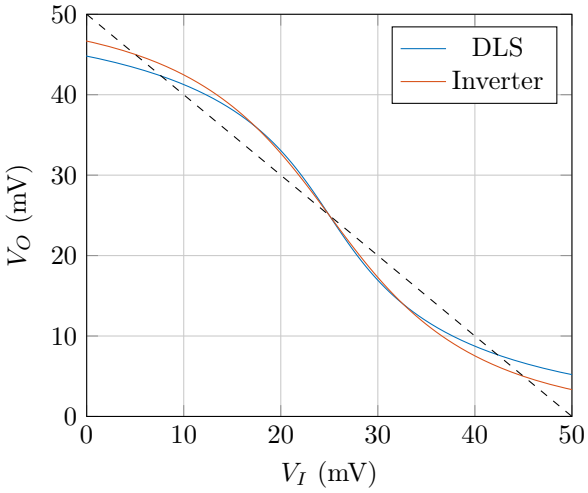

Figure 20 – DLS and inverter VTC curves ($V_{DD} = 50$ mV, $I_0/I_1 = 2$, $n = 1$).

3.6 Stacked-Inverter Gate (SIG)

The stacked-inverter gate, shown in Figures 6 and 21, is alternative to the standard inverter [19, 20]. The main inverter is composed of transistors P_1 and N_1.

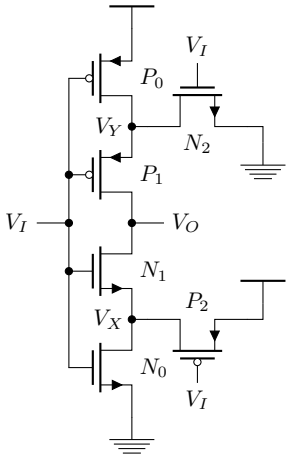

Figure 21 – Schematic of the SIG.

Contrary to the classical ST, which employs a positive feedback that results in hysteresis, the SIG makes use of a feed-forward loop to increase its gain. The VTC is obtained from the following nodal equations:

$$I_0(\mathrm{e}^{\frac{V_I}{\phi_t}} - \mathrm{e}^{\frac{V_I - V_X}{\phi_t}}) = I_2(\mathrm{e}^{\frac{V_{DD} - V_i}{\phi_t}} - \mathrm{e}^{\frac{V_X - V_I}{\phi_t}}) + I_1(\mathrm{e}^{\frac{V_I - V_X}{\phi_t}} - \mathrm{e}^{\frac{V_I - V_O}{\phi_t}}) \tag{3.18}$$

$$I_0(\mathrm{e}^{\frac{V_{DD} - V_I}{\phi_t}} - \mathrm{e}^{\frac{V_Y - V_I}{\phi_t}}) = I_2(\mathrm{e}^{\frac{V_I}{\phi_t}} - \mathrm{e}^{\frac{V_I - V_Y}{\phi_t}}) + I_1(\mathrm{e}^{\frac{V_Y - V_I}{\phi_t}} - \mathrm{e}^{\frac{V_O - V_I}{\phi_t}}) \tag{3.19}$$

$$\mathrm{e}^{\frac{V_I - V_X}{\phi_t}} - \mathrm{e}^{\frac{V_I - V_O}{\phi_t}} = \mathrm{e}^{\frac{V_Y - V_I}{\phi_t}} - \mathrm{e}^{\frac{V_O - V_I}{\phi_t}} \tag{3.20}$$

Figure 22 shows the voltage transfer characteristic of the SIG. It is noticeable that the gain is as high as the classical ST and the latch stable points are higher than any other presented cell.

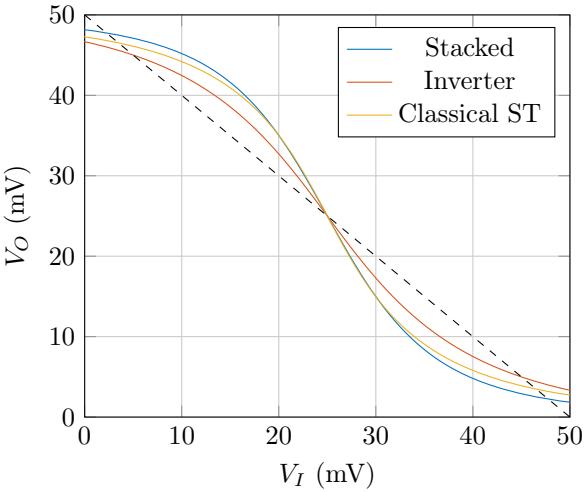

Figure 22 – Stacked, inverter and classical ST VTC curves ($V_{DD} = 50$ mV, $K = 2$, $n = 1$).

3.6.1 Small-Signal Analysis

The small-signal model for the SIG is built from a simplification of the classical inverter results (Subsection 3.2.1), as in Figure 23. This simplification can be done since it is assumed the boundary condition $V_I = V_O = V_{DD}/2$.

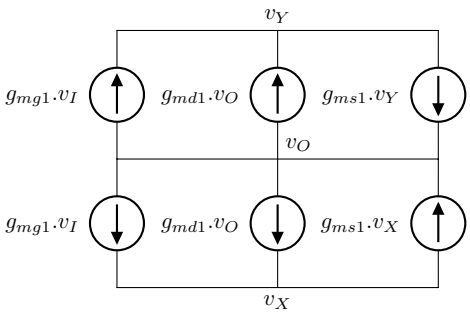

Figure 23 – Stacked-inverter gate small-signal model.

Using (3.5) node voltages v_X and v_Y are defined as in equation (3.21).

$$A_{V_{X,Y}} = \frac{v_{X,Y}}{v_I} = -\left(\frac{g_{mg0} + g_{mg2}}{g_{md0} + g_{md2}}\right) \tag{3.21}$$

From the model on Figure 23 the correspondent equation to node v_O is given by (3.22).

$$2g_{md1}v_O - g_{ms1}(v_X + v_Y) + 2g_{mg1}v_I = 0 \tag{3.22}$$

Finally, the gain can be calculated by combining (3.21) and (3.22), resulting in (3.23).

$$A_V = -\left[\frac{g_{ms1}}{g_{md1}}\left(\frac{g_{mg0} + g_{mg2}}{g_{md0} + g_{md2}}\right) + \frac{g_{mg1}}{g_{md1}}\right] \tag{3.23}$$

The stacked-inverter gate design can be simplified by considering the scale factor as a ratio $K = I_0/I_2$ and $J = I_1/I_2$.

In order to calculate $V_{DD_{min}}$, we start with a value of V_{DD} close to the expected value of $V_{DD_{min}}$, sweep V_{DD} around the expected $V_{DD_{min}}$ to find the value of A_V for $V_I = V_O = V_{DD}/2$. The value of $V_{DD_{min}}$ corresponds to that for which $A_V = -1$. In a first approach, J is kept constant and equal to 1. As can be seen, this numerical solution reveals a lower unity gain supply voltage than 31.5 mV of the classical ST with a $K \approx 2.5$.

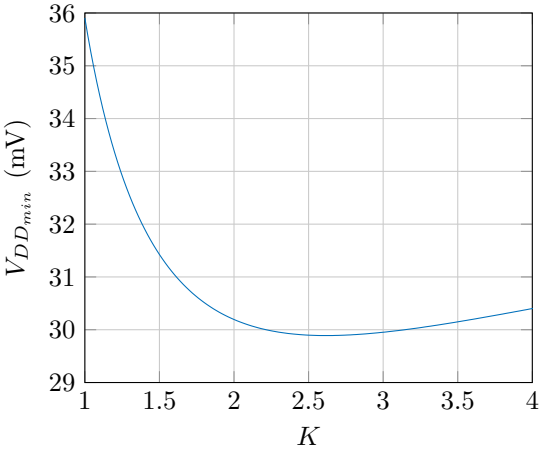

Figure 24 – Stacked-inverter gate unity gain for different K values, and $J = 1$.

3.7 Considerations

In this chapter several inverter topologies were discussed and analyzed considering ideal working conditions and simplified models for weak inversion. The classical inverter is a basic cell for benchmarking and performance comparison.

The TI-ST, which is based on the basic inverter cell, is able to provide hysteresis from a supply voltage V_{DDH} coincident with that of the classical inverter for a unity gain. However, for higher supply voltages, the hysteresis grows excessively to a point that the cell locks itself in an arbitrary (LOW or HIGH) state, which cannot be changed for any input voltage within the rails. Figure 25 shows a TI-ST with $K = 5$ locked at a LOW logic level.

The DLS inverter is built using less transistors, and according to [12], has lower leakage than the classical inverter but has lower gain and latch stable points.

The stacked-inverter gate, which employs a feedforward path, achieves the lowest supply voltage for unity gain of all cells of this work. The stacked-inverter does not present hysteresis, even for high voltages, since it does not have a positive feedback path.

Despite all the improvements of the alternative topologies the basic inverter still uses less silicon area and, for this reason, has a lower input capacitance.

In the next chapter, some of the topologies presented in this chapter are going to be compared through simulations. Some of these cells were fabricated and measured to validate part of the theoretical results.

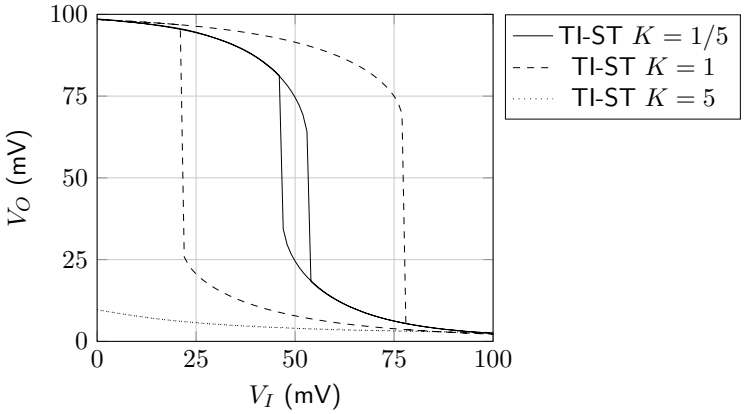

Figure 25 – TI-ST measured VTC for different K values at $V_{DD} = 100$ mV.

4 SIMULATIONS AND MEASUREMENT

This chapter comprises results from either simulation or experiment, in order to validate the outcomes of this work. The BSIM4 model (V4.5) is used as a computational model into Cadence® Virtuoso® tools. The technology node used is 0.18 μm.

4.1 Voltage Transfer Characteristics (VTC)

For the purpose of comparison, the previously VTC results are displayed in Figure 26. The figure is generated by solving the transcendental VTC equations, obtained throughout Chapter 3. The design scale factors have been chosen arbitrarily as $I_N = 1$ nA and slope factor $n = 1$. The transistor widths are shown in Table 1, or equivalently to a design ratio of $K = 2$. The channel length for all the transistors is $L = 600$ nm, since secondary effects become less prominent with a channel length higher than minimum. It is seen in Figure 26 that the classical ST presents a higher gain and higher latch points for $V_{DD} = 50$ mV; also, the TI-ST presents hysteresis even at such a low voltage.

The cells were built with medium Vt ($V_{T0P} = V_{T0N} \approx 0.3$ V) transistors. In order to prevent the border effects to affect the relative aspect ratios, the W multiplicity was realized through the use of parallel devices. It should be noted that the gain and the latch stable points are lowered considerably due to

W (μm)	P_0	P_1	P_2	N_0	N_1	N_2
Inverter	-	2	-	-	6	-
SIG	4	2	2	12	6	6
Classical ST	4	2	2	12	6	6
TI-ST	4	2	2	12	6	6

Table 1 – Transistor width sizes for simulations and measurements.

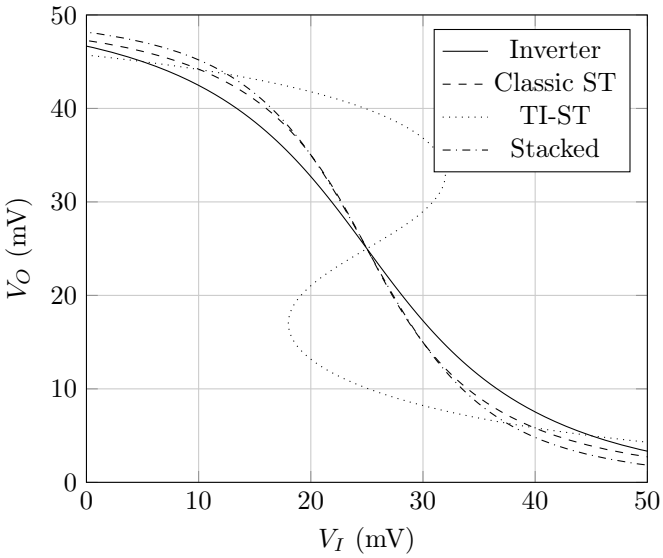

Figure 26 – Numerical VTC comparison between all cells (V_{DD} = 50 mV, $K = 2$, $n = 1$).

the increase of the slope factor from $n = 1$, in the case of Figure 26, to $n \approx 1.3$ for Figure 27. Despite this difference, the trend verified in the numerical results is still present in the simulation.

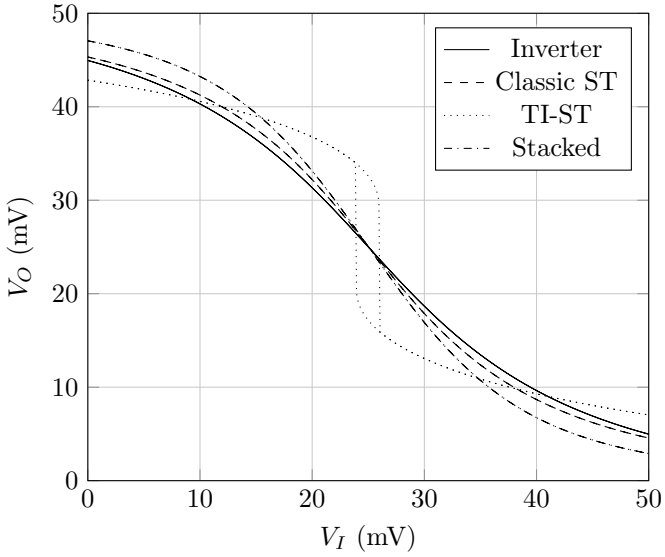

Figure 27 – Simulated VTC comparison ($V_{DD} = 50$ mV, $K = 2$, $n \approx 1.3$).

4.2 Output Voltage Swing

Figure 28 shows plots of V_H versus V_{DD} obtained through the numerical simulation of the VTC equations. Since V_H and V_L are symmetrical with respect to $V_{DD}/2$, only the upper latch stable point is shown.

It can be noted that, as regards the VTC characteristic, the performance of the stacked-inverter gate is considerably better than that of the classical ST topology for voltages lower than 50 mV and also, the TI-ST has the same performance as the inverter.

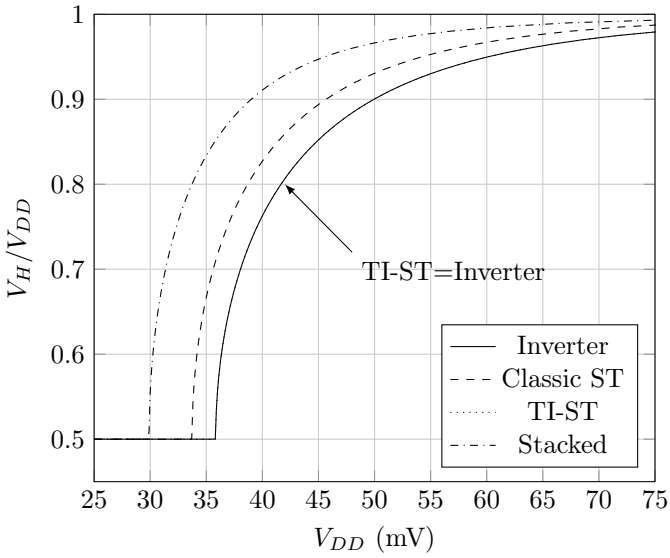

Figure 28 – Latch stable points for the studied circuit topologies. ($n = 1$, $K = 2$)

Table 2 shows a comparison of the simulated and numerical values from Figure 26, operating at $V_{DD} = 50$ mV. As explained before, the discrepancy between simulation and numerical results is due to different slope factors.

	Numerical (%)	Simulation (%)
Inverter	90	81.6
SIG	95.5	91.9
Classical ST	93	85.3
TI-ST	90	81.6

Table 2 – V_H/V_{DD} for $V_{DD} = 50$ mV.

4.3 Ring Oscillators

In order to evaluate the AC performance of the cells as well as the regenerative properties, two types of ring oscillators (RO) were built and simulated: a five-stage RO and an eleven-stage RO. The design of each circuit has been kept according to Table 1.

4.3.1 Five-stage ROs

Figure 29 shows the basic five-stage RO topology employed for the AC test.

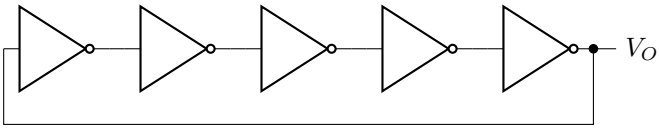

Figure 29 – Five-stage ring oscillator.

The steady state response for the various RO's is shown in Figure 30. It is noticeable that all cells are well balanced as the oscillations are centered around $V_{DD}/2$. As expected, the inverter-based oscillator has the highest frequency. The stacked-based oscillator has the highest amplitude performance, followed by the TI-ST and the classical ST. Even though the classical ST has better higher latch stable points, the low number of stages favors the TI-ST, for it has a higher gain and achieves its maximum possible amplitude at $V_{DD} = 50$ mV with less stages.

Table 3 shows the operating frequency of each circuit as well the power. PDP the Power-Delay-Product, which is a common benchmark for logic cells that reflects the energy per operation. The PDP is lower in the inverter, followed by the SIG

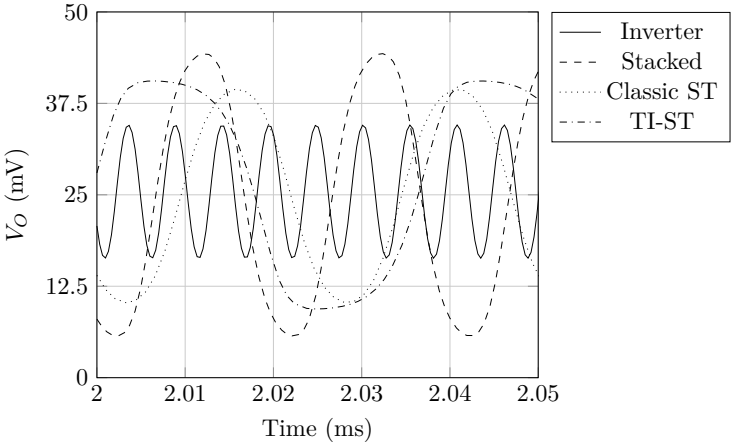

Figure 30 – Simulation results of five-stage oscillators with $V_{DD} = 50$ mV.

and the TI-ST. The best performance concerning amplitude is seen in stacked-inverter cell, as it has high gain, as the classical ST, and the closest to the rails latch stable points.

	Freq. (kHz)	Power (nW)	PDP (fJ)	V_{PP} (mV)	V_{PP}/V_{DD} (%)
Inverter	187.8	0.11	0.06	18.2	36
SIG	49.9	0.29	0.58	38.6	77
Classical ST	40.0	0.23	0.58	29.2	58
TI-ST	27.0	0.43	1.59	31.2	62

Table 3 – Measurements of the five-stage ring oscillator at $V_{DD} =$ 50mV.

A Monte Carlo analysis was run to check the behavior of the cells due to variability. To do so, the foundry model for process variation and mismatch was used to simulate 200 samples. The

criterion for establishing the yield is that of a minimum oscillation peak-to-peak voltage of 10 mV. The SIG and classical ST based oscillators had a 100% yield and a considerably lower coefficient of variation.

V_{PP} (mV)	Yield (%)	μ	σ	σ/μ (%)
Inverter	79	13.2	5.7	43.0
SIG	100	38.2	0.6	1.5
Classical ST	100	28.2	1.1	3.7
TI-ST	89.5	26.1	9.1	34.8

Table 4 – Peak-to-peak oscillation of the five-stage ROs obtained through Monte Carlo analysis

Freq. (kHz)	Yield (%)	μ	σ	σ/μ (%)
Inverter	79	185.1	93.5	50.5
SIG	100	57.8	24.2	41.8
Classical ST	100	46.1	19.4	42.0
TI-ST	89.5	25.2	11.5	45.7

Table 5 – Frequency of the five-stage ROs obtained through Monte Carlo analysis

4.3.2 Eleven-stage ROs

The simulated eleven-stage RO employed the same unit cells as the five-stage RO. The oscillations are shown in Figure 31. As the number of stages increases, the peak-to-peak voltages tend to converge to the latch stable points presented in Figure 28. The TI-ST amplitude approaches that of the inverter, whereas the amplitude of the classical ST is slightly higher. Table 6 details these results.

Using the same criterion for yield as in the five-stage RO, the Monte Carlo analysis resulted in a 100% yield for the

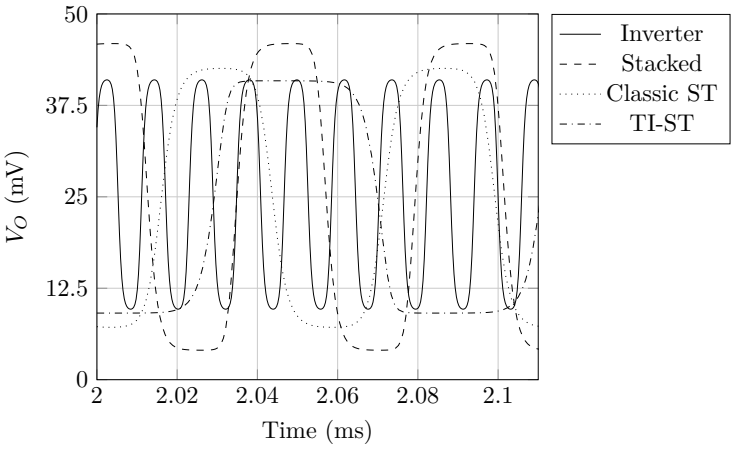

Figure 31 – Simulation results of eleven-stage oscillators with $V_{DD} = 50$ mV.

	Freq. (kHz)	Power (nW)	PDP (fJ)	V_{PP} (mV)	V_{PP}/V_{DD} (%)
Inverter	84.5	0.23	0.27	31.3	62.6
SIG	22.5	0.58	2.57	41.9	83.8
Classical ST	18.0	0.48	2.66	35.4	70.8
TI-ST	12.3	0.88	7.17	31.8	63.6

Table 6 – Measurements of the eleven-stage ring oscillator at $V_{DD} = 50$mV.

inverter-, stacked-, and classical ST-based oscillators. The TI-ST shows a lower yield due to process variations and mismatch causing an imbalance on the N and P networks, which shifts the VTC metastable region and causes a lock state.

V_{PP} (mV)	Yield (%)	μ	σ	σ/μ (%)
Inverter	100	30.0	1.7	5.5
SIG	100	41.7	0.4	1.1
Classical ST	100	35.0	0.6	1.7
TI-ST	80	24.8	12.4	50.2

Table 7 – Peak-to-peak oscillation of the eleven-stage ROs obtained through Monte Carlo analysis

Freq. (kHz)	Yield (%)	μ	σ	σ/μ (%)
Inverter	100	95.0	37.7	39.7
SIG	100	26.0	10.8	41.4
Classical ST	100	20.7	8.7	41.8
TI-ST	80	11.3	4.4	39.2

Table 8 – Frequency of the eleven-stage ROs obtained through Monte Carlo analysis

4.4 Measurements

The following blocks were designed in a 0.18 μm technology and sent for tape-out through MOSIS MPW University Program:

- An inverter with unit transistors as in Table 1.
- Three TI-STs with scale factors of $K = 5$, $K = 1$ and $K = 1/5$ as in Table 9.
- A Classical ST with $K = 2$ as in Table 1.

The measured slope factor n for both N and P-channel transistors, extracted using the g_m/I_D [22] method, is around $n = 1.3$. Figure 33 shows the layout of a TI-ST cell with $K = 1$.

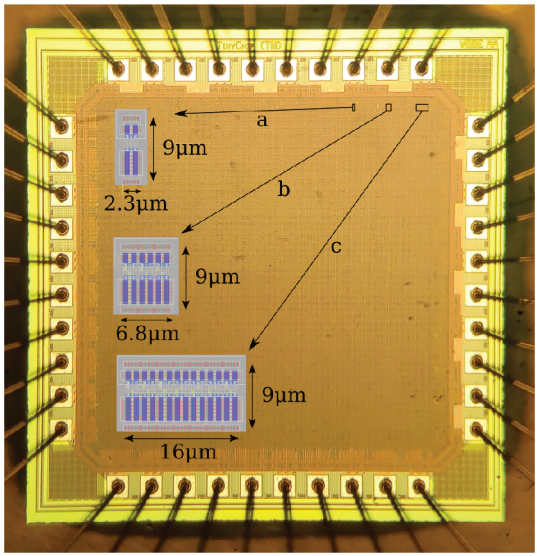

Figure 32 Photo of 2 mm × 2 mm die, fabricated in 0.18 μm technology node. a: CMOS inverter cell, b: TI-ST $K = 1$, c: TI-ST $K = 5$

W (μm)	P_0	P_1	P_2	N_0	N_1	N_2
$K = 1/5$	2	2	10	6	6	30
$K = 1$	2	2	2	6	6	6
$K = 5$	10	2	2	30	6	6

Table 9 Transistor dimensions for the fabricated TI-ST.

A basic comparison of the inverter, the classic ST with $K = 2$ and the TI-ST with $K = 1$ can be seen in Figure 34. A small imbalance is visible but the relative voltage gains of the cells vary as expected. Figure 35 exposes the small-singal gain through the derivative of each measured curve.

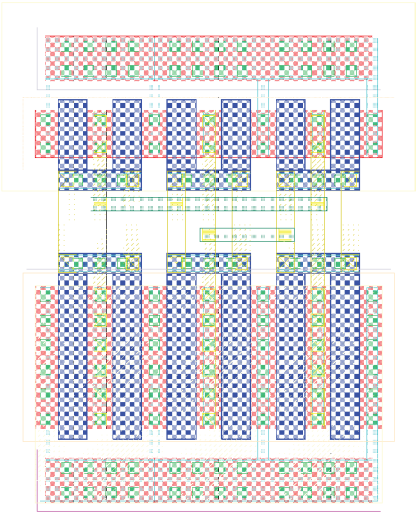

Figure 33 Layout of TI-ST with $K = 1$.

For the TI-ST, five inverters were connected in parallel in place of inverter 3 for obtaining $K = 5$, and the same procedure was performed with inverter 1 for $K = 1/5$. The expected minimum V_{DDH} for the appearance of hysteresis for $K = 5$, according to (3.17), is approximately 46 mV.

Figure 36 shows the measured VTCs for each design. As can be seen, the gain increases with the scale factor K of the TI-ST. Also, as predicted, the VTC presents hysteresis for $K = 5$ and $V_{DD} = 50$ mV. The measured minimum voltage for the appearance of hysteretic behavior is $V_{DD} = 48.5$ mV, which matches closely the value (46mV) predicted using small-signal analysis.

Figure 37 shows a comparison between the calculated

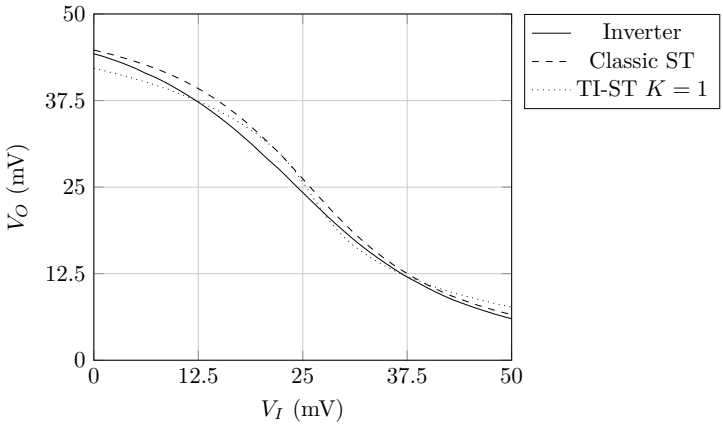

Figure 34 – Measured VTC curves for the three cells at $V_{DD} = 50$ mV.

and measured small-signal gains of the inverter cell and the TI-ST with $K = 1$, temperature of 27°C and $n = 1.3$. The circles represent the inverter measurements, while the diamonds, represent the TI-ST measurements with $K = 1$.

Figure 38 presents the measured hysteresis loop widths for different supply voltages. The hysteresis curves start to appear for the supply voltages predicted by (3.17). It should be noted that for the case of high positive feedback ($K = 5$), the hysteresis width is higher than the supply voltage for $V_{DD} \geq 70$mV.

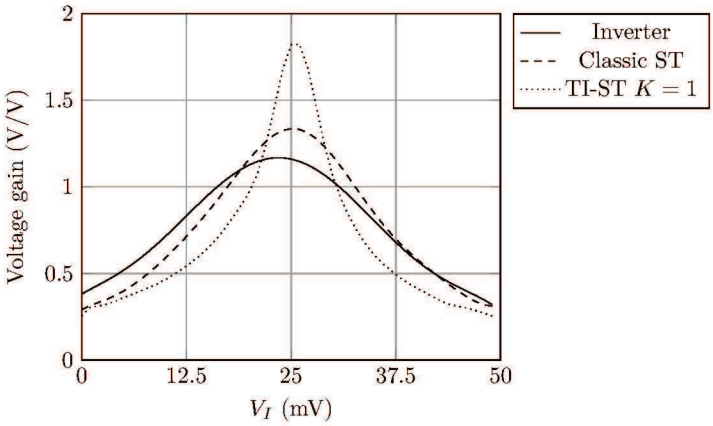

Figure 35 Voltage gain calculated from the VTC curves at $V_{DD} = 50$ mV.

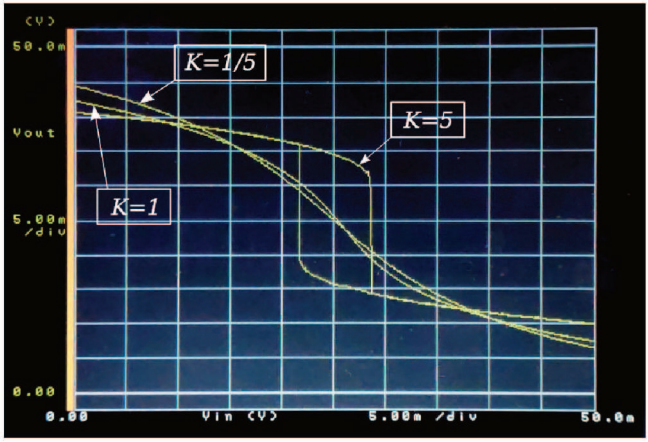

Figure 36 Measured VTC curve of TI-ST for three K values at $V_{DD} = 50$ mV.

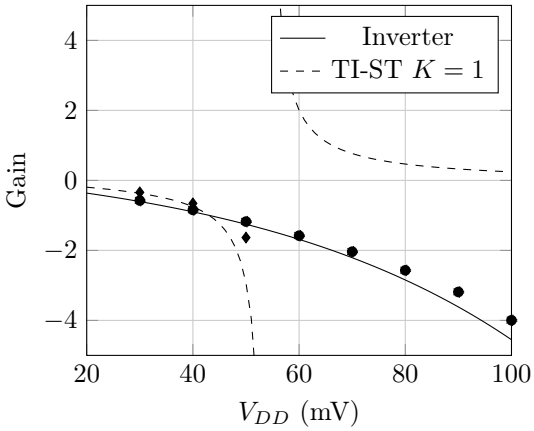

Figure 37 – Calculated and measured gains for a single CMOS inverter compared to a TI-ST.

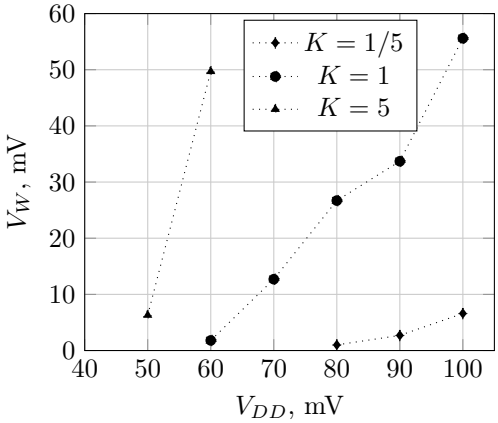

Figure 38 – Measured hysteresis loop widths versus supply voltage V_{DD}.

5 DISCUSSIONS AND CONCLUSIONS

In this work, several cells of inverters and ST-inverters were analyzed in order to provide a consistent comparison between them for operation under ultra low supply voltages.

In Chapter 3, three circuits have been analytically described. The stacked-inverter gate was proven numerically to break once again the unity gain barrier, lowering the value to $V_{DD} \approx 30$ mV. The stacked-inverter also showed latch stable points closer to the rails than the classical ST. Finally, we have demonstrated, for the first time, that the TI-ST provides hysteresis from the lowest supply voltage, as compared to other ST architectures. Theoretically, the TI-ST can provide hysteresis from supply voltages equal to the Meindl limit of $2\phi_t \ln 2$.

The TI-ST circuit can be better employed when there is a design need for a considerably amount of hysteresis, whilst the stacked has advantages in terms of gain and latch points. The classical ST stands in a middle class, presenting hysteresis and latch points closer to the rails. The DLS inverter did not show superiority in terms of gain and latch points, so its results were omitted. A deeper analysis in power consumption may present some advantages of using it to avoid static power consumption, as stated by the reference authors.

Despite a reduction in the speed performance as compared to the standard inverter, the cells analyzed along this work

can be advantageously employed in ultra-low-voltage circuits to improve the static noise margins. With the rising demand for highly efficient circuits operating from very low supply voltages, they can represent an interesting choice for the realization of logic and memory, and as useful components for generating hysteresis windows for very low supply voltages.

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Appendix

APPENDIX A – UICM MODEL

Figure 39 shows the symbol of a MOS transistor, where G represents the gate, D the drain, S the source and B the bulk. In this work, the bulk terminal (B) is always connected to the lowest electric potential of the circuit, usually ground, for N channel transistors and to the highest electric potential (V_{DD}), for P channel transistors. For this reason, the bulk terminal has been omitted along the main text of this dissertation.

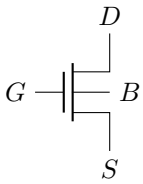

Figure 39 – MOS transistor.

For a long channel device, the drain current I_D can be split into two terms (A.1): the forward current I_F and the reverse current I_R. The UICM model maintains the device symmetry, between source and drain.

$$I_D = I_F(V_G, V_S) - I_R(V_G, V_D) = I_S(i_f - i_r) \tag{A.1}$$

I_S is the normalization current, which is dependent on technological parameters as well as on device dimensions, shown

in (A.2) and slightly on gate bias. I_{SH} is the sheet normalization current, which, in a first order approximation, is independent of device dimensions.

$$I_S = \mu_n C'_{ox} n \frac{\phi_t^2}{2} \frac{W}{L} = I_{SH} \frac{W}{L} \tag{A.2}$$

Here, μ_n is the electron mobility, C'_{ox} the oxide capacitance per unit area, n the slope factor and W and L the transistor width and length, respectively.

From the Unified Current-Control Model (UICM) [22], the relationship between voltage and current in a transistor is given by (A.3),

$$\frac{V_P - V_{S(D)}}{\phi_t} = \sqrt{1 + i_{f(r)}} - 2 + \ln\left(\sqrt{1 + i_{f(r)}} - 1\right) \tag{A.3}$$

where the pinch-off voltage is linearly approximated as

$$V_P \cong \frac{V_G - |V_{T0}|}{n} \tag{A.4}$$

and V_S, V_D and V_G are source, drain and gate voltages, respectively, i_f and i_r the normalized forward and reverse currents. For operation in the subthreshold regime only (i_f and $i_r << 1$), equation (A.3) is simplified to (A.5).

$$i_{f(r)} = 2\mathrm{e}^{\frac{V_P - V_{S(D)}}{\phi_t} + 1} \tag{A.5}$$

Denormalizing the equation and using the relation (A.1) gives the format that will be oftentimes further used, as in (A.6),

$$I_D = I_N \mathrm{e}^{\frac{V_G}{n\phi_t}} \left(\mathrm{e}^{\frac{-V_S}{\phi_t}} - \mathrm{e}^{\frac{-V_D}{\phi_t}}\right) \tag{A.6}$$

where

$$I_N = 2I_S \mathrm{e}^{-\frac{V_{T0}}{n\phi_t}+1} = \mu_n C'_{ox} n \phi_t^2 \frac{W}{L} \mathrm{e}^{-\frac{V_{T0}}{n\phi_t}+1} \qquad \text{(A.7)}$$

I_N is the linear scale factor of the transistor which contains technological parameters and dimensions. I_N represents the strength of the device. Note that all voltages are referred to the bulk terminal since this is a symmetrical model, thus (A.6) can be used for N-channel devices only. For P-channel transistors, the voltages must be referred to the bulk, always connected to the positive rail, as said before.

A.1 Small-Signal Transconductances

With the purpose of analyzing the small-signal low-frequency gain, we have used the model in Figure 40.

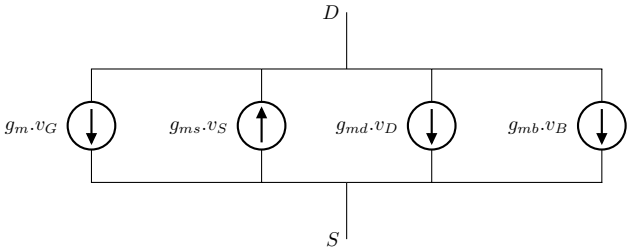

Figure 40 – MOSFET small-signal model.

The four transconductances in weak inversion are calculated by taking the following partial derivatives from (A.5) and

(A.1):

$$g_m = \frac{\partial I_D}{\partial V_G},\ g_{ms} = -\frac{\partial I_D}{\partial V_S},\ g_{md} = \frac{\partial I_D}{\partial V_D},\ g_{mb} = \frac{\partial I_D}{\partial V_B} \tag{A.8}$$

which give (A.9) and (A.10)

$$g_{ms(d)} = \frac{2I_S \mathrm{e}^{\frac{V_P - V_{S(D)}}{\phi_t}+1}}{\phi_t} = \frac{I_N}{\phi_t}\mathrm{e}^{\frac{V_G - nV_S}{n\phi_t}} \tag{A.9}$$

$$g_m = \frac{g_{ms} - g_{md}}{n} = \frac{g_{ms}}{n}\left(1 - \mathrm{e}^{-\frac{V_{DS}}{\phi_t}}\right) \tag{A.10}$$