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A Compact Model for Flicker Noise in MOS Transistors for Analog Circuit Design

Alfredo Arnaud and Carlos Galup-Montoro

***Abstract*—Designers need accurate models to estimate 1/f noise in MOS transistors as a function of their size, bias point, and technology. Conventional models present limitations; they usually do not consistently represent the series-parallel associations of transistors and may not provide adequate results for all the operating regions, particularly moderate inversion. In this brief, we present a consistent, physics-based, one-equation-all-regions model for flicker noise developed with the aid of a one-equation-all-regions dc model of the MOS transistor.**

***Index Terms*—1/f noise, compact modeling, flicker noise, MOSFET, noise.**

I. INTRODUCTION

Flicker noise or simply 1/f noise is such that its power spectral density (P.S.D.) varies with frequency in the form [1]–[7]

$$S(f) = \frac{K}{f^{\gamma}} \tag{1}$$

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with K, γ constants, and $\gamma \approx 1$. The physics behind flicker noise in the MOS transistor is still a topic of discussion. It is quite well accepted that the sources of low frequency noise are mainly carrier number and mobility fluctuations due to random trapping–detrapping of carriers in energy states near the surface of the semiconductor [3], [4]. However, the exact mechanism and the statistics of the resulting noise current, as well as how it is related to such technology parameters as doping concentration or surface quality, are not yet clear.

From the designer's perspective, it is desirable to have noise models that allow an accurate prediction of the noise power spectral density in terms of bias, size and technology of the transistor. These models should not be complex for noise calculation and should employ variables easily handled by a simulator, such as currents or charges in transistor nodes. A considerable effort has been made to set up MOS transistor models with the above characteristics, but a general, single-piece flicker noise model has not yet been developed.

In this brief, we develop a one-equation-all-regions model for the flicker noise in long channel MOS transistors. To calculate the total current noise in a MOS transistor, the noise current caused by trapping-detrapping of carriers in each channel element must be integrated. To perform this integration we employ the MOSFET model from [8]. The fundamental approximation of this model is the linear dependence of the inversion charge density Q_I' on the surface potential ϕ_S, which encompasses the weak, moderate, and strong inversion regions:

$$dQ_I' = \left(C_b' + C_{ox}'\right) d\phi_S = nC_{ox}' d\phi_S \tag{2}$$

where n is the slope factor, slightly dependent on the gate voltage C_b' and C_{ox}' are the depletion and oxide capacitance per unit area. The drain current in a long-channel transistor is calculated with the aid of (2) and the charge-sheet approximation [9]

$$I_D = \frac{\mu W}{nC_{ox}'}\left(-Q_I' + \phi_t n C_{ox}'\right)\frac{dQ_I'}{dx}. \tag{3a}$$

W and L are transistor dimensions, μ is the effective mobility, and ϕ_t is the thermal voltage.

Because the derivative of the channel charge density with respect to the channel potential $V_X (V_S \le V_X \le V_D)$ in [8] is $nC_{ox}' Q_I'/(Q_I' - nC_{ox}'\phi_t)$, the drain current is also given by

$$I_D = -\mu \frac{W}{dx} Q_I' \cdot dV_X. \tag{3b}$$

Consequently, the model in [8] is fully consistent with the quasi-Fermi potential formulation for the drain current [9, Annex J].

II. COMPACT MODEL FOR FLICKER NOISE

To integrate the elementary noise contributions along the channel we split the transistor into three series elements: the upper transistor, the lower transistor, and a small channel element of length Δx and area $\Delta A = W \cdot \Delta x$ [Fig. 1(a)]. Small-signal analysis can be carried out, considering the general expression for the source (drain) transconductance $g_{ms(d)}$ defined as the derivative of the drain current with respect to the source (drain) voltage [8], [9]

$$g_{msu} = -\mu \frac{W}{L - x} Q_{IX}' \quad g_{mdl} = -\mu \frac{W}{x} Q_{IX}' \tag{4}$$

where Q_{IX}' is the inversion charge density evaluated at a point X in the channel and μ is the effective mobility. We define the resistance ΔR of a small element of the channel of length Δx with the aid of (3b): $\Delta R = \Delta V_X / I_D = -\Delta x/(\mu W Q_I')$. Representing the channel element by a resistance, and considering the transconductances proportional to the inversion charge densities (4) [9], are both consequences of the quasi-Fermi potential formulation for the drain current. Calling

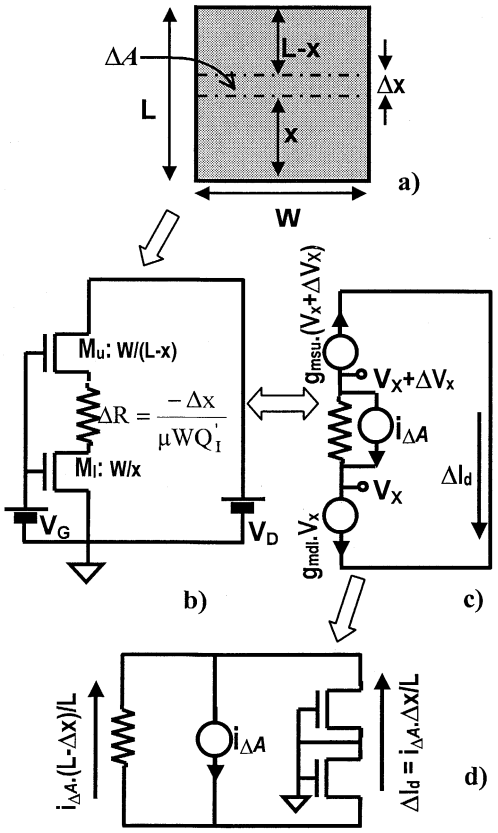

Fig. 1. (a) MOS transistor channel. (b) The transistor is separated into three series components. (c) Small signal analysis to calculate the noise contribution to the drain current of the noisy element ΔA. (d) Small signal equivalent circuit showing current division.

the noise current produced by the channel element $i_{\Delta A}$ [Fig. 1(c)], small-signal analysis allows one to calculate the resulting effect of $i_{\Delta A}$ on the drain current noise. As shown in Fig. 1(d), current division between the channel element and the equivalent small signal resistance of the rest of the channel gives $\Delta I_d = (\Delta x/L)\cdot i_{\Delta A}$. Thus, if $S_{\Delta A}(x,f)$ is the P.S.D. of $i_{\Delta A}$ multiplied by Δx, then the total noise current of the transistor is

$$S_{I_d}(f) = \frac{1}{L^2}\int_0^L S_{\Delta A}(x,f)\cdot dx. \tag{5}$$

Note that since $i_{\Delta A}$ is related to the average of the local fluctuations of the carrier density N in the channel in the area ΔA, its P.S.D. must be proportional to $1/\Delta A = 1/(\mathrm{W}\cdot\Delta x)$. Equation (5) is widely general and could be employed with any model for the noise $i_{\Delta A}$ of a single channel element such as the thermal noise model, Hooge's model [5], or the carrier number fluctuation model usually employed for the deduction of physical based flicker noise models [3], [11]. We will employ the latter so we must relate the carrier number fluctuation to the noise current $i_{\Delta A}$. Following [2], [3], and [11]

$$i_{\Delta A} = I_D\cdot\frac{\delta N}{N} \tag{6}$$

where δN is the fluctuation of the number of carriers per unit area N in the channel element of area ΔA. For the sake of simplicity we will consider only fluctuation in the number of carriers, but the analysis could be extended to include fluctuation in the mobility [3].

To compute the total drain noise produced by the carrier number fluctuation, we use the same hypothesis as Reimbold [2] and the models of inversion and depletion capacitance per unit area of [8]. It follows that the P.S.D. of the fluctuations δN of the ΔA carrier density in the channel area can be written as

$$S_N(f) = \frac{N_{ot}\cdot(Q'_I)^2}{\Delta A\cdot(Q'_I - nC'_{ox}\phi_t)^2}\cdot\frac{1}{f} \tag{7}$$

where N_{ot} is the effective number of traps [7], a technology parameter to be adjusted.

We obtain an expression of the P.S.D. of the drain current using (6) and (7) to calculate $S_{\Delta A}(x,f)$, and inserting the result into (5). With the aid of (3a) the integration over the channel length in (5) is changed into the integration over the channel charge density

$$S_{I_d} = \frac{q^2N_{ot}\mu I_D}{nC'_{ox}L^2}\cdot\frac{1}{f}\int_{Q'_{IS}}^{Q'_{ID}}\frac{1}{nC'_{ox}\phi_t - Q'_I}dQ'_I. \tag{8}$$

It follows

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2N_{ot}\mu}{L^2nC'_{ox}I_D}\cdot\ln\left[\frac{nC'_{ox}\phi_t - Q'_{IS}}{nC'_{ox}\phi_t - Q'_{ID}}\right]\cdot\frac{1}{f} \tag{9}$$

An expression similar to (9) is used in BSIM [10] to model strong inversion noise due to charge trapping, but we must emphasize that (9) is valid for any inversion level, including moderate inversion.

- In weak inversion, $Q'_{IS}, Q'_{ID} \ll nC'_{ox}\phi_t$. Making a first order series expansion, it is possible to rewrite (9) in a more concise manner

$$\frac{S_{I_d}}{I_D^2} = \frac{N_{ot}}{WLN^{*2}}\cdot\frac{1}{f} \tag{10}$$

  where $N^* = nC'_{ox}\phi_t/q$. Equation (10) is the same expression used in BSIM3 and 4 [10] to model flicker noise in weak inversion ($N_{ot} = A\cdot k_BT/\gamma$ in [3]) and, is equivalent to the formula proposed by Reimbold in 1984 [2].
- In strong inversion and in the linear region, $Q'_{IS} \cong Q'_{ID} \cong -C'_{ox}(V_G - V_T)$ and the first-order expansion of (9) leads to

$$\frac{S_{I_d}}{I_D^2} = \frac{q^2N_{ot}}{WLC'^2_{ox}(V_G - V_T)^2}\cdot\frac{1}{f} \tag{11}$$

  In this case also, the result is the same as that obtained by Reimbold in [2].

Summarizing the bias dependence of the drain current P.S.D., in subthreshold, S_{I_d} increases with I_D^2 following (10) while in saturation in strong inversion S_{I_d} increases with I_D as predicted by (9) if we neglect the variation of the logarithmic term.

Finally, let us remark that the model in (9) is consistent when applied to the parallel or series association of transistors. Effectively suppose we do a virtual cut of a transistor, splicing it in two series elements quite similar to those in Fig. 1. Suppose the upper transistor introduces a noise current with a P.S.D. $S_{i_{du}}$ and the lower transistor a noise current $S_{i_{dl}}$. Small signal analysis allows the calculation the noise current $S_{i_{d\_s}}$ of the series-composed transistor:

$$S_{i_{d\_s}}(f) = S_{i_{du}}(f)\cdot\left[\frac{1}{1+k}\right]^2 + S_{i_{dl}}(f)\cdot\left[\frac{k}{1+k}\right]^2. \tag{12}$$

The coefficient k is defined as $k = (g_{msu}/g_{mdl})$. Equation (12) is satisfied in all operation regions using the flicker noise model of (9) for the calculation of the P.S. D. $S_{i_{du}}, S_{i_{dl}}, S_{i_{d\_s}}$ and the transconductance expression (4) to evaluate k.

III. Measurements

Some noise measurements have been performed in MOS transistors covering all the regions of operation. Noise spectra were recorded with the aid of a Stanford Research SR560 low noise amplifier, and a Hewlett Packard HP3582A spectrum analyzer. To measure the drain

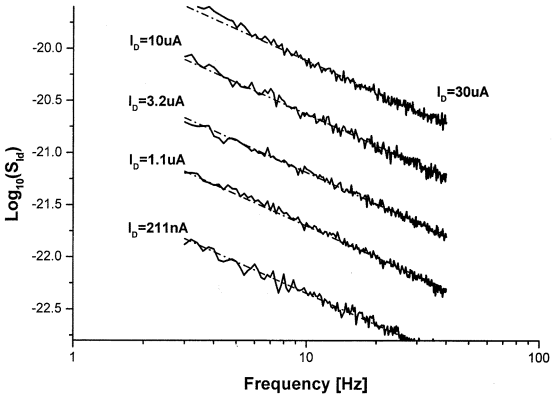

Fig. 2. Measured flicker noise spectra for a saturated NMOS transistor fabricated in a 2.4 μm process. $\mathrm{W/L} = 40\ \mu\mathrm{m}/12\ \mu\mathrm{m}$.

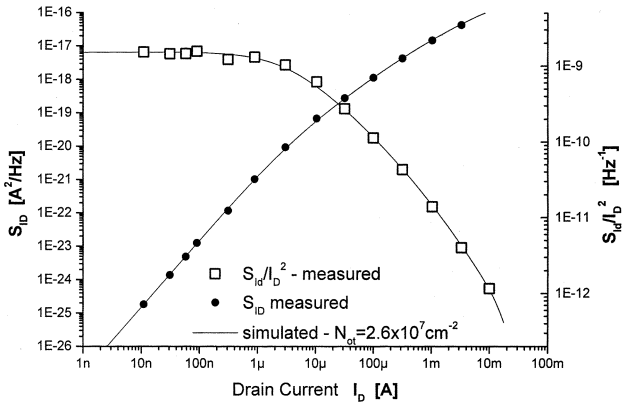

Fig. 3. Flicker noise P.S.D., and normalized P.S.D. S_{I_d}/I_D^2, at $\mathrm{f} = 1$ Hz for a saturated NMOS transistor $(\mathrm{W/L} = 200\ \mu\mathrm{m}/5\ \mu\mathrm{m})$.

current and fix the node voltages, a Hewlett Packard HP4155 Semiconductor Parameter Analyzer with the addition of *RC* filters for noise reduction was employed. In all cases the P.S.D. closely follows a $1/f$ dependence. This is consistent with the assumption $\gamma = 1$ associated with a uniform spatial distribution of the traps inside the oxide [4]. For the adjustment of the noise model, the measured noise spectra were acquired from 0.3 to 30 Hz because in this region, the P.S.D. is high enough to measure flicker noise particularly in weak inversion; we also avoid the effect of the ac line and its harmonics. Once acquired, every measured spectrum $S_{I_d}(f)$ is adjusted by means of least squares to (1) to obtain the value of K with $\gamma = 1$. Each estimated K value is used to a single point in Figs. 3–6; so in spite of the graphs show either S_{I_d} or S_{I_d}/I_D^2 at a frequency of 1 Hz, each point in the graphs represents information obtained over the whole frequency range of measurement. In Fig. 2 several measured frequency spectra are shown; each dashed line fits a measured spectrum, and corresponds to a single point in Fig. 6. For the calculation of the theoretical model, the charge densities $Q'_{IS(D)}$ were estimated with the aid of a circuit simulator and the ACM model [8] with typical parameters for the MOS transistor. The parameter N_{ot} of the model in (9) is adjusted to best fit the measurements in the logarithmic domain.

Figs. 3–4 show the simulation and measurements of flicker noise for an n-channel MOSFET of a 0.8 μm CMOS process. The transistor has an aspect ratio $\mathrm{W/L} = 200\ \mu\mathrm{m}/5\ \mu\mathrm{m}$. We chose a wide transistor in order to be able to comfortably characterize weak inversion operation. Fig. 3 covers all the operation regions for the saturated transistor, from weak to strong inversion; note here the plateau of the normalized P.S.D. S_{I_d}/I_D^2 in weak inversion. Fig. 4 was obtained for the transistor operating in strong inversion and in the linear region. In Fig. 5 the flicker noise is shown for a saturated p-channel transistor of the same technology and with the same aspect ratio. As in Fig. 3, is still possible to observe the plateau in weak inversion.

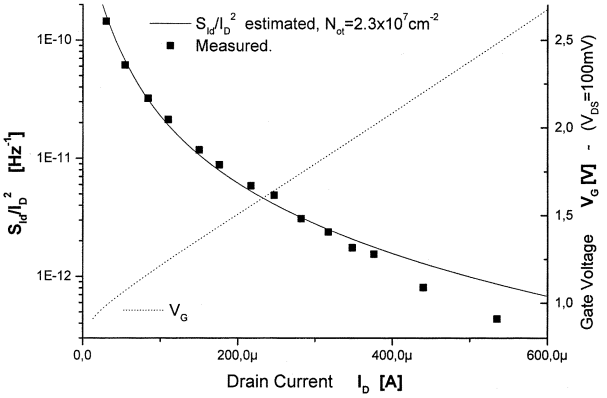

Fig. 4. Normalized P.S.D. S_{I_d}/I_D^2 at $\mathrm{f} = 1$ Hz for a NMOS transistor $(\mathrm{W/L} = 200\ \mu\mathrm{m}/5\ \mu\mathrm{m})$ in the linear region. Gate voltage $\mathrm{V_G}$ ranging up to 3 V with drain-to-source voltage $\mathrm{V_{DS}}$ fixed at 100 mV.

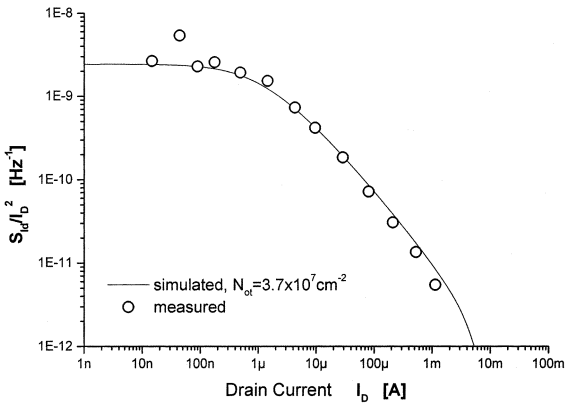

Fig. 5. Normalized P.S.D. S_{I_d}/I_D^2 at $\mathrm{f} = 1$ Hz for a saturated PMOS transistor $(\mathrm{W/L} = 200\ \mu\mathrm{m}/5\ \mu\mathrm{m})$.

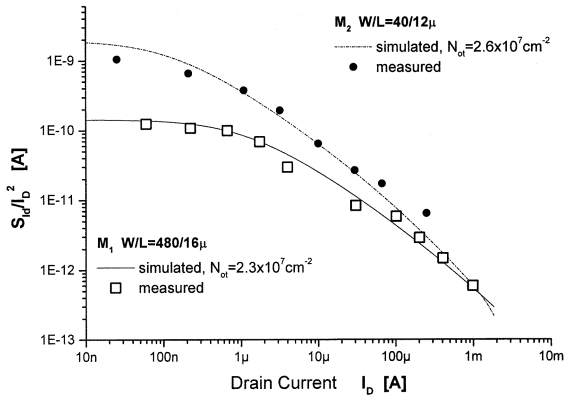

Fig. 6. Normalized P.S.D. S_{I_d}/I_D^2 at $\mathrm{f} = 1$ Hz for two saturated NMOS transistors fabricated in a 2.4 μm process.

Finally in Fig. 6, measurements and simulations of flicker noise for a $\mathrm{L_{min}} = 2.4\ \mu$m technology are also presented. In this case the measurements were performed for two NMOS transistors of different size. Once again the measurements show a good agreement with the model and the extracted N_{ot} value is similar to the values determined for the 0.8-μ process.

IV. Conclusion

A flicker noise model for long channel CMOS transistors, continuous in all the operation regions from weak to strong inversion has been developed. The new model is based on common physics hypotheses but we use a procedure to integrate the contribution to the transistor noise current of all the noisy elements in the channel that inherently preserves the series association properties of the model. With the aid of an advanced compact transistor model, this integration procedure results in a simple, single piece, and consistent model for flicker noise in MOS transistors.

Some measurements confirm that the presented model accurately represents the behavior of flicker noise under various bias conditions. Particularly, it has been observed that the normalized P.S.D. remains approximately constant in weak inversion and decays with the predicted slope as the transistor enters the strong inversion region, for both saturated PMOS and NMOS devices.

Although a compact model could hardly fit every transistor situation, we expect this work could help predict accurately and in a simple manner, the behavior of flicker noise from weak to strong inversion of nonminimum size transistors usually found in analog design.

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