Title: **MOSFET Threshold Voltage: Definition, Extraction, and some Applications**

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Abstract: This paper exploits a universal current-based definition of the threshold voltage (V_T) and discusses some direct methods to measure it. The consistency, accuracy, and sensitivity of the extraction procedures to second-order effects are examined through numerical simulations and experimental measurements. In addition to three procedures based on dc current measurements we propose an automatic V_T-extractor circuit which allows the direct determination of the threshold voltage with minimum influence of second-order effects.

Keywords: threshold voltage, MOSFET characterization, parameter extraction, threshold voltage extractor circuit

1 Introduction

The threshold voltage V_T of the MOSFET is a fundamental parameter in circuit design and testing, as well as in technology characterization, and should be used whatever the model adopted for the transistor. The classical definition of threshold, the gate voltage at which $\phi_s = 2\phi_F + V$, which links the surface (ϕ_s), the Fermi (ϕ_F), and the channel (V) potentials is indeed 'surface-potential-based'. Thus, even if a designer is using for circuit simulations a ϕ_s -based model of the transistor that does not explicitly use the threshold voltage as a parameter, he or she must be aware of its value.

V_T represents a physical change in the phenomenon that prevails in the current flow through the device as it goes from weak to strong inversion. Since this transition is very gradual, no specific point can be directly identified as the threshold voltage in the I_D vs. V_G characteristic. This is one of the reasons why many extraction methods of the threshold voltage have been presented in the literature [1]. Another reason is the sometimes poor modeling, since to accurately extract V_T it is essential that the model includes the drift and diffusion transport mechanisms, both important near the threshold condition. Extraction methods based solely on the strong (SI) or weak (WI) inversion models are inherently inaccurate since to determine the threshold voltage (which is

found between the SI and WI regions) experimental data are extrapolated from only one of these two operating regions.

This study is based on a universal threshold voltage definition for field-effect transistors. We begin by recalling this general threshold voltage definition (equality between the drift and diffusion components of the drain current) and compare it to the classical surface-potential-based definition.

We then describe three V_T-extraction procedures that can be applied to measured or simulated data. In the constant current (*CC*) method the MOSFET operates in the saturation region while in the g_{ch}/I_D and g_m/I_D methods the MOS transistor operates in the linear region. The consistency and accuracy of these methods are verified through numerical simulations using MOSFET long-channel models. Next we study how parasitic series resistance, carrier velocity saturation, channel-length modulation (CLM) and drain-induced barrier lowering (DIBL) affect each V_T-extraction method. Experimental results for V_T-extraction are then presented along with examples of applications of V_T measurements to quantify mismatch between transistors and in temperature sensing.

Finally, we present an automatic V_T-extractor circuit based on the g_{ch}/I_D procedure which allows the direct determination of V_T with minimum influence of CLM, DIBL, and carrier velocity saturation.

2 Current-based threshold definition and V_T-extraction methods

The weak inversion current in a MOSFET is essentially due to carrier diffusion, whereas the strong inversion current is mostly due to carrier drift, as shown in Fig. 1. At some point, the drift and diffusion components of the current are equal. Taking this point to define the threshold [2] allows a universal definition of threshold voltage, which can be applied even to intrinsic substrate MOSFETs [3] for which the classical definition of threshold based on the $2\phi_F$ potential drop is meaningless.

The current-based threshold definition is easily understood in the case of bulk MOSFETs, recalling the incrementally linear relationship between the inversion charge density Q_I' and the surface potential ϕ_s[2], [4]:

$$dQ_I' = (C_{ox}' + C_b')d\phi_s = nC_{ox}'d\phi_s \quad (1)$$

where C_{ox}' and C_b' are the oxide and depletion capacitances per unit area, respectively, and n is the slope factor. Since the drift current is proportional to

$$-Q'_I \frac{d\phi_s}{dx} = -\frac{Q'_I dQ_I'}{nC_{ox}' dx} \quad (2)$$

and the diffusion current is proportional to $\phi_t dQ_I'/dx$, both components are equal when $Q_I' = Q_{IP}' = -nC_{ox}'\phi_t$ [2]. x is the coordinate along the channel and Q_{IP}' is called the thermal charge density since it is the effective channel capacitance per unit area nC_{ox}' times the thermal voltage ϕ_t. For bulk MOS transistors there is a small difference, of the order of the thermal voltage ϕ_t, between the classical and the current-based threshold voltages, as shown in Table 1 [5]. Thus, if we are interested in the classical definition of threshold (in which case we must have n>1), we can easily correct the

value of the current-based threshold using Table 1. In the following we will focus only on the current-based definition of threshold.

2.1 Constant current (*CC*) procedure

The most direct procedure to extract the current-based threshold voltage is the CC method. In effect, for a saturated long-channel transistor (i_r = 0) the drain current is $3I_S$ (i_f =3) and V_P=V_S when the inversion charge density at the source equals Q'_{IP}, as can be easily verified from equations (3)-(6) in Table 2. Thus, when biasing a MOSFET in the diode connection with a constant drain current (I_D=3I_S) (Fig. 2), we have $V_G = V_T$ for V_S = 0.

The procedure is similar to that of the CC method widely used in industry, but in our case the bias current is related to a specific inversion charge density (the thermal charge density). However, the procedure has two drawbacks. Firstly, we must measure or estimate the value of I_S before the method is applied. I_S can be estimated from equation (4); even though (4) gives a rough approximation of I_S, it has been shown in [6] that the sensitivity of the extracted V_T with respect to the bias current $3I_S$ is low. Secondly, the transistor operates in the saturation region, where short-channel effects interfere with the value of the measured threshold voltage. To circumvent these two drawbacks the g_m/I_D procedure was introduced.

2.2 g_m/I_D procedure

The transconductance-to-current ratio g_m/I_D given by

$$\frac{g_m}{I_D} = \frac{1}{I_D}\frac{dI_D}{dV_G} = \frac{g_{ms} - g_{md}}{nI_D} = \frac{2}{n\phi_t(\sqrt{1+i_f}+\sqrt{1+i_r})} \quad (8)$$

can be easily obtained from equations (3)-(5). In the linear region ($i_f \cong i_r$) (8) reduces to

$$\frac{g_m}{I_D} \cong \frac{1}{n\phi_t\sqrt{1+i_f}}. \quad (9)$$

Thus, if we neglect the variation of the slope factor *n* with the gate voltage, the channel is under the threshold condition ($i_r \cong i_f = 3$) when the transconductance-to-current ratio g_m/I_D is at half its maximum value. Consequently, we have a direct method that allows us to determine the threshold voltage and the specific current from the g_m/I_D curve in the linear region.

The effect of a non-zero drain-to-source voltage can be included to improve the accuracy. For V_{DS}=ϕ_t/2 and i_f=3 we obtain i_r=2.12 from eq. (6). For this value of i_r, V_T is the gate voltage for which g_m/I_D=0.531*$(g_m/I_D)_{max}$ and I_S =1.136 *I_D.

The circuit configuration for the g_m/I_D procedure is shown in Fig. 3. The transconductance-to-current ratio (g_m/I_D) is extracted as a function of the gate voltage for a constant $V_{DS} = \phi_t/2$. Figure 4 shows the determination of I_S and V_T from the I_D vs. V_G and g_m/I_D vs. V_G curves.

2.3 g_{ch}/I_D procedure

The main drawback of the g_m/I_D method is the variation in the slope factor with V_{GB}. In order to avoid this drawback we can determine the threshold voltage at constant gate-to-substrate voltage and low drain-to-source voltage. The circuit configuration used to determine the channel conductance-to-current ratio g_{ch}/I_D in the linear region is shown in Fig. 5. The drain current (I_D) at a constant drain-to-source voltage ($V_{DS}=\phi_t/2$) is measured as a function of the source voltage (V_S).

For the circuit in Fig. 5, the variation of the drain current is:

$$\Delta I_D = -g_{ms}\,\Delta V_S + g_{md}\,\Delta V_D \quad (10)$$

where g_{ms} and g_{md} are the source and drain transconductance, respectively.

Since in our case $\Delta V_D = \Delta V_S$, we can calculate the channel conductance-to-drain current ratio from equations (3) and (5) as

$$\frac{g_{ch}}{I_D} = -\frac{1}{I_D}\frac{dI_D}{dV_S} = \frac{2}{\phi_t(\sqrt{1+i_f}+\sqrt{1+i_r})} \quad (11)$$

For $V_{DS} \ll \phi_t$, $i_f \cong i_r$ and (11) becomes

$$\frac{g_{ch}}{I_D} = \frac{1}{\phi_t(\sqrt{1+i_f})} \qquad (12)$$

Thus, as in the previous case, for i_f=3 the channel conductance-to-current ratio is one-half of the peak value $1/\phi_t$. In order to account for the error introduced by $V_{DS}=\phi_t/2$, we use Eq. (6) to calculate the value of i_r, which equals 2.12. Substituting these values (i_f=3 and i_r=2.12) in (11) we find $g_{ch}/I_D=0.531/\phi_t$. At this point of the g_{ch}/I_D curve, $V_S = V_P$ and I_S =1.136 *I_D, as can be easily verified using equations (3), (5), and (6).

Finally, V_T is the gate voltage at which the condition V_P = 0 holds (see Eq. (7)). The points on the I_D and g_{ch}/I_D curves that are used to determine I_S and V_T are presented in Fig. 6.

Comparing (9) and (12), we note that the advantage of the extraction method based on the channel conductance over that based on the gate transconductance is that the former is independent of the slope factor (body factor) since V_{GB} is kept constant during the measurement.

Important characteristics related to the g_m/I_D, g_{ch}/I_D, and *CC* extraction methods are summarized in Table 3. The *CC* method is, in principle, the simplest one; however, the transistor operates in the saturation region. Therefore, the *CC* method is more sensitive to second-order effects (*e.g.* DIBL, CLM and velocity saturation).

The g_{ch}/I_D and g_m/I_D methods are similar, but the drawback of the g_m/I_D method is the influence of the variation in the slope factor on the determination of V_T.

3 Consistency of current-based methods for the extraction of V_T

In order to verify the consistency and accuracy of the V_T-extraction methods, numerical simulations were carried out using charge-based and surface-potential-based long-channel transistor models. Details of the models are given in the Appendix.

The consistency of a V_T-extraction method can be checked through simulation of the extraction circuit using a long-channel MOSFET model. Consistency means that the extracted value of V_T must be very close to the V_T calculated from the model parameters.

Numerical simulations were carried out using the MATLAB software and technological parameters from a generic 0.18µm CMOS process (acceptor doping concentration N_A=2.3E+17 cm^{-3}; gate oxide thickness t_{ox}=4.5nm; low field mobility μ_0 =264cm^2/V.s and flat-band voltage V_{FB}=-0.9V). A long-channel NMOS transistor (W/L=2µm/2µm) at a temperature of 27°C was employed. The equilibrium threshold voltage (V_{TO}) for this process, calculated from (A2), is 386.4mV.

From Fig. 7 we note that the g_{ch}/I_D characteristics using Q_I'-based and ϕ_s-based models are very close to each other. The V_T values using the g_{ch}/I_D procedure are 386.5mV and 384.8mV for Q_I'-based and ϕ_s-based models, respectively. These V_T values are very close to the expected value of threshold voltage (V_{TO}=386.4mV), especially for the charge-based model.

The extracted values using the g_m/I_D, g_{ch}/I_D, and *CC* methods are presented in Table 4. The three methods have consistent and accurate results which differ from the expected value by no more than 2.6mV.

4 Influence of second-order effects

In this section, the influence of second-order effects, namely channel-length modulation (CLM), velocity saturation (v_{sat}), series resistance, and drain-induced barrier lowering (DIBL), on the V_T-extraction methods is investigated through electrical simulations.

The procedure adopted in this study consists of changing a specific set of input parameters to make the influence of a certain phenomenon negligible and then analyzing the difference in the outcome. For instance, if we change the default value of the velocity saturation parameter (v_{sat}) to a much greater value, the effect of velocity saturation becomes negligible. In this way, we can verify whether the velocity saturation phenomenon has any impact on the result obtained with the V_T-extraction method.

4.1 V_T extraction for a 0.35µm CMOS process

The parameters for the electrical simulations (BSIM3v3) are taken from a 0.35µm CMOS process. Four sets of input parameters were used to study the impact of second-order effects. The list of models and the input parameters that have been changed are presented in Table 5 [7]. All simulations were performed using the Spectre simulator (version 7.2). The results for a short-channel NMOS transistor (W/L=16µm/0.4µm) are presented in Fig. 8.

For a MOS transistor operating in the linear region, both drain and source series resistance can affect the outcome of the extraction methods. On the other hand, for a transistor in saturation the drain series resistance has no significant effect on the electrical behavior of the transistor. For these reasons, the *CC* method, which uses the transistor in saturation and with a current level comparable to that of the g_m/I_D and g_{ch}/I_D methods (which operate in the linear region), is less affected by parasitic resistances (Fig. 8).

As shown in Fig. 8, the effects of channel-length modulation and saturation velocity are more important in the *CC* method because the transistor operates in the saturation region.

DIBL is strongly dependent on both the drain voltage and the channel length. Therefore, the *CC* method, in which $V_{DS}=V_T$, is more affected by DIBL than the g_m/I_D and g_{ch}/I_D methods (Fig. 8).

The *CC* method is the procedure most affected by second-order effects with a maximum V_T variation of 2.7mV. On the other hand, the g_m/I_D and g_{ch}/I_D methods present very similar behavior and are less sensitive to second-order effects with a maximum V_T variation of 1mV.

It is worth mentioning that the impact of DIBL, CLM, v_{sat} and series resistance on the extraction method is considerably reduced for long-channel devices.

The V_T values extracted from the g_m/I_D, g_{ch}/I_D and constant current methods are shown in Fig. 9. In this figure, we can see that the V_T values obtained with these methods present similar behavior; in particular the g_m/I_D and g_{ch}/I_D methods give close values for the extracted V_T. Also, we can observe that the difference between the V_T values extracted applying the different methods is clearly reduced for long-channel devices due to the smaller impact of second-order effects on the extraction methods.

4.2 V_T extraction for a 90 nm CMOS process

The V_T values extracted from the g_m/I_D, g_{ch}/I_D and constant current methods as a function of the channel length for a 90nm CMOS process are shown in Fig. 10, where the roll down of the V_T of the transistors with the shortest channel length is clear.

As shown in Table 6, the g_m/I_D and g_{ch}/I_D methods are insensitive to second-order effects presenting a maximum V_T variation of the order of 1mV. On the other hand, the impact of DIBL, CLM and v_{sat} in the constant current method is really large (20-40 mV variations) for the 90nm CMOS.

5 Applications

The threshold voltage is a fundamental electrical parameter used in technology characterization, aging evaluation, matching assessment, and in temperature and radiation sensors.

As an example of matching assessment, 20 matched NMOS transistors were measured and the V_T was extracted using the g_m/I_D and *CC* methods. Figure 11 shows that the two methods present very close results as regards the deviation of each sample with respect to the average value. The *CC* method is of considerable interest because it is very simple and rapid. In fact, the *CC* method can be used as a V_T extractor circuit for tracking the V_T variation as a function of a specific parameter, *e.g.* temperature or ionizing radiation.

An example of the use of the *CC* method for temperature sensing is presented in Fig. 12. In this figure we can see that the thermal coefficient of V_T is approximately -0.9mV/°C. It is important to note that the specific current is slightly dependent on temperature (see equation (4) in Table 2), through ϕ_t and μ, and, to a lesser extent, n. Thus, the bias current was forced to track the variation of I_S, which was determined for

each temperature through electrical simulation. In a more practical realization, I_S can be generated by means of a specific current (I_S) generator, as described in [8].

6 Automatic V_T-extractor circuit

An automatic V_T-extractor based on the g_{ch}/I_D method is shown in Fig. 13. In order to test the accuracy and feasibility of this circuit, a prototype was built using a commercial integrated circuit (OPA2340) as the operational amplifier. The biasing signals (I_D=0.88*I_S and V_D= ϕ_t/2) were generated by a semiconductor parameter analyzer (Agilent 4156C). The experimental results for an NMOS transistor (W/L=16μm/2μm – in a 0.35μm CMOS process) using this V_T-extractor circuit and the g_{ch}/I_D method are presented in Table 7.

It should be noted that this circuit can be fully integrated. The biasing signals (I_D *=0.88*I_S* and V_D=ϕ_t/2*)* can be generated using a self-cascode MOSFET (SCM) (Fig. 14). In the SCM, the voltage V_x at the intermediate node is proportional to absolute temperature while the reference current (I_{ref}) is proportional to I_S. Therefore, we can combine two SCMs to generate signals proportional to I_S and ϕ_t. An example of an ultra-low-power self-biased current reference using the SCM can be found in [8].

The proposed V_T-extractor operates in moderate inversion and not in strong inversion as the previously reported circuits (see for example [9]- [12]). As a consequence, the new extractor circuit is suitable for low-power and low-voltage applications and additionally provides an accurate measurement of V_T insensitive to second-order effects.

7 Subthreshold I-V characteristic: experimental vs. modeled values

The drain current in weak inversion can be expressed as [5]

$$I_D = n\mu_0 C_{ox}^{'} \frac{W}{L} \phi_t^2 e^{\left(\frac{V_G - V_T}{n\phi_t} + 1\right)} \left(1 - e^{\frac{-V_{DS}}{\phi_t}}\right) \quad (13)$$

Thus, we can compare the drain current measured experimental with that of equation (13). For this comparison, we extracted from the experiment the values of μ_0, n, and V_T (from the automatic V_T-extractor circuit of Fig.13). Figure 15 shows that the difference between the values obtained using (13) and the measured drain current is no greater than 5% for deep weak inversion over three decades of current. It should be noted that the difference between fitting curve and the experimental data increases for higher gate voltages due to a closer approximation to the moderate inversion regime, where the exponential model starts to collapse.

8 Conclusions

This work extends that of [13] in the study of the g_m/I_D, g_{ch}/I_D, and *CC* extraction methods of the MOSFET threshold voltage using experimental results and numerical simulations. Numerical evaluation and measurements carried out using long-channel models showed that the three extraction procedures are self-consistent. Also, it is shown that the g_{ch}/I_D and g_m/I_D methods, which use the transistor in the linear region, are relatively insensitive to short-channel effects (DIBL, CLM and velocity saturation).

The g_{ch}/I_D procedure has two important advantages over the g_m/I_D method. Firstly, the g_{ch}/I_D procedure is independent of the variation in the slope factor and, secondly, we can build a simple low-power V_T-extractor circuit based on this method.

Finally, it is important to remark that, as shown in this study, the threshold voltage extraction procedures reviewed here can be applied to most of the MOSFET models, including BSIM 3, BSIM 4 and surface-potential-based models.

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Appendix

In the charge ($Q_I^{'}$)-based Advanced Compact MOSFET (ACM), the drain current is given by [5]:

$$I_D = \frac{\mu W}{L}\left[\frac{Q_{IS}^{'2} - Q_{ID}^{'2}}{2nC_{ox}^{'}} - \phi_t(Q_{IS}^{'} - Q_{ID}^{'})\right] \text{(A1)}$$

where $Q_{IS}^{'}$ and $Q_{ID}^{'}$ are the inversion charge per unit of area at the source and drain terminals, respectively. In the ACM model, the current-based threshold voltage V_{TO} in terms of the technological parameters is given by

$$V_{TO} = V_{FB} + 2\phi_F + \phi_t\left[1 + \ln\left(\frac{n}{n-1}\right) + \gamma\sqrt{2\phi_F + \phi_t \ln\left(\frac{n}{n-1}\right)}\right] \text{(A2)}$$

where V_{FB} is the flat-band voltage, ϕ_F is the Fermi potential and γ is the body effect factor $\gamma = \sqrt{2q\varepsilon_s N_A / C'_{ox}}$, N_A being the concentration of dopants and ε_s the silicon permittivity.

The consistency of a V_T-extraction method can be checked using a long-channel MOSFET model since the extracted value of V_T must be very close to V_{TO}.

The Brews' $\phi_s -$ based model is given by the following set of equations [14]

$$I_D = I_{drift} + I_{diff} \text{ (A3)}$$

$$I_{drift} = \frac{\mu W}{L} C'_{ox}\left[(V_{GB} - V_{FB})(\phi_{sL} - \phi_{s0}) - \frac{1}{2}(\phi_{sL}^2 - \phi_{s0}^2) - \frac{2}{3}\gamma\left[(\phi_{sL} - \phi_t)^{3/2} - (\phi_{s0} - \phi_t)^{3/2}\right]\right] \text{(A4)}$$

$$I_{diff} = \frac{\mu W}{L} C_{ox}^{'} \phi_t\left[(\phi_{sL} - \phi_{s0}) + \gamma\left[\sqrt{\phi_{sL} - \phi_t} - \sqrt{\phi_{s0} - \phi_t}\right]\right] \text{(A5)}$$

where ϕ_{sL} and ϕ_{s0} are the surface potential at drain and source, respectively.

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Vitae

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Figures

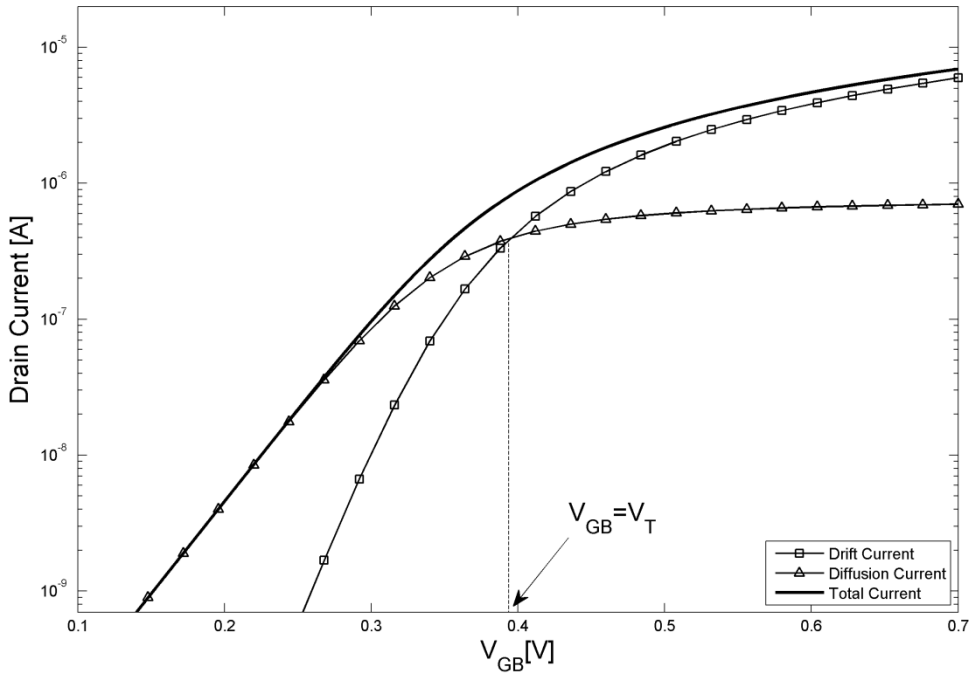

Figure 1: Drain current and its diffusion and drift components vs. gate voltage for a MOSFET operating in the linear region with V_{DS}=ϕ_t/2=13mV.

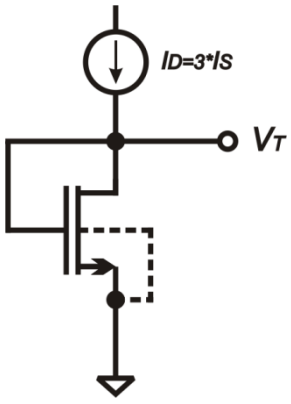

Figure 2: Common source circuit driven by a constant current source of $3I_S$.

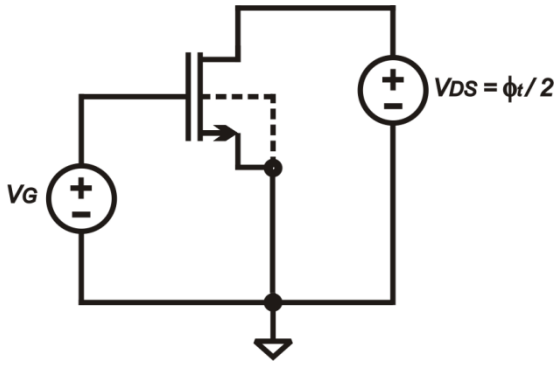

Figure 3. Circuit configuration for measuring the g_m/I_D characteristic in the linear region

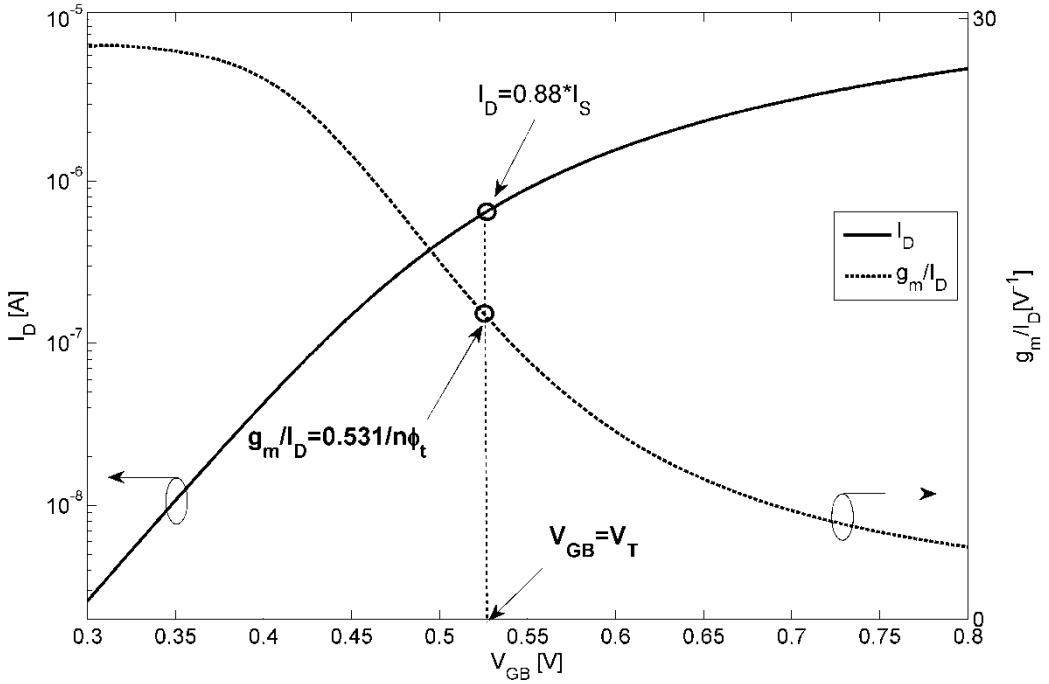

Figure 4. Experimental measurements of I_D and g_m/I_D as a function of V_G for the circuit in Fig. 3. The circles on the g_m/I_D and I_D plots were used to extract the values of V_T (=525mV) and I_S (=0.72μA) for an NMOS transistor (W/L=16μm /2μm) in a 0.35μm CMOS process.

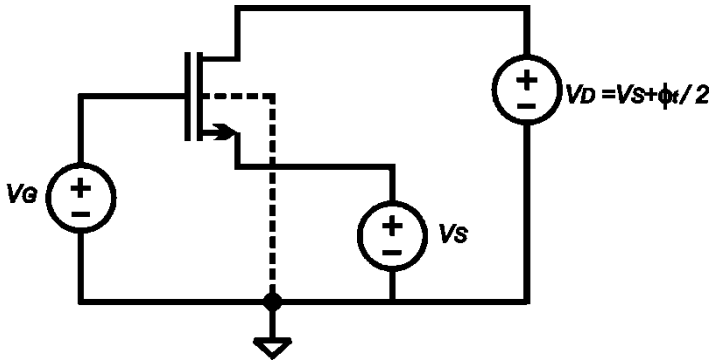

Figure 5. Circuit configuration for measuring the g_{ch}/I_D characteristic in the linear region.

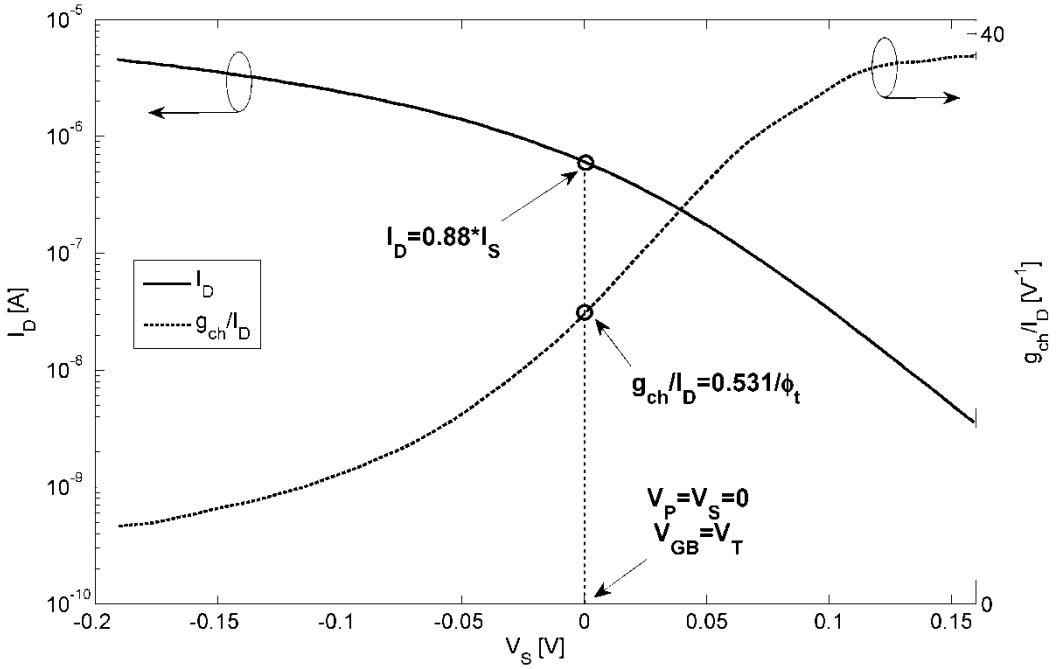

Figure 6. Experimental measurements of I_D and g_{ch}/I_D characteristics as a function of V_S for the circuit presented in Fig. 5. The extracted values are V_T=522mV and I_S=0.697μA for an NMOS transistor (W/L=16μm/2μm) in a 0.35μm CMOS technology. In this case, the value of the gate voltage is equal to the threshold voltage since $g_{ch}/I_D=0.531/\phi_t$ for V_S=0.

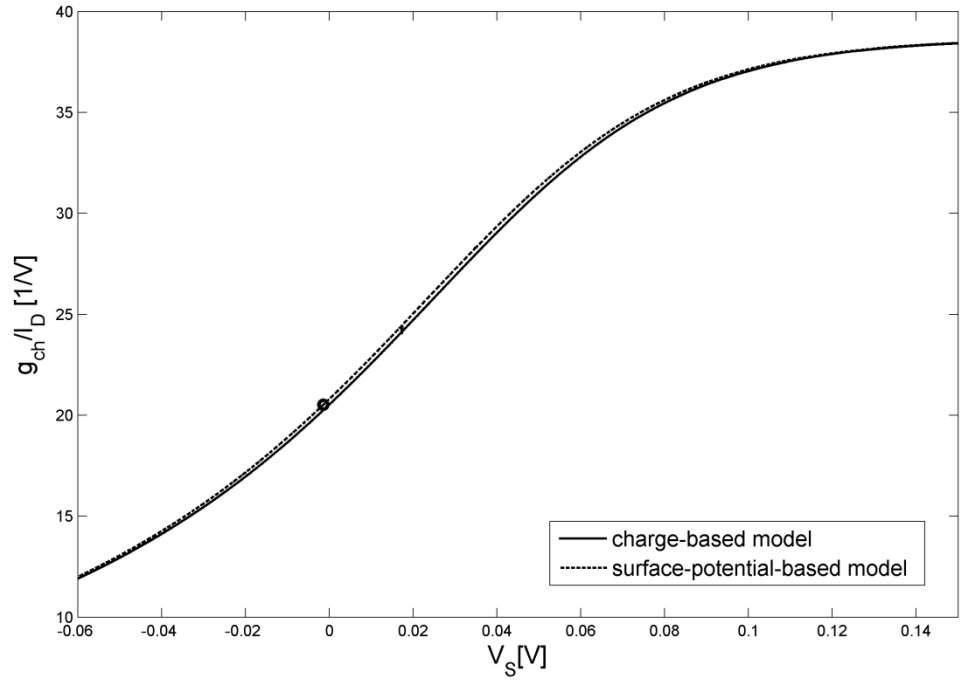

Figure 7. g_{ch}/I_D characteristics for an NMOS transistor (W/L=2μm/2μm – Generic 0.18μm CMOS process) using charge-based and surface-potential-based MOSFET long-channel model. The circle indicates the point where $g_{ch}/I_D=0.531/\phi_t$. The extracted V_T values are 386.5mV and 384.8mV for the charge-based and surface-potential-based models, respectively.

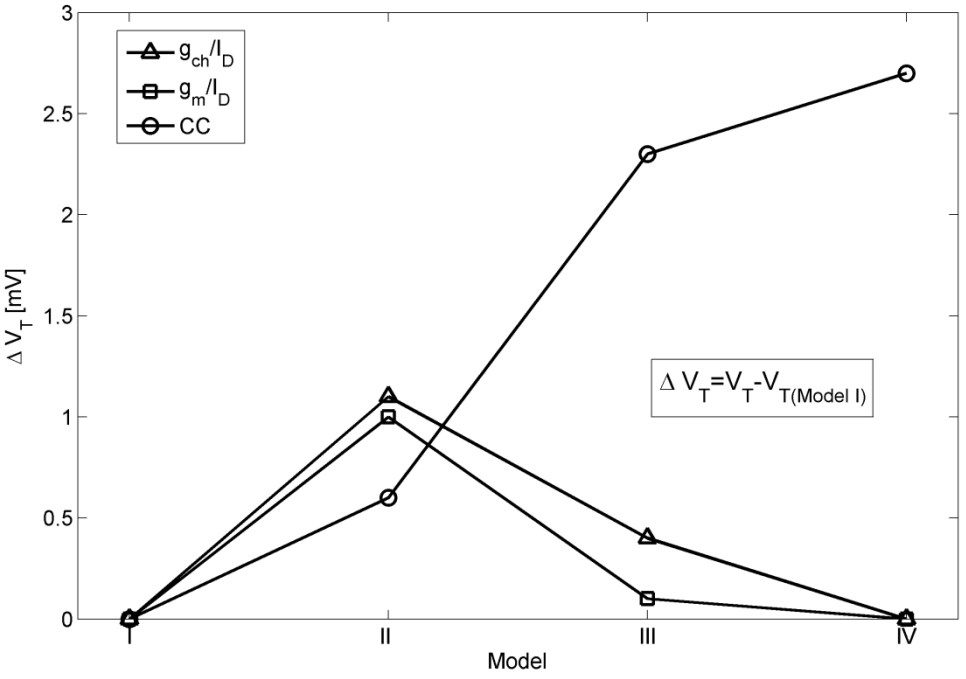

Figure 8. Variation of extracted V_T for g_{ch}/I_D, g_m/I_D and *CC* methods using different models for an NMOS (W/L=16μm /0.4μm) in a 0.35μm CMOS process. Model I refers to the original set of input parameters (BSIM3v3), model II disregards the effect of series resistance, in model III the effects of velocity saturation and CLM are negligible, and model IV has no DIBL effect.

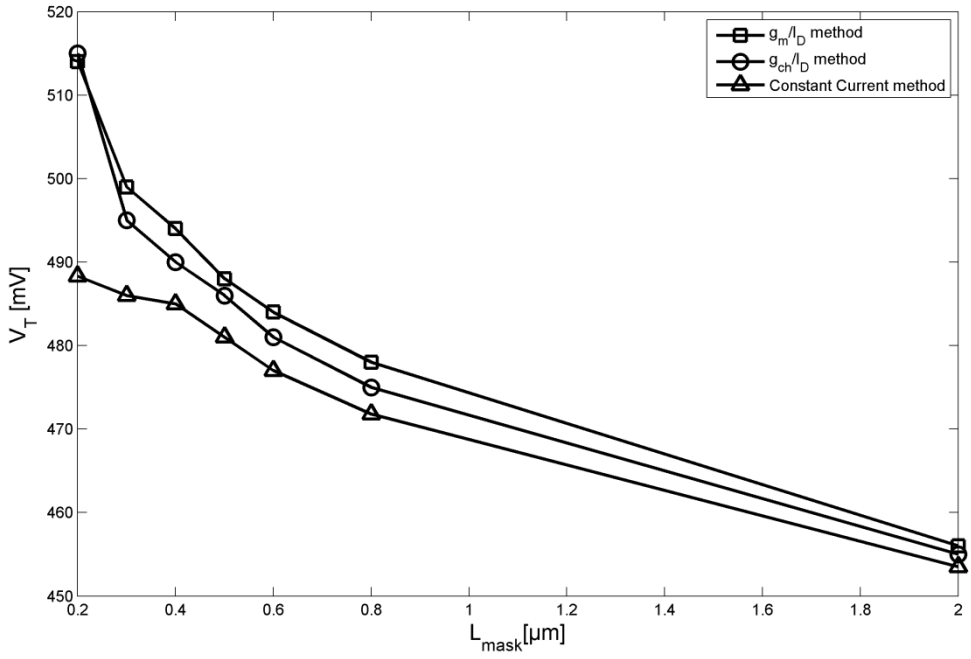

Figure 9. Measured V_T values vs. mask channel length (L_{mask}) for g_m/I_D, g_{ch}/I_D and constant current methods for NMOS transistors with L_{mask} ranging from 0.2µm to 2µm and W/L=100, in a 0.18µm CMOS technology.

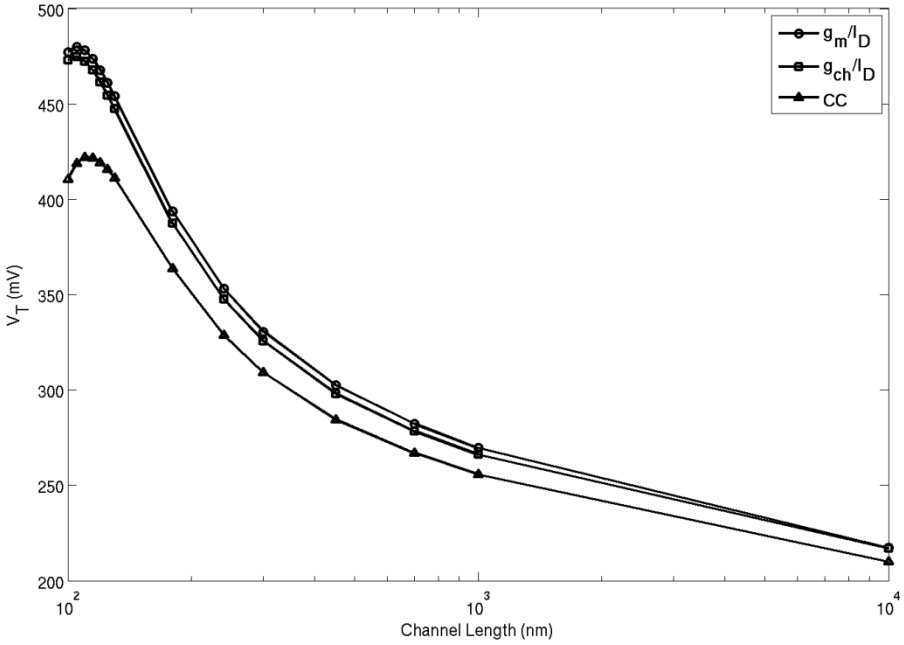

Figure 10. Extracted V_T values vs. channel length for g_m/I_D, g_{ch}/I_D and constant current methods for NMOS transistors with channel length ranging from 100nm to 10µm and W=120nm, in a 90nm CMOS technology.

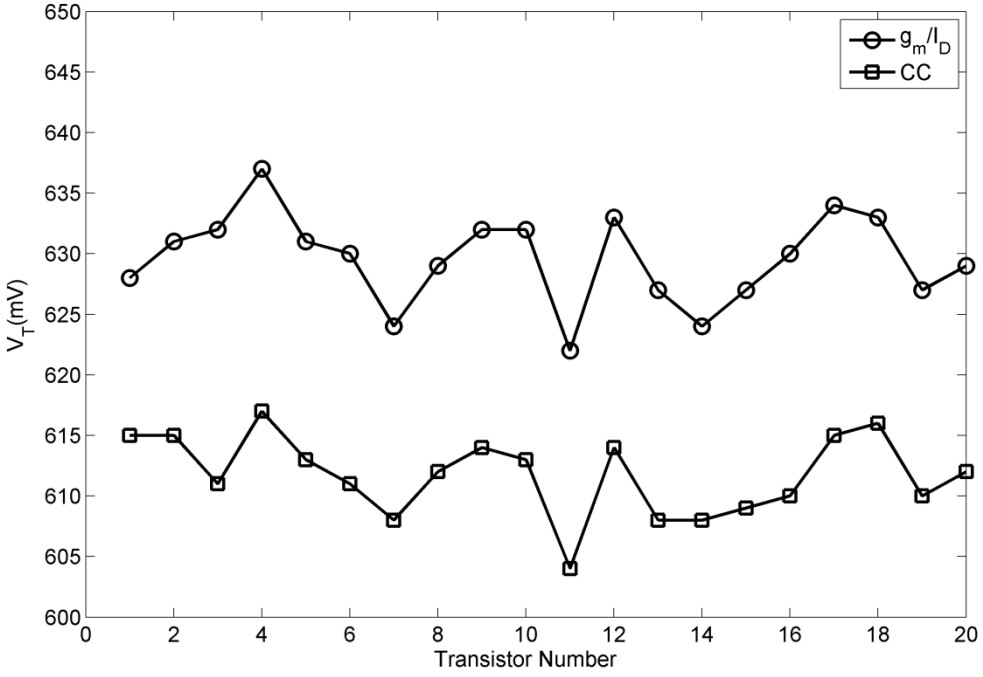

Figure 11. V_T measurements using g_m/I_D and constant current (*CC*) methods for 20 matched NMOS transistors (W=12µm and L=0.5µm – 0.35µm CMOS process) at room temperature. The V_T average values are 629mV (g_m/I_D) and 612mV (*CC*) and the relative standard deviations are 0.59% (g_m/I_D) and 0.54% (*CC*).

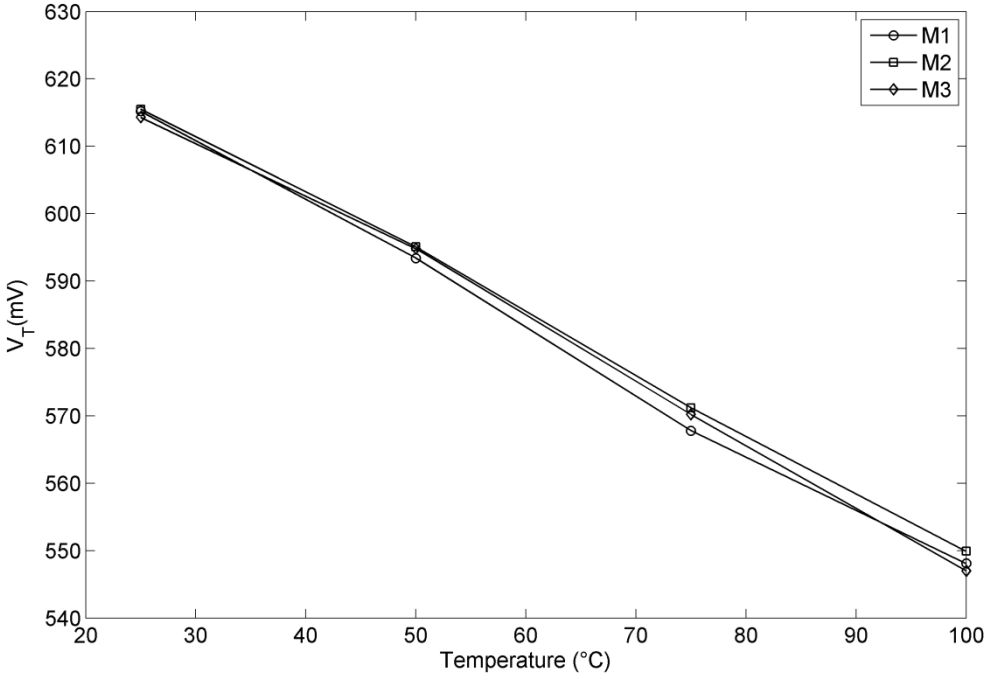

Figure 12. V_T measurements using constant current (*CC*) methods vs. temperature for 3 matched NMOS transistors (M1, M2, M3) with W=12µm and L=0.5µm in a 0.35µm CMOS process.

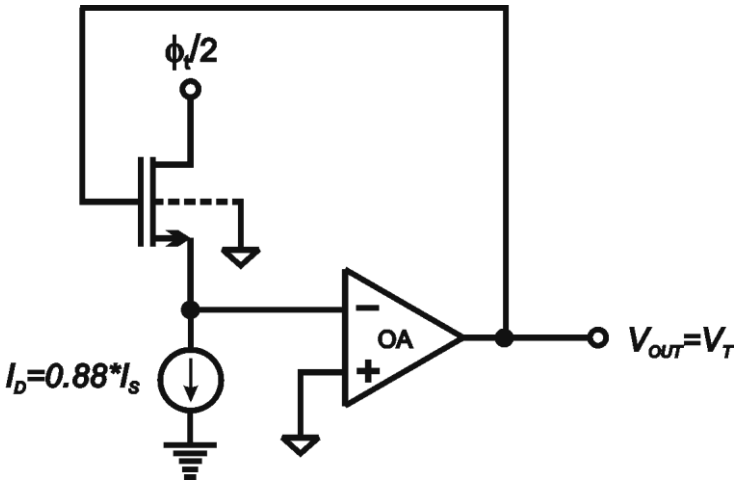

Figure 13. Schematic of an automatic V_T-extractor circuit based on the g_{ch}/I_D method. OA is a low-offset operational amplifier.

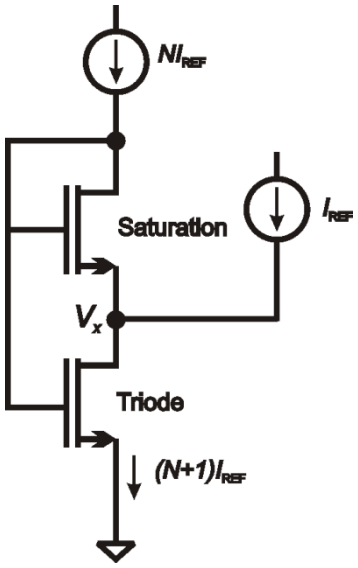

Figure 14. Schematic of the self-cascode MOSFET (SCM) connected in diode configuration [8].

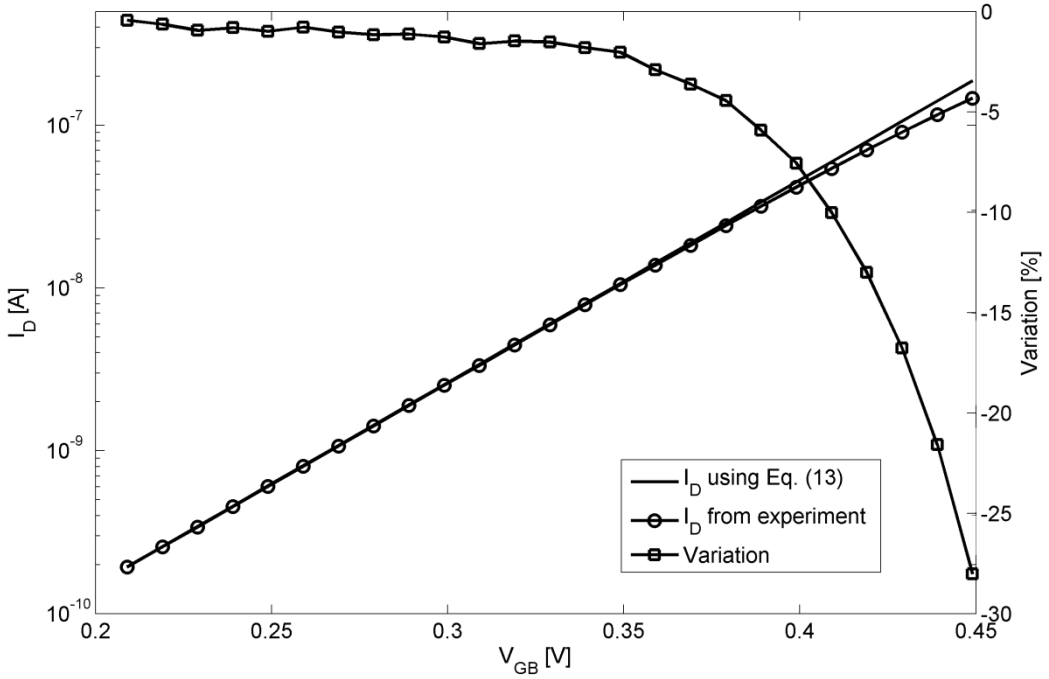

Figure 15. Comparison between the drain current values obtained from eq. (13) and experimental data for an NMOS (*W*/*L*=16μm/2μm – in a 0.35μm CMOS process). The drain current values are indicated on the left y-axis while the difference between the two values is presented on the right y-axis. The values for the extracted parameters used in (13) are n=1.35, V_T=526mV, and μ_0=482cm^2/V.s

Tables

Table 1: Classical and current-based threshold definitions [5].

Physical Meaning	**Value of ϕ_s at threshold**	**Value of Q_I' at threshold**	**Difference in V_T relative to the classical definition**
Surface concentration of electrons= bulk concentration of holes	$2\phi_F + V$	$-(n-1)C_{ox}'\phi_t$	0
Drift component = Diffusion component of drain current	$2\phi_F + V + \phi_t \ln\left(\frac{n}{n-1}\right)$	$-nC_{ox}'\phi_t$	$\phi_t\left[1 + n\ln\left(\frac{n}{n-1}\right)\right]$

Table 2: Long-channel MOSFET expressions [3]. I_S is the specific current, i_f is the forward normalized current, i_r is the reverse normalized current, μ is the mobility, W is the channel width, and L is the channel length.

Variable	Expression
Drain current	$I_D = I_F - I_R = I_S(i_f - i_r)$ (3)
Specific current	$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2}\frac{W}{L}$ (4)
Source (drain) transconductance	$g_{ms(d)} = -\mu \frac{W}{L} Q'_{IS(D)} = \frac{2I_S}{\phi_t}\left(\sqrt{1+i_{f(r)}} - 1\right)$ (5)
Source (drain)-to-bulk voltage (Unified current control model (UICM))	$V_P - V_{S(D)} = \phi_t\left[\sqrt{1+i_{f(r)}} - 2 + \ln\left(\sqrt{1+i_{f(r)}} - 1\right)\right]$ (6)
Pinch-off voltage	$V_P \cong \frac{V_G - V_T}{n}$ (7)

Table 3. Characteristics of the g_m/I_D, g_{ch}/I_D and constant current extraction methods.

Method	Operating region	$I_D@V_{GB}=V_T$	V_{DS}
g_{ch}/I_D	Linear	$0.88*I_S$	$\phi_t/2$
g_m/I_D	Linear	$0.88*I_S$	$\phi_t/2$
Constant current	Saturation	$3*I_S$	V_T

Table 4. Extracted V_T values using g_m/I_D, g_{ch}/I_D and *CC* methods for Q'_I-based and ϕ_s-based long-channel models. V_{TO} (=386.4 mV) is the threshold voltage calculated from (A2).

Method		Q'_I-model	ϕ_s-model
g_{ch}/I_D	V_T (mV)	386.5	384.8
	$\Delta V = V_T - V_{TO}$	0.1mV	-1.6mV
g_m/I_D	V_T (mV)	389.0	387.5
	$\Delta V = V_T - V_{TO}$	2.6mV	1.1mV
CC	V_T (mV)	387.8	386.8
	$\Delta V = V_T - V_{TO}$	1.4mV	0.4mV

Table 5 – Characteristics of the models, with the list of changed input parameters, used to study the impact of second-order effects on the V_T-extraction methods.

Model	Input parameter changed
I – complete model	none
II – without series resistance	rsh, rdsw
III – without velocity saturation and CLM	vsat, pclm
IV – without DIBL	pdiblcb, pdiblcl, pdiblc2, eta0, etab, dsub

Table 6- Difference between the V_T extracted either using the complete model (original set of parameters of BSIM4) or the V_T extracted with the complete model in which short-channel effects are eliminated one at a time (or both CLM and v_{sat} effects are eliminated). The g_{ch}/I_D, g_m/I_D and *CC* methods are applied to an NMOS transistor (W/L=120nm /100nm) in a 90nm CMOS process.

Method	Model disregarding DIBL effect	Model disregarding CLM effect	Model disregarding v_{sat} effect	Model disregarding CLM and v_{sat} effects
g_m/I_D	0.7mV	0.8 mV	1.1mV	0.9mV
g_{ch}/I_D	*	0.9mV	1.1mV	1.3mV
CC	22.9mV	40.6mV	20.9mV	39.6 mV

* The simulation could not be run using the g_{ch}/I_D method because of the discontinuity in the g_{ch}/I_D characteristic around V_{DS}=0V when the DIBL was eliminated.

Table 7 – Experimental results for an NMOS transistor (W/L=16μm/2μm – in a 0.35μm CMOS process) using the V_T-extractor circuit presented in Fig. 13 and the g_{ch}/I_D method.

Transistor	g_{ch}/I_D method	V_T-extractor circuit
NMOS (W/L=16μm/2μm)	522mV	526mV