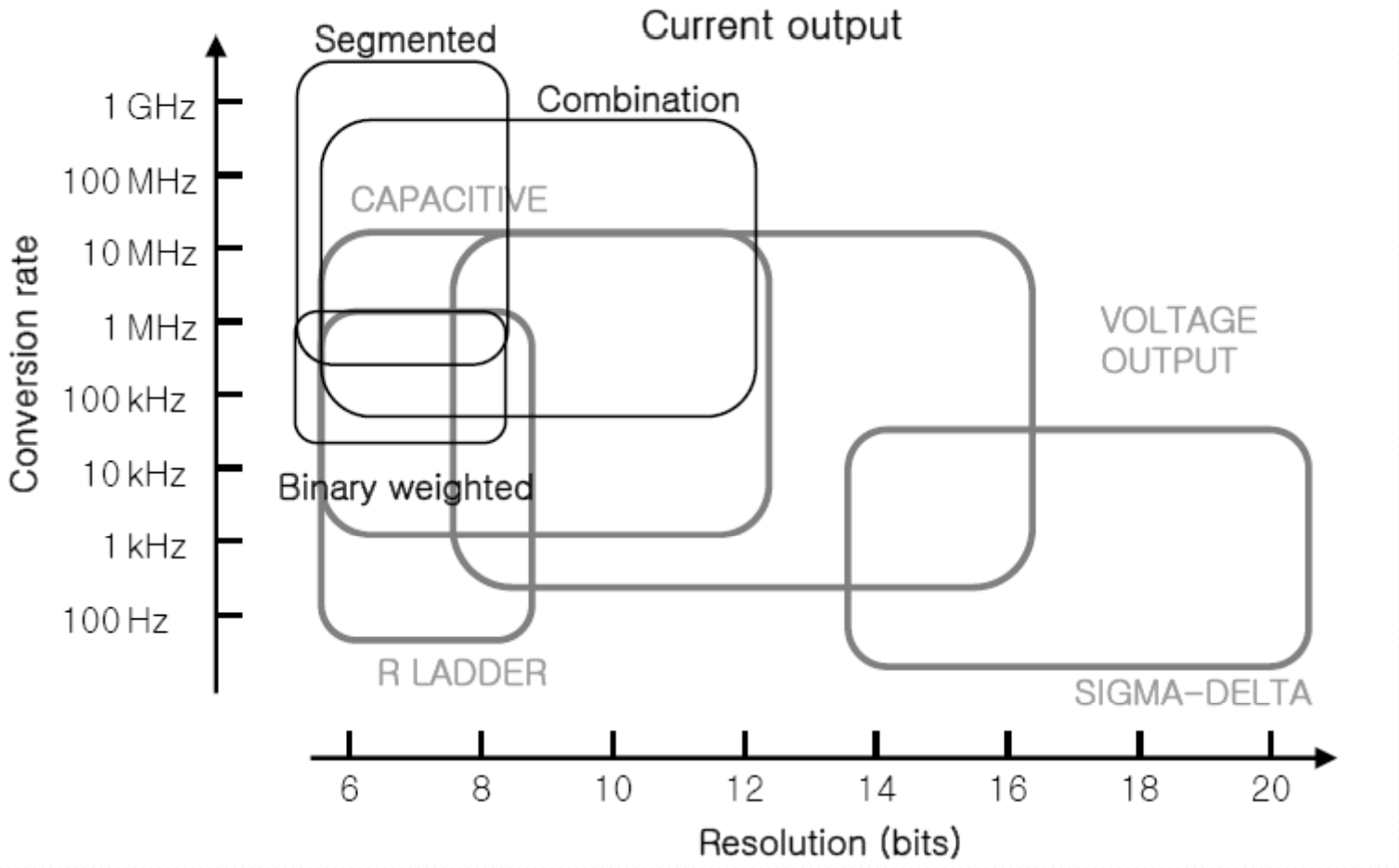
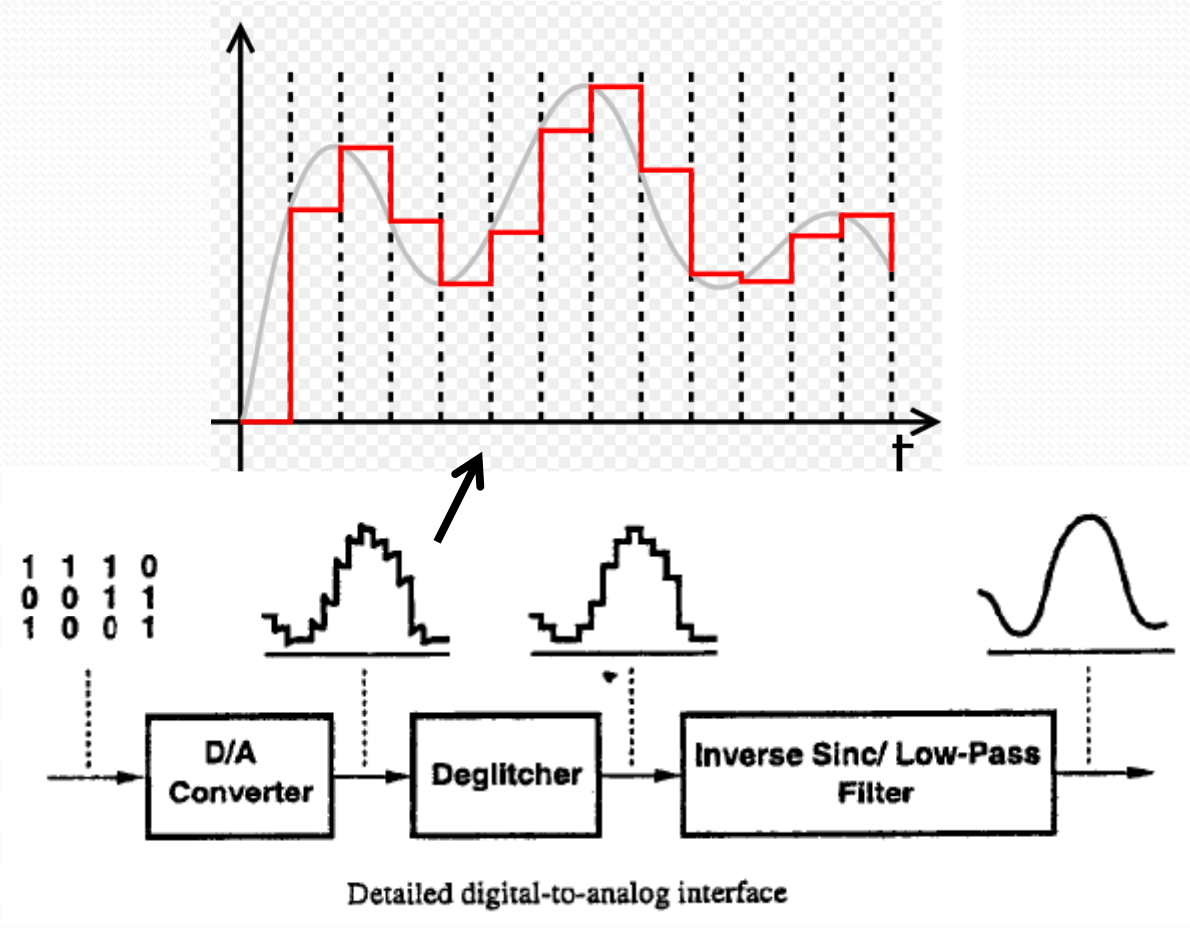
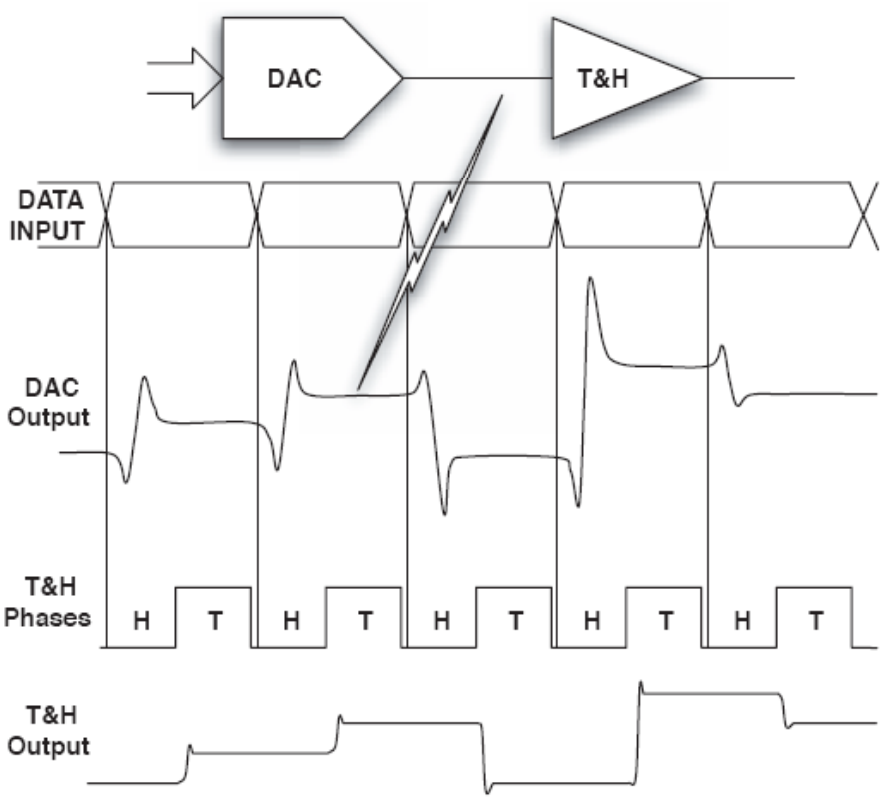
D/A Converters





Detailed digital-to-analog interface

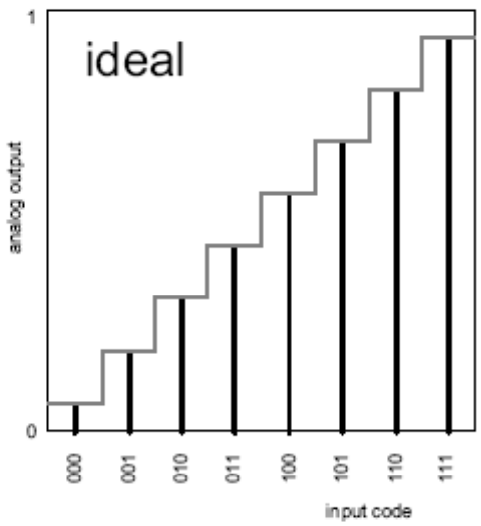
Deglitching

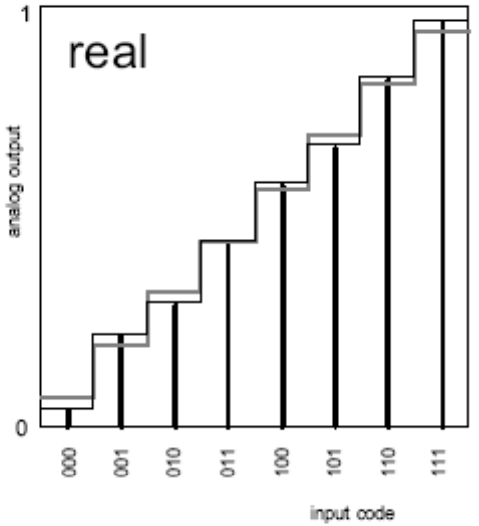


Deglitch circuit and possible voltages.

Static transfer characteristic

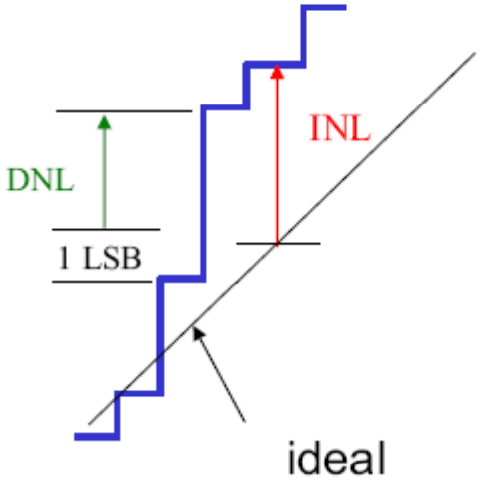
D to A converters

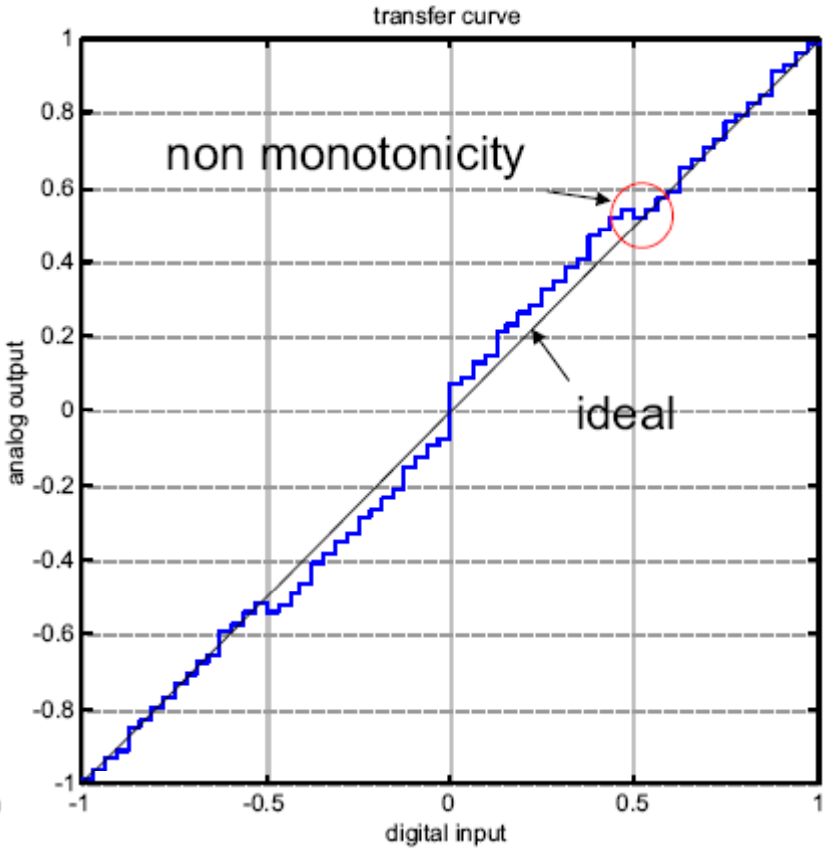




Linearity characterization

- D to A converters

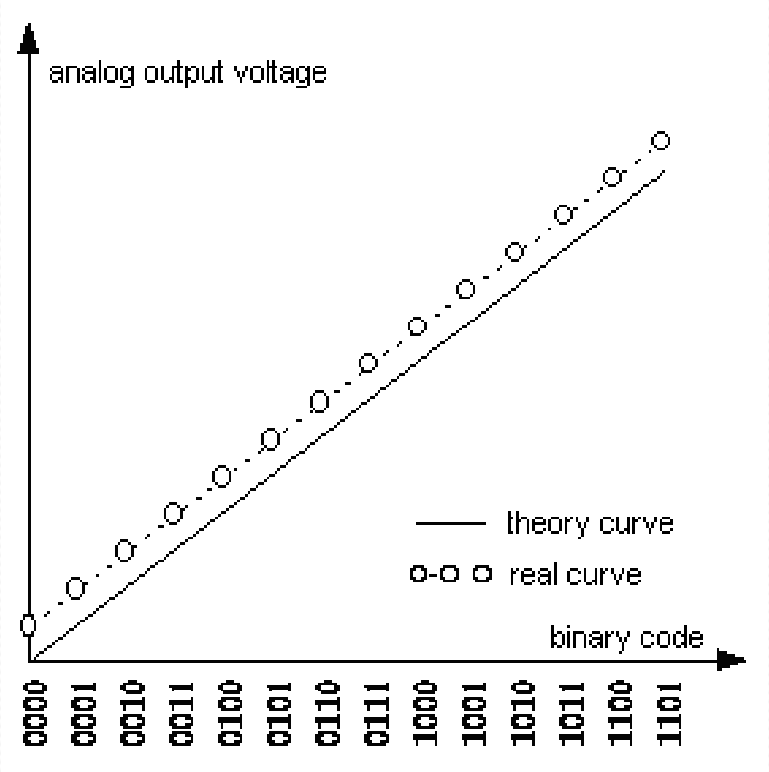


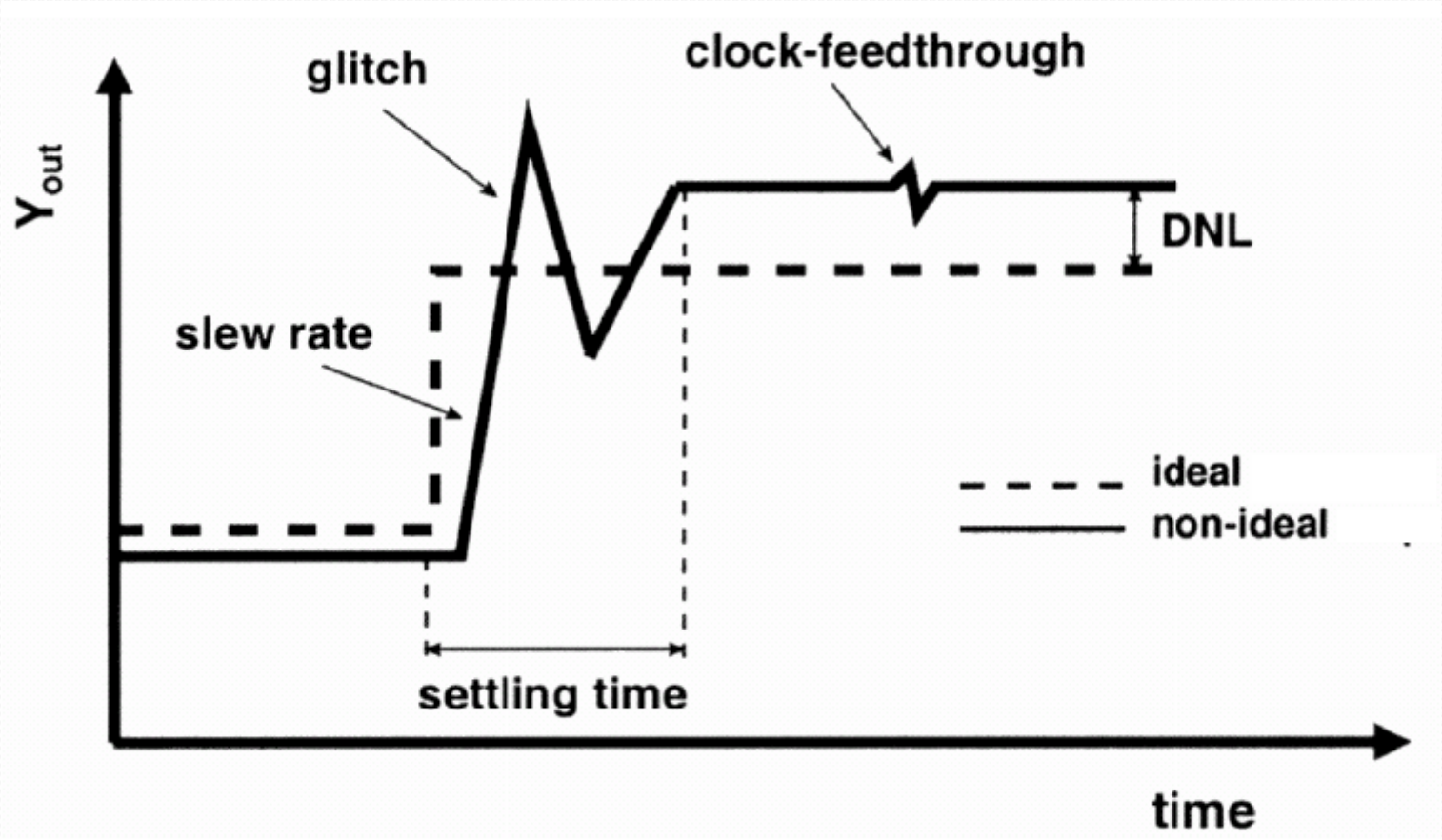


INL **Integral Non Linearity**
DNL **Differential Non Linearity**
(both are expressed in terms of LSB's)

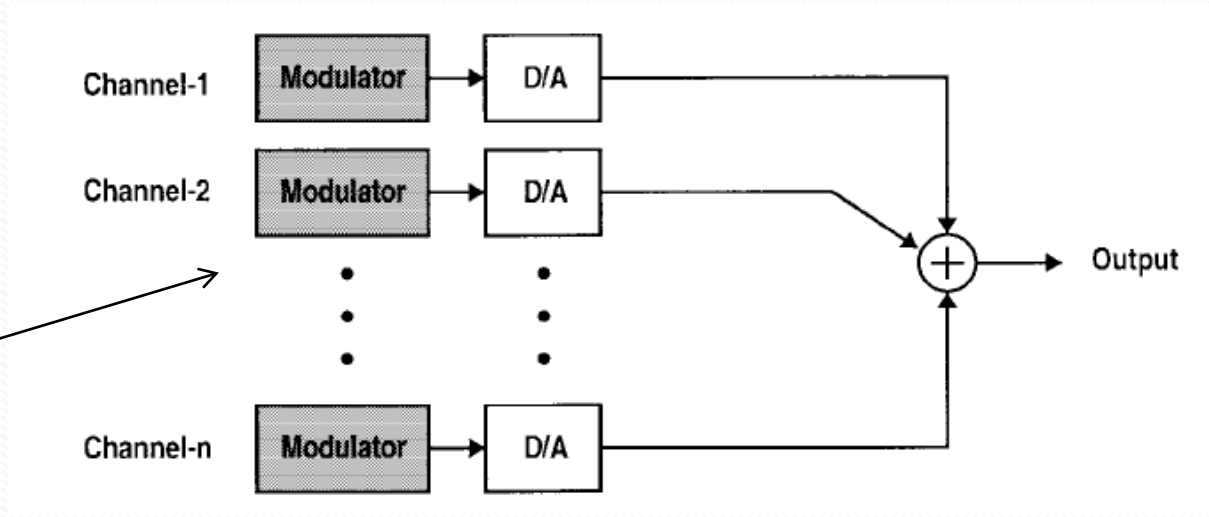
⇒ monotonicity is guaranteed only in a thermometer-coded DAC

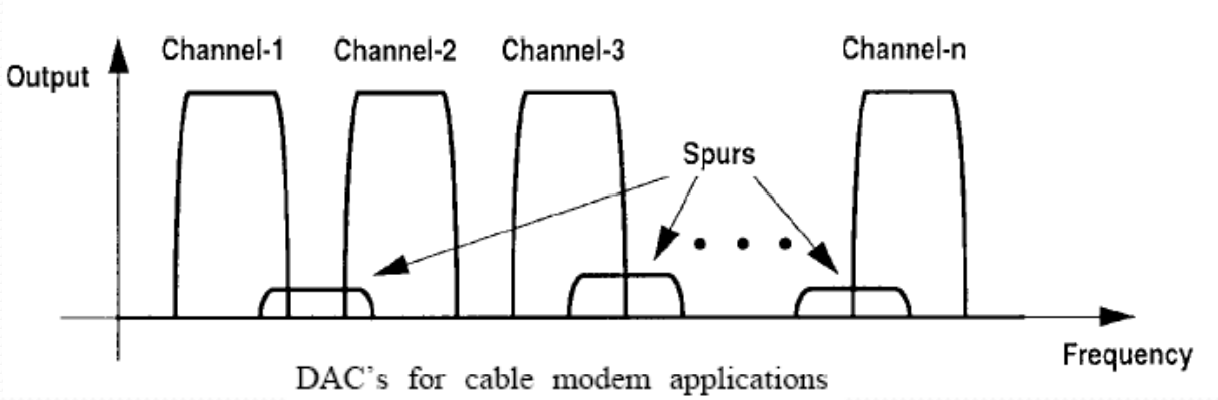
offset error



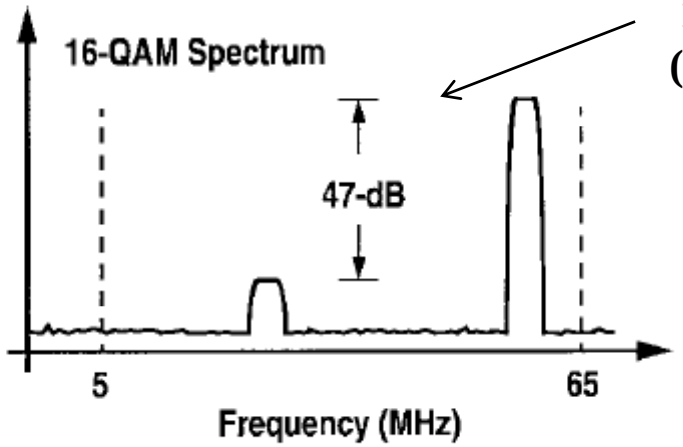

glitch
clock-feedthrough
Y_{out}
DNL
slew rate
ideal
non-ideal
settling time
time

DACs for frequency-domain applications





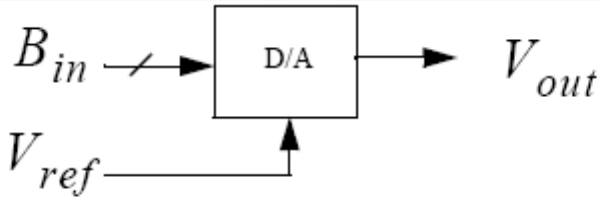
DAC's for cable modem applications



10-bit resolution
(difficult to achieve at HF)

16-QAM spectrum including an aliased harmonics 47 dB below fundamental

D/A Converter Basics.



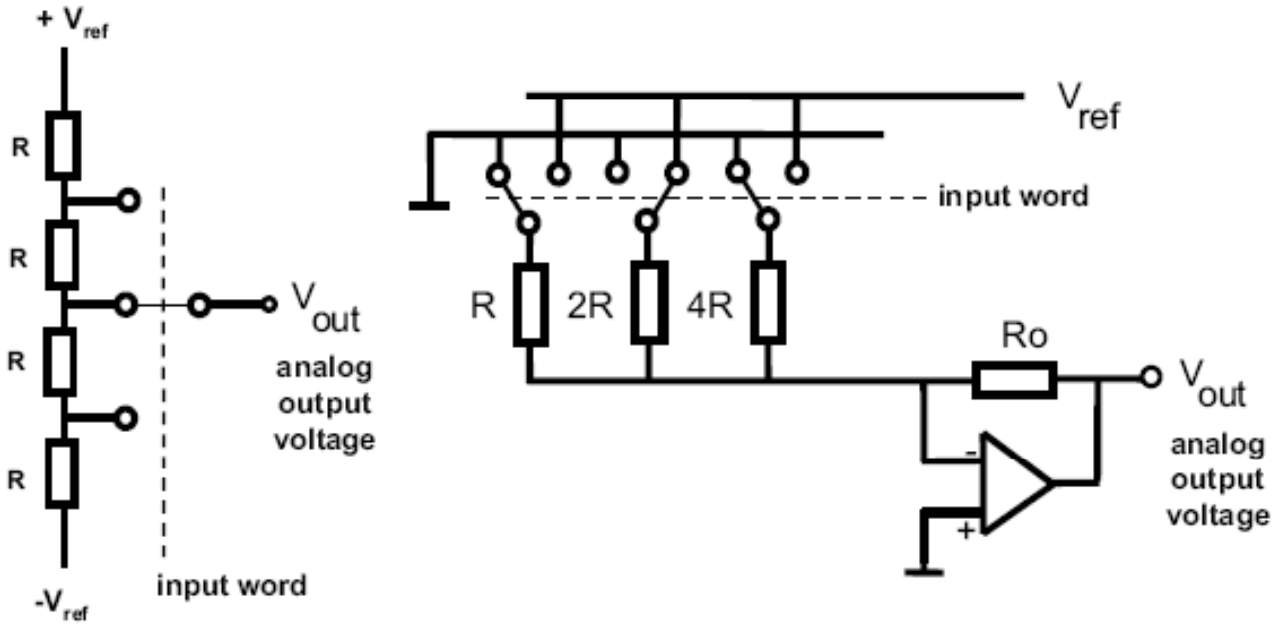
- B_{in} is a digital signal (or word),

$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

- b_i equals a “1” or a “0” (i.e. a binary digit).
- V_{ref} — an analog reference; V_{out} — output .

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

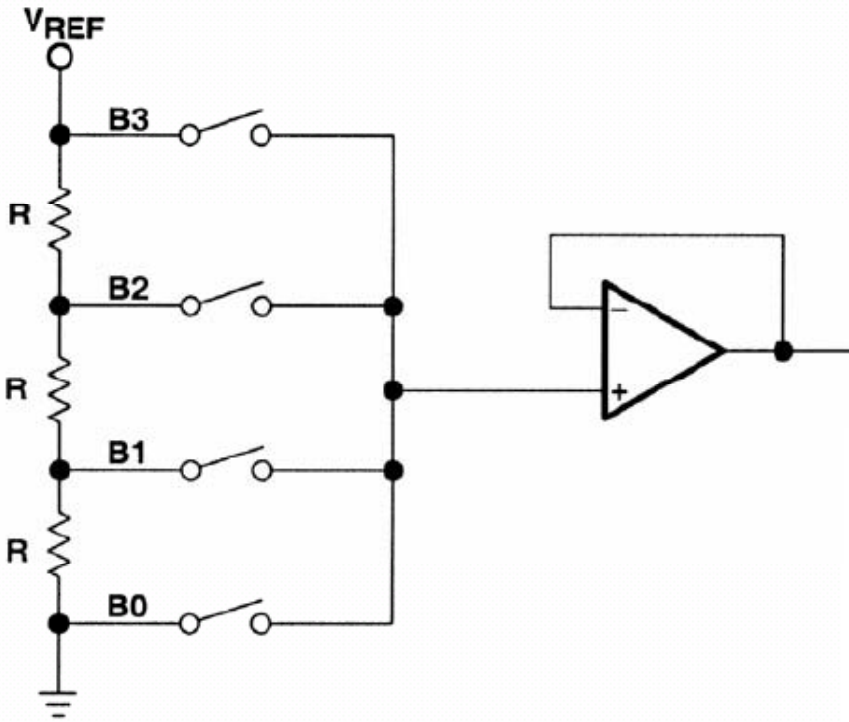
D/A Converter (Nyquist Rate)



voltage mode

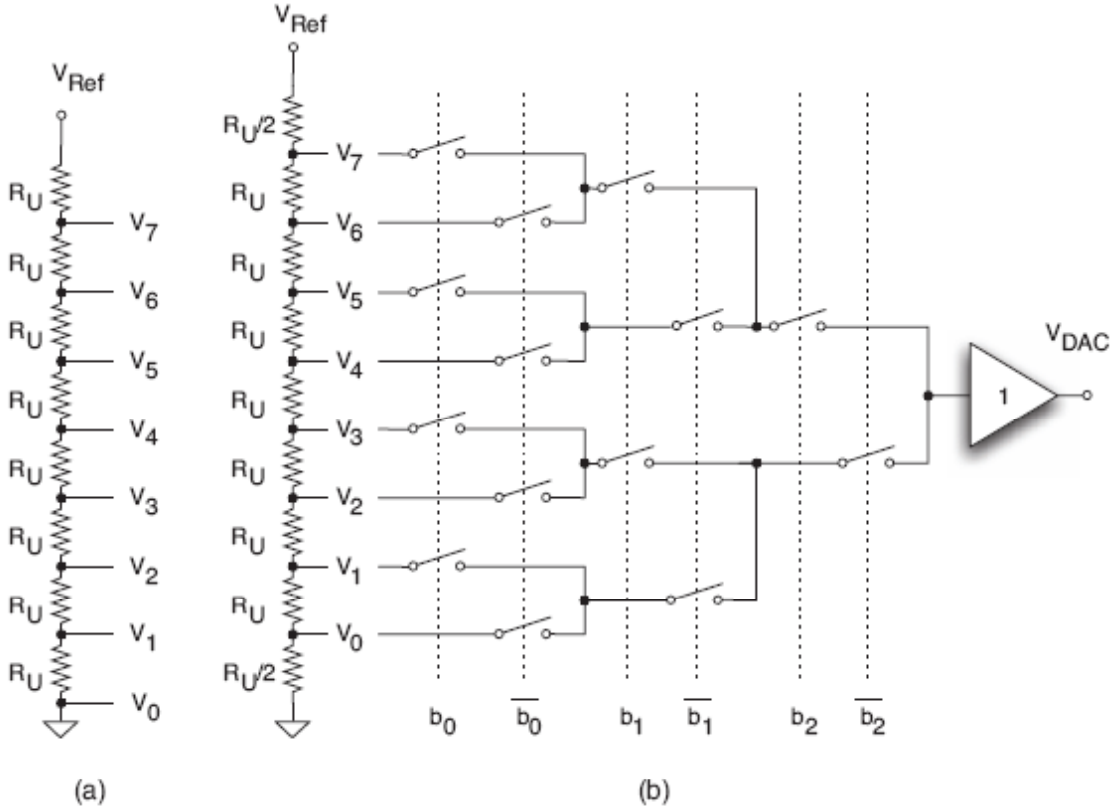
current mode

Thermometer Resistive-Divider D/A

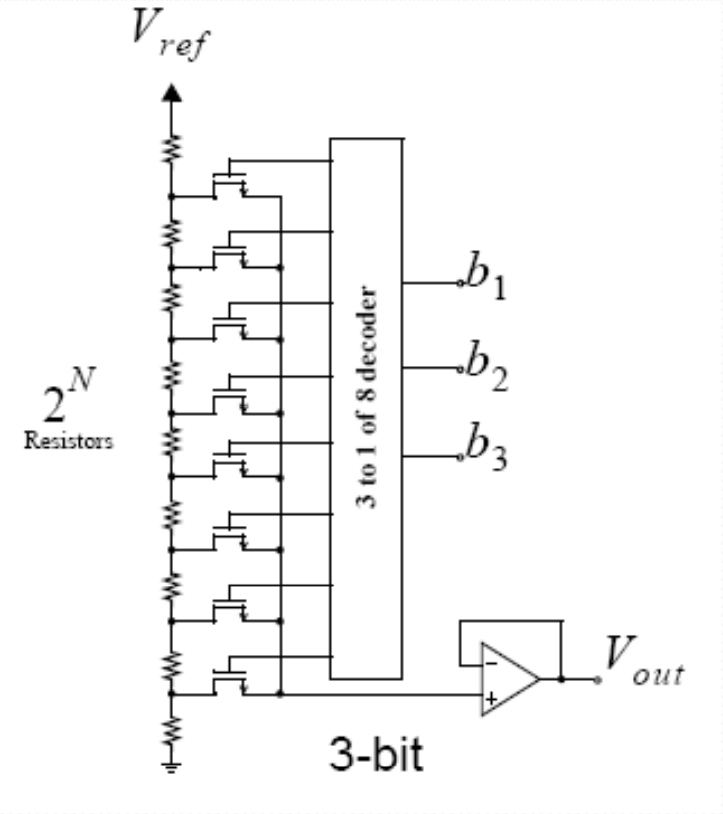


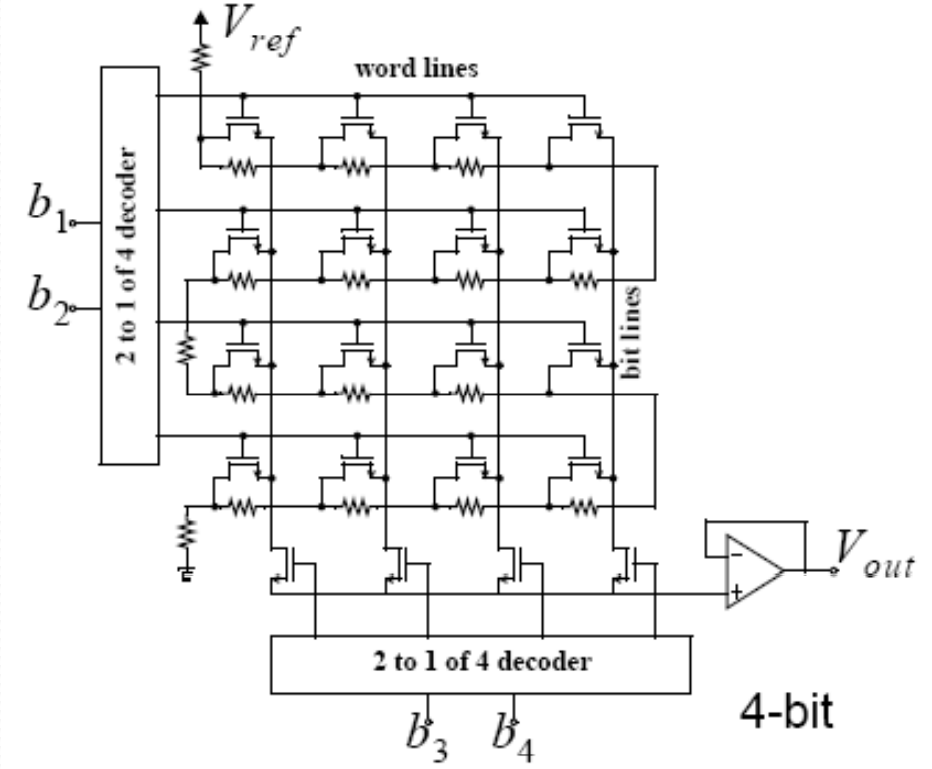
For 10 bit:
1023 resistors and
1024 switches!

- Inherently monotonic: no glitch
- $\approx 2^N$ resistors, switches for N bit converter
- Good DNL; INL problem as resistor mismatch accumulates in string



(a) Resistive divider. (b) Resistive divider with 1/2 LSB offset, Switch tree selector and output buffer.


V_{ref}
2^N
Resistors
3 to 1 of 8 decoder
b_1
b_2
b_3
V_{out}
3-bit


V_{ref}
word lines
b_1
b_2
2 to 1 of 4 decoder
bit lines
V_{out}
2 to 1 of 4 decoder
b_3
b_4
4-bit

Binary			Thermometer						
A	B	C	T_1	T_2	T_3	T_4	T_5	T_6	T_7
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

$T_1 = A + B + C$

$T_2 = A + B$

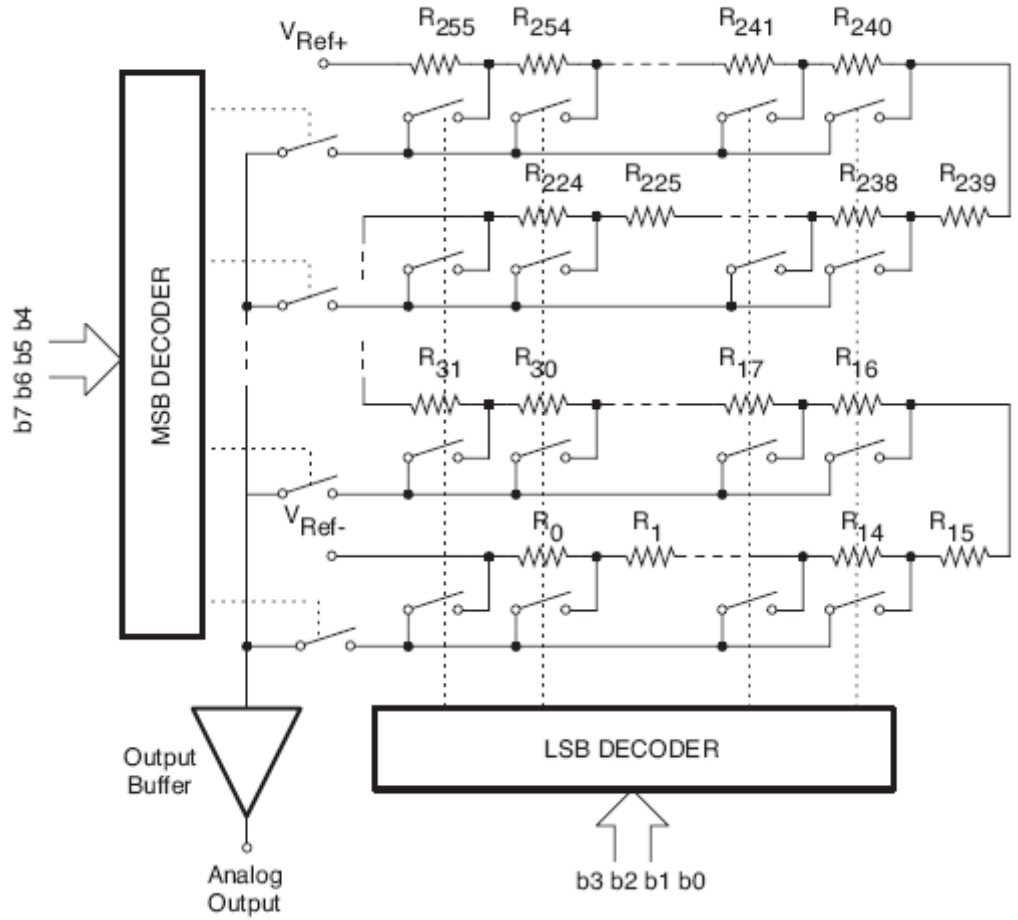
$T_3 = A + BC$

$T_4 = A$

$T_5 = A\,(B + C)$

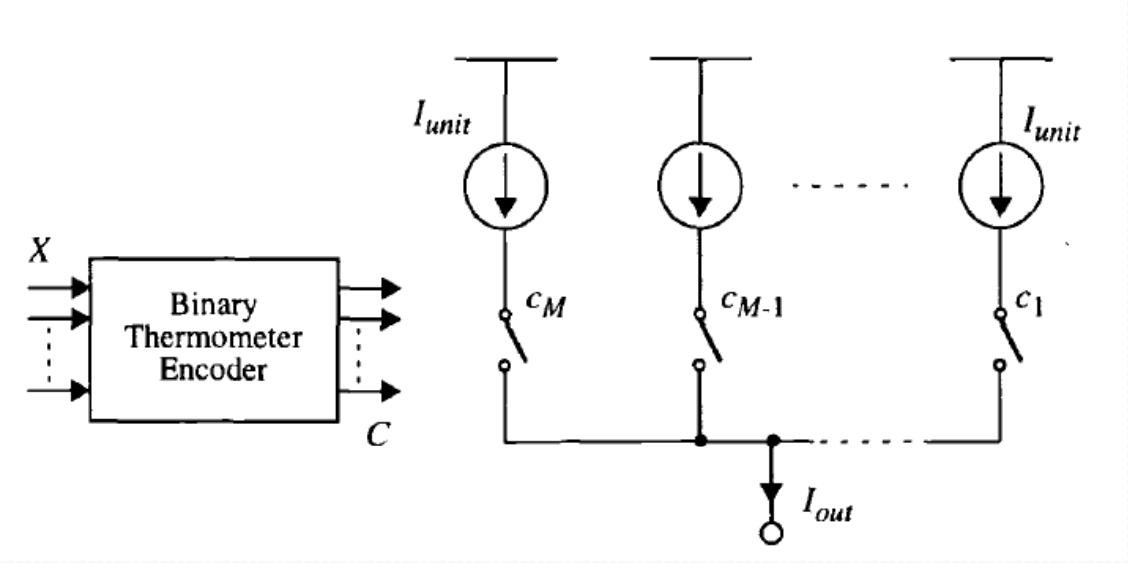
$T_6 = AB$

$T_7 = ABC$



Resistive DAC with X-Y addressing scheme.

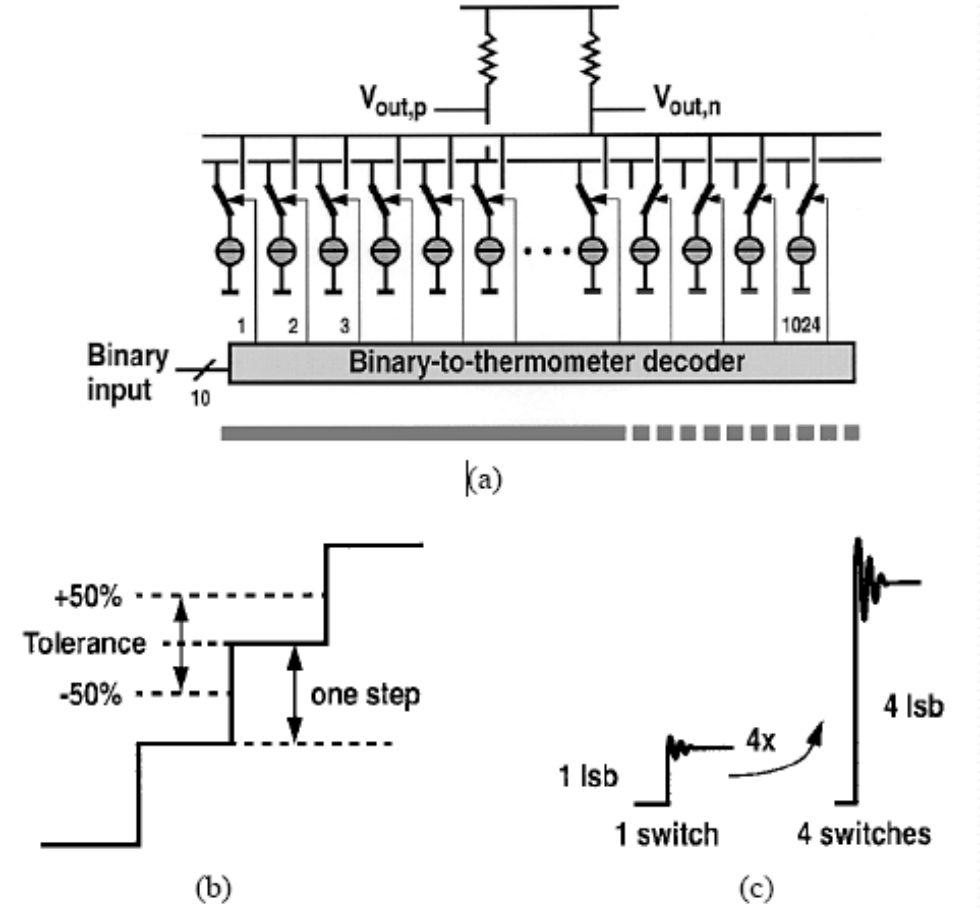
Thermometer Code Current Steering DAC



• reference elements are all equally large and their matching becomes simpler than for the binary case

• even if the matching is within a 50% margin, the converter is still monotonic (spread < DNL of 1 LSB)

• for N bits, $2^N - 1$ current sources are needed



Matching and glitch advantages of a thermometer-coded DAC

pros:

- monotonic by construction: analog output always increases with digital input

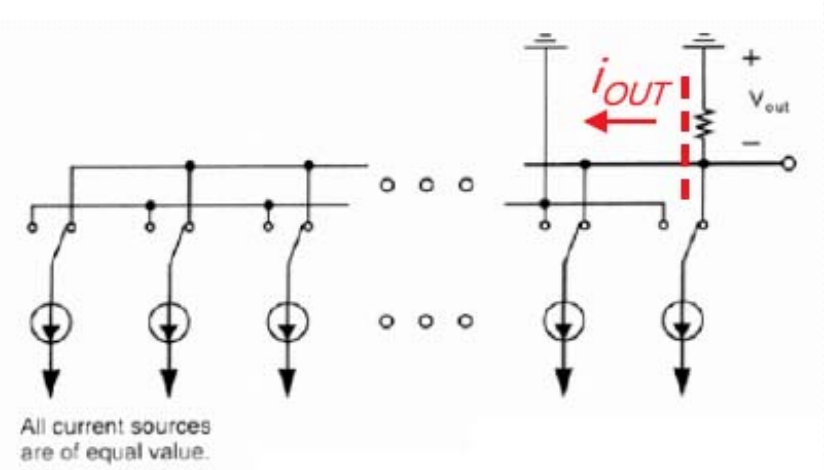
- no problem at mid-code transition (ex: 0111 1111 → 1000 0000) as only ONE current source is switched. Glitches are reduced.

cons:

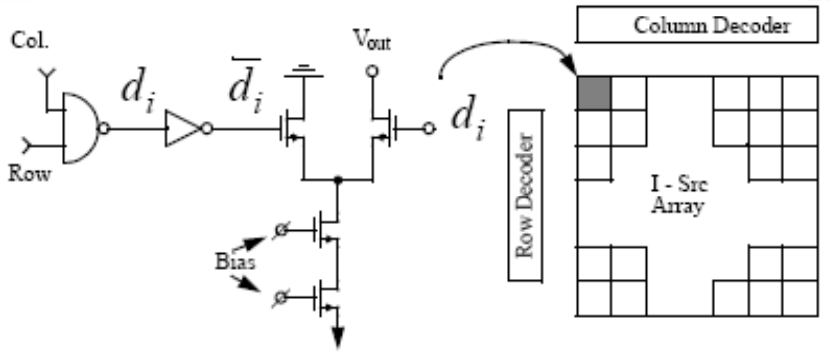
- design complexity: $2^N - 1$ current sources. Large output capacitance (Ex: 12 bits, 4095 current sources and switches)

- large area
  - matching problems
  - larger timing uncertainty of the switches.

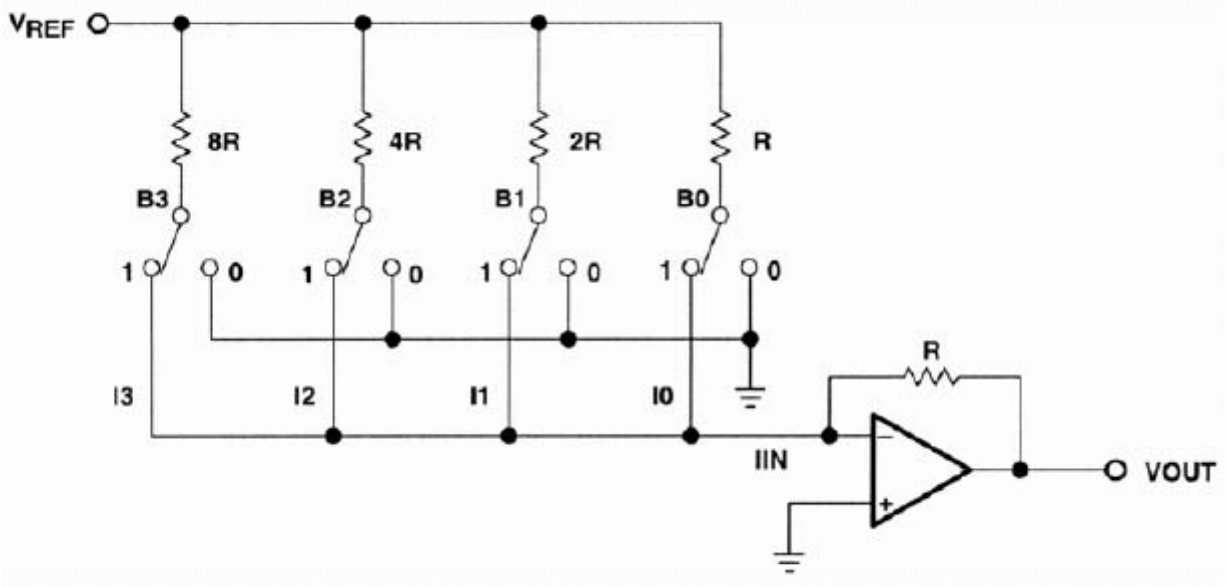
- All current sources of equal value
- Reduces glitches



- Switch with differential pair Q1/Q2, cascode Q3:
  - V_{DS} of current source Q4 remains constant



Binary-Weighted Resistor DAC

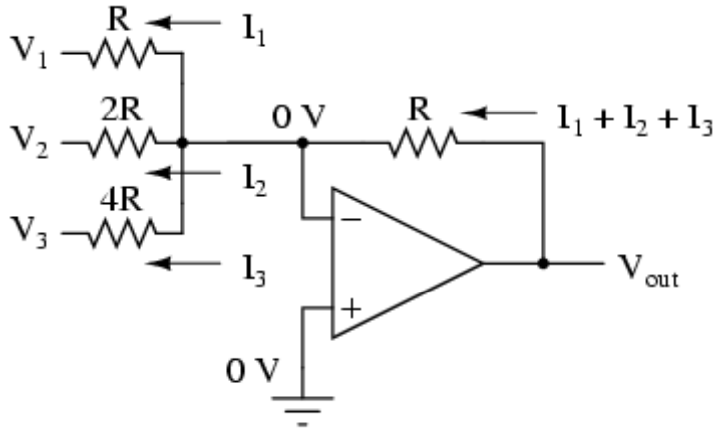


Matching

- Resistor values vary over wide range: R to $2^{(N-1)}$R for N-bit converter.
- Difficult to acquire accurate matching over wide range.

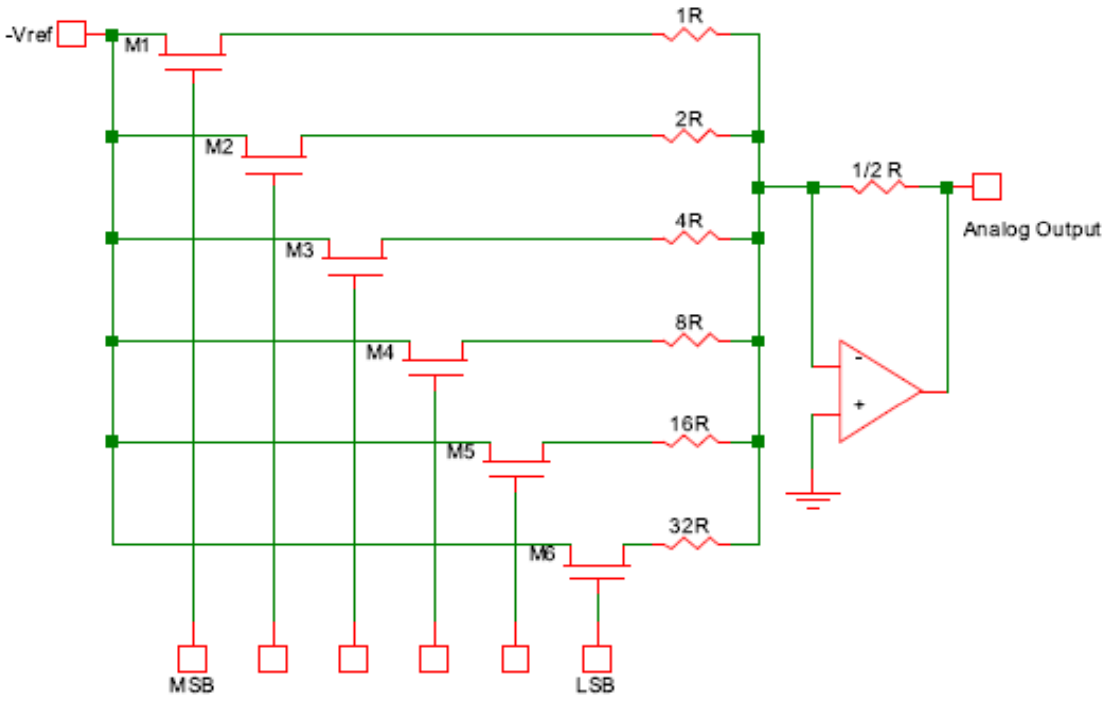
• no guarantee of monotonicity!

$$Vout = -\frac{Vref}{2^{n-1}}(2^{n-1}b_{n-1} + 2^{n-2}b_{n-2} + \ldots + 2b_1 + b_0)$$

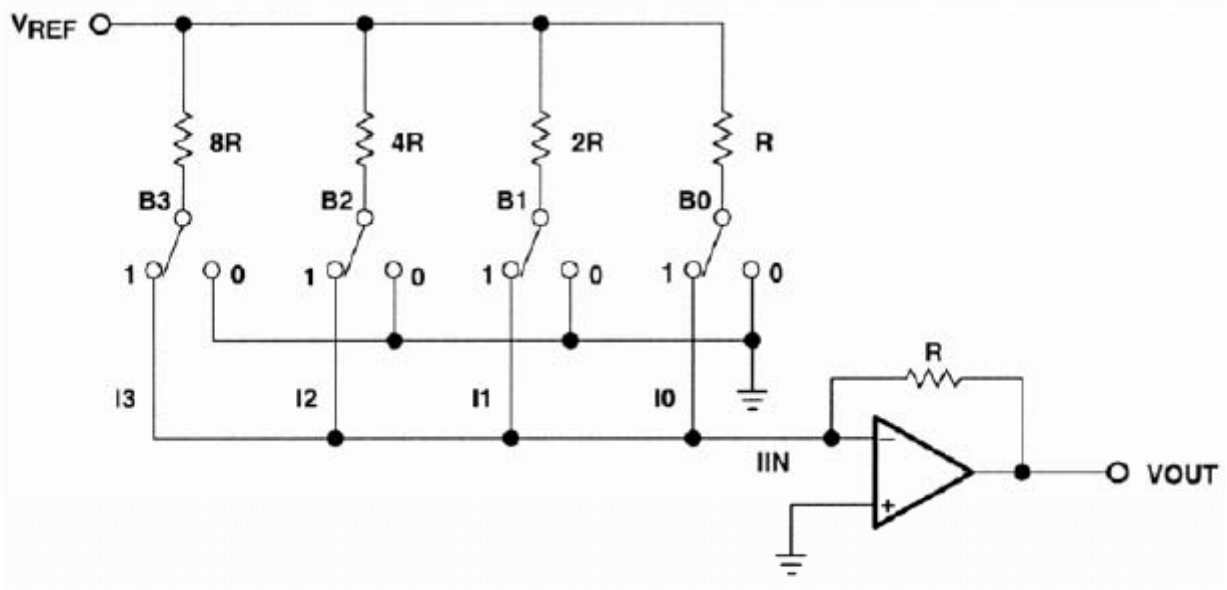


$$V_{out} = -R\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R}\right)$$

$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

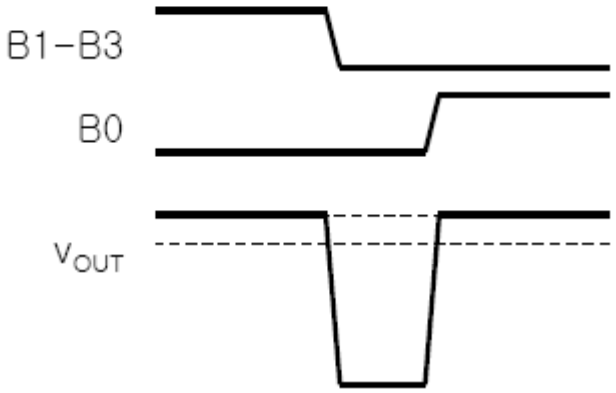


DAC with binary weighted resistors.

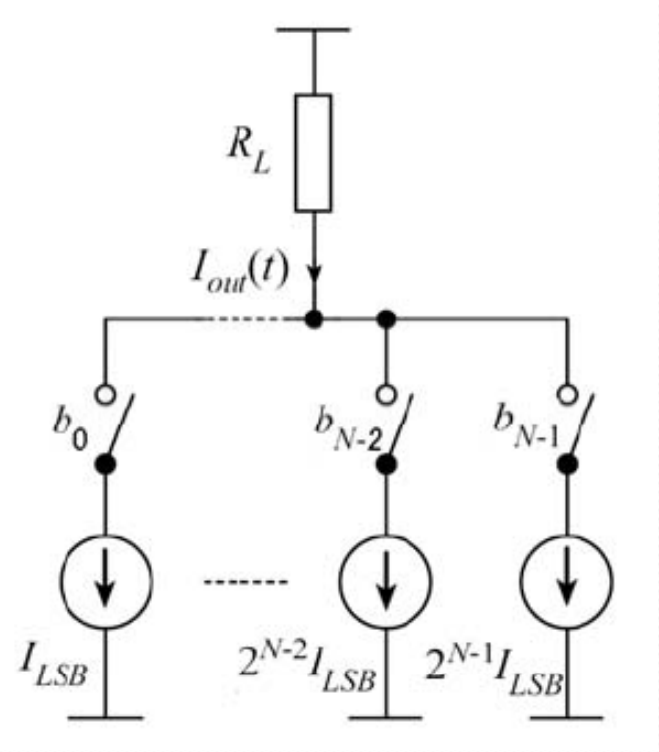


Glitch

- Consider 0111 to 1000 transition
- Timing mismatch: glitch



Binary-weighted current-steering D/A



$$I_{out(w)} = 2^{(N-1)} I_{LSB} \cdot b_{N-1} + \cdots + 2I_{LSB} \cdot b_1 + I_{LSB} \cdot b_0 = I_{LSB} \cdot w$$

digital word

$$w = 2^{(N-1)} \cdot b_{N-1} + \cdots + 2 \cdot b_1 + b_0 = \sum_{m=0}^{N-1} 2^m \cdot b_m$$

pros:

- simple circuit: Ex. for 12-bit converter, only 12 current sources and equal number of switches

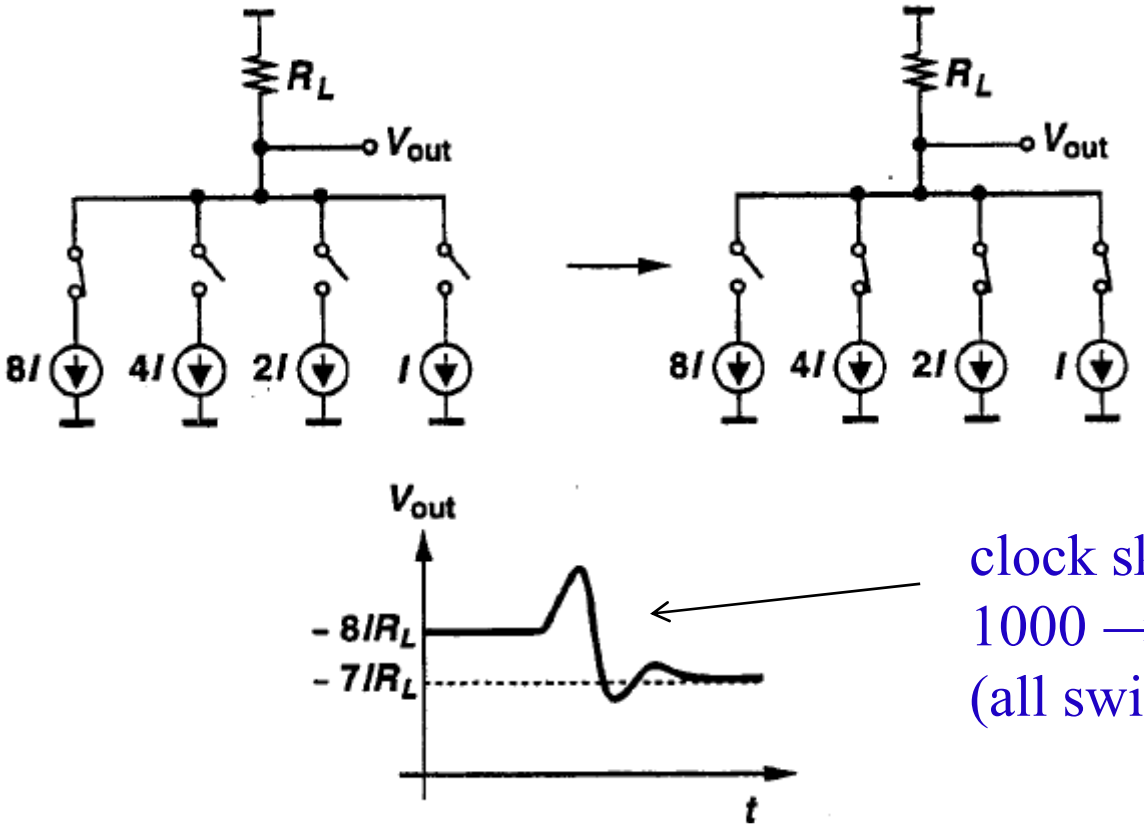
- no need for decoding logic: all switches controlled directly by input bits.

cons:

- good matching required: MSB has to be matched within ½ LSB to the sum of all other bits (ex, difficult to guarantee for 12 bits)

- DAC monotonicity is not ensured. Ex mid-code transition (ex: 0111 1111 → 1000 0000) missing-code (DC) + glitch (transient)

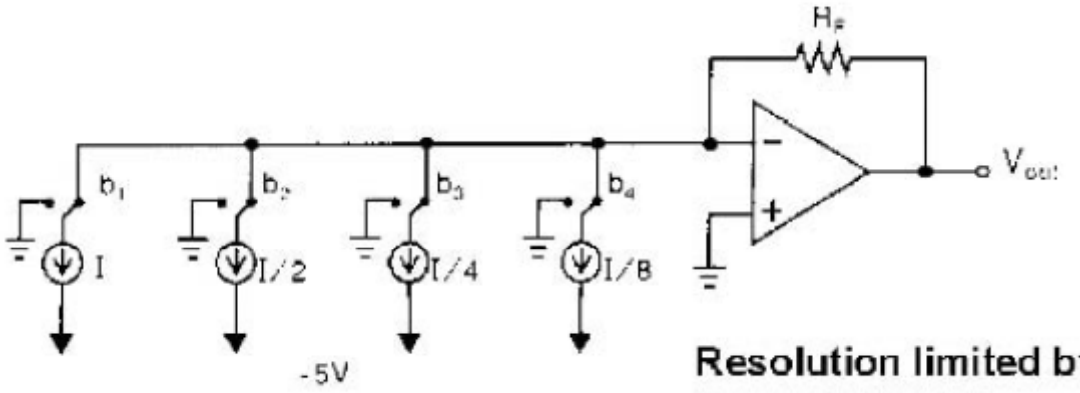
- fully binary DACs commonly limited to 10 bits



Glitch impulse in a current-steering DAC.

clock skew during
1000 → 0111
(all switches change)

Binary-weighted current-steering D/A



• no guarantee of monotonicity!

R-2R Divider D/A

- **to decrease resistor spread**

$$R_4' = 2R$$

$$R_4 = 2R \parallel 2R = R$$

$$R_3' = R + R_4 = 2R$$

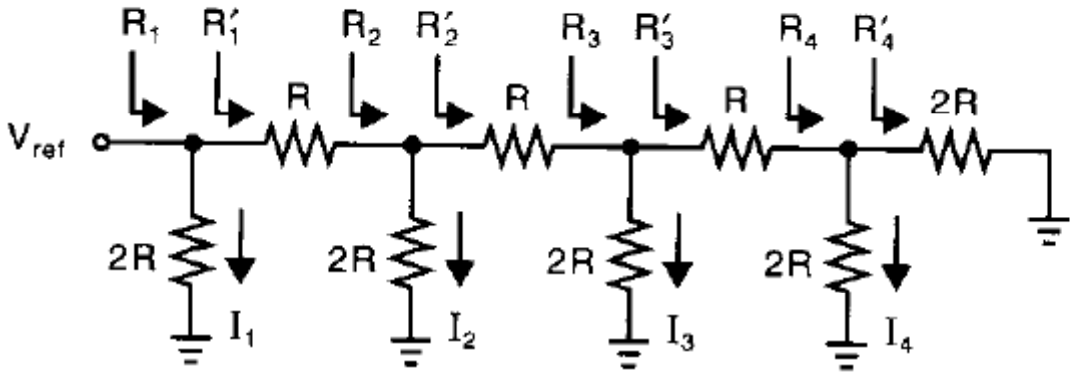
$$R_3 = 2R \parallel R_3' = R$$

and so on. Thus, $R_i' = 2R$ for all i. This result gives the following current relationships:

$$I_1 = \frac{V_{ref}}{2R}$$

$$I_2 = \frac{V_{ref}}{4R}$$

$$I_3 = \frac{V_{ref}}{8R}$$

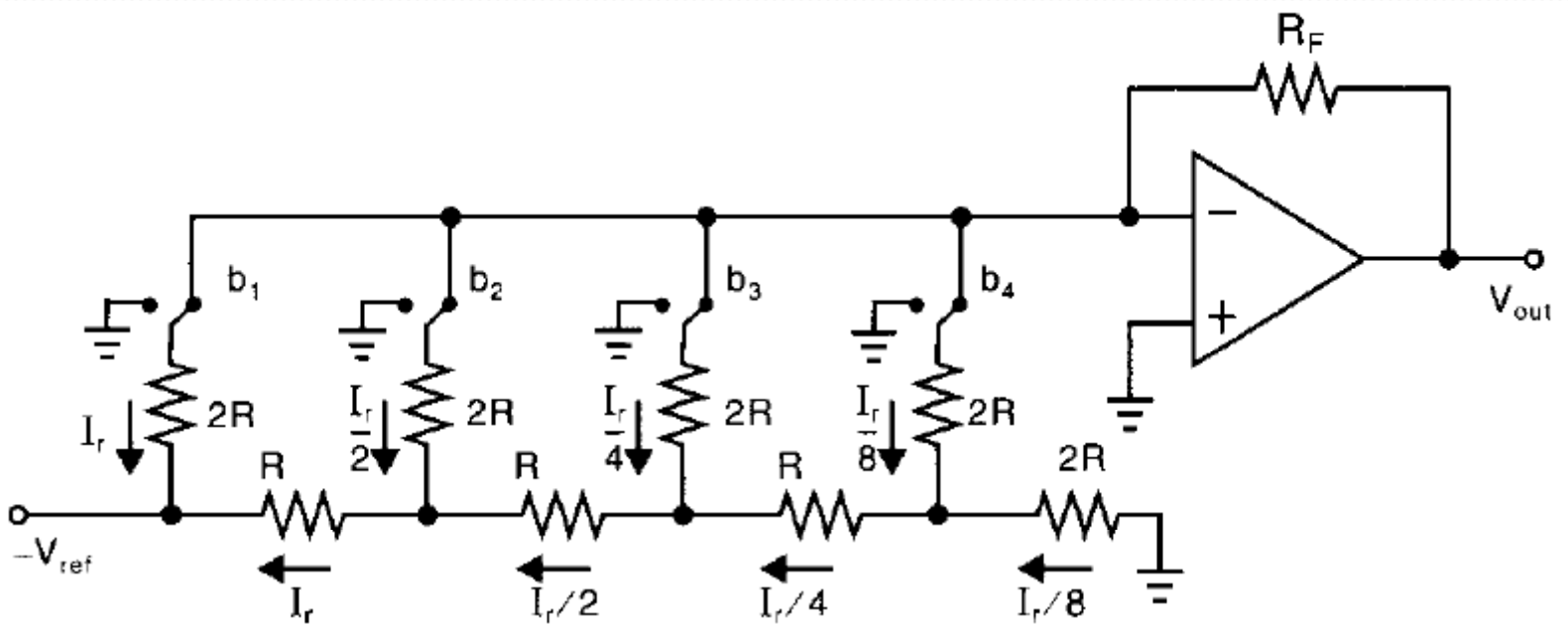


R-2R resistance ladder.

$$I_r = V_{ref}/(2R)$$

$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref} \left(\frac{R_F}{R} \right) \sum_{i=1}^{N} \frac{b_i}{2^i}$$

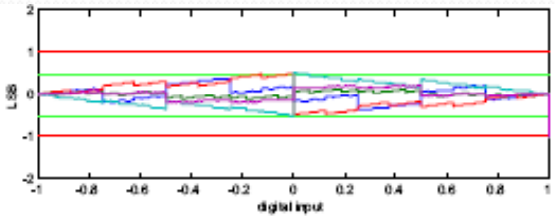
R-2R Divider D/A

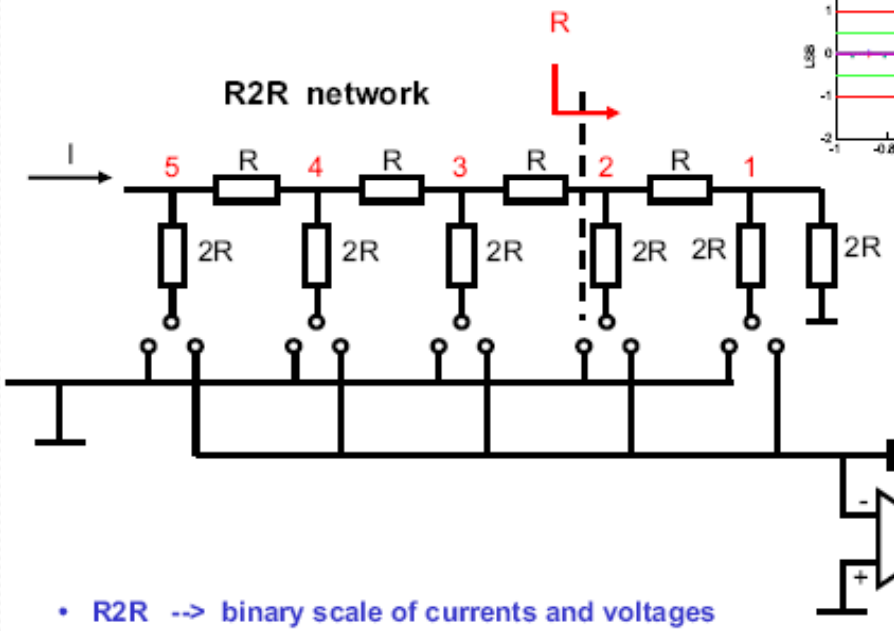


4-bit R-2R based D/A converter.

R-2R Divider D/A

- resistor count reduced from 2^n to ≅3n

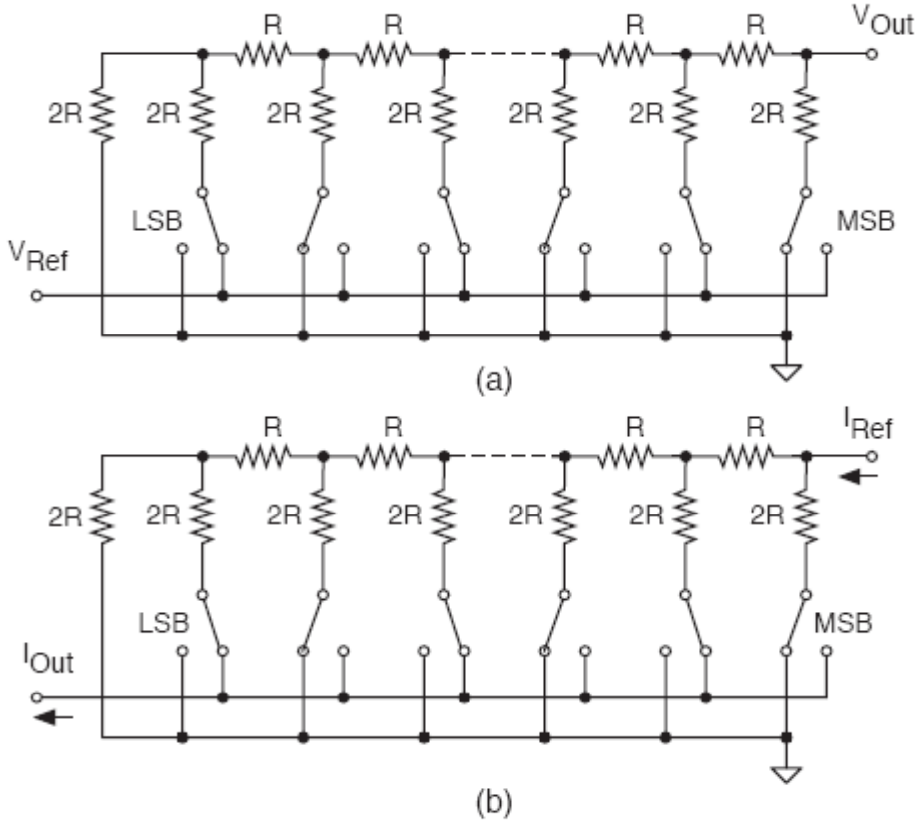




example
10 - bit R2R converter
(5 samples)
sigmR = 0.001

- R2R --> binary scale of currents and voltages
- large transition errors may occur when MSB's change
  expl: 0 1 1 1 1 --> 1 0 0 0 0
- the accuracy of the MSB's resistors must be nearly the same as that of the converter

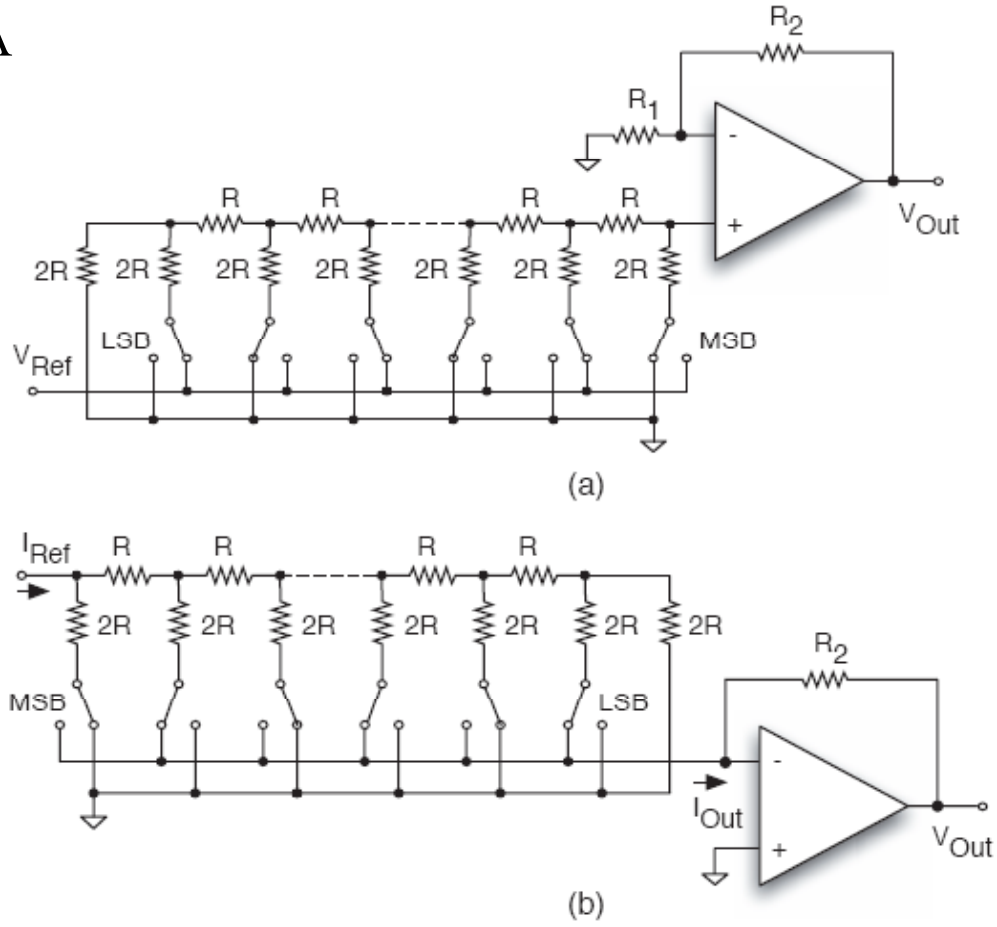
R-2R Divider D/A



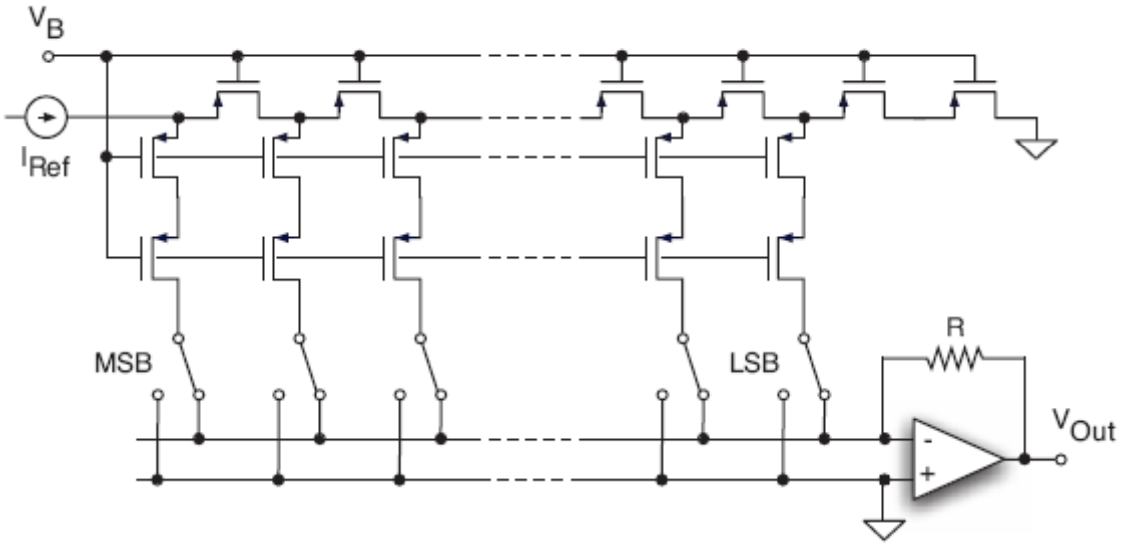
(a) Voltage mode R-2R ladder network. (b) R-2R current mode ladder networks.

$$V_{Out} = \frac{V_{Ref}}{2} b_{n-1} + \frac{V_{Ref}}{4} b_{n-2} + \cdots + \frac{V_{Ref}}{2^{n-1}} b_1 + \frac{V_{Ref}}{2^n} b_0$$

R-2R Divider D/A



(a) Use of the voltage-mode R-2R ladder network. (b) Use of the current-mode R-2R ladder network in an output voltage DAC.



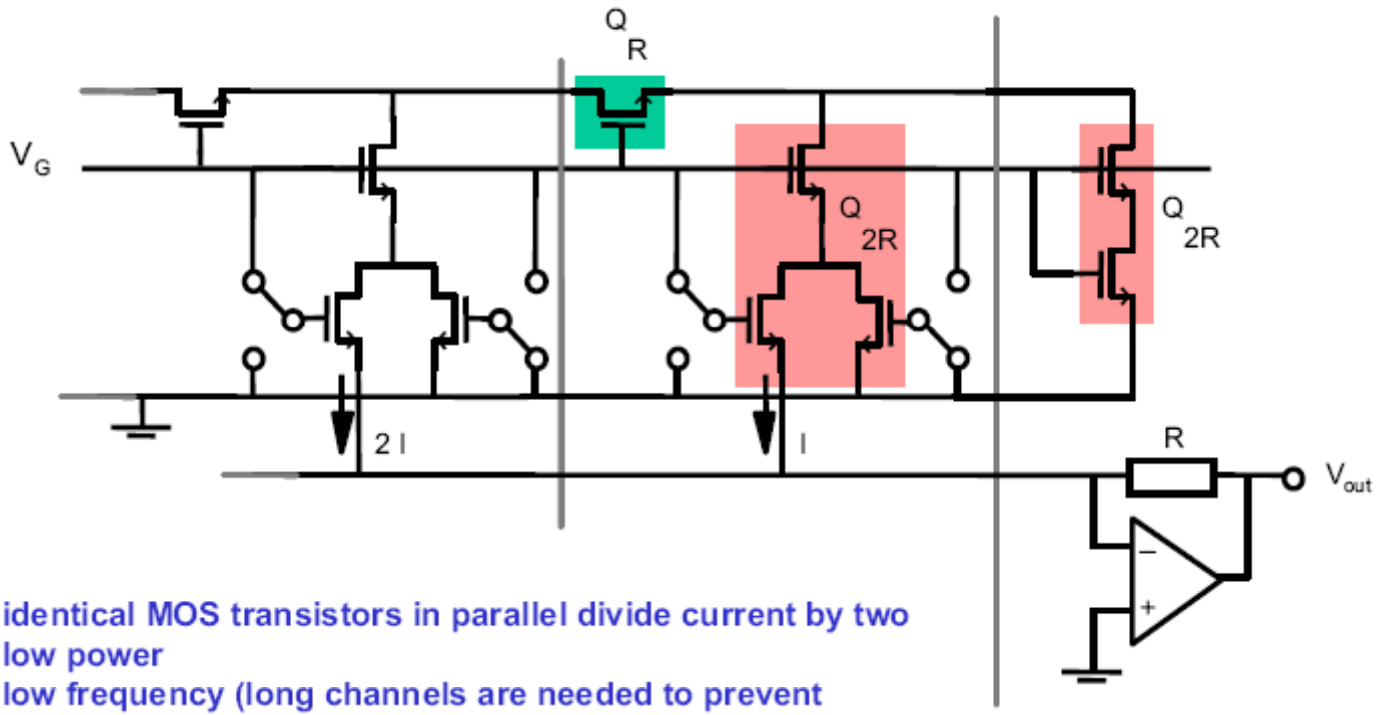
R-2R architecture with MOS transistors replacing the resistors.

• the layout of resistors consumes a relatively large area if the value of unity resistance is large and the used layer has a low specific resistance (like low-resistive poly)

• for medium accuracy it is possible to save silicon area by replacing the resistors with MOS transistors

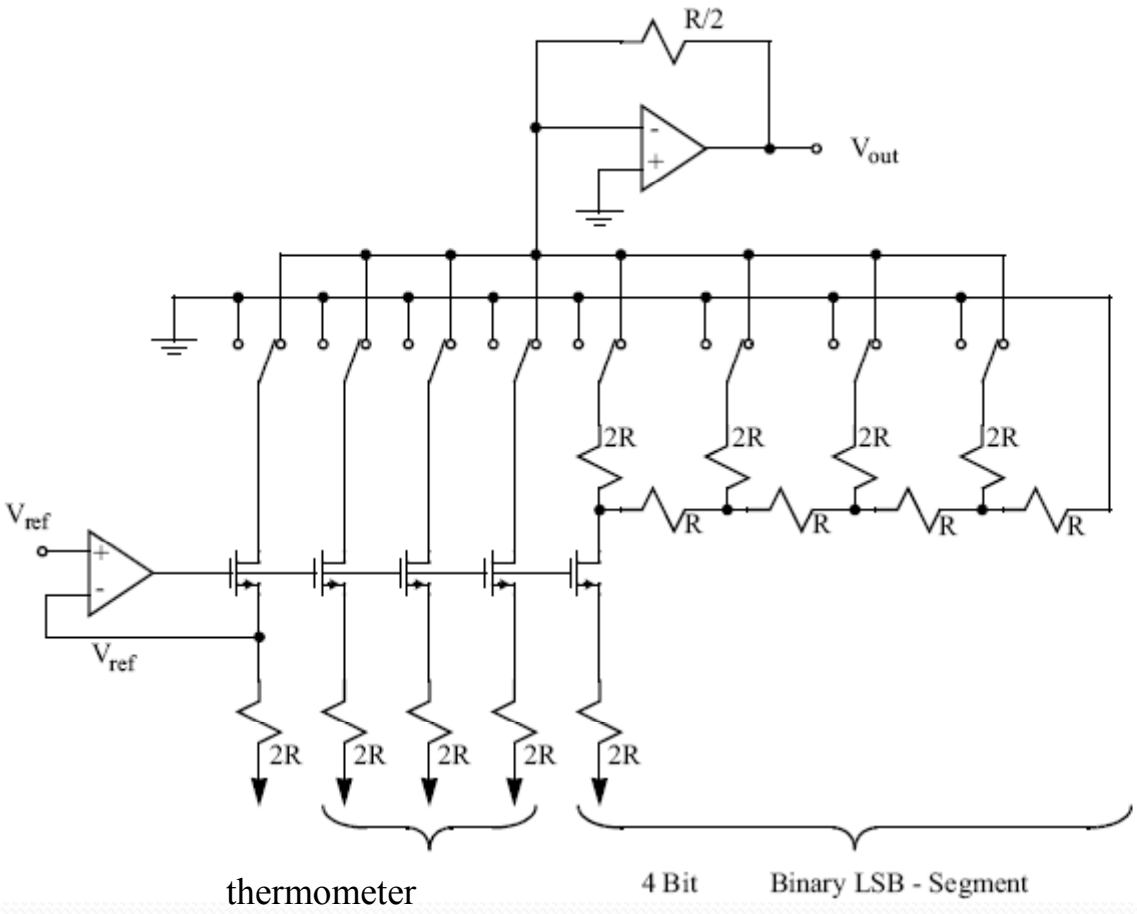
• all transistors have identical (W/L)

MOSFET - only R2R converter



- identical MOS transistors in parallel divide current by two
- low power
- low frequency (long channels are needed to prevent velocity saturation mismatch)

Segmented D/A



- Combine thermometer and binary
- Accuracy needed for LSB reduced
- Glitches reduced
- Very popular

• **segmentation**: combination of binary and thermometer coding

• thermometer code is used for MSBs, while binary code for LSBs

• 0% segmentation = fully binary converter

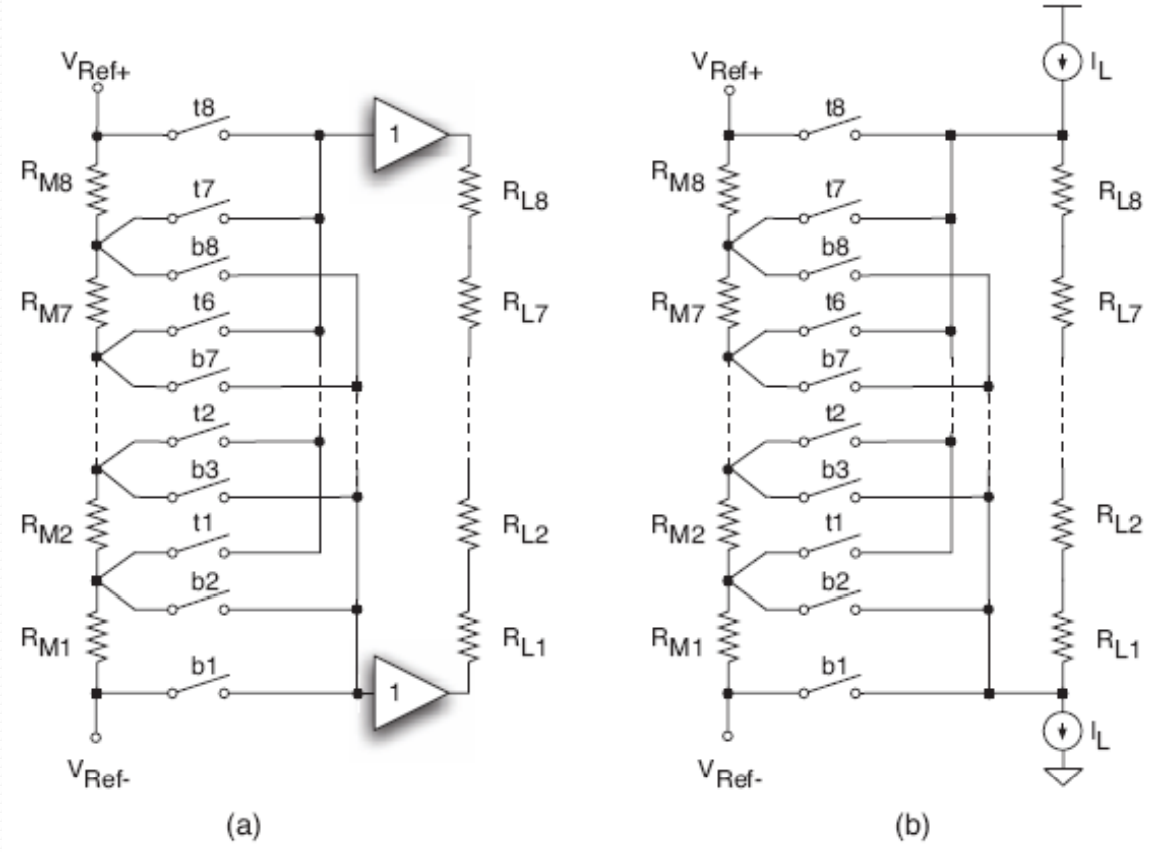
•100% segmentation = a full thermometer code converter

• low segmentation ⇒ circuit simplicity (only a few current sources and switches), but larger DNL

• large segmentation ⇒ lower DNL, but increased problems due to output conductance, capacitance and charge feedthrough, as well as larger area and power consumption.

⇒ optimum segmentation has to be found by the designer!

Thermometer-code segmented D/A



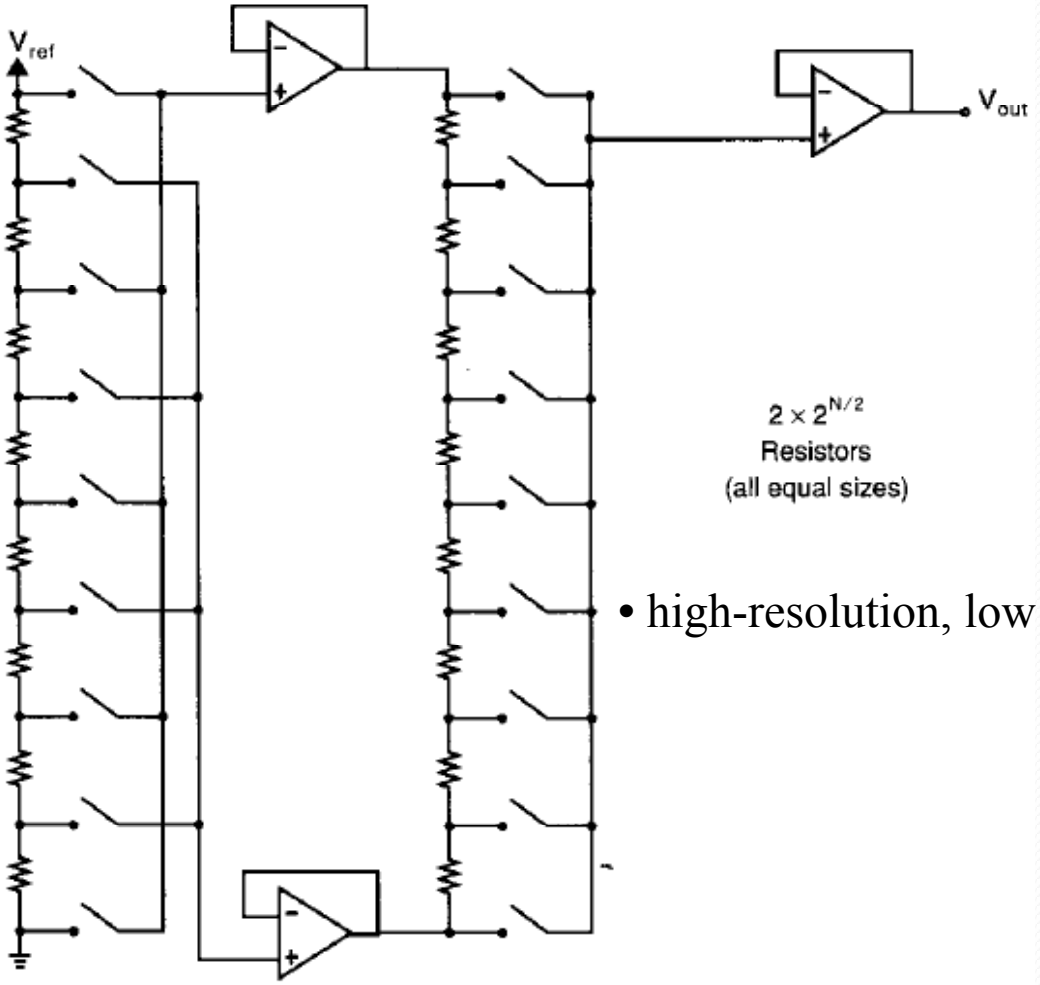
(a) Cascade of two DACs with decoupling buffers. (b) Volt-metric interconnection of the LSB DAC

• Switches select one of the coarse intervals and use it in the fine divider RL1 − RL8

•Two unity-gain buffers decouple the coarse and the fine dividers. The offset of the buffers must match well (< LSB), and must have an input common mode range V_{REF}

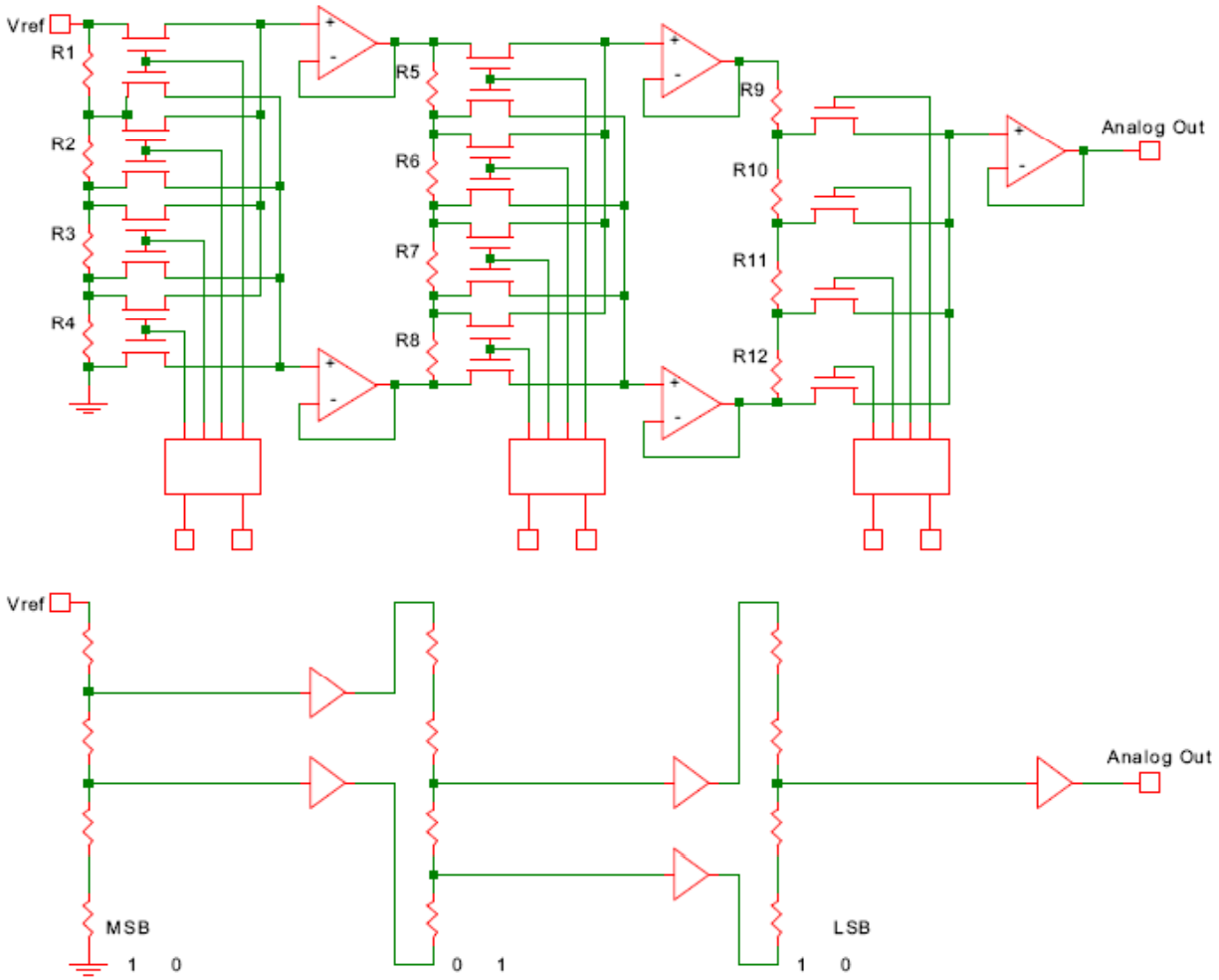
• Moreover, the input impedance must be very high for sensing the coarse voltages in a volt-metric manner: the output resistance of the buffer must be much less than the total resistance of the *LSB divider.*

Thermometer-code segmented D/A



Multiple R-string 6-bit D/A converter.

- high-resolution, low consumption



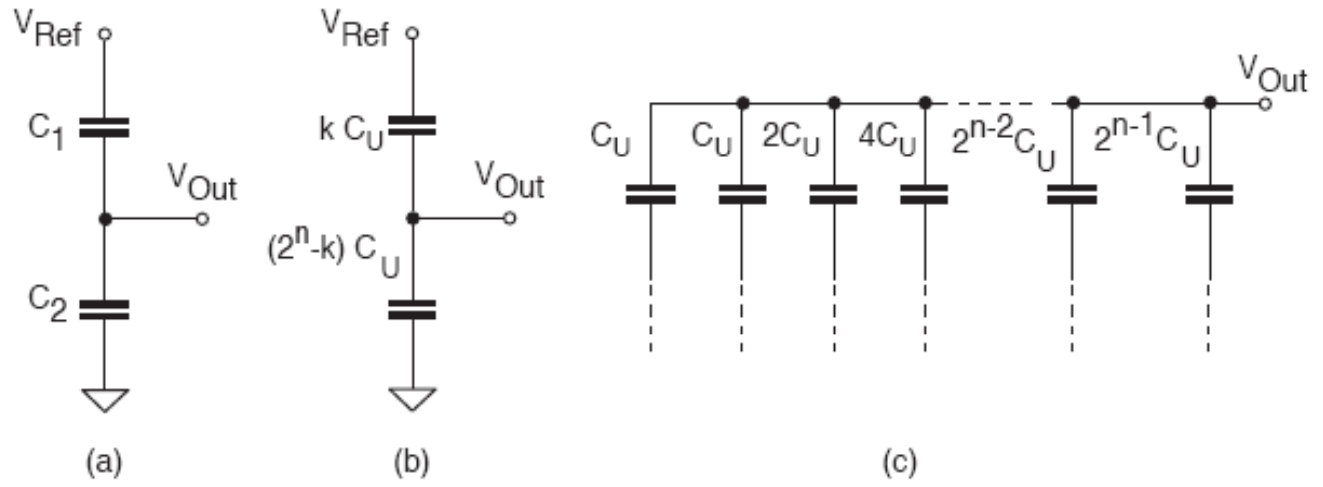
6-bit segmented DAC.

Capacitor-divider D/A

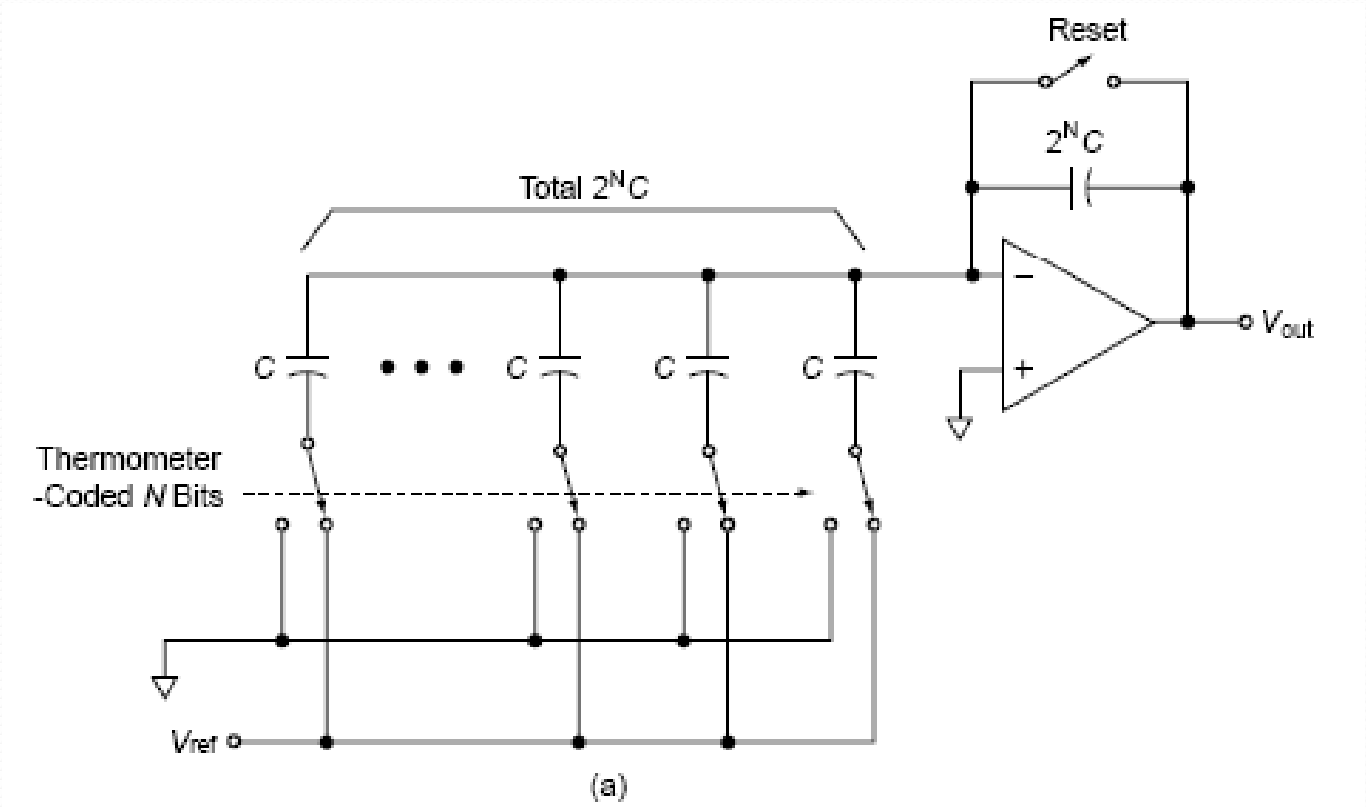
Capacitor	*Absolute tolerance* %	*Matching tolerance* %	*Voltage coeff* ppm/V	*Temperat. coeff* ppm/°C
Poly - poly	± 10 to 30	± 1 area > 500 μm^2 ± 0.1 area > 10^4 μm^2	10 to 20	20 to 50
Poly - diff	± 10	same	20 to 100	50

Capacitor-divider D/A

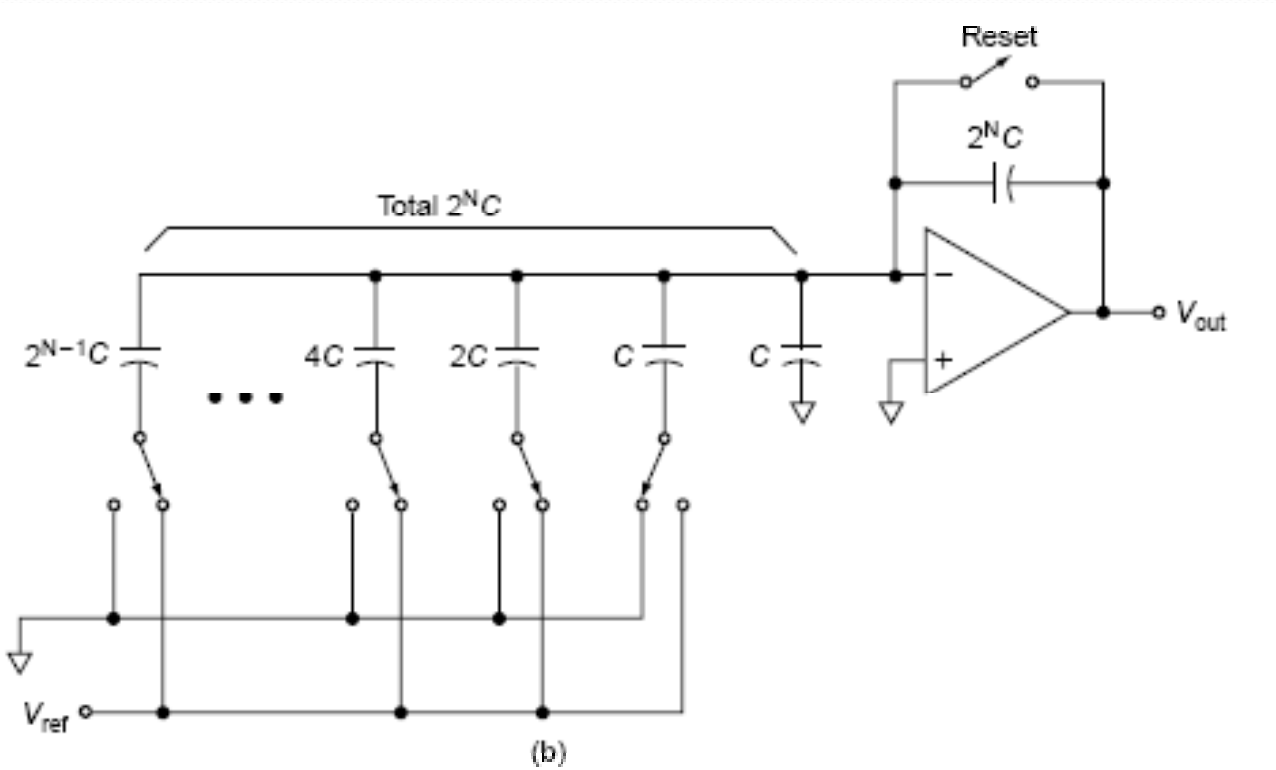
$$V_{Out} = V_{Ref}\frac{C_1}{C_1 + C_2}$$



(a) and (b) Simple capacitor divider. (c) Array of binary weighted capacitors.

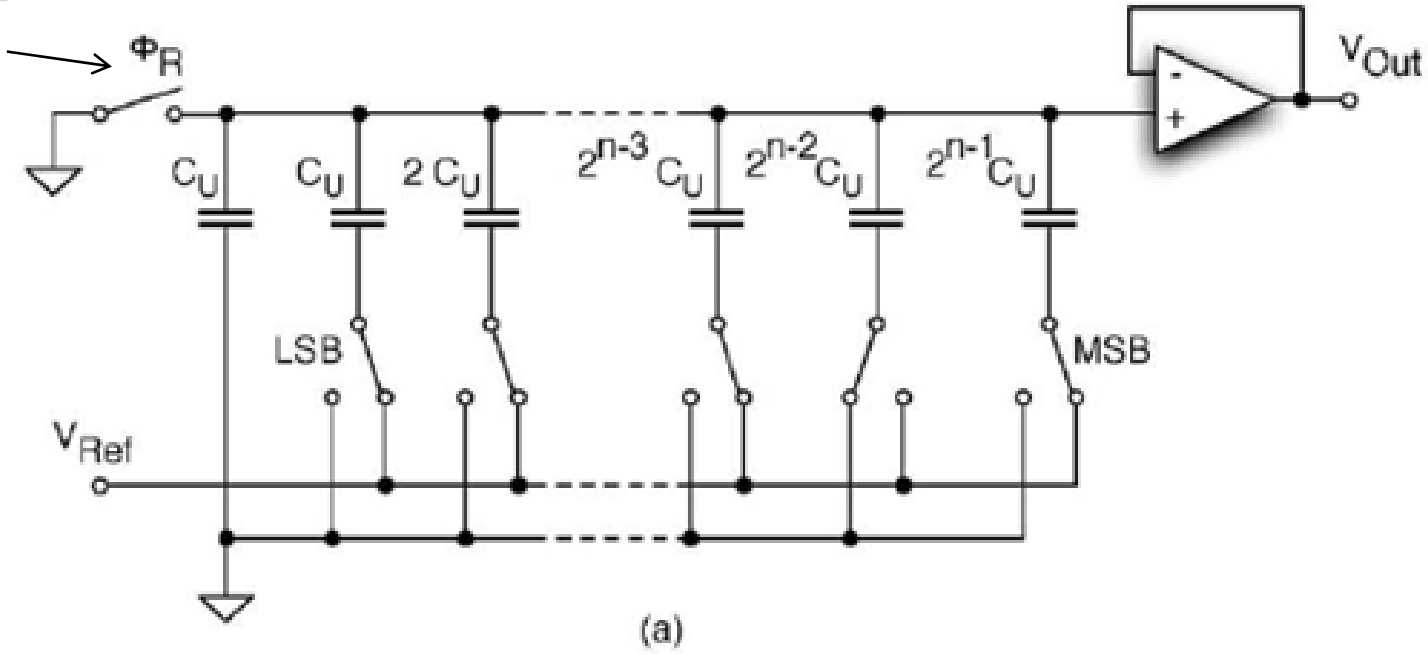


Capacitor-array DACs: (a) thermometer-coded



Capacitor-array DACs (b) binary-weighted.

Reset phase



(a) n-bit Capacitive divider DAC.

•A drawback of capacitive divider architecture: the number of capacitors increases exponentially with the number of bits.

• The capacitors' count can be reduced by dividing the capacitive array into two parts separated by an attenuation capacitance, C_A.

The series of attenuation capacitance and the entire right array must equal the C_U

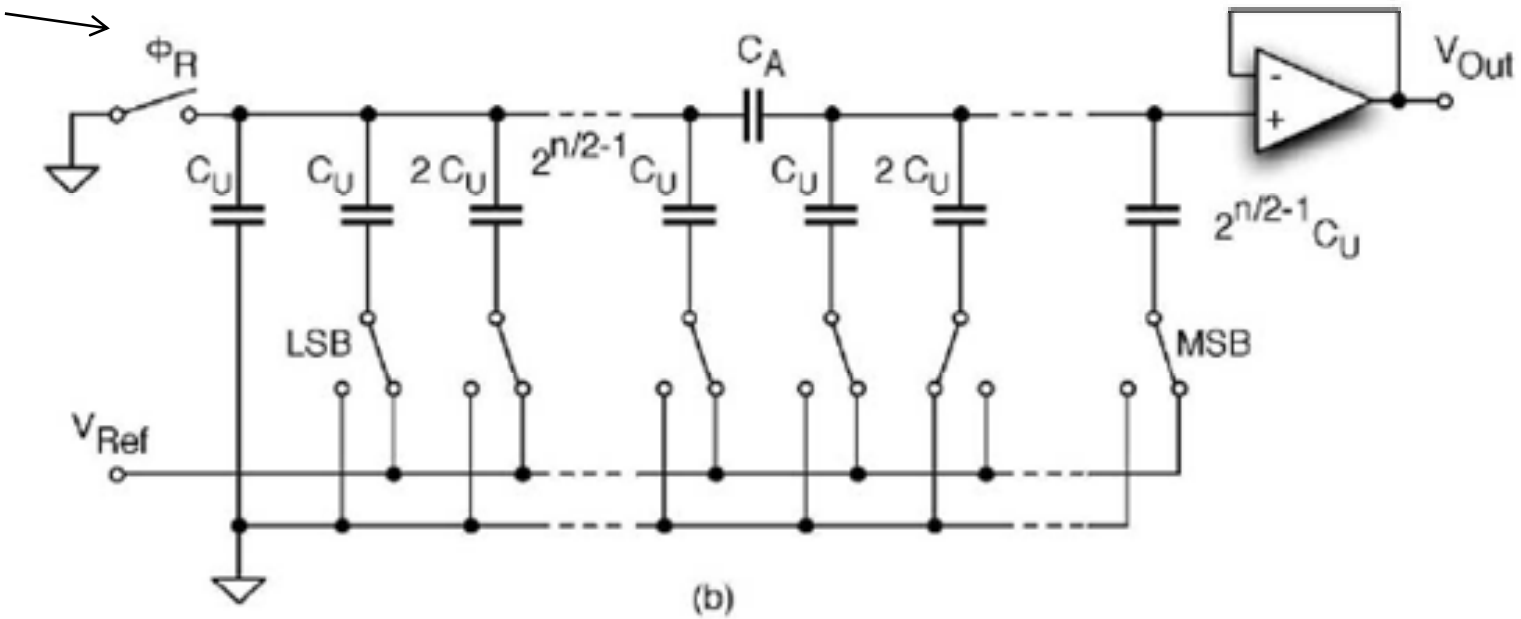
$$\frac{C_A \cdot 2^{n/2} C_U}{C_A + 2^{n/2} C_U} = C_u$$

which yields the value of C_A

$$C_A = \frac{2^{n/2}}{2^{n/2} - 1} C_U.$$

Unfortunately the value of C_A is a fraction of C_U: obtaining the necessary accuracy requires care in the layout.

Reset phase



(b) The use of an attenuator in the middle of the array reduces the capacitance spread.

Oversampling (Σ–Δ) DAC

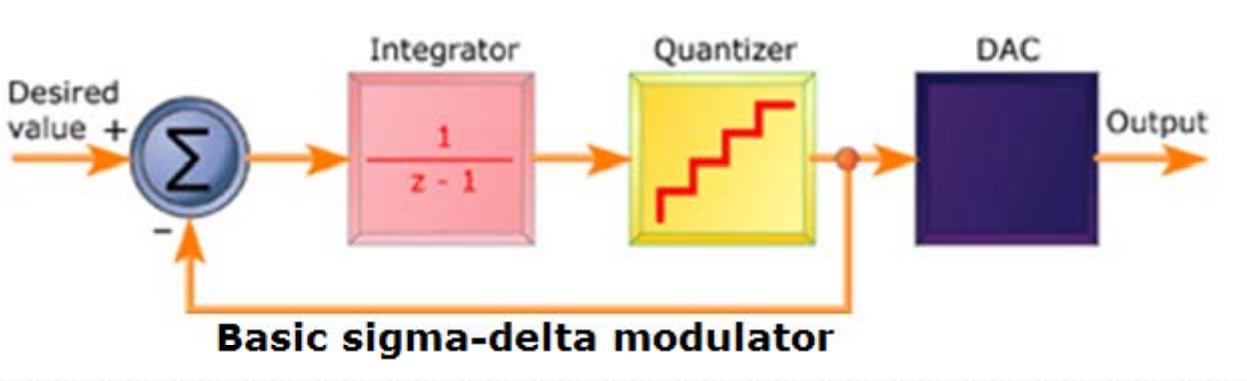
• basically, a Σ–Δ ADC in reverse!

• principle of operation of oversampled DAC is very similar to oversampled ADC (resolution increases with sampling frequency)

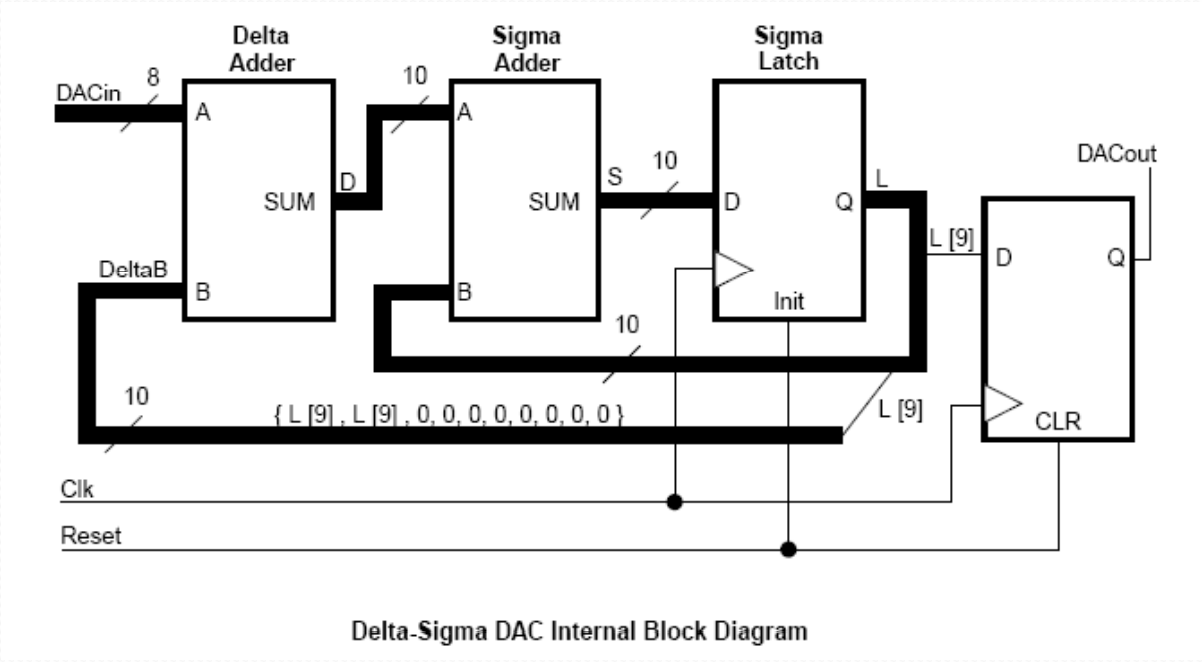
• improves SNR using noise shaping

• processing is done in the digital domain to generate a digital string at one-bit DAC output. The average duty-cycle of the output string is proportional to the value of the binary input

• the analog signal is created by passing the pulse string through an analog low-pass filter

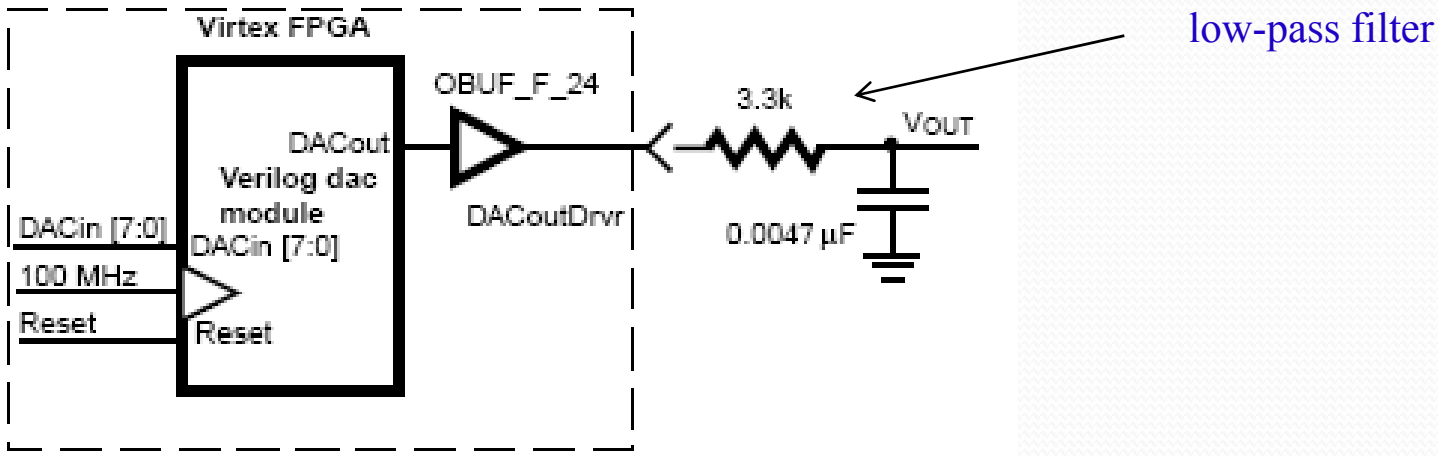


Basic sigma-delta modulator



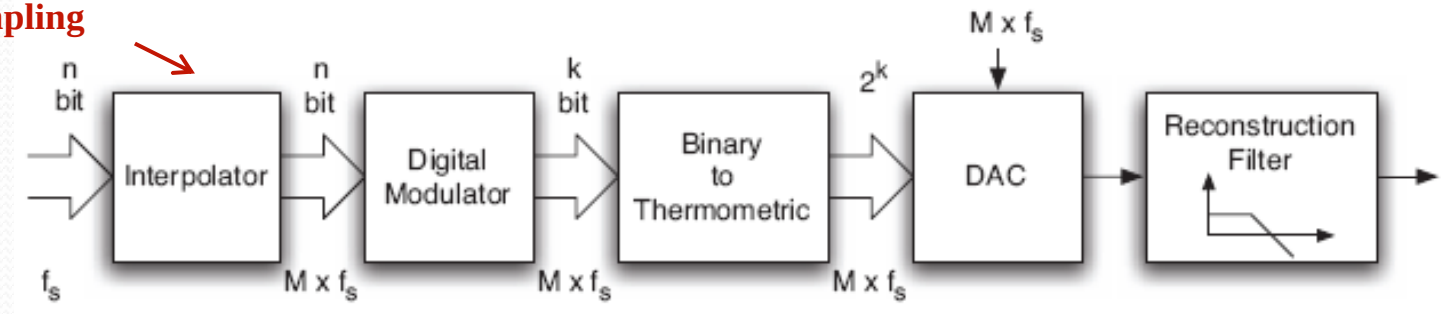
Delta-Sigma DAC Internal Block Diagram

• Delta Adder calculates the difference between input and current 1-bit DAC output (represented as a binary number)



Top-level DAC Implementation

oversampling



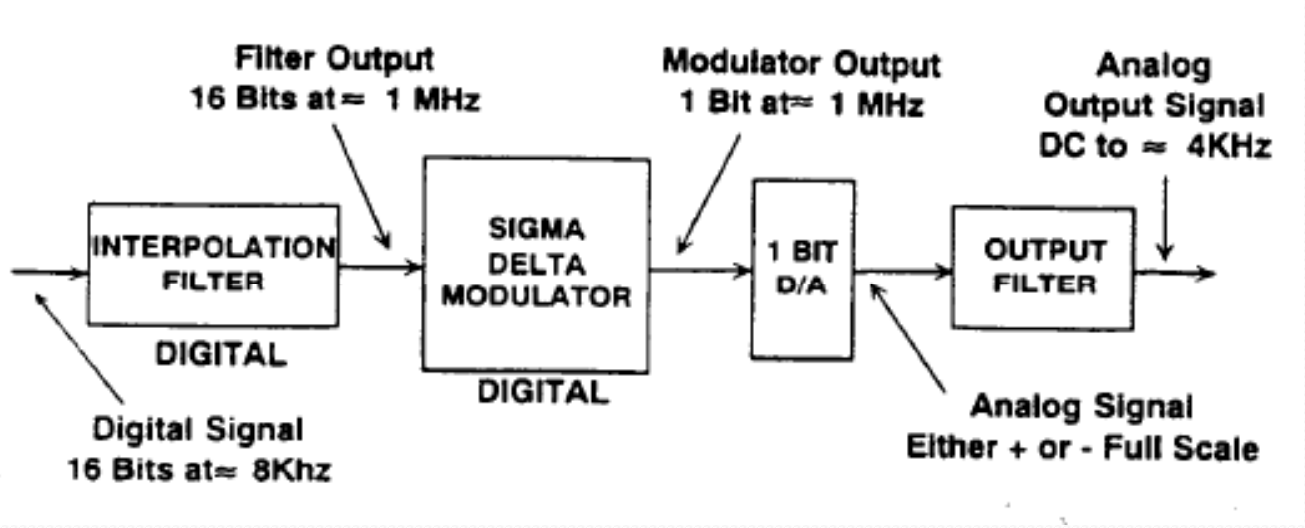
Block diagram of an oversampling DAC.

• interpolator increases the data-rate used for storing or transmitting digital signals to a much higher level: $2f_B \cdot OSR$ (reduce quantization noise) – commonly $2f_B$ close to Nyquist limit

• digital modulator reduces the number of bits for a possible thermometric representation

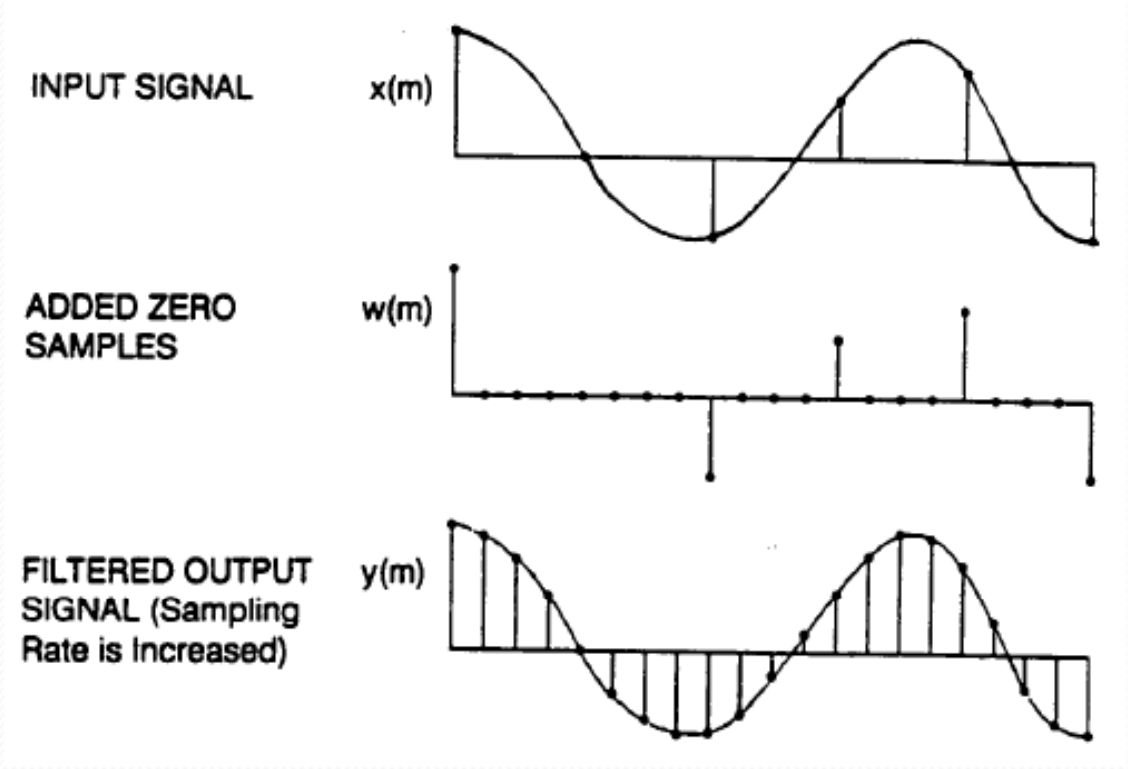
• the thermometric code is then used to control the low resolution DAC which precedes the reconstruction filter.

Ex:


Filter Output
16 Bits at≈ 1 MHz
Modulator Output
1 Bit at≈ 1 MHz
Analog
Output Signal
DC to ≈ 4KHz
INTERPOLATION
FILTER
DIGITAL
SIGMA
DELTA
MODULATOR
DIGITAL
1 BIT
D/A
OUTPUT
FILTER
Digital Signal
16 Bits at≈ 8Khz
Analog Signal
Either + or - Full Scale

• interpolation (upsampling)

ex: interpolation by a factor L = 4



• the interpolation factor (L) is normally large because a ΣΔ DAC aims at a significant reduction of the number of bit (at the limit it should go down to 1-bit)

• oversampling is common in digital audio CD players, where the basic update rate of the data from the CD is 44.1 KSPS

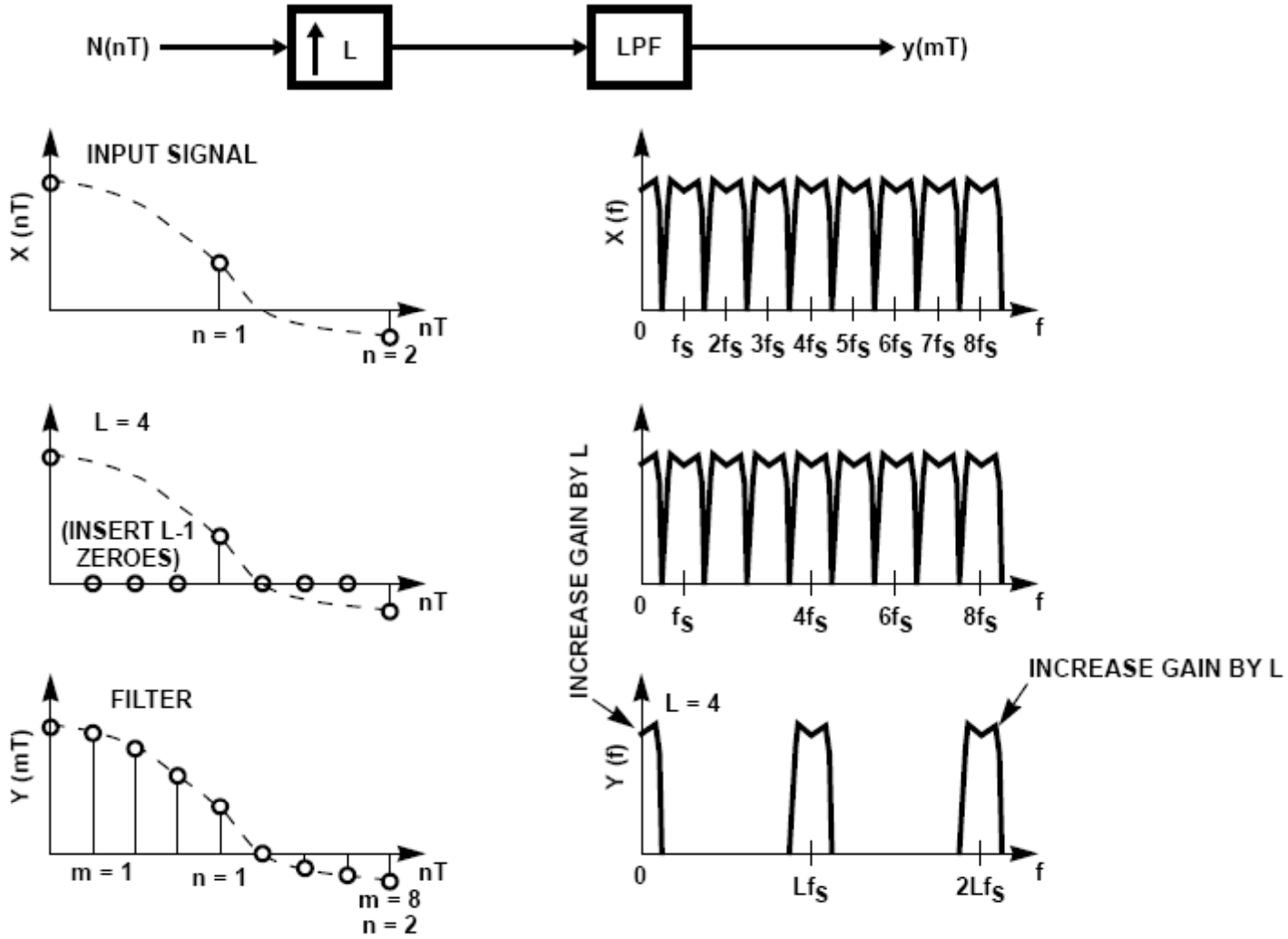
• early CD players used traditional binary DACs and inserted "zeros" into the parallel data, thereby increasing the effective update rate to 4-times, 8-times, or 16-times the fundamental throughput rate

• the 4×, 8×, or 16× data stream is passed through a digital interpolation filter which generates the extra data points.

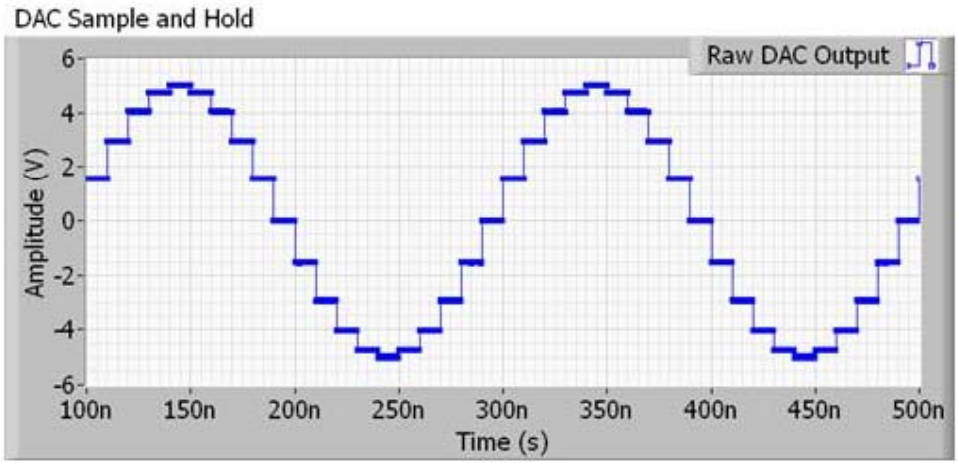
• first step: to stuff (L-1) zero-valued samples between each valid input sample, expanding the sampling rate by L, and causing the original signal spectrum to be repeated L-1 times.

• to perform the actual interpolation, the zero-valued input samples must be converted to approximations of signal samples ⇒ equivalent to preserving the original signal spectrum.

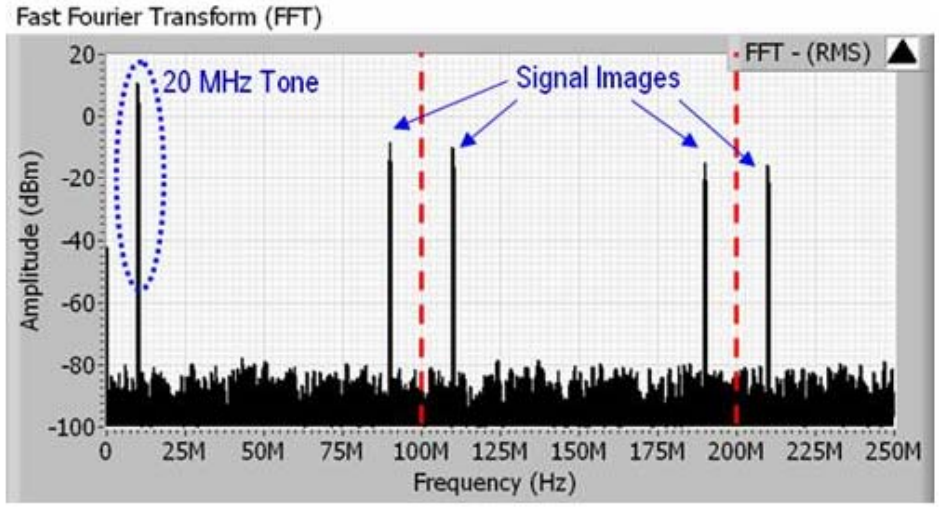
• effectively, the zero-stuffed input stream is filtered by a low-pass filter with a pass band at the original spectrum location. ⇒ this filters out all of the repeated spectra.



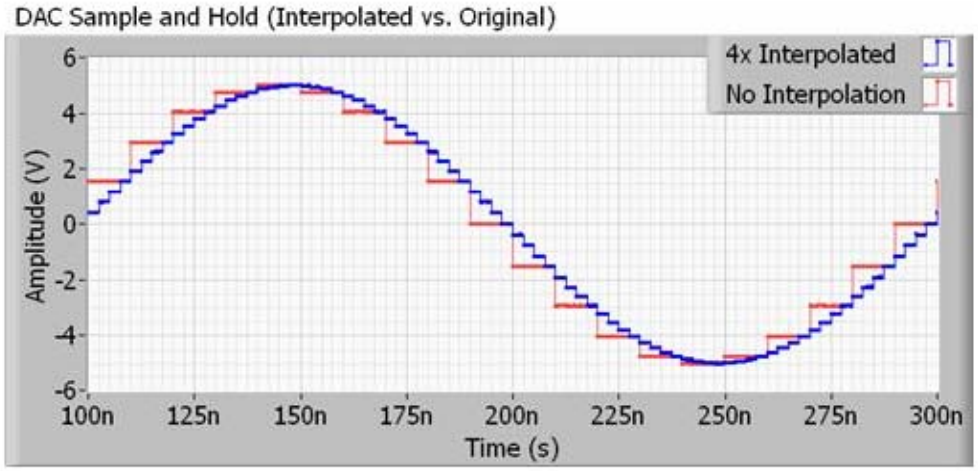
BLOCK DIAGRAM AND SPECTRAL REPRESENTATION OF THE INTERPOLATION PROCESS



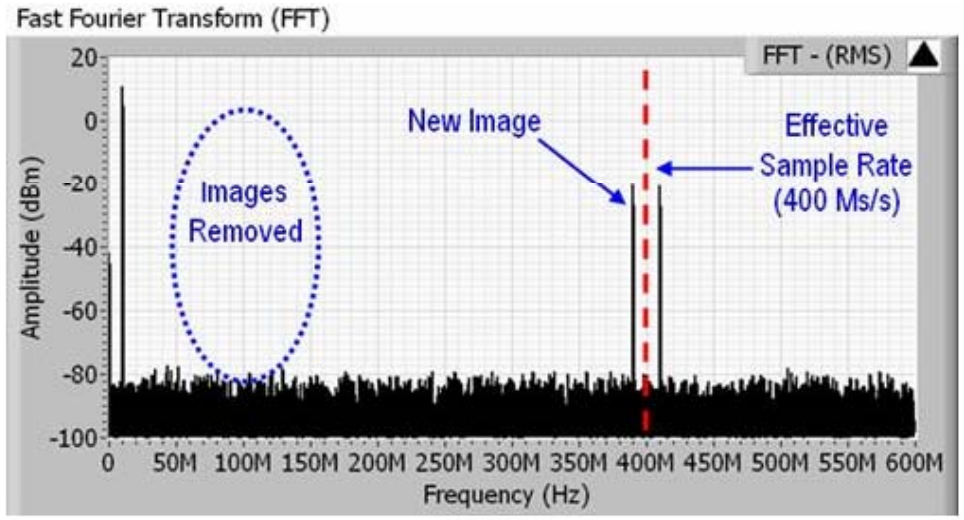
DAC Sample-and-Hold Output



Spectral Images of a 20 MHz Sine Wave

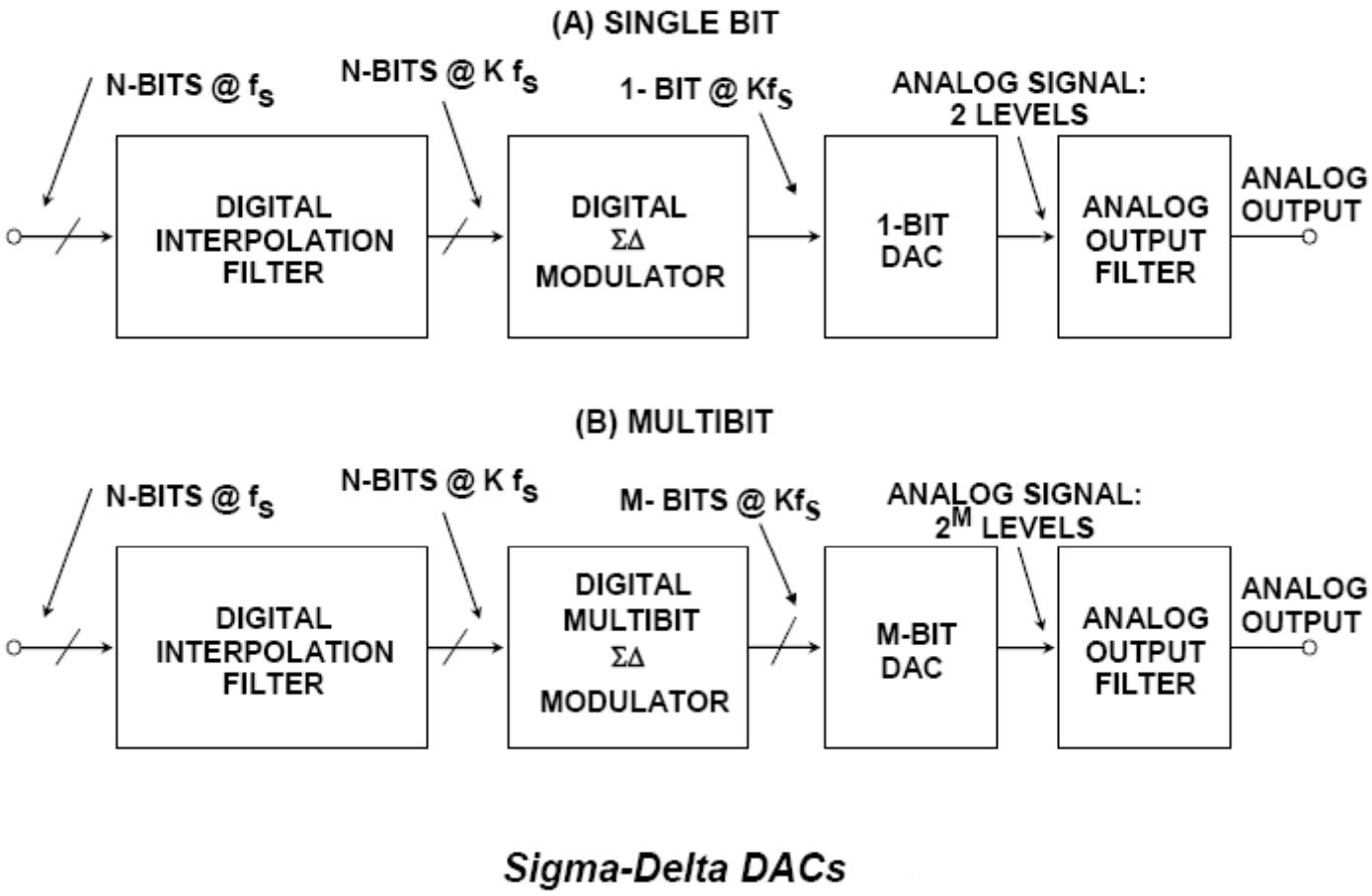


Interpolated DAC Output



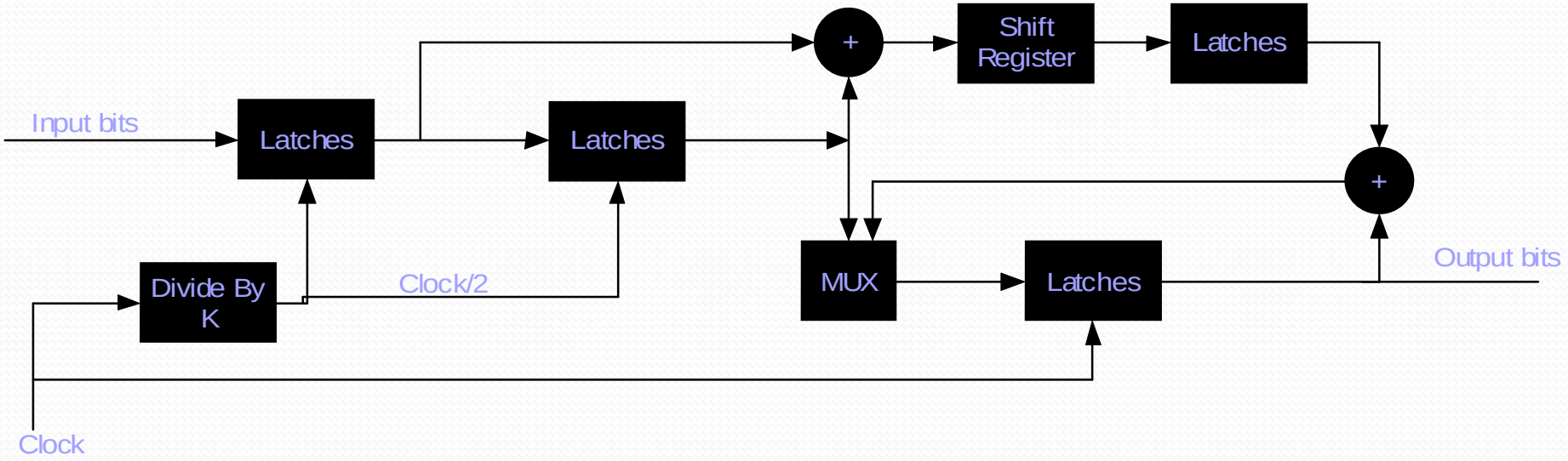
Spectral Images of a 20 MHz Sine Wave with 4X Interpolation

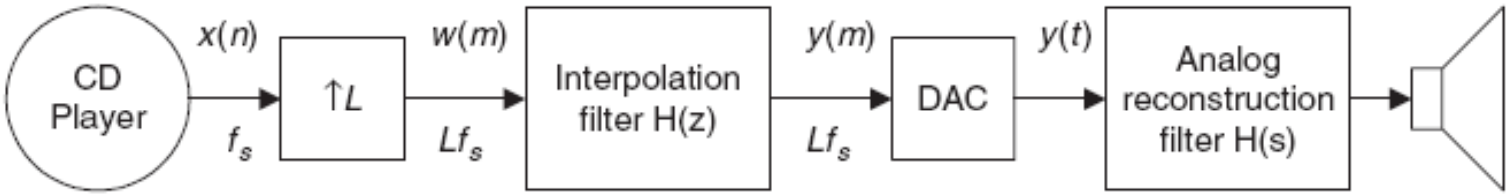
Σ–Δ DAC: fully digital



Sigma-Delta DACs

Interpolation filter block diagram





Sample rate conversion in the CD audio player system.

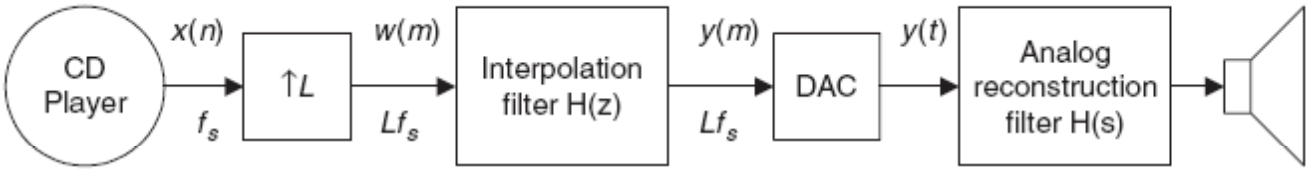
• each raw digital sample recorded on the CD audio system contains 16 bits and is sampled at the rate of 44.1 kHz.

• audio signal has a bandwidth of 22.05 kHz

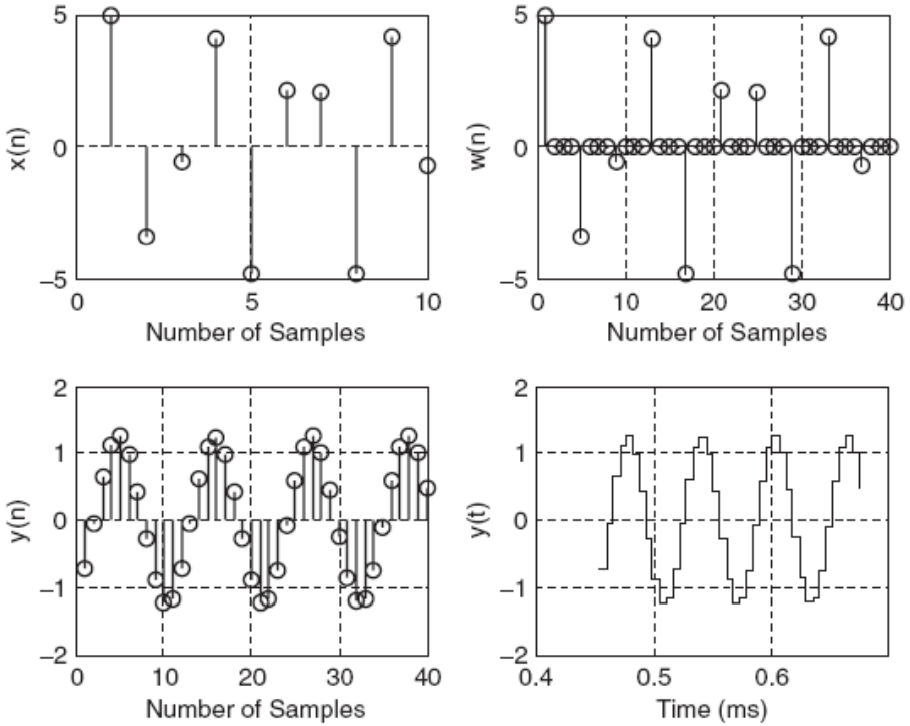
• without upsampling and application of a digital interpolation filter
⇒ reconstruction filter (also called a smooth filter or anti-image filter) to remove all image frequencies beyond the Nyquist frequency of 22.05 kHz.
⇒ high-order filter required (complex)

• **after digital interpolation**, the audio band is kept the same, while the sampling frequency is increased fourfold
(L = 4), that is, 44.1 x 4 = 176.4 kHz

• Since the audio band of 22.05 kHz is now relatively low compared with the new folding frequency (176.4/2 = 88.2 kHz), the use of a simple first-order or second-order analog anti-image filter may be sufficient.



Sample rate conversion in the CD audio player system.



Plots of signals at each stage according to the block diagram