Resizing Rules for MOS Analog-Design Reuse

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The migration of an analog circuit to a new technology usually requires a complete redesign. With the procedure presented here, designers can calculate parameters for a given circuit in a new technology, starting from the same design in an earlier technology. The procedure's simple resizing rules have been verified with standard MOSFET simulation models.

THE SCALING OF physical dimensions has long been a subject of curiosity, fiction, and scientific investigation. As Fowler points out, one of Galileo's most remarkable contributions to science is the observation that if an object's size increases, with all its proportions remaining the same, the enlarged object may have dramatically different physical properties than the original object—that is, it will not be just a scaled-up version of the same thing.[1] To illustrate his observation, Galileo drew the sketch shown in Figure 1.[2] The sketch shows two bones, one three times the length of the other. The longer bone's thickness has multiplied to the point that, for a correspondingly large animal, it would perform the same function—sustaining the animal's weight—that the small bone performs for a small animal. With this example, Galileo shows that a scaled-up physical structure may need to have a shape different from the original shape to preserve its function. Galileo explained that "the smaller the body, the greater its relative strength."[2]

Galileo's observation holds true in the world of ICs. Scaling down all dimensions has continuously reduced digital circuits' power-delay product, an important measure of device performance. Indeed, in so-called constant-electric-field scaling, whereby all dimensions and supply voltage are divided by the same constant factor α, researchers[3] have shown that to a first-order approximation the power-delay product scales down by the factor α^3. On the other hand, analog circuits do not clearly benefit when technology scales down. In fact, scaling down circuit dimensions can adversely affect some properties or functions of analog circuits.

The advent of deep-submicron processes has facilitated system-on-a-chip (SoC) design, while widening the gap between design complexity and designers' productivity. Time-to-market pressure makes this gap more challenging and consequently makes a more efficient design methodology mandatory. Systematic design reuse is such a methodology. It is a practical solution to designing SoCs that incorporate both analog and digital functions.[4]

In conventional digital-circuit design, transistor width is usually the only degree of freedom, whereas in analog-circuit design, bias is an additional fundamental variable.[5] For digital-circuit designers, the primary tradeoff is between speed and power dissipation, but analog-circuit designers must consider other specifications such as dynamic range and gain-bandwidth product. Because CMOS technology is scaled to improve the integration of digital

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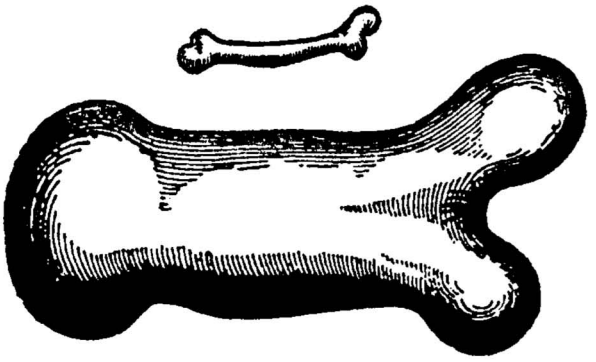
circuits, an analog design's migration to a new technology is not straightforward and usually involves a complete redesign.[6]

We have developed a methodology for analog-circuit technology migration using the physics-based MOSFET model described in an earlier article.[7] We have derived simple formulas for calculating transistor dimensions and bias for a given circuit in a new-generation technology, starting from the same circuit topology in an earlier technology. The MOSFET model we chose is particularly suitable for transistor sizing because one equation covers all its operating regions, it uses normalized variables, and it has fewer parameters than other models. Although we derived our set of resizing rules from a particular MOSFET model, these rules are generally valid. They are based on the MOS transistor's fundamental structural parameters and are applicable to widely available simulation models.



From Galileo Galilei, *Dialogues Concerning Two New Sciences*, p. 131 (Amherst, N.Y.: Prometheus Books), published 1991. Reprinted by permission of the publisher.

Figure 1. Galileo's sketch shows the large disproportion between two bones that perform the same function for a small animal and a large animal.

MOSFET model

As Figure 2a shows, the MOSFET in voltage amplifiers operates as a voltage-to-current converter, with the gate voltage controlling the drain current. Two of an amplifier's main design parameters are gate transconductance, g_m, and output conductance, g_d, which represent the drain current's dependence on the gate voltage and the drain voltage, as Figure 2b shows. Figure 2c illustrates a small-signal, low-frequency, equivalent MOSFET circuit whose source and bulk are short-circuited. A voltage amplifier achieves maximum gain if the MOSFET operates in the saturation region, where the drain current's dependence on the drain voltage is minimal. In Figure 2b, the saturation region is to the right of the curve's knee.

For analog amplifier design reuse, we associate the small-signal parameters g_m and g_d with technology, drain current, and transistor dimensions. The MOSFET model we used was developed for the needs of analog designers. It uses the current as the main variable and provides a unified treatment of the MOSFET for any operating region, whether the MOSFET is in weak, moderate, or strong inversion. In weak inversion, the current depends exponentially on the gate voltage; in strong inversion, the current is

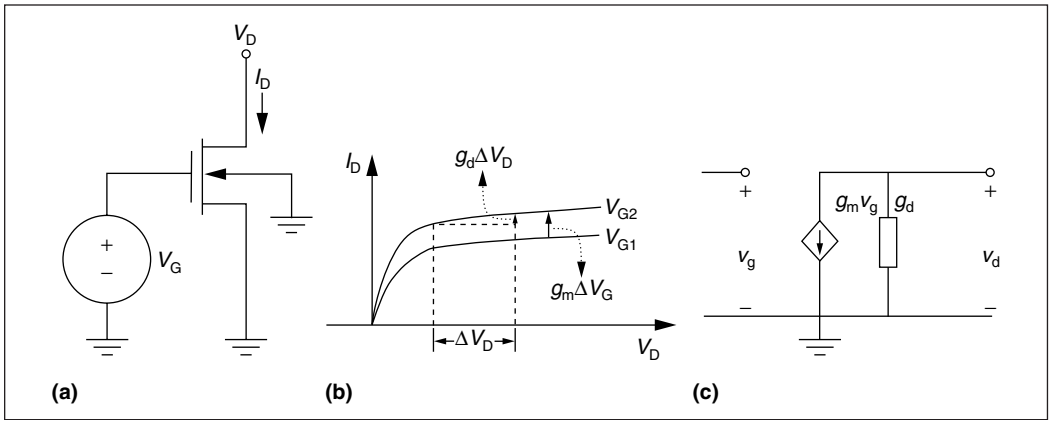


Figure 2. An *n*-channel MOSFET (a); a graphical representation of the MOSFET's gate transconductance and output conductance (b); and a small-signal, low-frequency, equivalent circuit (c).

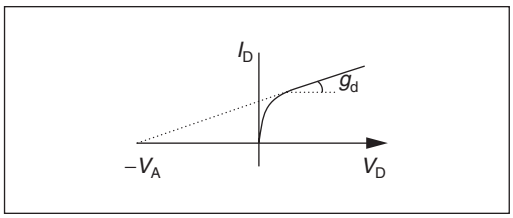


Figure 3. Definition of Early voltage.

proportional to the square of the gate overdrive voltage. Moderate inversion represents the transition from weak to strong inversion.

The following equations contain the basic information required to define the scaling rules and are suitable for MOSFETs operating in the saturation region:

$$\frac{\phi_t n g_m}{I_D} = \frac{2}{1+\sqrt{1+i_f}} \quad (1)$$

$$i_f = \frac{I_D}{I_S} \quad (2)$$

$$I_S = \mu n C'_{ox} \frac{\phi_t^2}{2} \frac{W}{L} \quad (3)$$

The MOSFET transconductance-to-current ratio given by equation 1 is a universal relationship, valid for any technology, dimensions, or temperature. The transconductance g_m depends on both the drain current, I_D, and the normalized drain current, or inversion level, i_f.[7] The inversion level represents the normalized carrier-charge density at the MOSFET source. As a rule of thumb, values of i_f greater than 100 indicate strong inversion, values less than 1 indicate weak inversion, and values from 1 to 100 indicate moderate inversion. I_S, the normalization current, depends on the aspect ratio (W/L, where W and L are the channel width and length) and on technological factors—namely, mobility, μ, and oxide capacitance per unit area, C'_{ox}. The term ϕ_t denotes the thermal voltage, and n is the slope factor, which is slightly greater than 1 and almost bias independent.

A transistor's maximum voltage gain is limited by its source-to-drain conductance g_d, which is approximately proportional to the ratio of the drain current to the channel length:

$$g_d = I_D/V_A = I_D/V_E L \quad (4)$$

where V_A is the Early voltage, as defined in Figure 3, and V_E is the Early voltage per unit length.[5] Values of V_E for 3-micron bulk and silicon-on-insulator technologies, as well as for a 1.2-micron process, are in the range of 5 to 10 V per micron.[5,8] Although V_E depends on the inversion level and on L, a constant V_E is a good approximation if the designer avoids using short-channel transistors in weak inversion, the usual practice in analog design.[5,8] As technology scales down, the Early voltage per unit length will increase slightly because of the increase in substrate doping concentration.

The MOSFET's internal capacitances limit its high-frequency operation. The transistor's ability to operate at high frequencies is indicated by the intrinsic cutoff, or transition frequency, f_T, whose value in saturation is approximated by

$$f_T \cong g_m / 2\pi\left(\frac{1}{2} C'_{ox} WL\right) = \frac{\mu\phi_t}{\pi L^2}\left(\sqrt{1+i_f}-1\right) \quad (5)$$

where $C'_{ox}\,WL$ is the gate oxide capacitance. In practice, we would limit the MOSFET's frequency operation to a fraction of f_T—say, $f_T/4$ or less. Equations 1 through 5, which model relevant aspects of analog circuits, are essential to MOS amplifier design, and we use them throughout this article to define scaling rules.

Scaling effects on analog circuits

For some applications, the gain-bandwidth product and the dynamic range, which Vittoz defines as the maximum signal-to-noise ratio,[6] are basic specifications that should be maintained in a voltage amplifier designed in a scaled-down technology.[9]

One of the simplest MOSFET amplifiers is the common-source amplifier illustrated in Figure 4a. For simplicity, we assume that the bias current I_{bias} is generated by an ideal current source and that the amplifier drives a load capacitance, C. In this amplifier, the low-frequency voltage gain, easily derived from Figure 4b, is given by the negative of the ratio of the transconductance to the output conductance:

$$G_{VO} = -(g_m/g_d) = -(g_m/I_D) V_E L \quad (6)$$

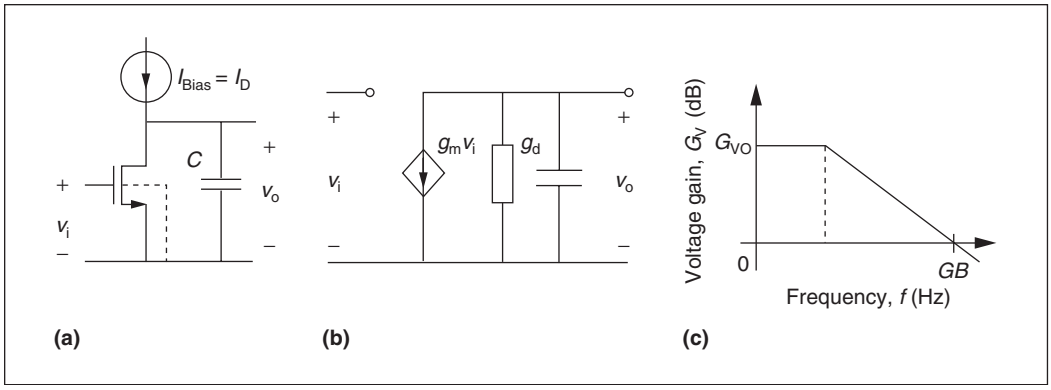


Figure 4. Common-source amplifier (a); small-signal equivalent circuit (b); gain magnitude versus frequency (c).

As the frequency increases, the capacitor reduces the voltage gain, as shown in Figure 4c. The frequency at which the voltage gain equals 1 is called the unity-gain frequency, or the gain-bandwidth product (*GB*), and is given as

$$GB = g_m/2\pi C \quad (7)$$

To comply with gain-bandwidth requirements, the MOSFET's intrinsic cutoff frequency should be higher than 4*GB*.

If we apply across *C* a sinusoidal signal voltage whose peak-to-peak value is V_{PP}, the signal power is $V_{PP}^2/8$. To keep distortion levels within acceptable values, V_{PP} must be less than the total supply voltage, V_{DD}. To simplify matters, we assume here that the maximum value of V_{PP} can equal V_{DD}. On the other hand, the minimum power *N* associated with thermal noise is limited by *C*, according to the expression $N = kT/C$, where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann's constant, and *T* is the absolute temperature.[6] In this case, the dynamic range *DR* is

$$DR = V_{DD}^2 C / 8kT \quad (8)$$

We conclude, from equations 7 and 8, that to keep the same *DR* and *GB*, both *C* and g_m must increase by the square of the supply-voltage-scaling factor (K_V^2), as long as the voltage supply scales down by a factor equal to K_V.

Analog resizing rules

To generalize the resizing rules for MOS analog-design reuse, we now define different scaling factors for supply voltage (K_V), oxide thickness (K_{ox}), and channel length (K_L), as Figure 5 shows. We also include scaling factor K_E, associated with Early voltage per unit length.

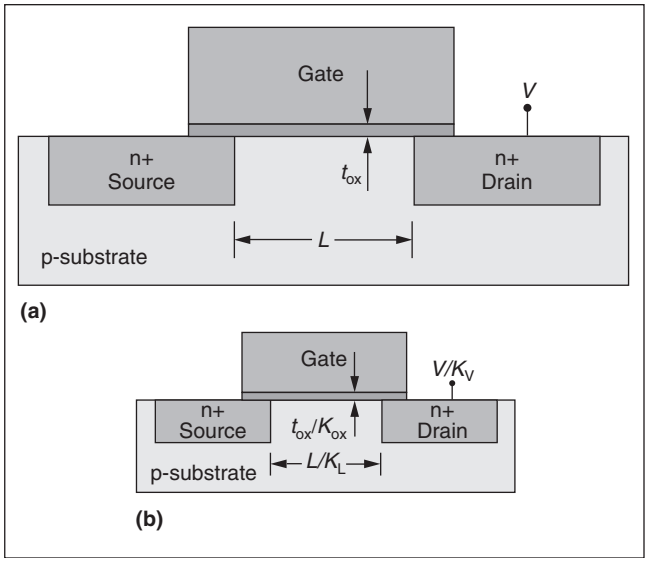


Figure 5. Generalized scaling: original design (a); scaled-down design (b).

In designing transistors for analog circuits, designers usually consider three independent parameters: channel width *W*, channel length *L*, and bias current I_D.[5] For the following resizing rules, we maintain the original dynamic-range and gain-bandwidth-product specifications. As long as the amplifier's frequency specification (*GB*) does not change in the new technology, we also maintain the transistors' original transition frequency. Constant-inversion-level and channel-length scaling are the strategies for reusing ana-

Table I. MOS transistor-resizing rules using generalized scaling factors $V_{PP} \rightarrow K_V^{-1}V_{PP}$, $C'_{ox} \rightarrow K_{ox}C'_{ox}$, $L \rightarrow K_L^{-1}L$, $V_E \rightarrow K_E V_E$.

Quantity	Constant-inversion-level scaling	Channel-length scaling	
L	1	K_L^{-1}	
W	$K_V^2 K_{ox}^{-1}$	$K_V^2 K_{ox}^{-1} K_L$	
		Weak inversion	Strong inversion
I_D	K_V^2	K_V^2	$K_V^2 K_L^{-2}$
i_f	1	K_L^{-2}	K_L^{-4}
G_{V0}	K_E	$K_E K_L^{-1}$	$K_E K_L$

log cells. Table 1 lists the transistor-resizing rules.

Constant-inversion-level scaling

As equation 1 shows, g_m/I_D is a function of inversion level i_f. Because n is almost technology insensitive, constant-inversion-level scaling keeps g_m/I_D constant. The scaling factor for g_m is K_V^2, so the current must also be multiplied by K_V^2. Assuming the carrier mobility is constant, it follows from equation 5 that L must remain the same for the transition frequency to remain constant. We deduce the scaling factor for W from equations 2 and 3. In constant-inversion-level scaling, static power consumption increases by K_V, and active area scales up by $K_V^2 K_{ox}^{-1}$. Finally, equation 6 shows that voltage gain is proportional to V_E; that is, voltage gain will increase slightly.

An interesting case is the redesign of an analog cell for a lower supply voltage in the same technology ($K_{ox} = 1$, $K_E = 1$). Table 1 verifies that the new analog circuit can be viewed as a width-scaled replica of the original circuit.[10] In effect, as the channel width scales up by K_V^2, transistor lengths and current densities remain the same as in the original design. Figure 6 illustrates the redesign of an analog circuit, showing how to scale the three main components to comply with the specifications when the supply voltage scales down by K_V.

Channel-length scaling

To take advantage of the smaller dimensions of a new-generation technology, channel-length scaling ($L \rightarrow L/K_L$) is a natural choice. For the same set of analog specifications, channel-length scaling implies a reduction of the inversion level, which can be advantageous in analog circuits.

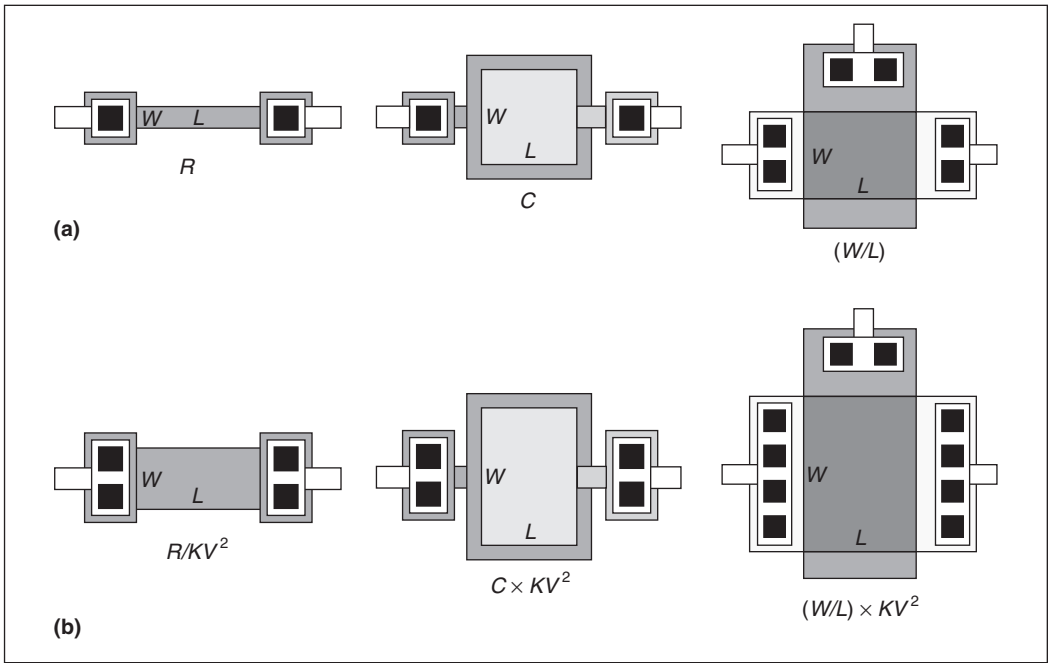


Figure 6. Redesign in the same technology of three components (resistor, capacitor, and transistor) of an analog circuit for a lower supply voltage ($K_{ox} = 1$): original design (a); new design (b).

Table 2. Simulated performance of a common-source amplifier in 1.2-micron and 0.35-micron technologies. (K_V = 2.5, K_{ox} = 3, and K_L = 3.4.)

Design	i_f	W (μm)	L (μm)	I_D (μA)	g_m/I_D (V^{-1})	G_{VO} (dB)	GB (MHz)	Noise (μV)
Original (1.2-μm technology)	24.0	160	10.0	6.0	10.7	67.3	1.03	11.2
Constant-i_f scaling (0.35-μm technology)	24.0	323	10.0	37.5	8.1	64.3	0.80	4.9
Channel-length scaling (0.35-μm technology)	0.8	1,109	2.8	14.6	22.1	63.3	0.86	4.9

We first scale down the channel length by the factor K_L. As follows from equation 5, for the transition frequency to remain the same as in the original design, the scaling factor for W must be $K_V^2 K_{ox}^{-1} K_L$. From knowledge of the scaling factors for L and W and from equation 3, it follows that we must scale normalization current I_S by $K_V^2 K_L^2$. We calculate the inversion-level reduction associated with channel-length scaling from equation 5. Finally, we derive the scaling factor for I_D from equation 2.

We now consider the important case in which the transistors operate in strong inversion and the channel shortens by a factor equal to K_L. Using the strong-inversion ($i_f > 100$) approximation for equation 5, we derive the inversion-level scaling factor K_L^{-4}. Scaling factor $K_V^2 K_L^{-2}$ for I_D follows from equation 2. In channel-length scaling at strong inversion, the inversion level decreases and the g_m/I_D ratio multiplies by K_L^2. Compared with constant-inversion-level scaling, static power consumption decreases by a factor equal to K_L^2. Finally, as equation 6 shows, the voltage gain increases by $K_E K_L$.

The results for weak inversion in Table 1 are easily derived from the weak-inversion ($i_f < 1$) approximation of equation 5.

Because weak and strong inversions are limiting conditions, a practical reuse procedure must handle operation under any inversion level, including moderate inversion. As shown in the "Redesign equations" sidebar (next page), each transistor's channel length scales according to its inversion level to attain a constant scaling factor for all currents.

The choice between constant-inversion-level and channel-length scaling depends on several factors. Strong-inversion operation is not power efficient but is unavoidable in some high-frequency applications. On the other hand, moderate inversion achieves the best compromise between consumption and speed.[8] Consequently, designers can more conveniently reuse a design in which transistors operate in strong inversion by using channel-length scaling to reduce the inversion level and thus decrease power consumption, rather than using constant-i_f scaling. For transistors operating in moderate inversion, designers can use channel-length or constant-i_f scaling, depending on the design's specific demands.

Examples

First, we designed a common-source amplifier with a p-channel driver biased by an ideal current source, and with C = 10 pF as the load, for a 1.2-micron CMOS technology and a 5-V power supply. Using both the constant-i_f and channel-length-scaling rules, we recalculated the amplifier's load capacitance (C = 62.5 pF), dimensions, and bias current for a 0.35-micron technology and a 2-V power supply. Our noise calculation assumed the amplifier would operate with a feedback factor equal to 1.

Table 2 shows the results of the scaling rules. For constant-i_f scaling, power consumption increases by K_V and the specifications are almost the same as in the primary design. Channel-length scaling shows an improvement in power consumption over constant-i_f scaling. The results show that the variation in low-frequency gain (G_{VO}) is not large. However, designers should not rely completely on simulation results to assess voltage gain because circuit simulators generally don't model output conductances well. Finally, to account for variations of the mobility and slope factors, some fine-tuning may be required after the scaling rules are applied.

As a second example, we redesigned the Miller Operational Transconductance Amplifier (Laker and Sansen,[5] p. 490), which is shown in

Redesign equations

The design of a MOS transistor in analog circuits involves three degrees of freedom: channel width (W), channel length (L), and drain current (I_D).[1] In our reuse procedure, each transistor is redesigned from an alternative set of specifications: intrinsic cutoff frequency (f_T), gate transconductance (g_m), and I_D. To maintain the same ac performance as in the original circuit, we keep f_T constant and scale the transconductances by the same factor K_V^2. In constant-inversion-level scaling, currents as well as transconductances are scaled by the same factor K_V^2. In channel-length scaling, currents are multiplied by a factor lower than K_V^2.

Constant-inversion-level scaling

Using scaling factor K_μ for the mobility of carriers ($\mu \rightarrow \mu \bullet K_\mu^{-1}$), the scaling rules for the channel geometry are

$$L \rightarrow L \bullet K_\mu^{-1/2} \quad \text{(A1)}$$

$$W \rightarrow W \bullet K_V^2 \bullet K_{OX}^{-1} \bullet K_\mu^{1/2} \quad \text{(A2)}$$

In the example shown in Figure 7, we reduced the channel length by a factor of $1.6^{1/2} \cong 1.25$ to compensate for mobility reduction.

Channel-length scaling

In the general case of arbitrary-inversion-degree i_f, we calculate the new inversion level i_{fN} from

$$i_{fN} = \left[K_\mu K_L^{-2}\left(\sqrt{1+i_f}-1\right)+1\right]^2 - 1 \quad \text{(A3)}$$

The drain current scaling factor I_{DN}/I_D is

$$(I_{DN}/I_D) = (i_{fN}/i_f) \bullet K_V^2 \bullet K_L^2 \bullet K_\mu^{-1} \quad \text{(A4)}$$

To apply channel-length scaling to a MOSFET circuit, we can fully scale the channel length of the device operating at the lowest inversion level ($L \rightarrow K_L^{-1}L$). We determine the current-scaling factor for the whole circuit, $K_I = I_{DN}/I_D$, from equations A3 and A4 for the transistor operating at the lowest inversion level. For the remaining devices, the channel-length-scaling factor K'_L depends on the inversion level i_f and is given by

$$K_L'^2 = K_\mu \frac{\sqrt{1+i_f}-1}{K_I K_V^{-2}\left(\sqrt{1+i_f}+1\right)-2} \quad \text{(A5)}$$

Because expression A5 is a decreasing function of i_f, the higher the inversion level, the lower the channel-length-scaling factor. In the example in Figure 7, we fully scaled the channel length of transistor M6, the one with the lowest inversion level. Using equation A3 with $i_f = 47$, $K_L = 8.6$, and $K_\mu = 1.6$, we obtained the value $i_{fN} = 0.27$ for transistor M6. We inserted the parameters of M6 ($i_f = 47$, $i_{fN} = 0.27$, $K_L = 8.6$), $K_V = 1.5$, and $K_\mu = 1.6$ into equation A4 to calculate the current's scaling factor. The result was $K_I = 0.61$.

We calculated the channel-length-scaling factors for the remaining transistors from equation A5, yielding $K'_L = 5.1$, 3.7, and 3.0 for transistors with inversion levels of 62.5 (M3, M4), 110 (M1, M2), and 275 (M5, M7, M8), respectively.

Reference

1. K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, New York, 1994.

Figure 7. We redesigned the OTA—originally in a 3-micron technology and a 5-V power supply—for a 0.35-micron technology and a 3.3-V power supply. In the redesign, we took mobility differences into account and used more accurate expressions for calculating the current and the inversion level, as described in the "Redesign equations" sidebar.

We performed channel-length scaling of the OTA as follows:

- We fully scaled the channel length of M6, the transistor with the smallest inversion level ($L \rightarrow K_L^{-1}L$). We calculated W_6 according to Table 1 and the inversion level and current according to equations A3 and A4 in the sidebar.
- We kept the same proportion in the currents through the new circuit's branches as in the original circuit. Therefore, once we determined the current through M6, we knew all the transistor currents in the new circuit.
- After determining the currents, we used equation A5 to determine the remaining transistors' channel-length-scaling factors. We calculated the transistor widths using

Table 1 and the corresponding channel-length-scaling factors already determined.

Table 3 shows the transistors' dimensions, and Table 4 summarizes the OTA's simulated ac behavior. We obtained the simulation results using a level-2 MOSFET model[5] for the 3-micron design and the Berkeley Short-Channel IGFET Model (BSIM 3v3) for the 0.35-micron technology. As Table 4 shows, the OTA's ac performance is almost the same for constant-inversion-level and channel-length scaling. Channel-length scaling, however, shows improved performance over constant-i_f scaling with regard to power consumption.

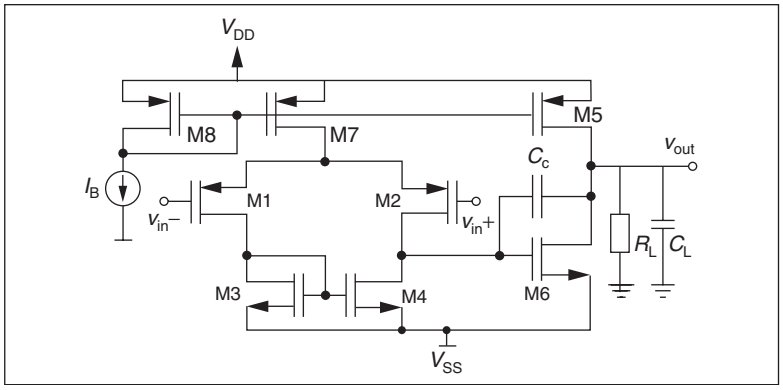


Figure 7. The Miller CMOS Operational Transconductance Amplifier.

Table 3. OTA parameter values.

Transistor	Design	W (μm)	L (μm)	i_f	I_D (μA)
M1, M2	(1)	26.00	16.00	110.00	1.25
	(2)	13.60	12.80	110.00	2.86
	(3)	40.40	4.25	3.40	0.75
M3, M4	(1)	10.00	10.00	62.50	1.25
	(2)	5.25	8.00	62.50	2.86
	(3)	21.70	1.90	0.96	0.75
M5	(1)	55.00	5.00	275.00	22.30
	(2)	28.75	4.00	275.00	48.70
	(3)	67.50	1.65	13.10	11.30
M6	(1)	115.00	5.00	47.00	22.30
	(2)	60.10	4.00	47.00	48.70
	(3)	404.60	0.60	0.27	11.30
M7, M8	(1)	13.00	10.00	275.00	2.50
	(2)	6.80	8.00	275.00	5.75
	(3)	16.00	3.35	12.80	1.50
	Design	**C_c (pF)**	**C_L (pF)**	**R_L (kΩ)**	
	(1)	1.0	10	100.0	
	(2)	2.3	23	43.6	
	(3)	2.3	23	43.6	

(1) Original design: 3-μm technology; (2) constant-i_f scaling: 0.35-μm technology; (3) channel-length scaling: 0.35-μm technology

THE WORK PRESENTED HERE is an example of how using a current-mode approach based on a MOSFET model in which the current is the fundamental variable can reduce analog-design complexity. In the current-based model, only one parameter, the specific current I_S, contains the essential information on the transistor's technology, geometry, and temperature. The reuse procedure for amplifiers can be extended to both continuous-time filters and sampled-data circuits. A systematic current-mode analog-design methodology is under development in our laboratory. ■

Acknowledgment

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Table 4. Simulated performance of the OTA in 3-μm and 0.35-μm technologies. (K_V = 1.5, K_{ox} = 5.5, and K_L = 8.6.)

Design	G_{VO} (dB)	Phase margin (degrees)	GB (MHz)	Total current (μA)
(1)	73	65	1.00	27
(2)	77	63	0.91	60
(3)	74	60	0.90	14

(1) Original design: 3-μm technology; (2) constant-i_f scaling: 0.35-μm technology; (3) channel-length scaling: 0.35-μm technology

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