

Semicondutores e Nanotecnologia

Jacobus W. Swart

CCS e FEEC

UNICAMP

Sumário

1. Introdução e conceitos
2. Evolução dos semicondutores
3. Outras aplicações do processo planar
4. Atividades no CCS/UNICAMP
5. Considerações Finais.

1. Introdução

PITCE - Opções Estratégicas

Semicondutores

Software

Bens de capital

Fármacos e Medicamentos

Portadores de Futuro

Biotecnologia

Nanotecnologia

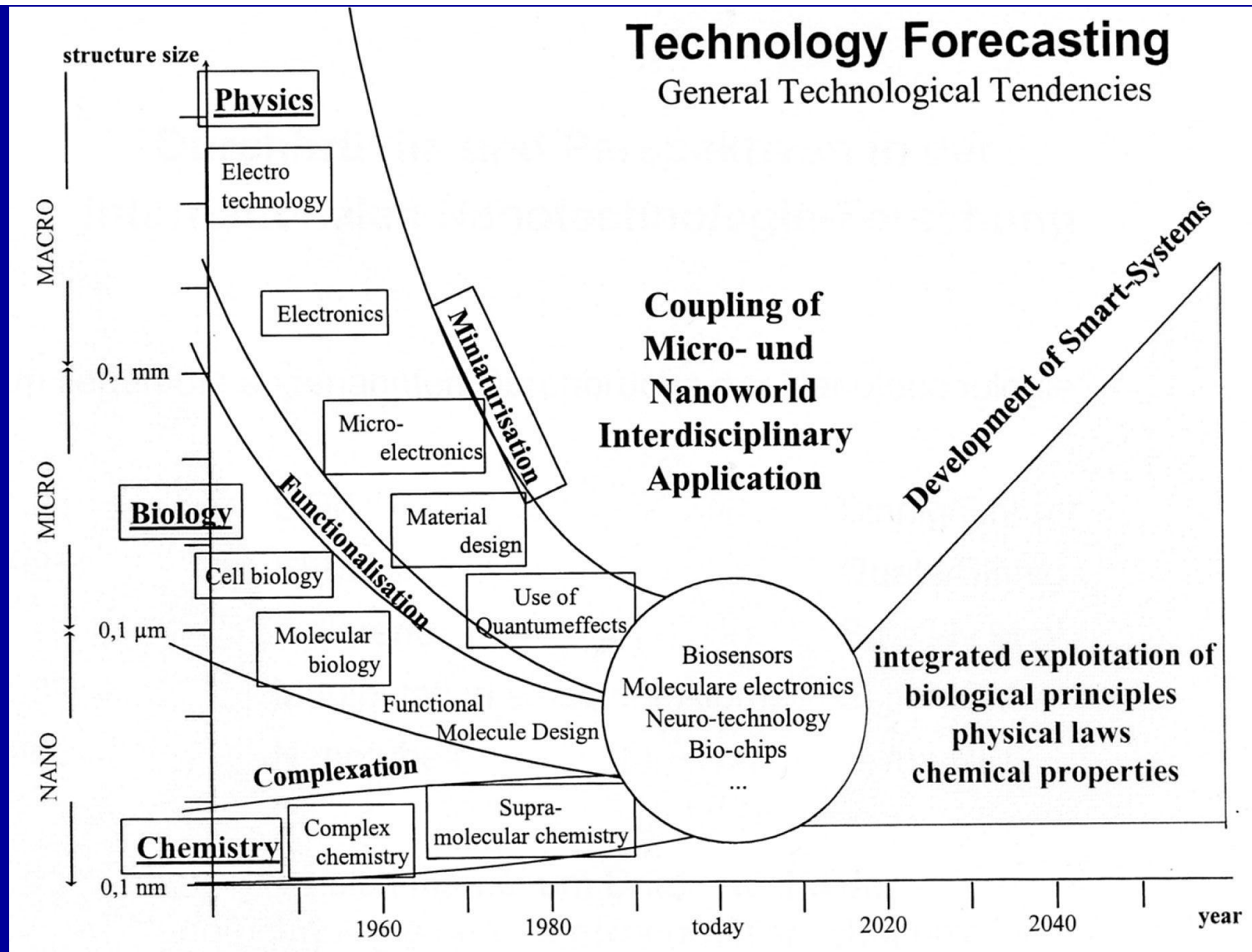
Biomassa

O que é nanotecnologia?

1. Estruturas com dimensões menores que 100 nm
2. Estruturas com dimensões tais que suas propriedades diferem das mesmas com dimensões maiores.
 - Exemplo: nano-partículas \Rightarrow discretização das bandas de energia \Rightarrow altera propriedades.
 - Há 2 séculos, Faraday já atribuiu as diferenças de cor entre amostras de ouro coloidal à diferença no tamanho das partículas.

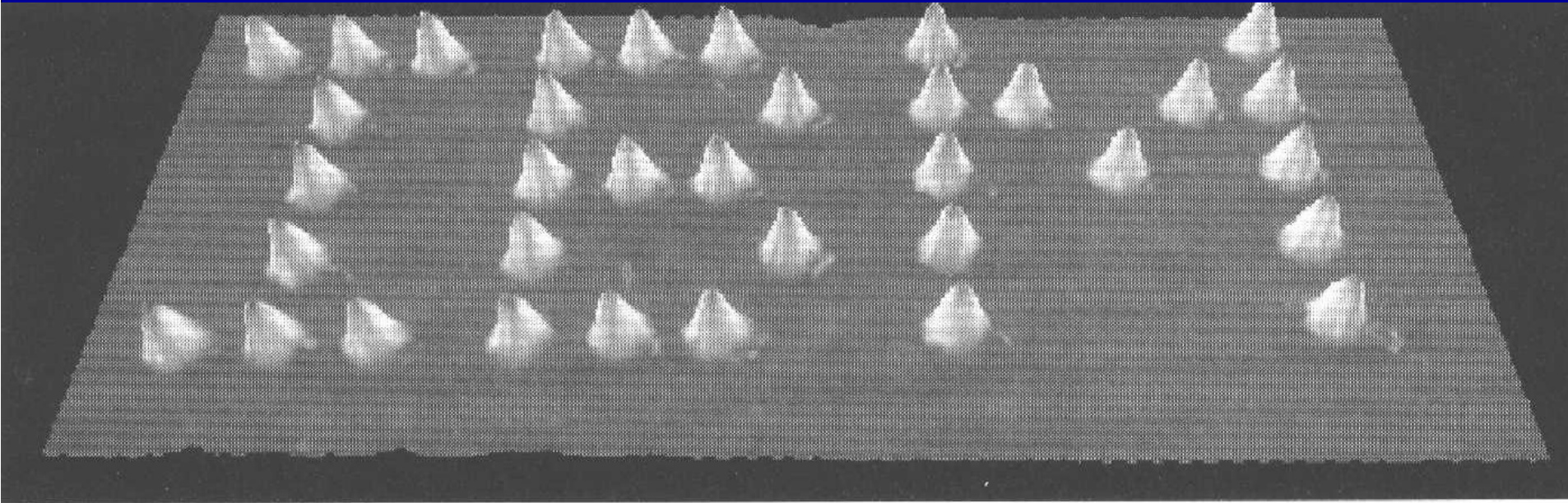
Qual a área de aplicação de nanotecnologia?

- Não tem resposta única!
- Ela é permeia todas as áreas (“*is pervasive*”).
- Vai de medicina, roupa, eletrônica a pavimentação de estradas.
- É uma convergência da física, química, materiais, engenharia, biologia, etc – trata de átomos e moléculas.



Richard Feynman, em 1959, disse corretamente:
“There is Plenty of Room at the Bottom e que um dia seria possível manipular átomos individualmente”.

Exemplo: logotipo IBM escrito por AFM em 1990:
posicionamento de átomos de Xe sobre superfície de Ni.



- (espaço ente átomos ~ 1 nm)
Eigler & Schweizer, Nature 1990.

Faz sentido criar um único centro de nanotecnologia?

- Possivelmente não. Nanotecnologia não cabe sob um único teto. É muito amplo.
- Faz sentido sim, centros de nanotecnologia para áreas x ou y, (*semicondutores, nanofabricação, bio-nano, por exemplo*).
- Nanotecnologia está em todas as áreas, é fundamental para cada uma.
- Nanotecnologia é o futuro para todas as áreas, é uma oportunidade para inovação.

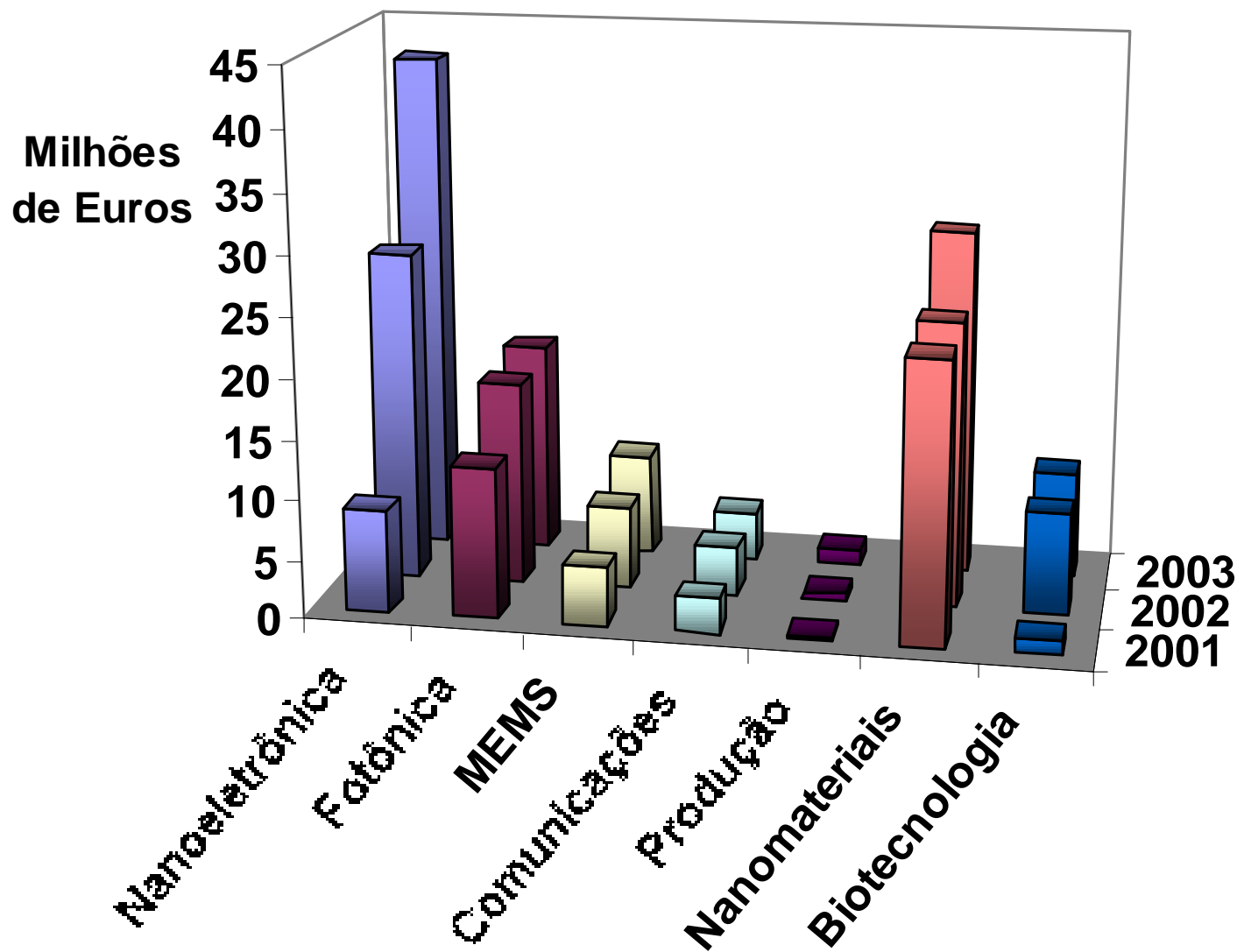
Temas de pesquisa em N&N propostos no PPA 2004-2007 – pelo GT do MCT:

- Nanofabricação
- Nanometrologia
- Materiais nanoestruturados
- Nanotecnologia funcional
- Energia
- Nanotecnologia molecular
- Nanoagregados
- Funcionalização de materiais
- Software.

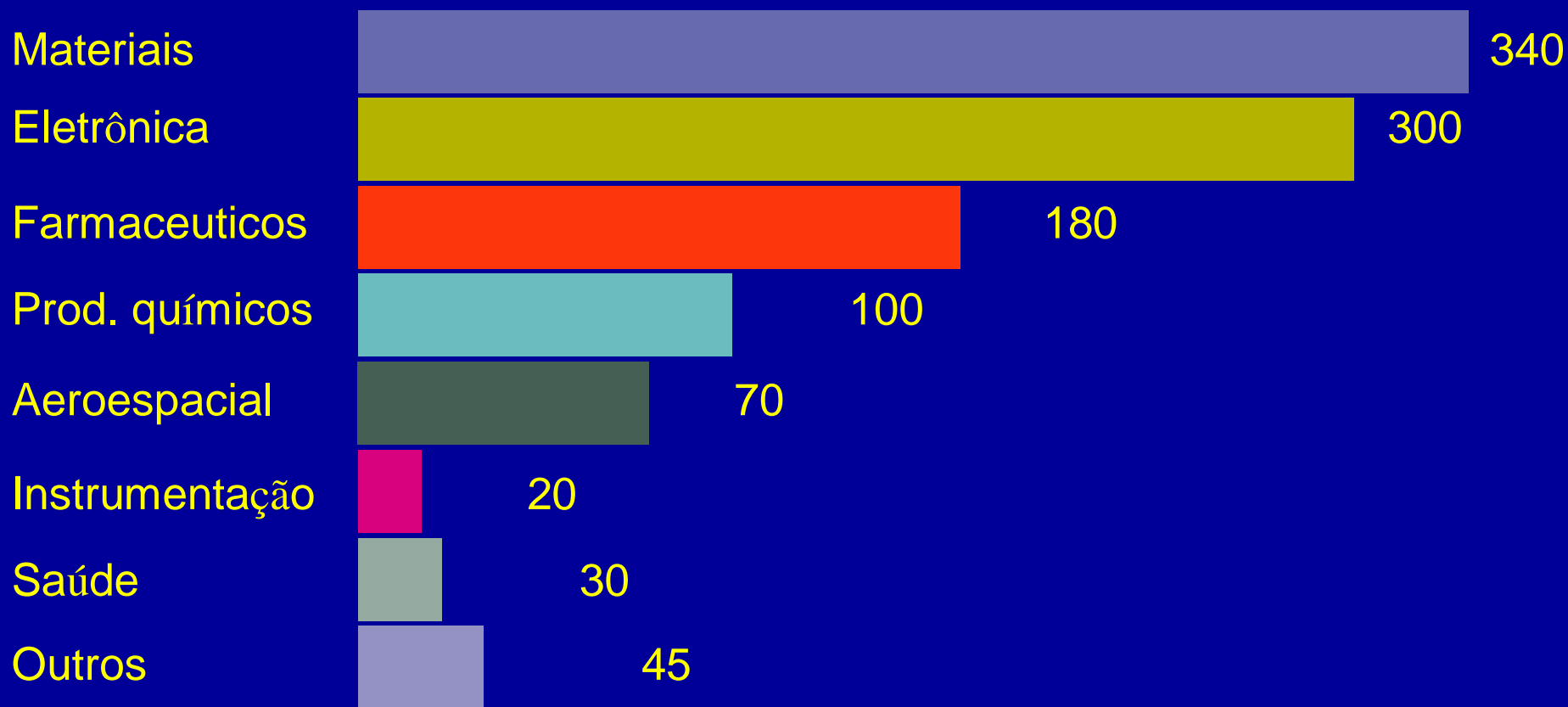
Tecnologias de nanofabricação

- “*Bottom-up*”: síntese química e criação de estrutura supramoleculares. Inclui também a manipulação de átomos por AFM, FIB, etc.
- “*Top-down*”: seqüência de deposição de filmes ou camadas seguido por processos de litografia (por luz, feixes de elétrons ou íons e *nanoimprinting*).

Temas e Investimentos em Nanotecnologias do BMBF / Alemanha



Mercados mais importantes em 2015 > 1 TUS\$



Fonte: National Science Foundation

Micro vs Nano: (Esquece micro e vamos diretamente ao nano?)

- Tem limite difuso
- *Nano* = evolução de *micro* e do conhecimento e domínio humano sobre a matéria.
- *Nano* requer infraestrutura similar (refinada) e faz uso de algumas técnicas e conceitos similares.
- *Nano* não pode prescindir da base tecnológica do *micro*. **“Microtechnology is an Enabler”**.
- **“Most nanosystems need to be embedded in a semiconductor based microsystem” (Jacques Schmitt)**

Exemplo:

Transistor com
nanotubo de
carbono.

J. Wind et. al.
A.P.L,
20/May/2002,
p.3817.

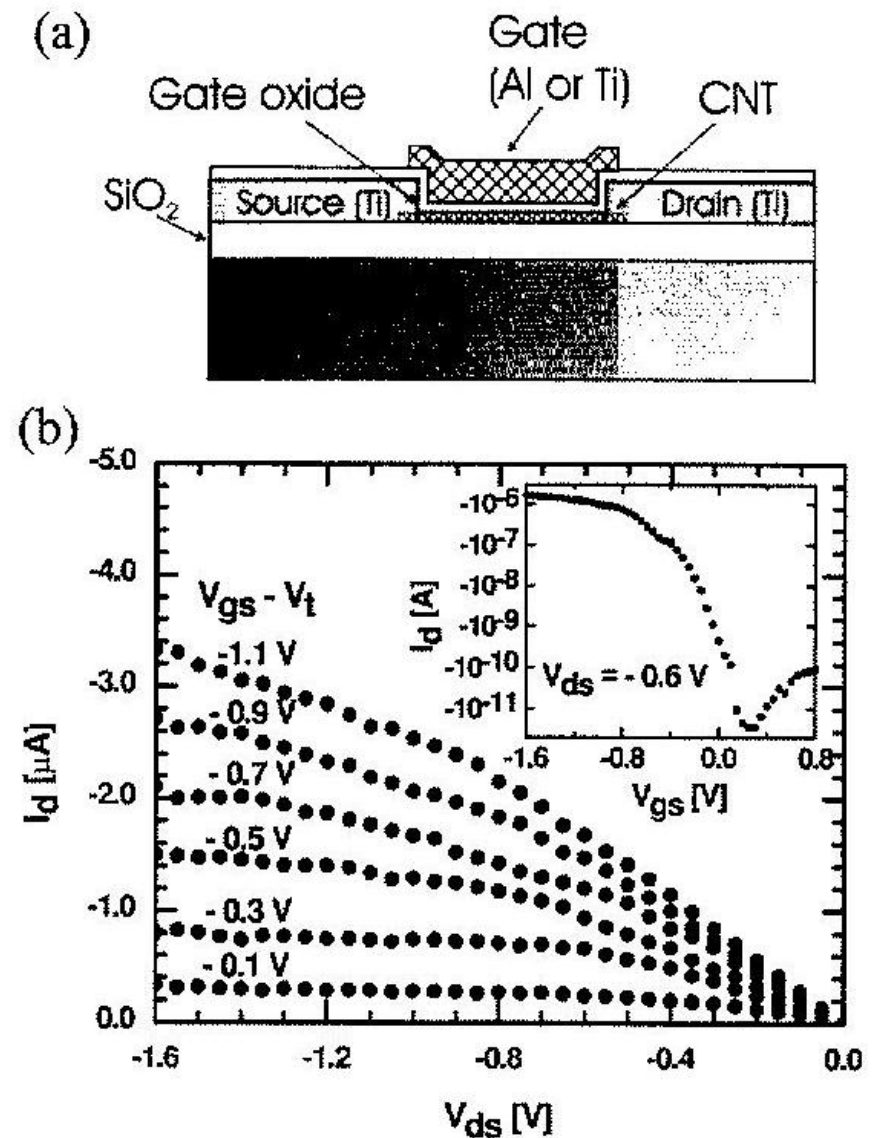


FIG. 1. (a) Schematic cross section of top gate CNFET showing the gate and source and drain electrodes. (b) Output characteristics of a top gate p-type CNFET with a Ti gate and a gate oxide thickness of 15 nm. The gate voltage values range from -0.1 to -1.1 V above the threshold voltage which is -0.5 V. Inset: Transfer characteristic of the CNFET for $V_{ds} = -0.6$ V.

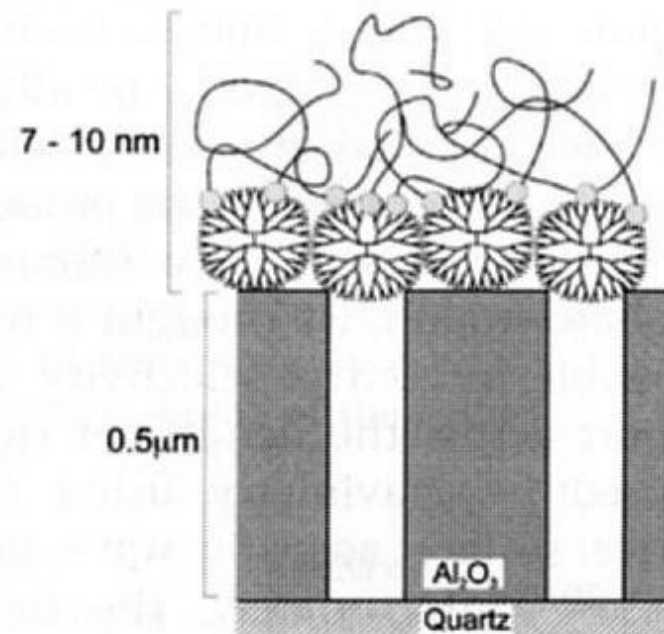
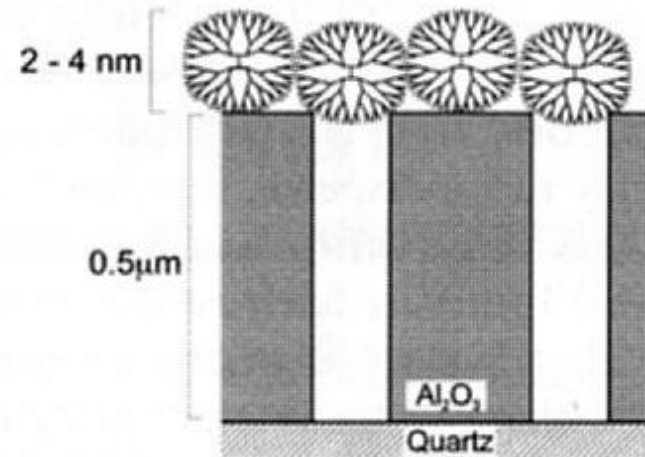
Exemplo 2:

- Língua Eletrônica (Embrapa)
- Microeletrodos e nanomembrana seletiva



Exemplo 3:

- Sensor químico:
 - Filtro seletivo de dendrímeros.
 - Alumina nanoporosa
 - Dispositivo SAW- detector de massa.



Centros de Nanofabricação Internacionais

- Vários laboratórios de microeletrônica foram transformados em centros de nanofabricação.
- Exemplos: Cornell, Stanford, NCMC, outros.

NNUN – National Nanofabrication Users Network

- Cornell, Howard, Stanford, Penn State, UCSB
- Finanziamento – NSF
- “NNUN has extensive experience in all phases of nanofabrication and its use in fields ranging **from nanophysics to biology to electronics**”.
- “Our technologies are largely based **on the thin film patterning techniques** so successfully employed in the **microelectronics** industry”.

Portanto, técnicas de micro & nano-fabricação:

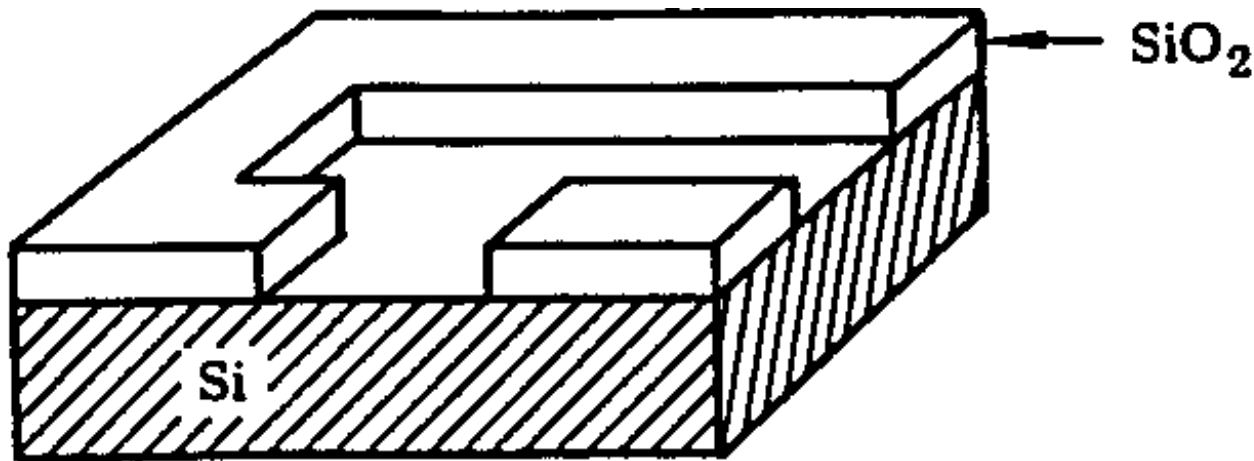
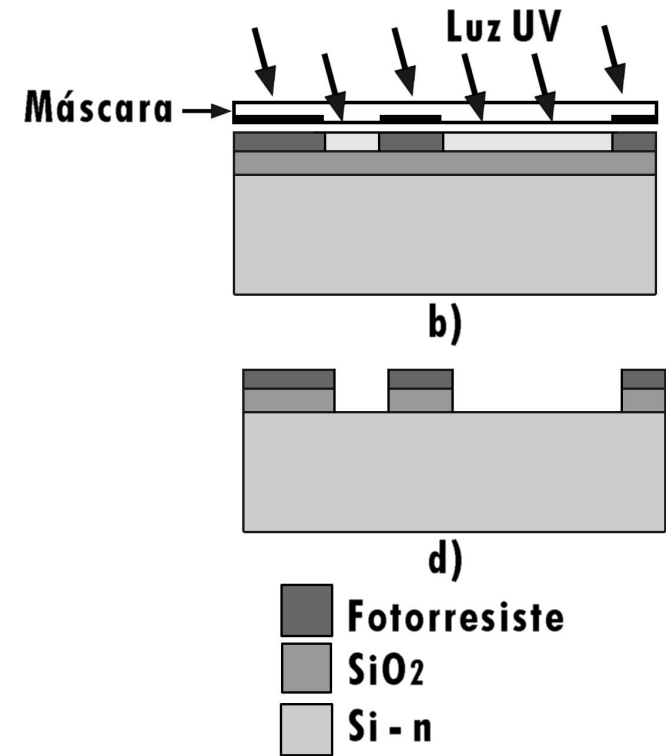
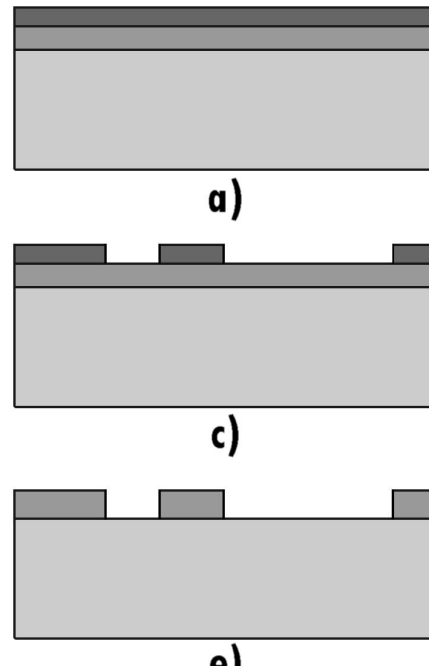
- São fundamentais para parte significativa do universo da nanotecnologia
- Devem ser estimuladas e apoiadas.
- *(pelo menos é assim no resto do mundo!)*

2. Evolução dos Semicondutores

- A) Dispositivos em Estado Sólido
 - Transistor Bipolar
 - Dez. 1947.

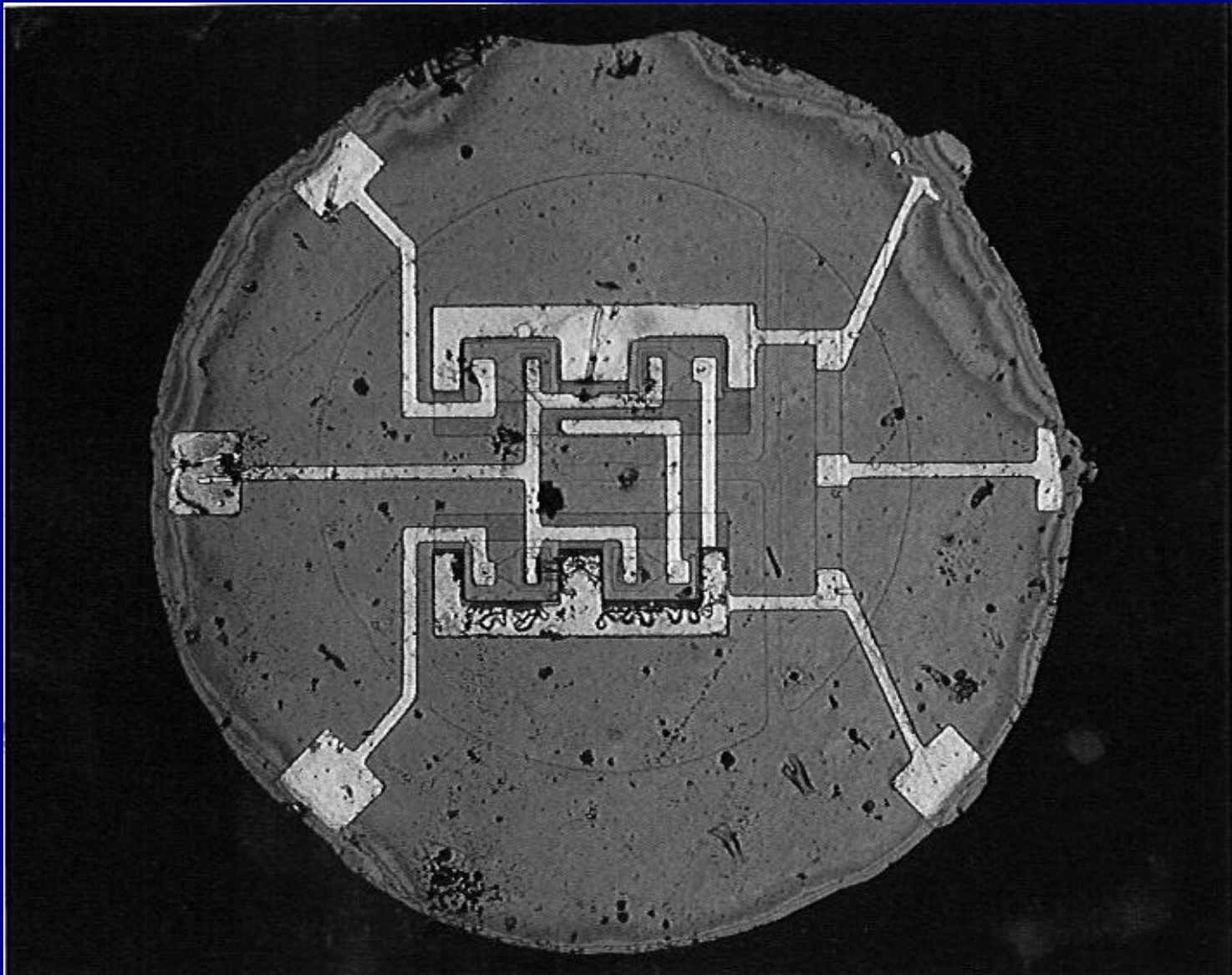


B) Processo Planar - 1958.

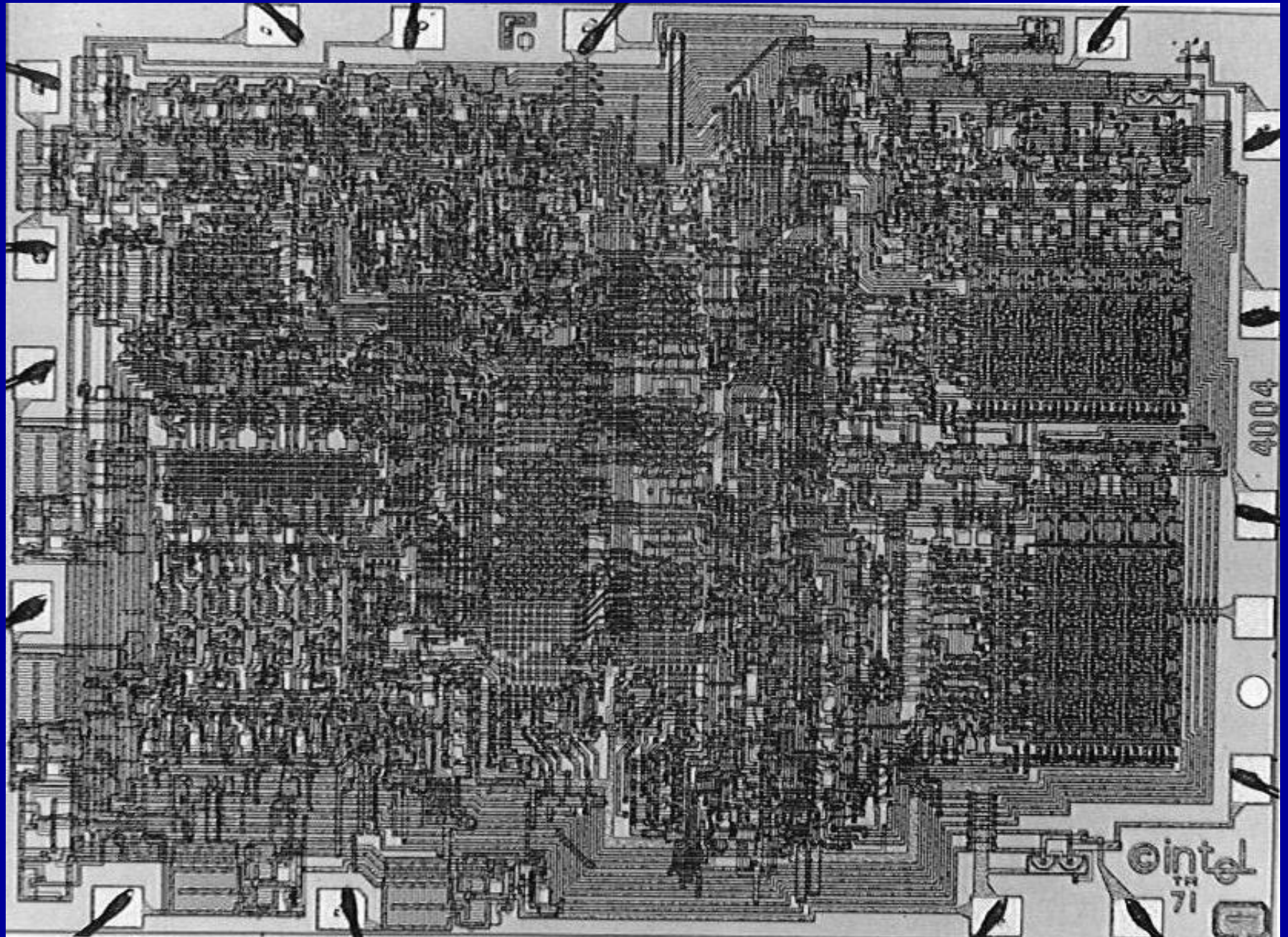


(e) Remove resist-pattern transferred to SiO₂

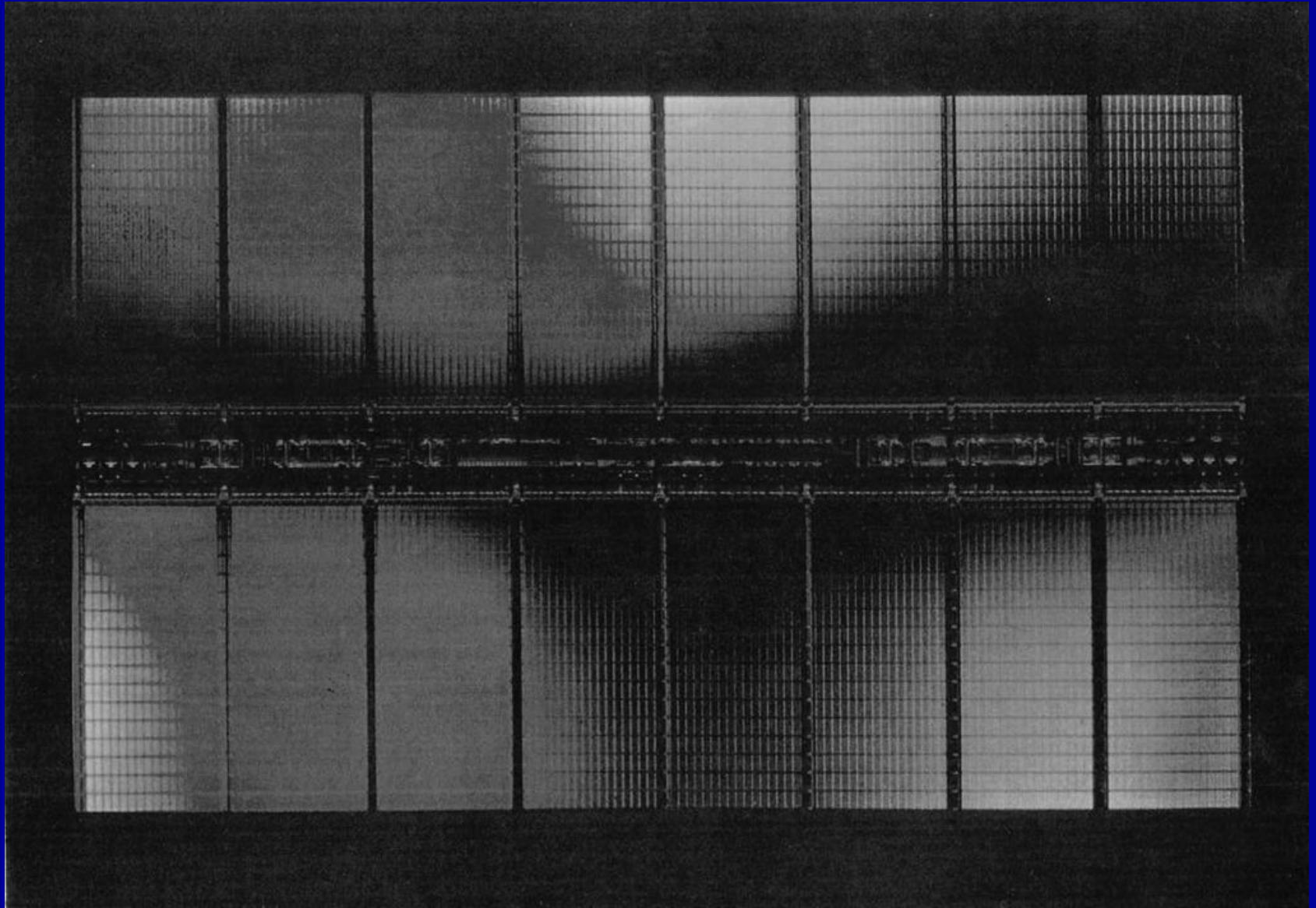
Primeiro CI, 1961 - Fairchild



1971 - Microprocessador 4004, Intel

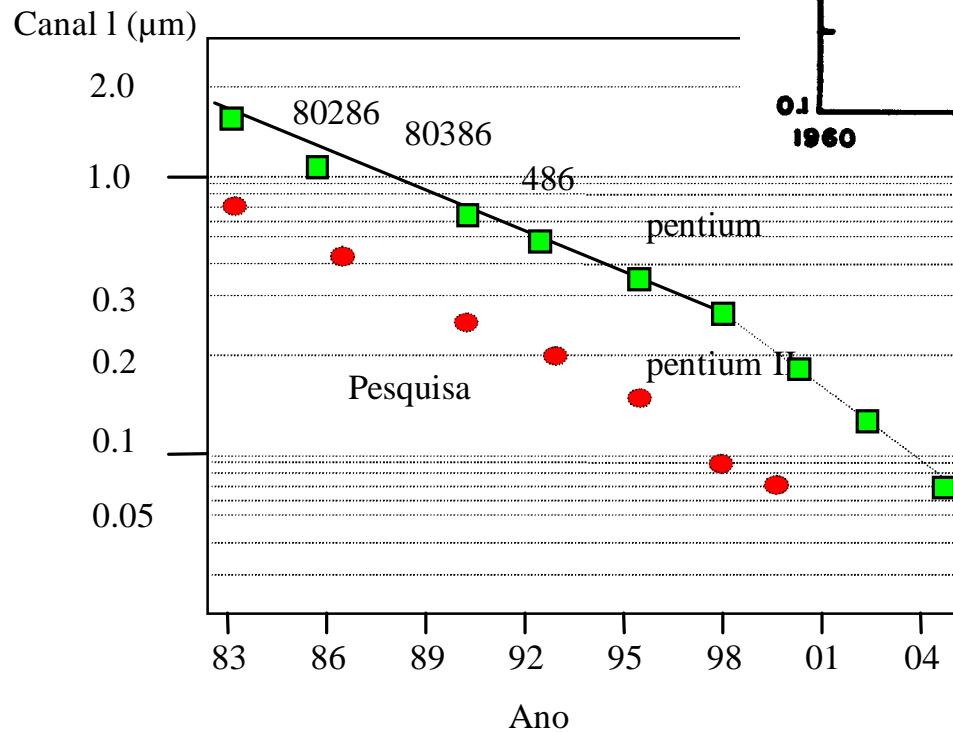
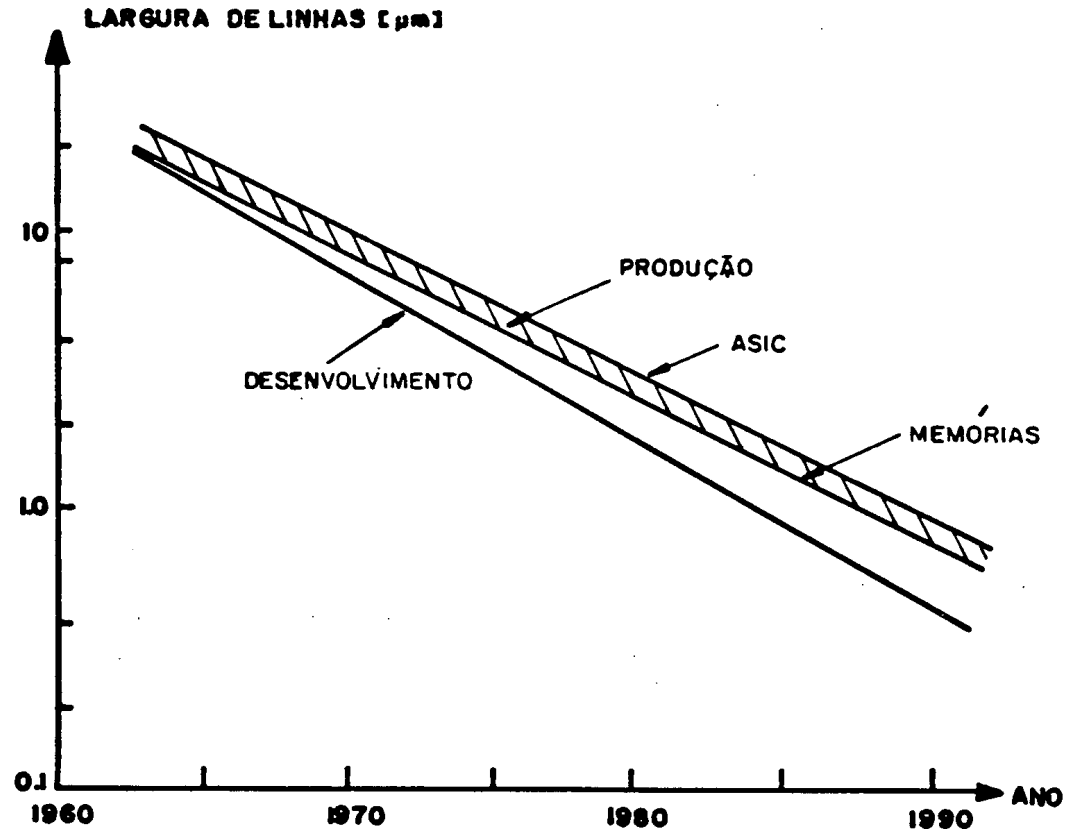


2001 - 256Mbit DRAM (TOSHIBA)



(from H. Iwai)

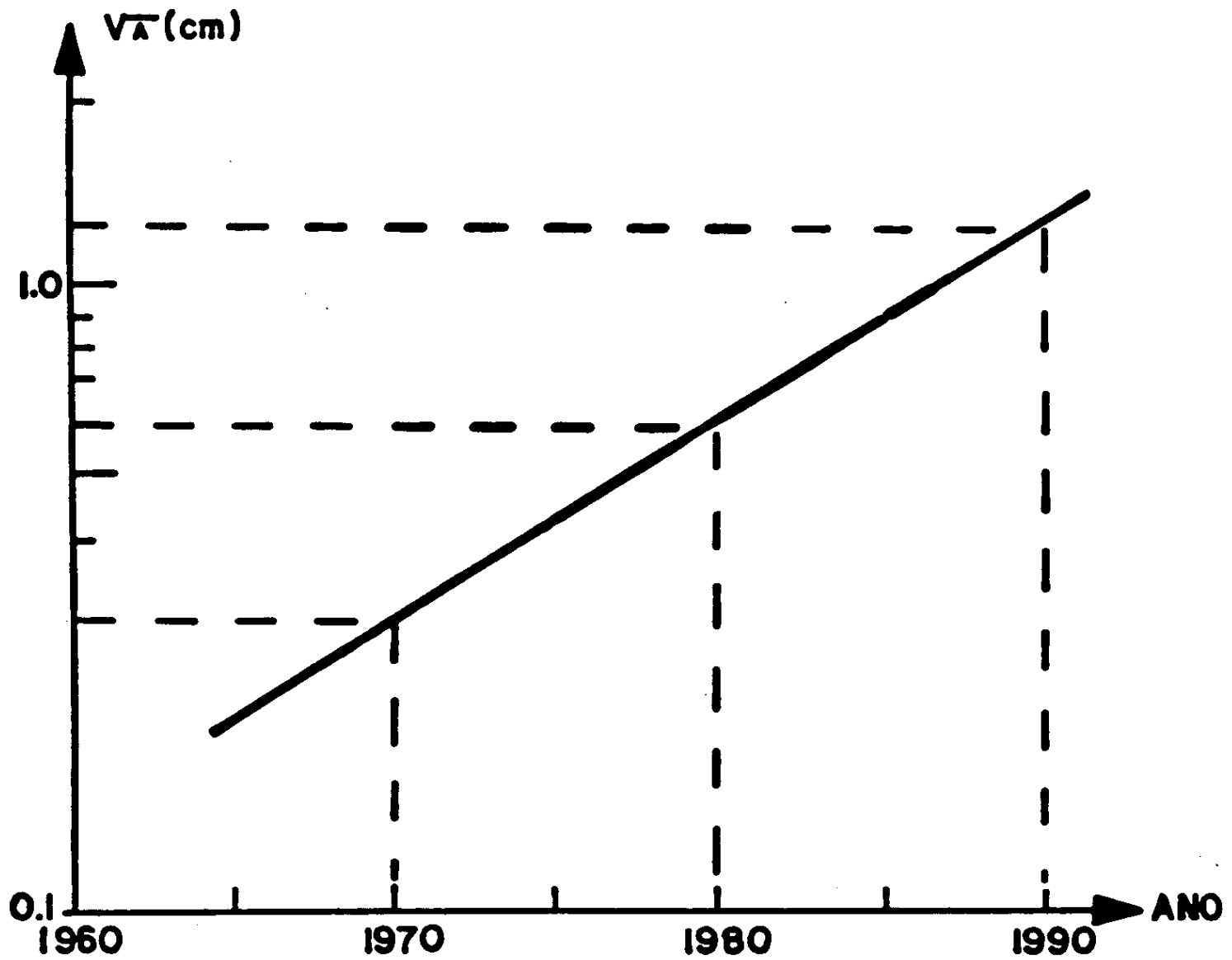
Evolução do Processo Planar



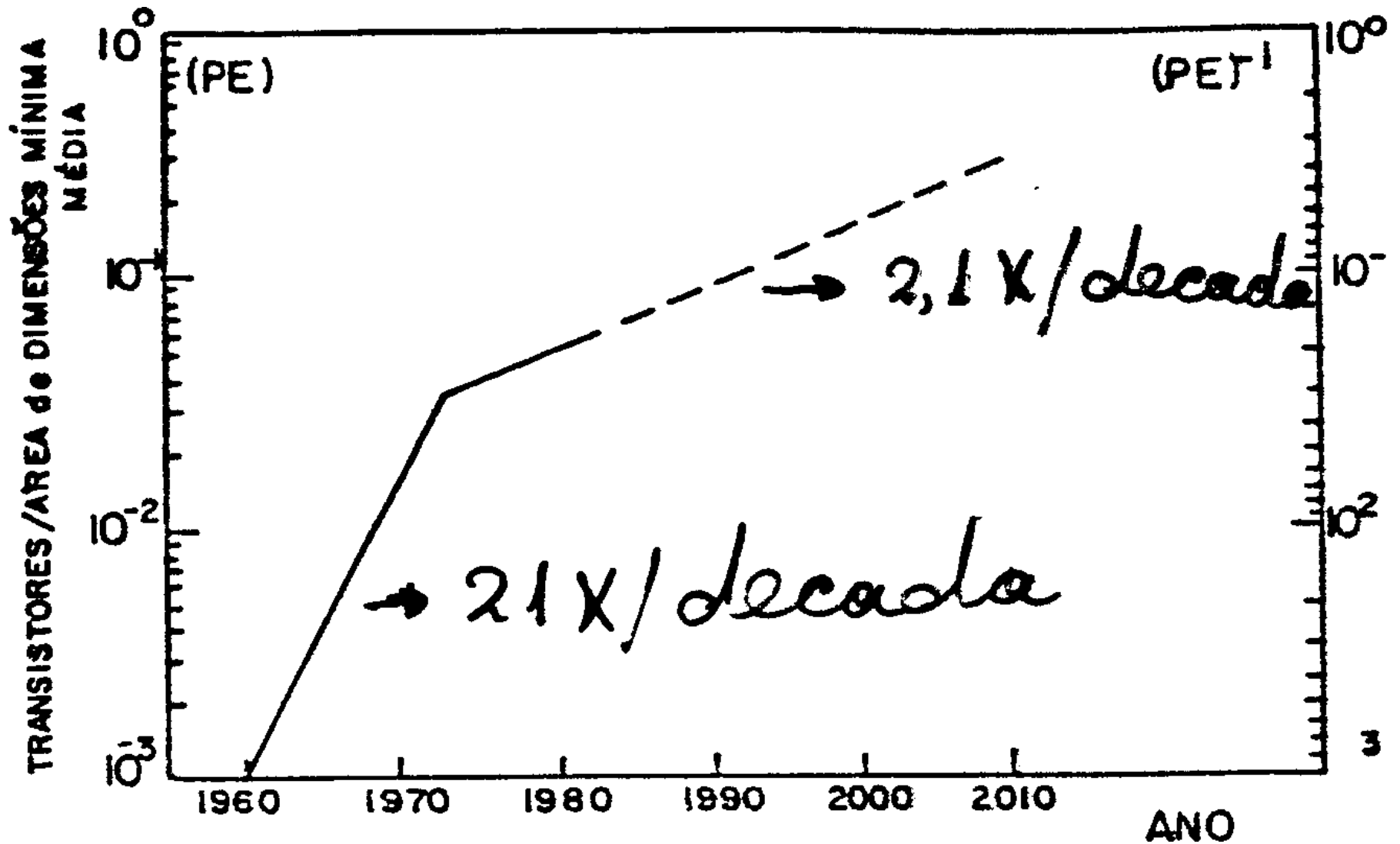
- 1962 - $\sim 20 \mu\text{m}$
- 1990 - $\sim 1 \mu\text{m}$
- 2003 - $< 100 \text{ nm}$

NANOELETRÔNICA!

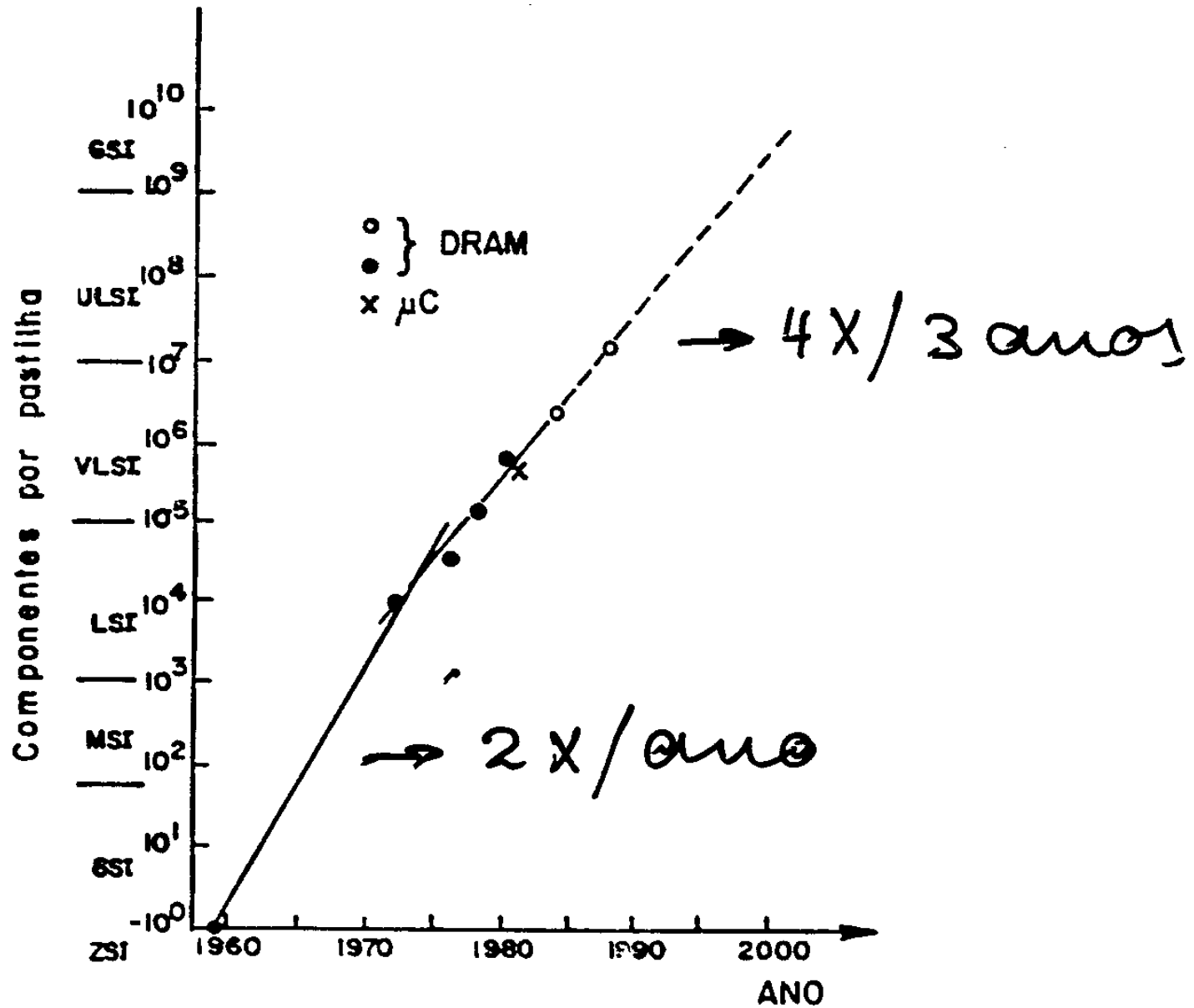
Área de chip



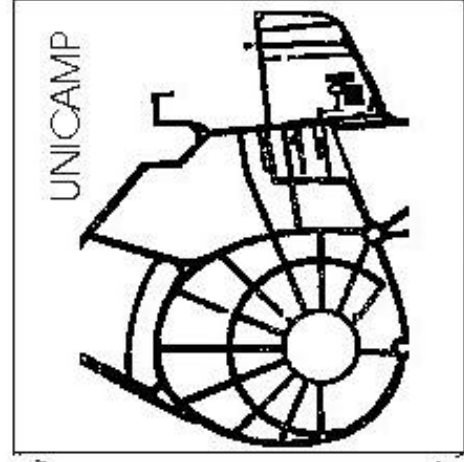
Eficiência de Empacotamento – Inovação



Número dispositivos por chip - Lei Moore



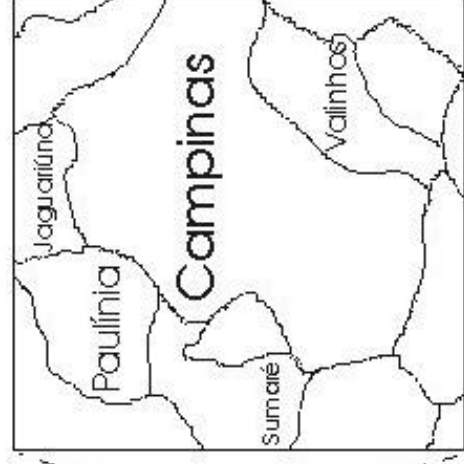
1960



1mm
25 μ m

2Km

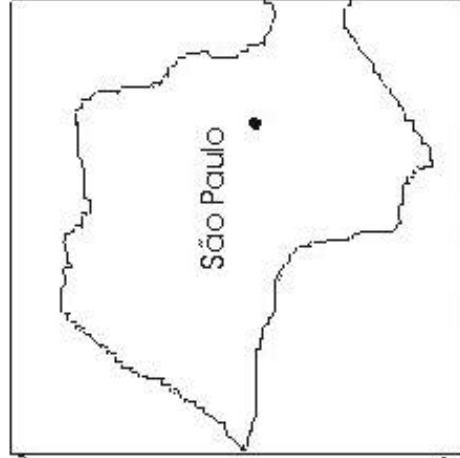
1975



4mm
5 μ m

40Km

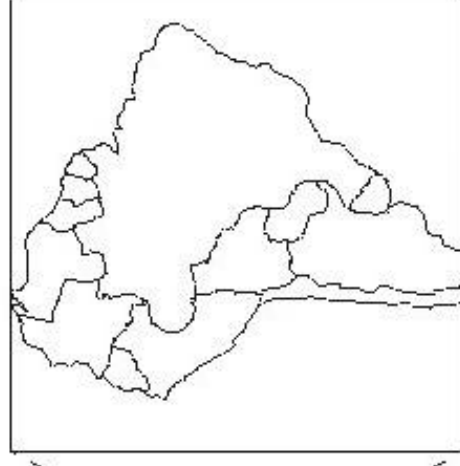
1990



12mm
0,8 μ m

750Km

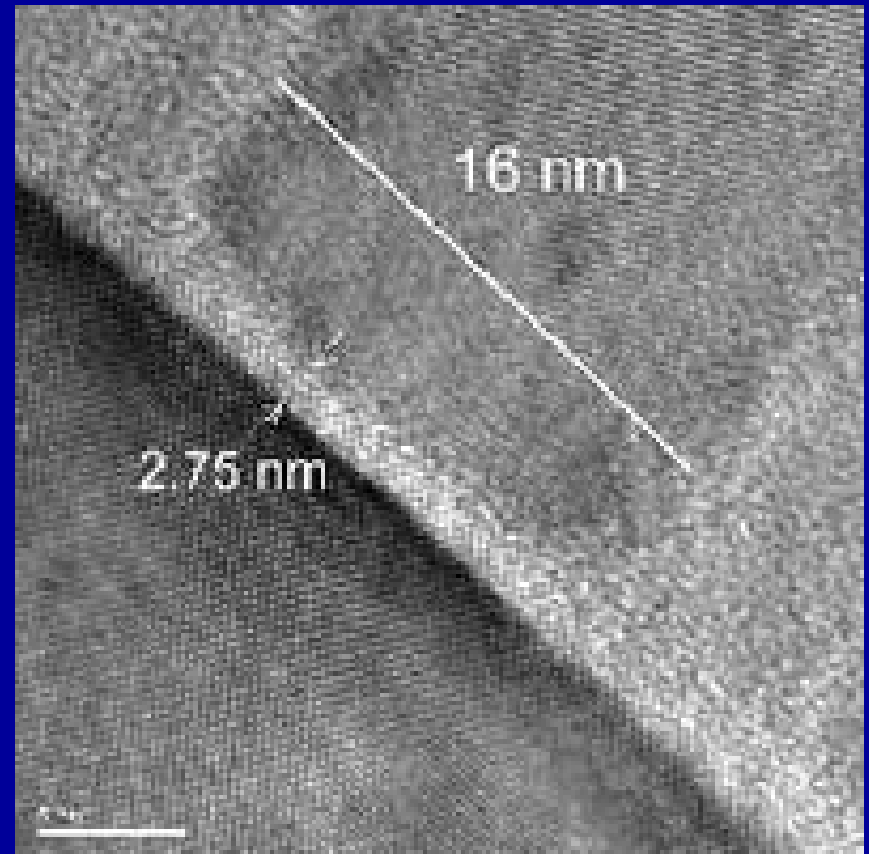
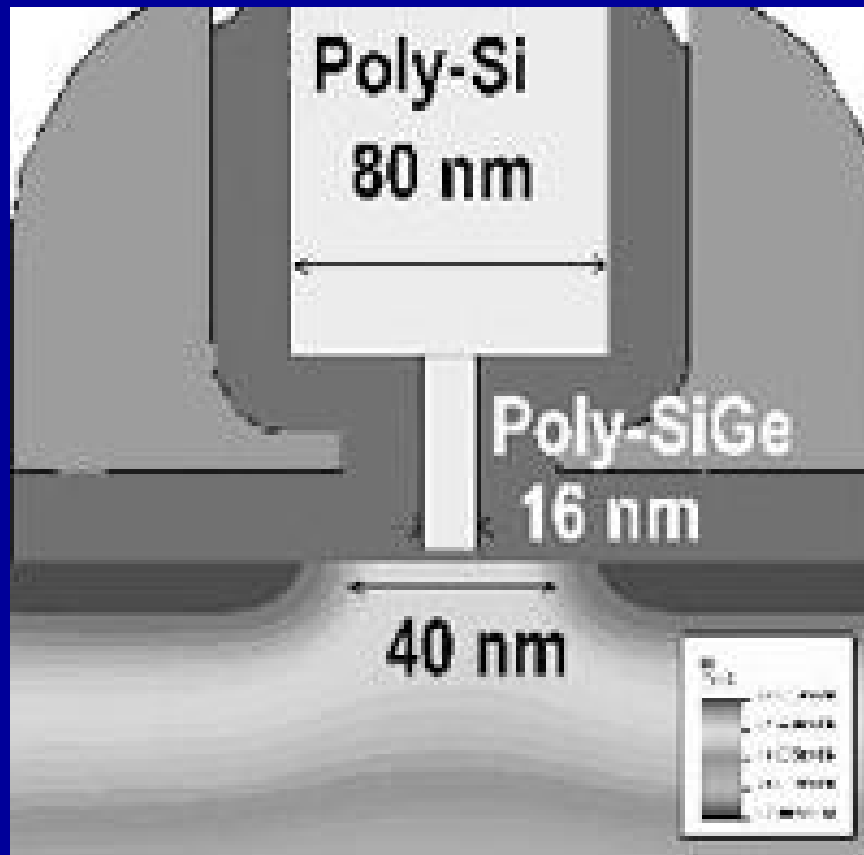
2000



20mm
0,15 μ m

6600Km

16 nm Gate Length Transistor

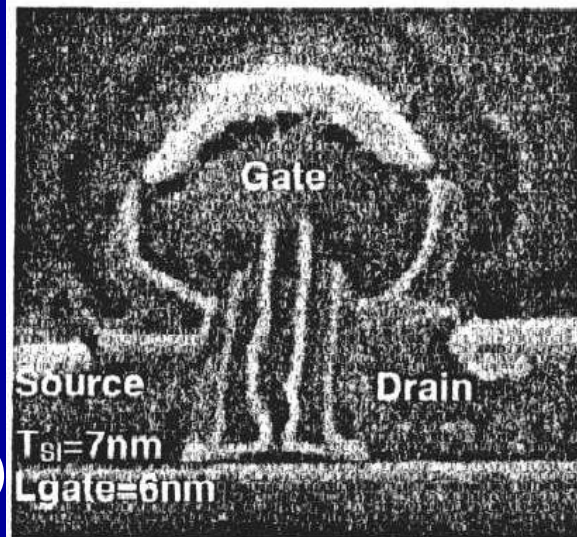


STMicroelectronics, Semiconductor International de Nov/2001.

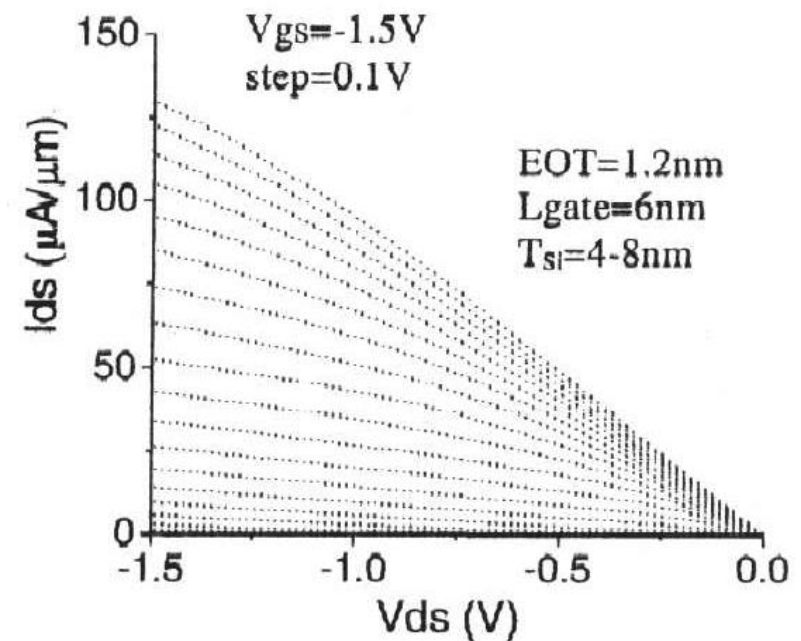
ITRS2001 – dimensões em nm

Ano	04	07	10	13	16	19	22	25
Nó tecnológico	90	65	45	32	22	15	10	7
Printed Gate	53	35	25	18	13	9	6	4
Physical Gate	37	25	18	13	9	6	4	3

Transistor
pMOS
L = 6 nm
(IBM-2004)



(a)



(b)

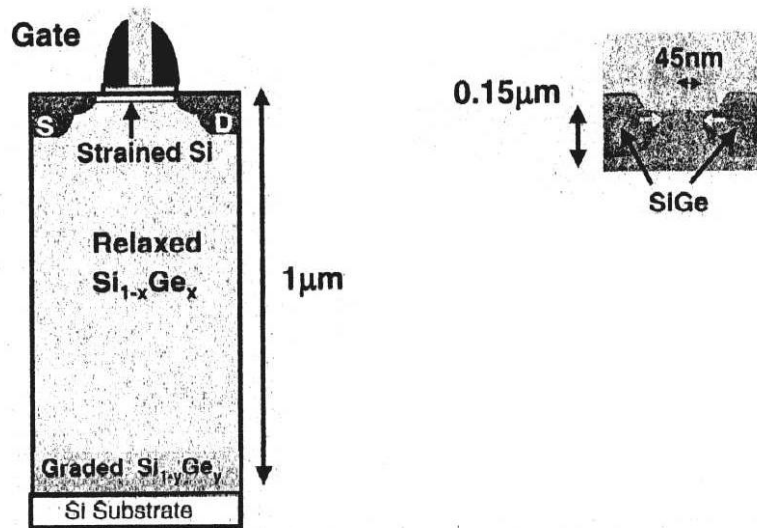
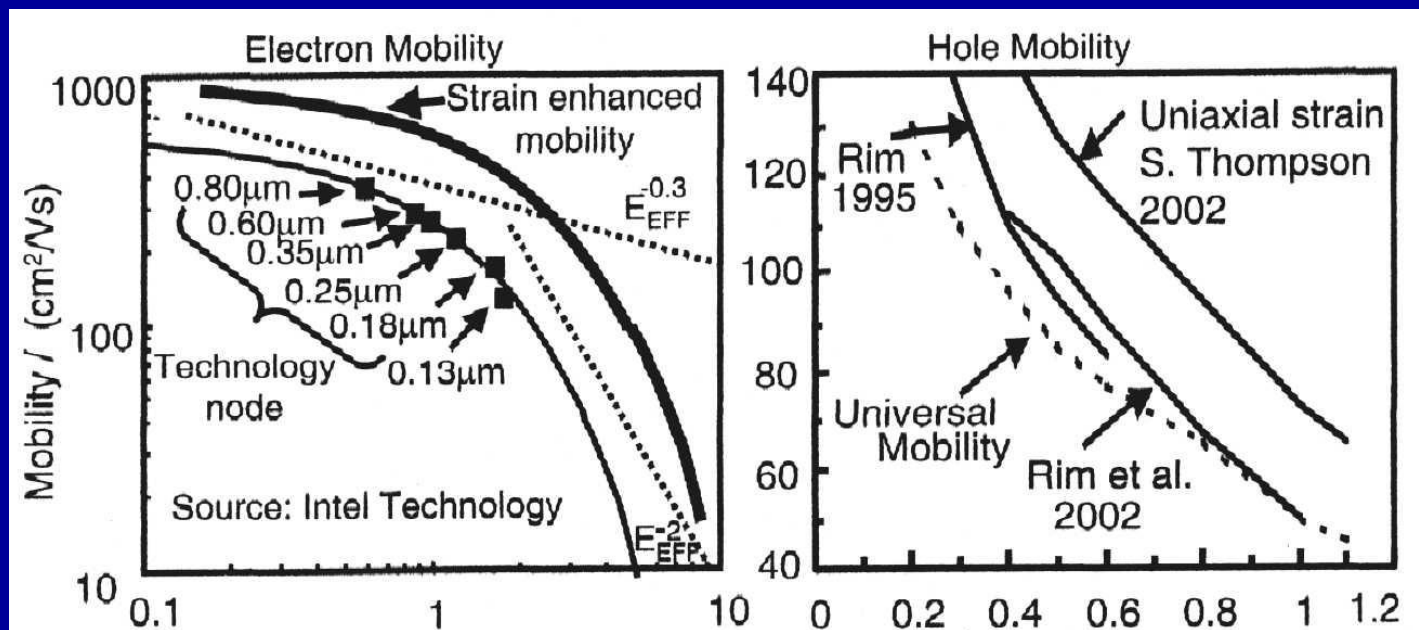


Fig. 7: Biaxial and uniaxial strained Si device cross-sections.

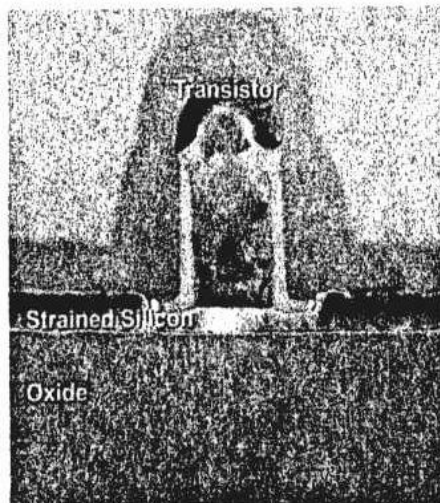
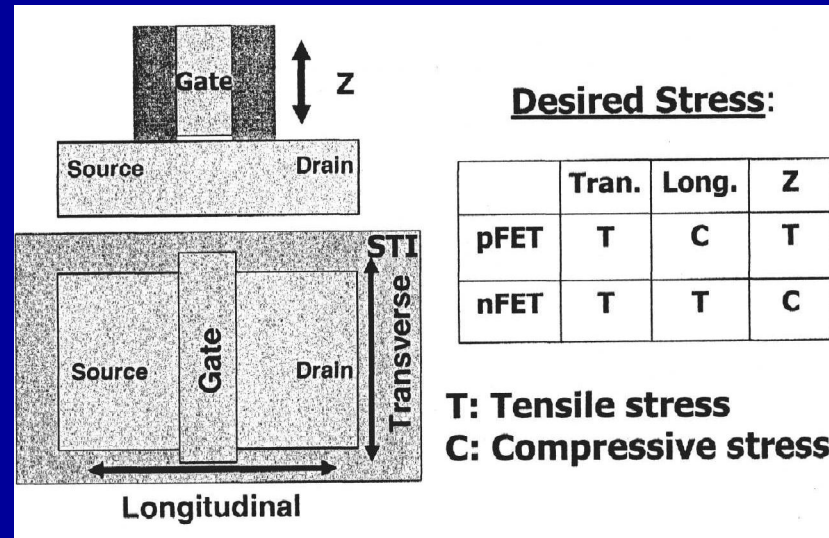


$\mu_n \downarrow$ de 400 a 120 em 10 anos!

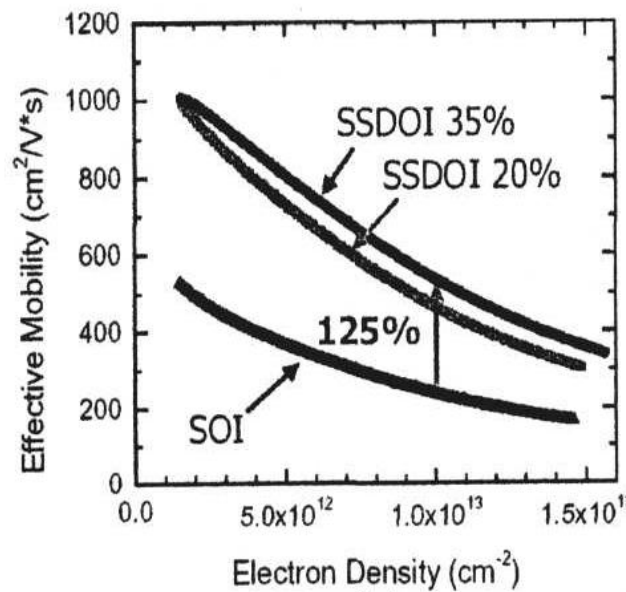
Si tensionado pode $\uparrow \mu$ até 2x (teórico) e 1.5x em uso (nó 90nm)

Uso de Si tensionado – aumenta mobilidade (ex. Si/SiGe)

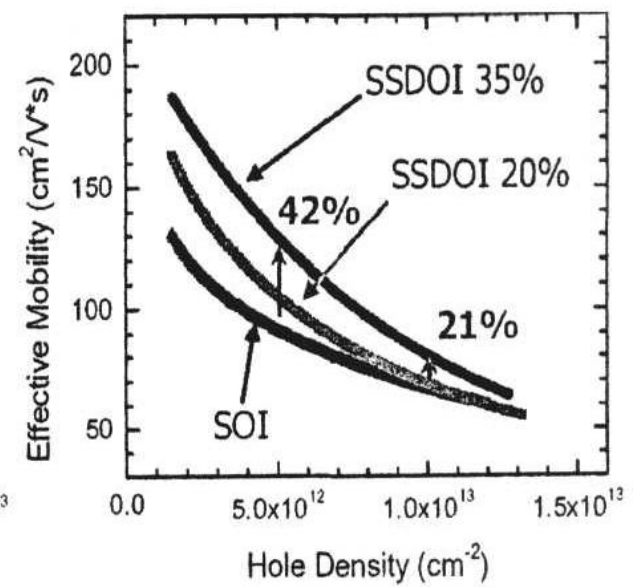
SSDOI = strained silicon directly on insulator, por técnica de transferência (smart cut)



(a)

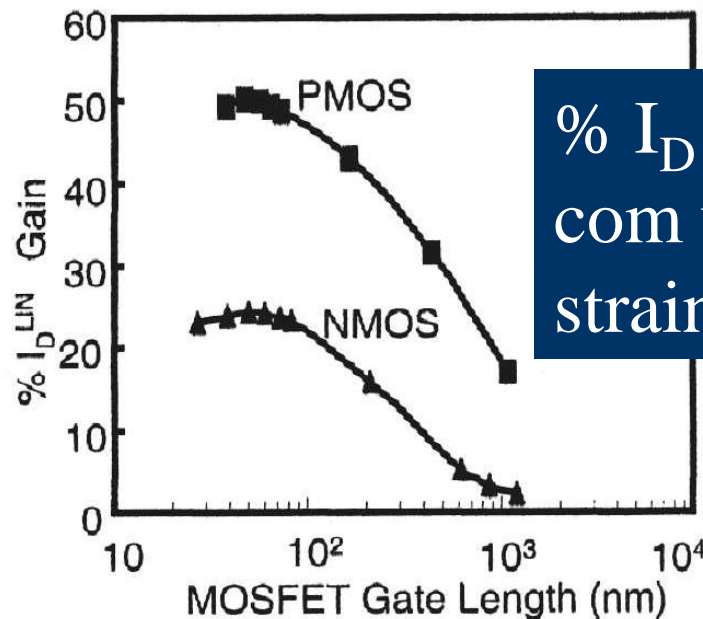
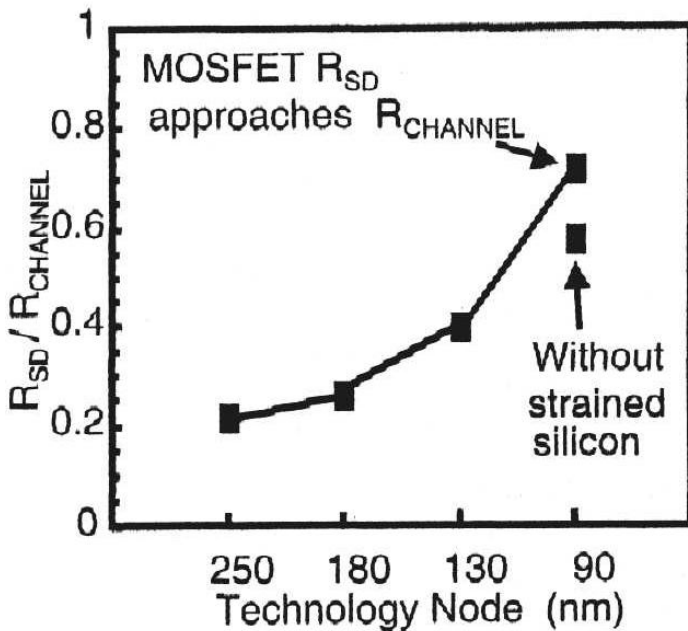
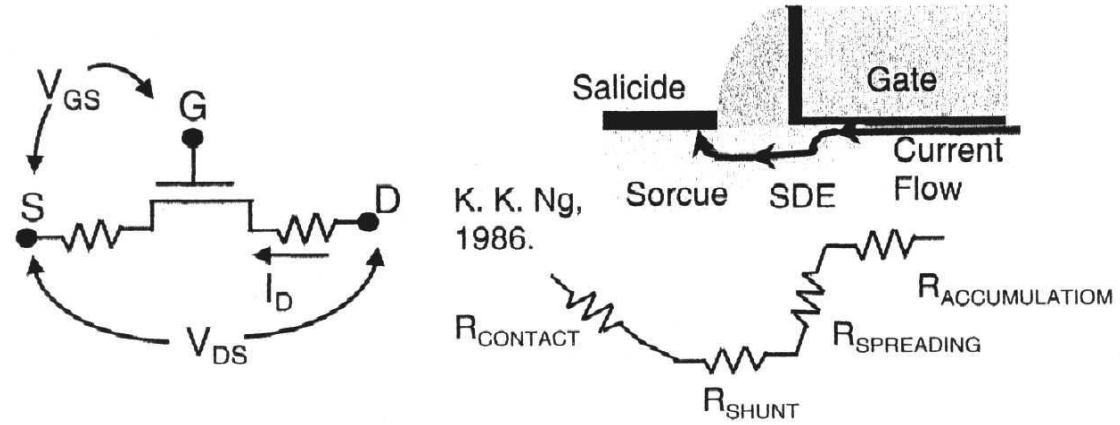


(b)



(c)

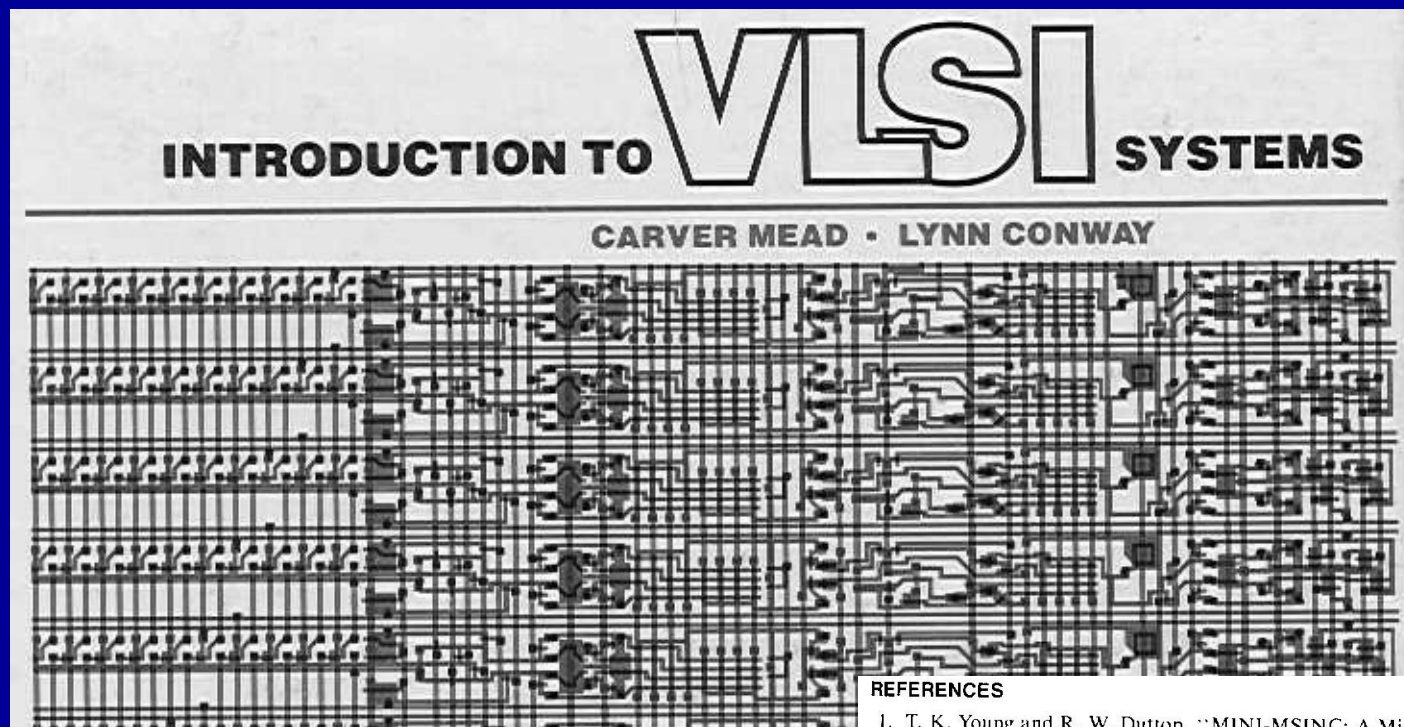
Séria limitação: R_{SD}



% I_D improvement
com uso de “uniaxial
strained Si”

- R_{SD}/R_{ch} era menor que 20%, agora tende a 1 !
- Ganho pelo strain tende a saturar para $L < 100\text{nm}$ (nMOS) e $L < 50\text{nm}$ (pMOS) devido à R_{SD} .
- Prioridade: reduzir R_{SD} ; não adianta melhorar a chave MOS (CNT ?)

Qual é o limite Prático para CMOS?



References 37

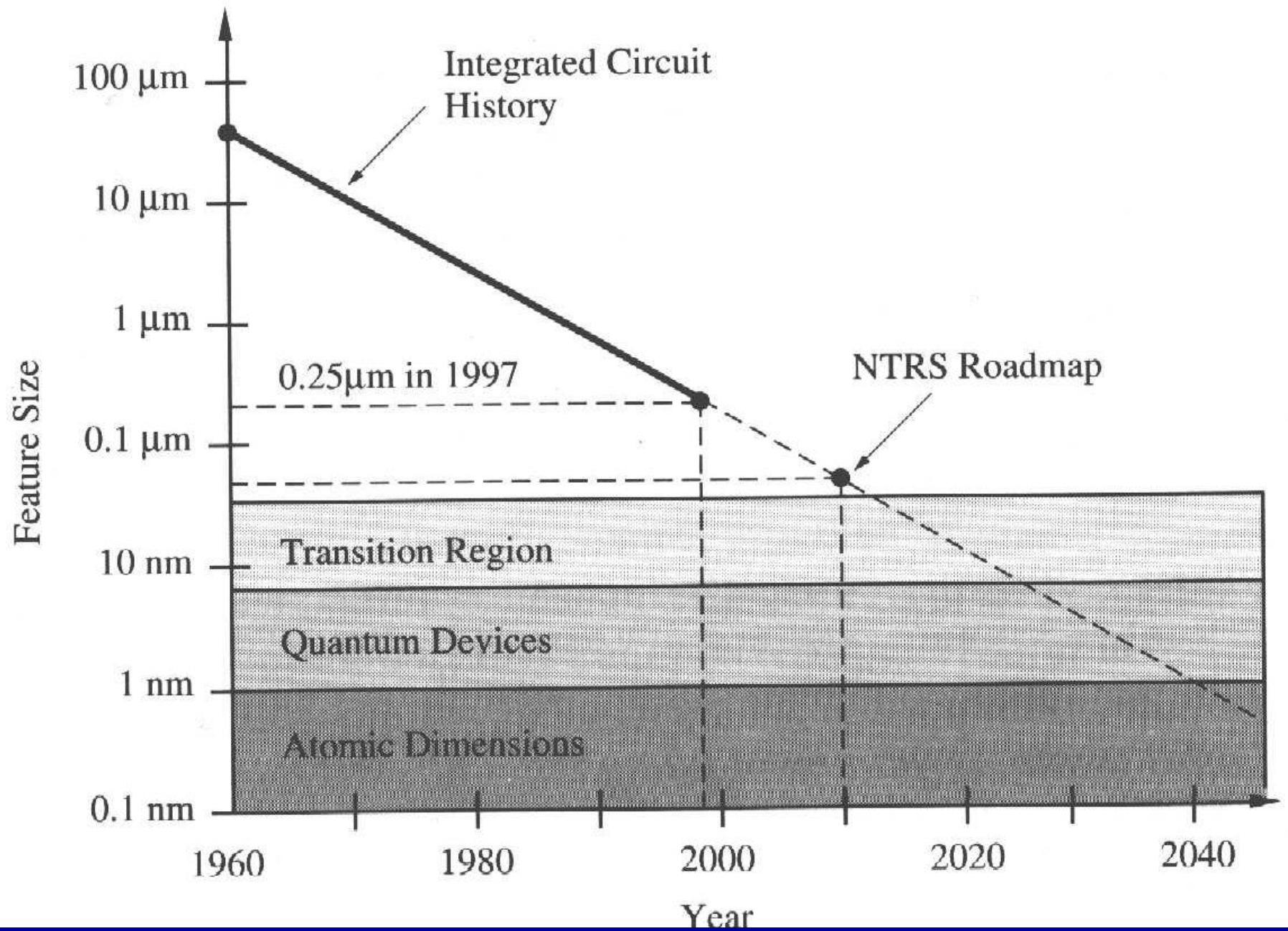
approximately five volts and minimum channel lengths of approximately six microns. Therefore, the kind of scaling we have envisioned here will take us to devices with approximately one-half micron channel lengths and current densities approximately ten times what they are today. Power per unit area will remain constant over that range. Smaller devices might be built but must be used without lowering the voltage any further. Consequently the power per unit area will increase. Finally, there appears to be a fundamental limit¹⁰ of approximately one-quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

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10. B. Hoeneisen, and C. A. Mead, "Fundamental Limitations in Micro-electronics—I. MOS Technology," *Solid-State Electronics*, vol. 15, 1972, pp. 819-829.

Qual é o limite Prático para CMOS?

- 25 nm (H. Iwai, IEEE, JSSC, Mar. 99)
Quando? Entre 2020 e 2030 $\Rightarrow 10^{10}$ a 10^{12} tr./chip
 \Rightarrow permite produtos não visualizáveis hoje.
- Vários fatores apontam 10 nm de comprimento de porta ser um limite prático para o escalamento de CMOS.
Como fatores limitantes apontam:
 - tunelamento pelo dielétrico de porta;
 - impossibilidade de escalar a tensão de alimentação
 - questões de ruído térmico e de *bandbap*;
 - impactos de tolerância e margens do número de átomos dopantes no dispositivo [Melliar-Smith and Helms].
- Transistores com L de 6 nm já foram demonstrados [IBM, 2004]



(Plummer et al)

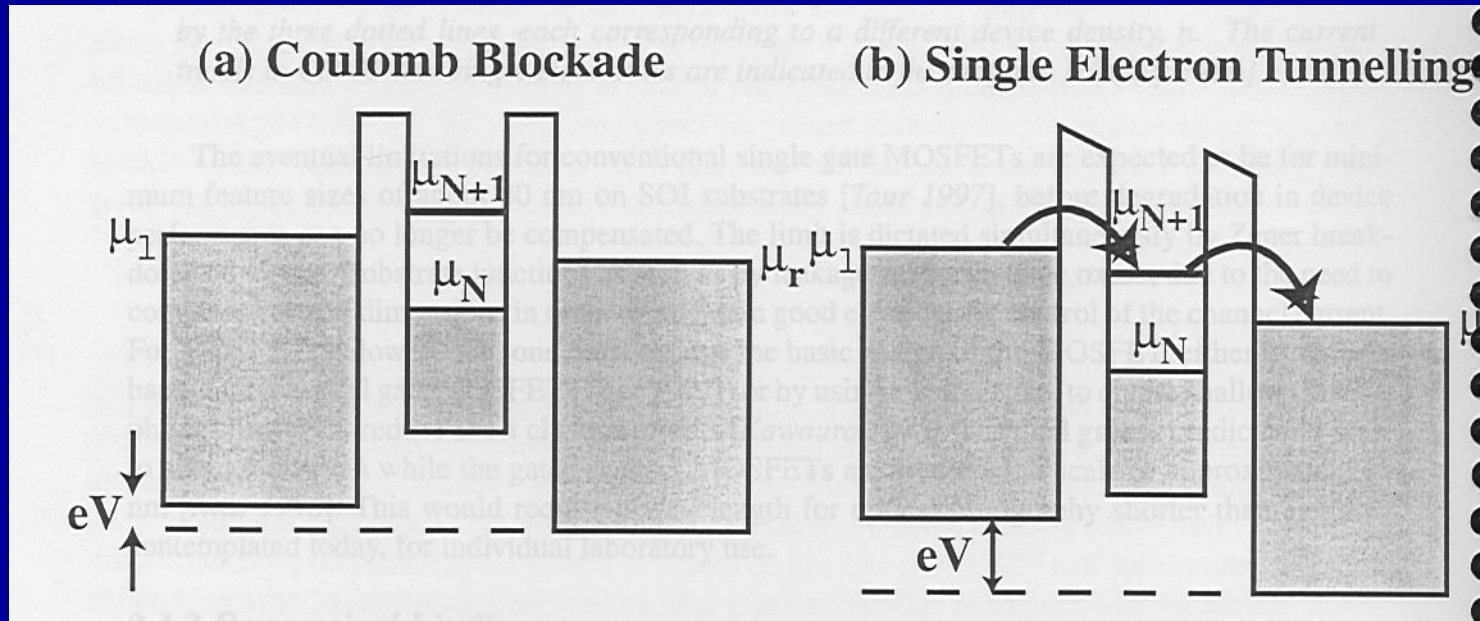
Qual o tempo de vida para CMOS?

- Pelo “roadmap” ainda ~ 15 anos de evolução.
- Porém, seu uso, provavelmente > 50 anos!
- Prevê-se a adição de novos dispositivos nano co-integrados com CMOS, baseados na plataforma da tecnologia CMOS.

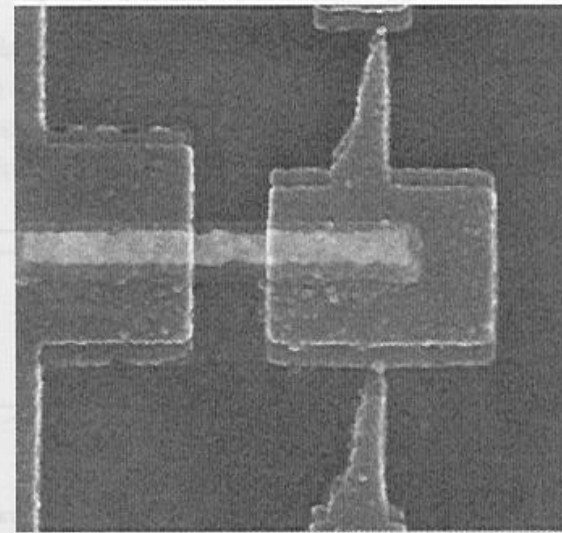
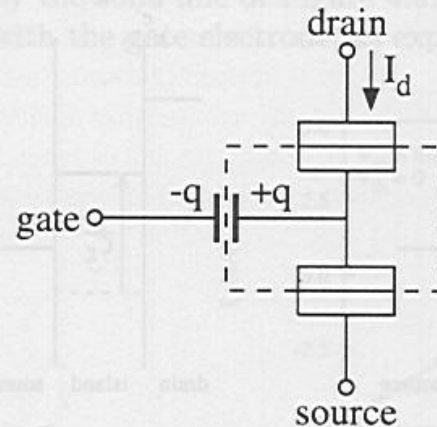
Após Limite de Escalamento CMOS?

- Novos Conceitos de Dispositivos e Circuitos:
 - a) dispositivos de bloqueio Coulombiano, entre outros dispositivos de um único elétron;
 - b) estruturas de nano-tubos de carbono
 - c) transistor molecular
 - c) dispositivos quânticos, onde se controla o estado do elétron = spintrônica.

Single Electron Tunneling Device - SET

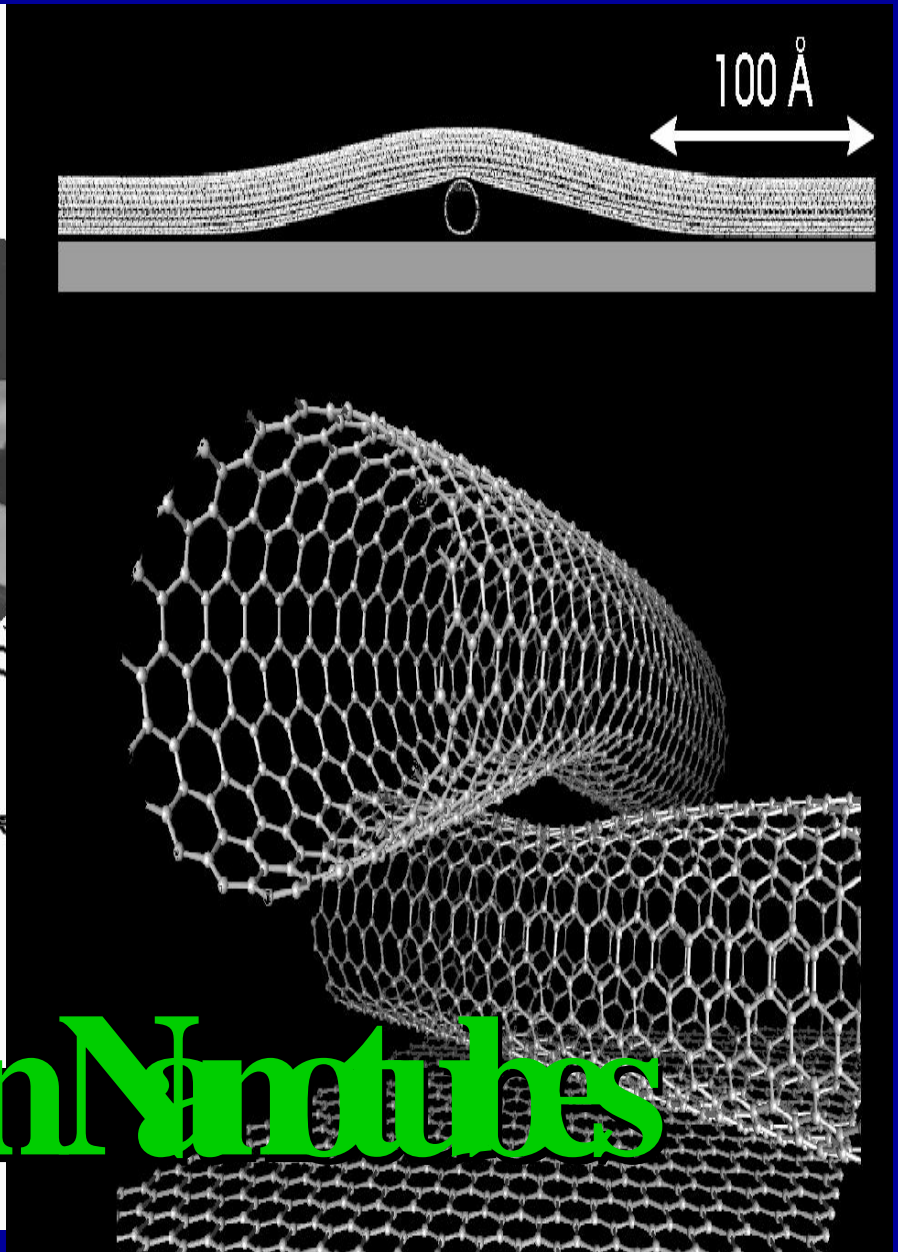
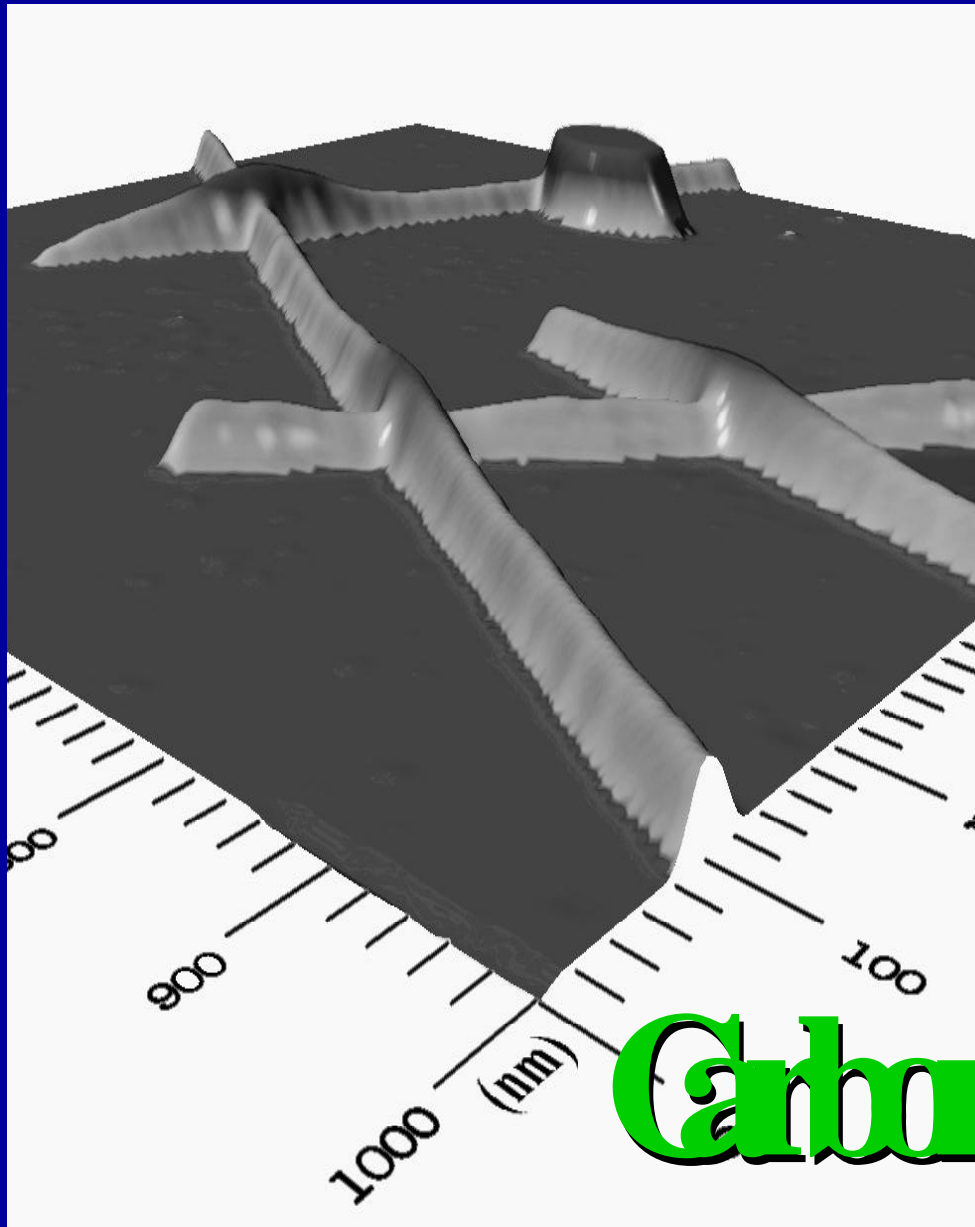


$$\Delta V = \frac{e}{C_\Sigma}$$



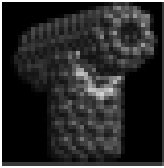
SET transistor

100



Carbon Nanotubes

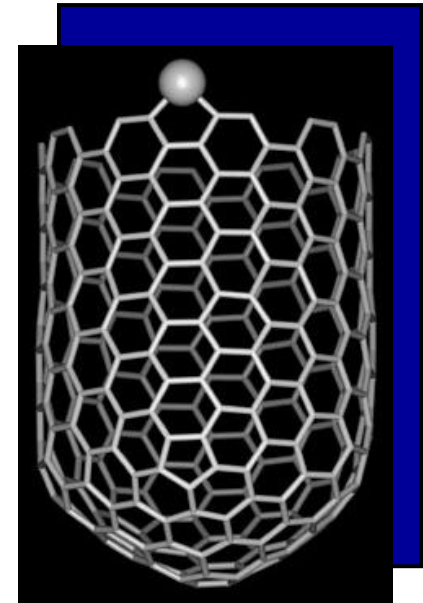
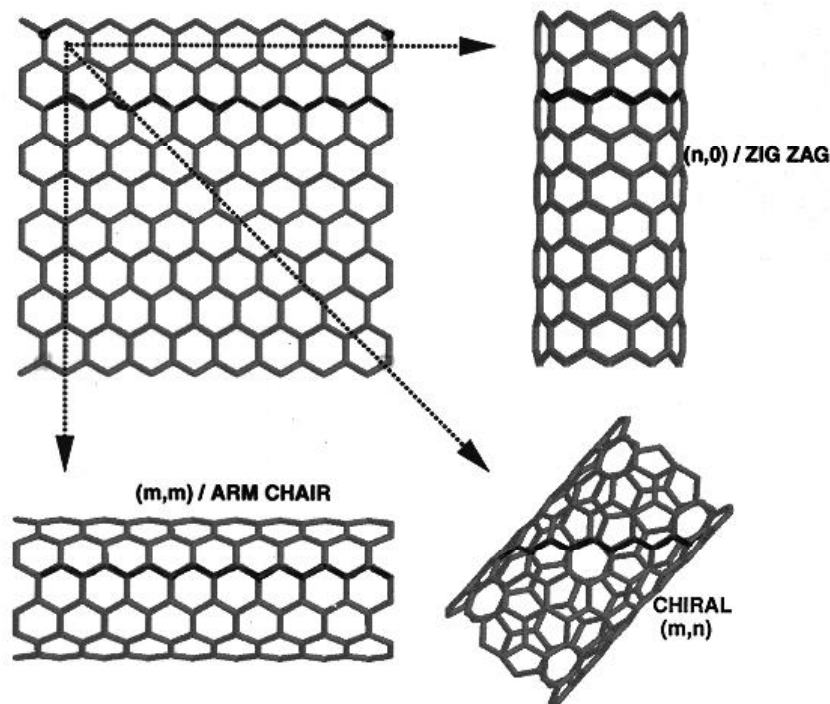
Carbon Nanotube



CNT is a tubular form of carbon with diameter as small as 1 nm.
Length: few nm to microns.

CNT is configurationally equivalent to a two dimensional graphene sheet rolled into a tube.

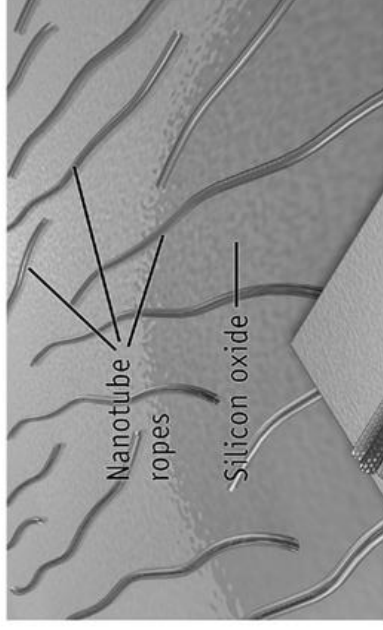
- STRIP OF A GRAPHENE SHEET ROLLED INTO A TUBE



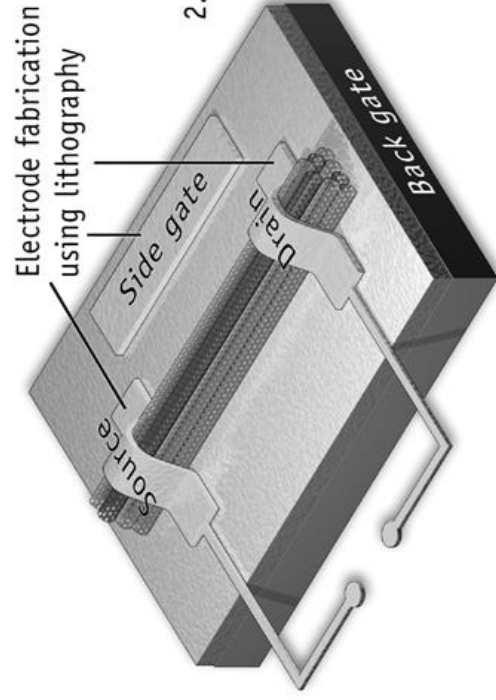
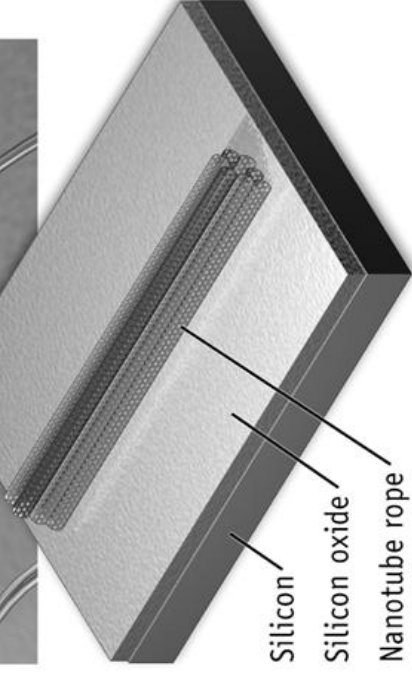
CNT exhibits extraordinary mechanical properties: Young's modulus over 1 Tera Pascal, as stiff as diamond, and tensile strength ~ 200 GPa.

CNT can be metallic or semiconducting, depending on chirality.

New Breakthrough Transistor Technology From IBM: Carbon Nanotubes - Constructive Deconstruction

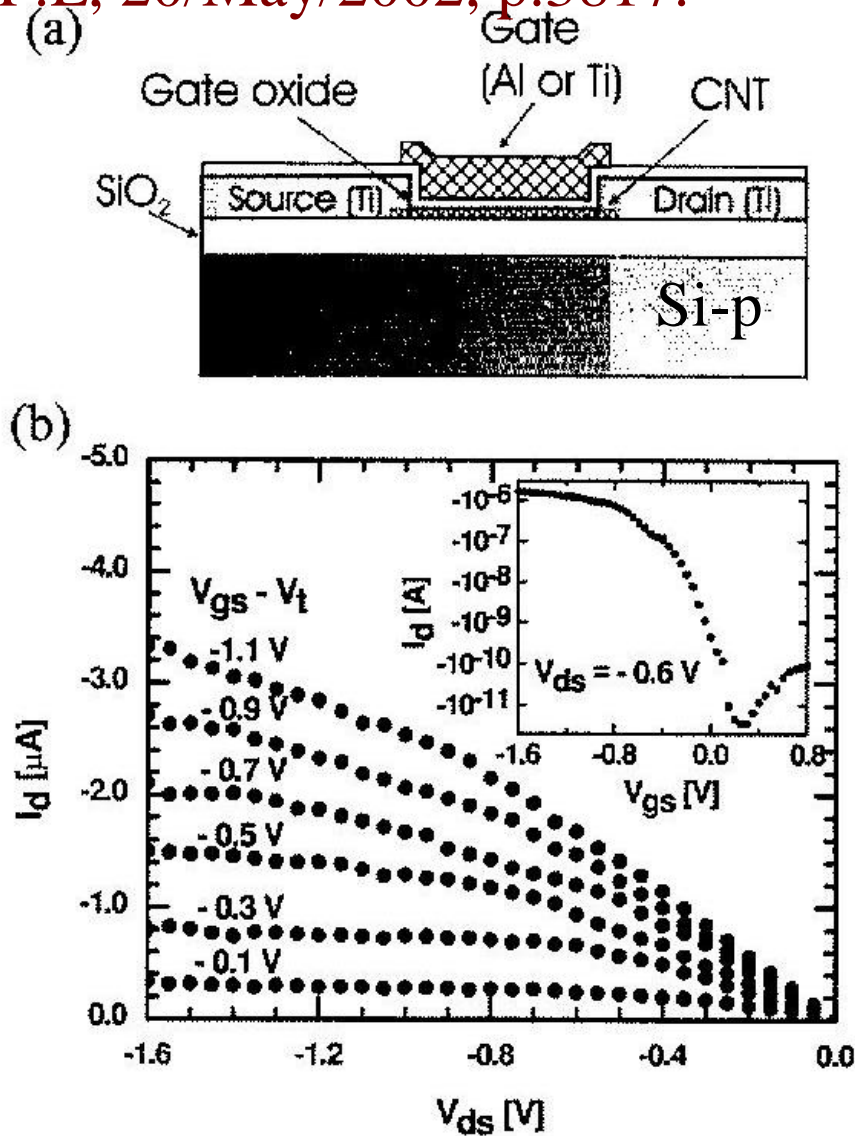


1. Ropes of Nanotubes:
The scientists deposit the ropes of metallic and semiconducting tubes onto a silicon wafer.



2. A mask is projected onto the tubes and the semiconducting tubes are switched off, insulating them from electricity.

A.P.L, 20/May/2002, p.3817.



Nantero (Woburn, Mas.,) introduziu CNT na fábrica: Usa CNT como chave eletromecânica, controlado por campo elétrico.

O CNT fica suspenso sobre uma trincheira, podendo mover-se.

Em alguns anos esperam ter uma memória não volátil no mercado (Semicond. Intl. Nov.2004, p45)

of the study. The first two authors were responsible for the data collection and the third author was responsible for the data analysis. The authors are grateful to the staff of the Hospital de Referência de Curitiba for their cooperation during the study. The authors also thank the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq) for the financial support of this study.

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- Almeida, A. C. S., Cabral, J. M. S., de Lencastre, E. A., de Lencastre, E. M., Severina, E. P., Severina, E. V. et al. (2009) Genetic diversity of *Staphylococcus aureus* strains isolated in the Hospital de Referência de Curitiba, Brazil. *Journal of Hospital Infection*, **41**, 169–176.

Correspondence

Dr J. M. S. Cabral, Hospital de Referência de Curitiba, Rua Coronel João Antônio, 150, Curitiba, Paraná, Brazil. Tel: +55 41 333 5500. Fax: +55 41 333 5500. Email: jmcabral@hospitalcuritiba.com.br

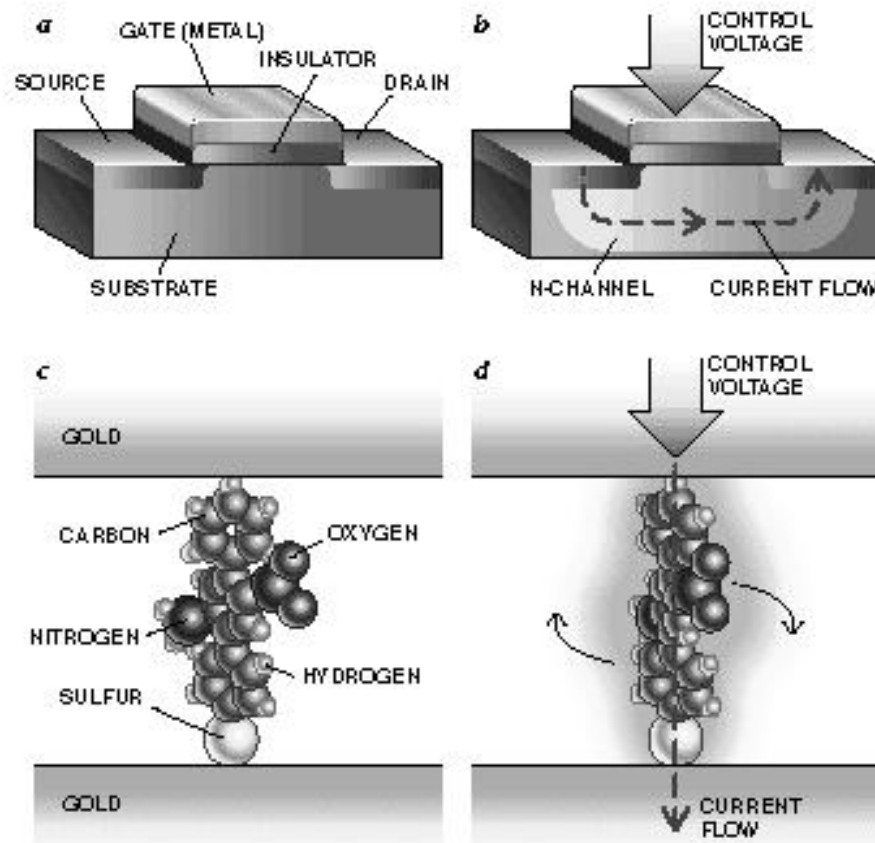
Accepted

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Transistor Molecular



CONVENTIONAL MICROTRANSISTOR (a) has three terminals, known as the source, gate and drain. A positive voltage applied to the gate draws electrons to the insulator (b), enabling current to flow from the source to the drain. A molecule based on three benzene rings (c) was also used to switch an electric current. The center ring had asymmetric fragments, enabling it to be twisted by an electrical field (d). With a specific voltage applied, the electrical field twisted the molecule and permitted current to flow.

Pesquisas em andamento:

- HP crossbar molecular swithes memory device.
- Molecular gates, by IBM.
- Biomolecular templates to use DNA-like materials, at Albany NanoTech. -

(Semicond. Intl. Nov.2004, p45)

3) Processo Planar – Outras Aplicações

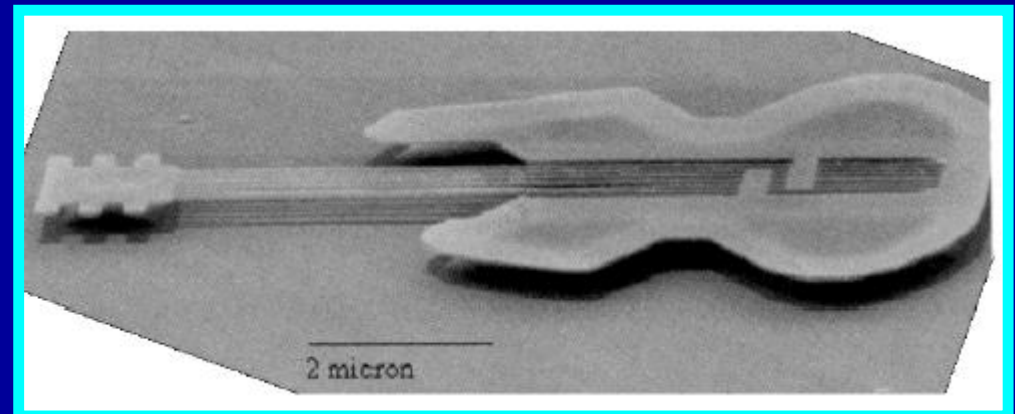
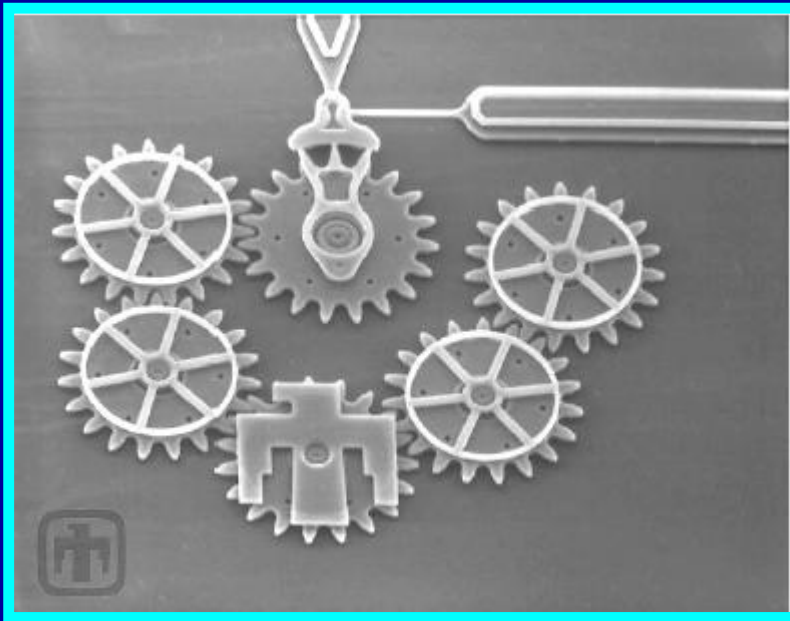
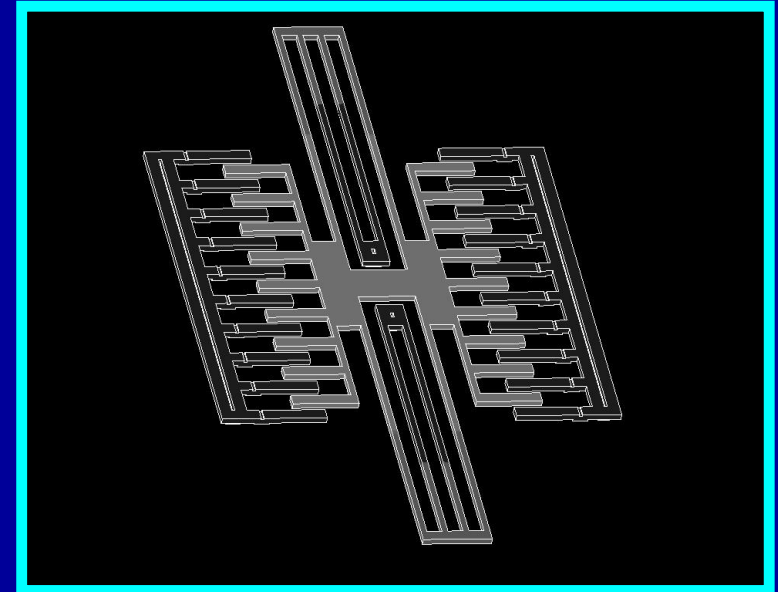
- Optoeletrônica
- Fotônica
- Microssistemas = MEMS ou MOEMS
 - Microssensores
 - Microatuadores
- NEMS, NOEMS
- Micro/Nano-estruturas para biologia
- etc.

Exemplos:

- *Lab-on-a-Chip*:
 - Análise de DNA
 - Análise de fermentação de cerveja (Siemens)
 - *Drug delivery* (Silicon probes with microfluidic channels)
- Automobilística:
 - Acelerômetro: \Rightarrow *airbag*.
 - Pressão: \Rightarrow ABS, pneu, motor, etc.

Exemplos: mecânica

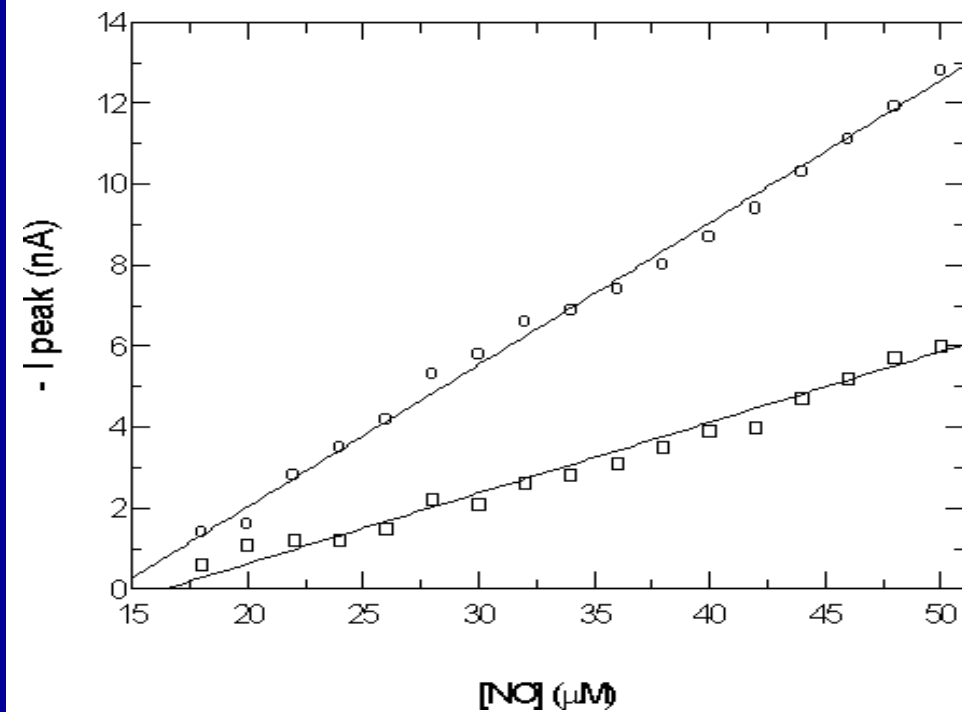
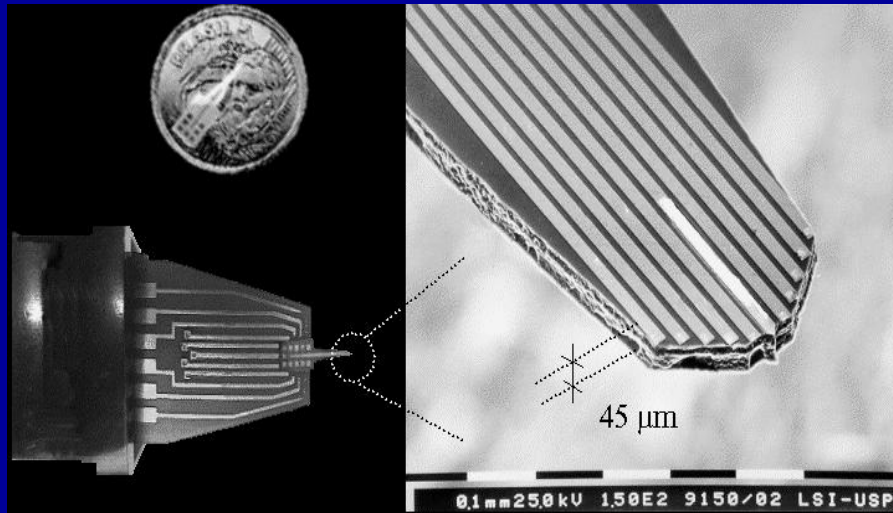
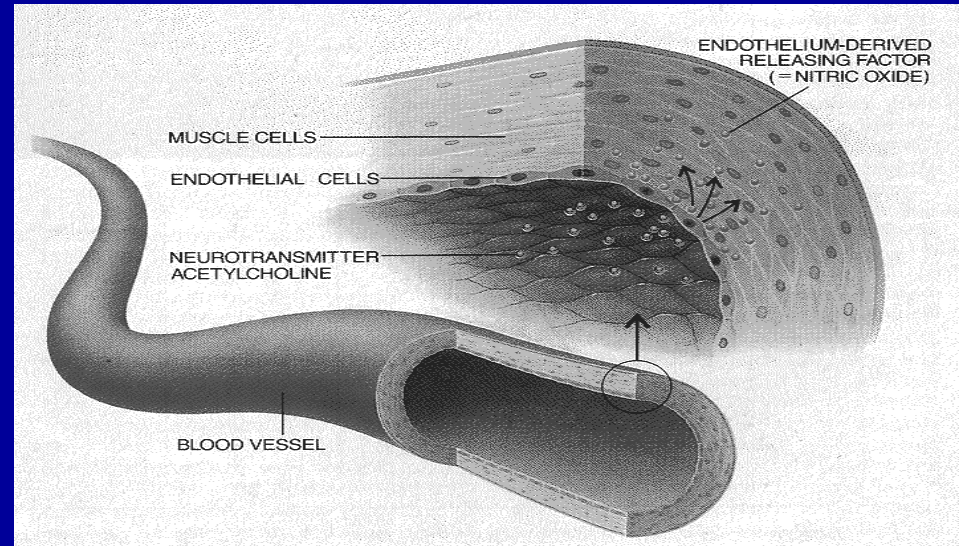
- *Surface Micromachining:*



Guitarra com fios de Si com largura de 100 átomos.

Exemplo: bio-sensores

- Detecção eletroquímica de NO
 - neurotransmissor
 - relaxação muscular
 - memória de longo prazo



4. Atividades nano no CCS/UNICAMP

A) Research on advanced process modules

1. New gate dielectric material
2. Poly-crystalline SiGe layers
3. Shallow junctions
4. Plasma etching processes
5. Si Nano-clusters
6. Carbon Nanotubes

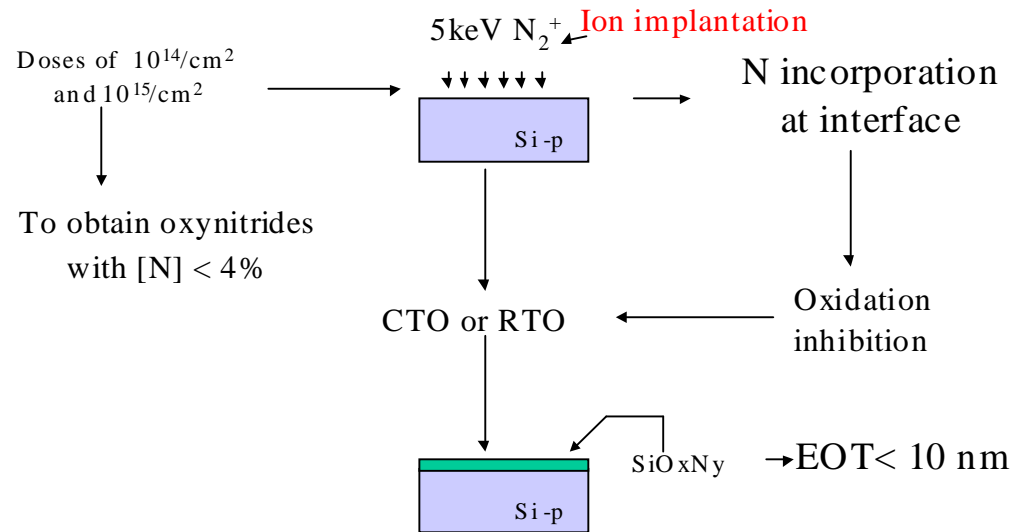
A.1 New gate dielectric materials

- SiO_xN_y by N_2^+ I/I + thermal oxidation
- SiO_xN_y by remote plasma oxidation
- $\text{Ti}_x\text{SiO}_y\text{N}_z$ by remote plasma oxidation + Ti diffusion
- AlN_xO_y by AlN_x reactive sputtering + thermal oxidation

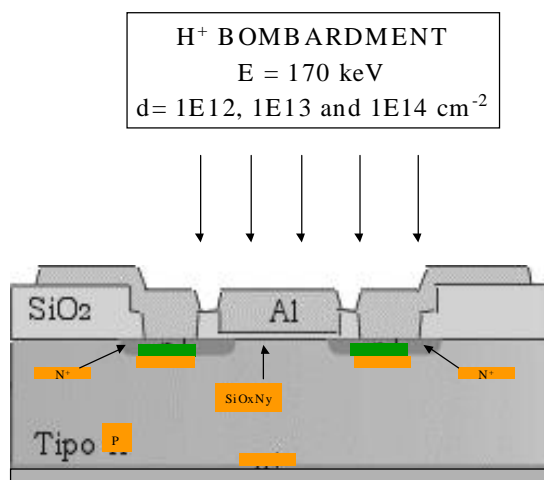
SiO_xN_y by - N₂⁺ I/I + thermal oxidation

SILICON OXYNITRIDE FORMATION

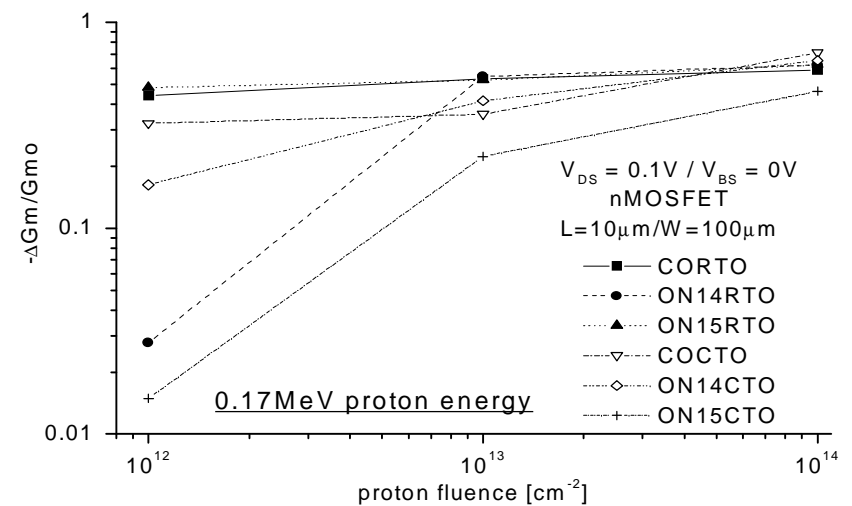
GATE nMOSFETS



Radiation Hardening experiments



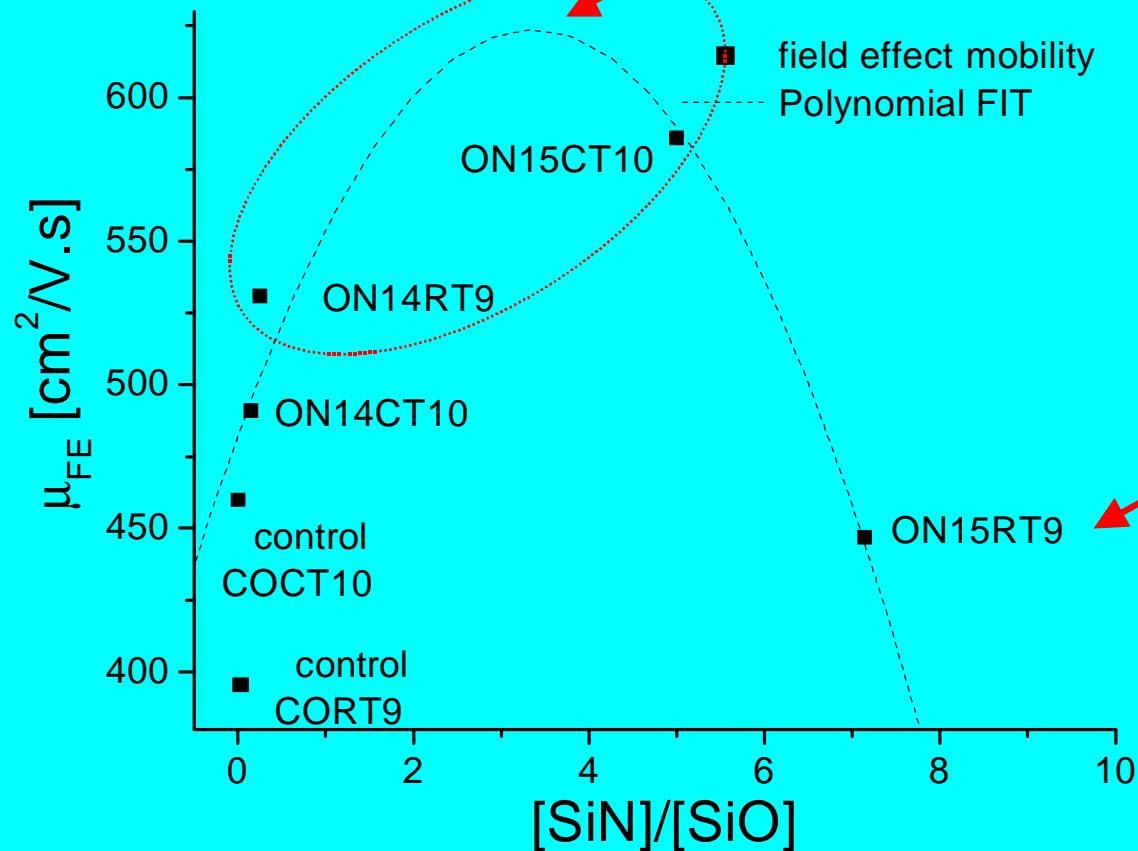
Transconductance degradation



SiO_xN_y by N_2^+ I/I + thermal oxidation

Mobility x SIMS results

Optimum [N] can be adjusted

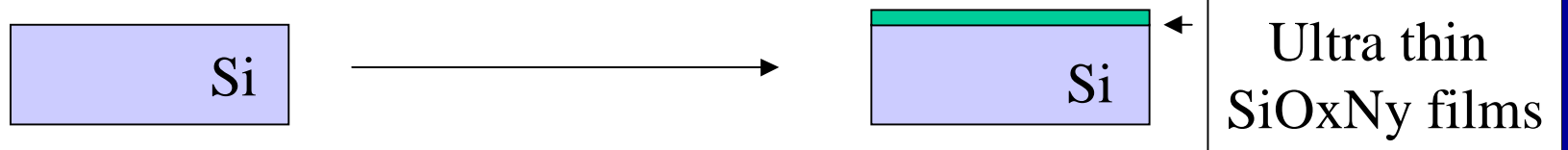


The mobility degradation with the high nitrogen concentration

Correlation between the maximum nitrogen concentrations at oxynitride/silicon structures, obtained from the $[\text{SiN}]/[\text{SiO}]$ ratio profile peaks and the nMOSFET field effect mobility

Thin Dielectrics – Remote Plasma

N₂O or N₂O/N₂ REMOTE PLASMA OXIDATION



Transmission Electron Microscopy

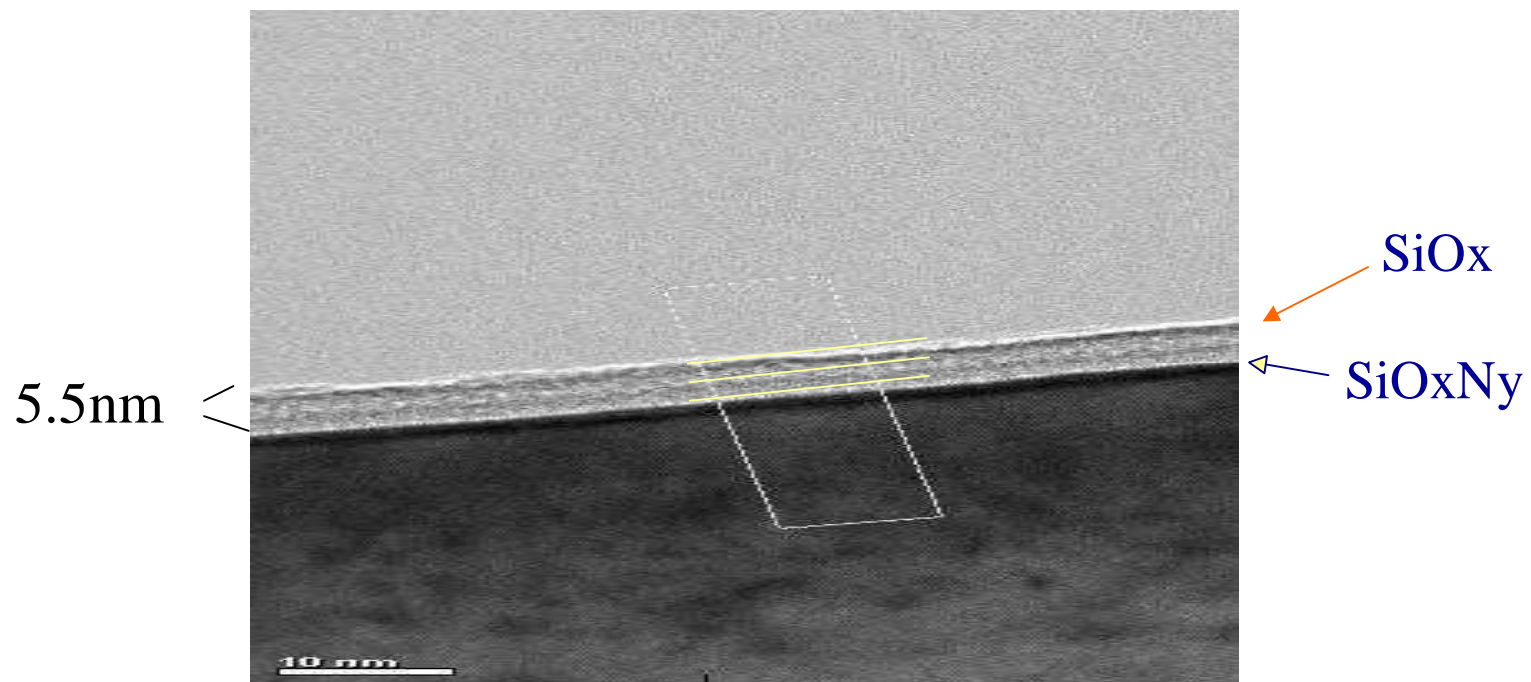
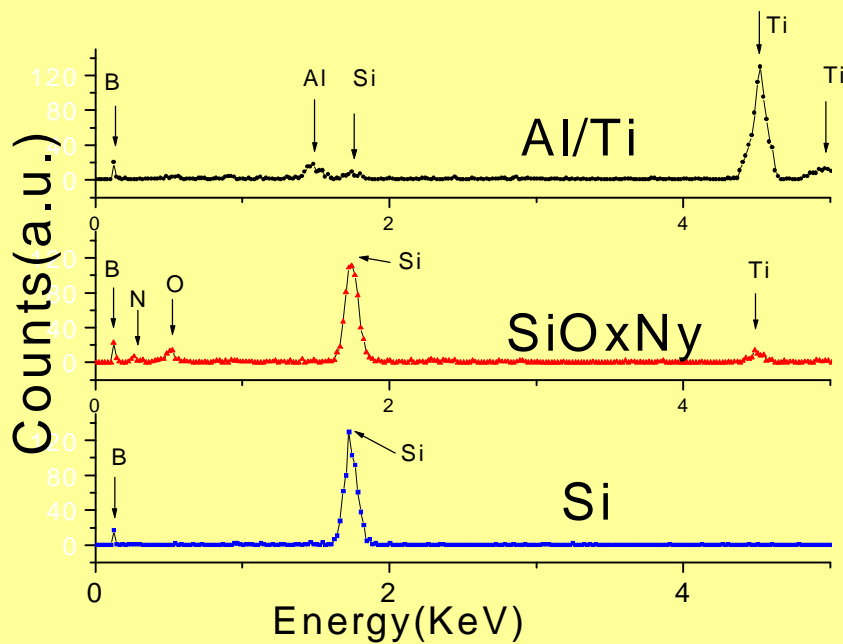
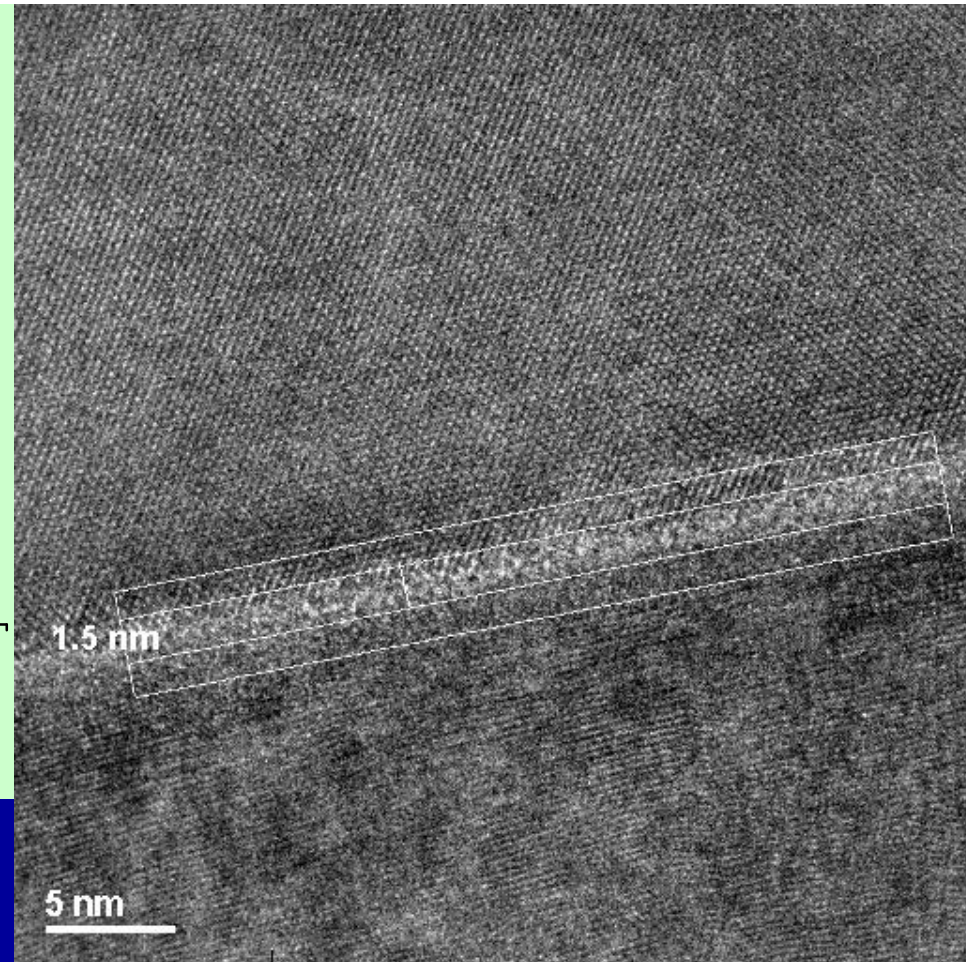
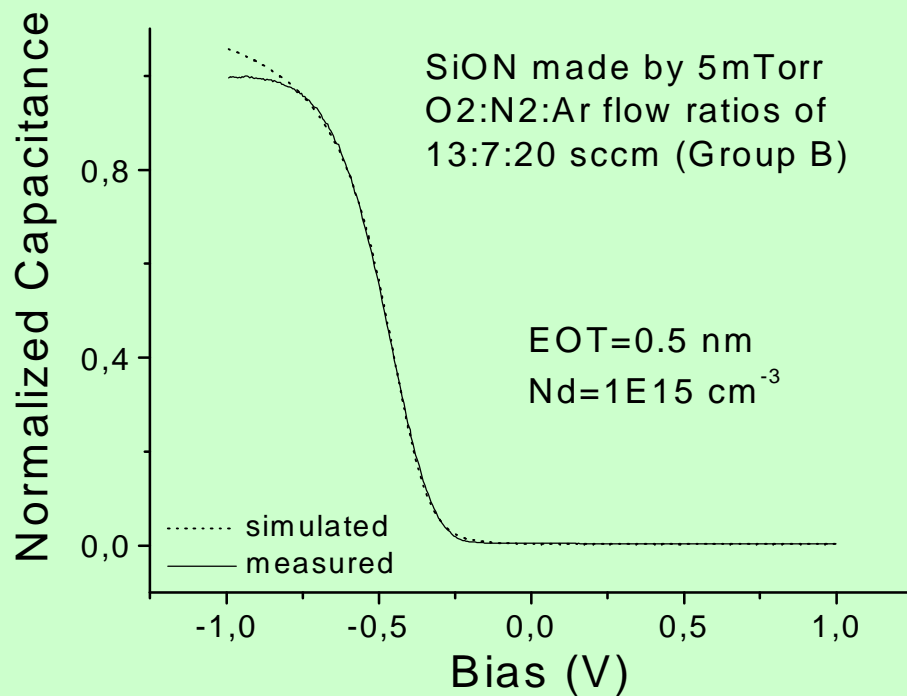


Image of SiO_x/SiO_xN_y/Si structure of ON1P1 samples with a magnification of 200Kx



K ~ 12

TiSiON with EOT = 0.5nm

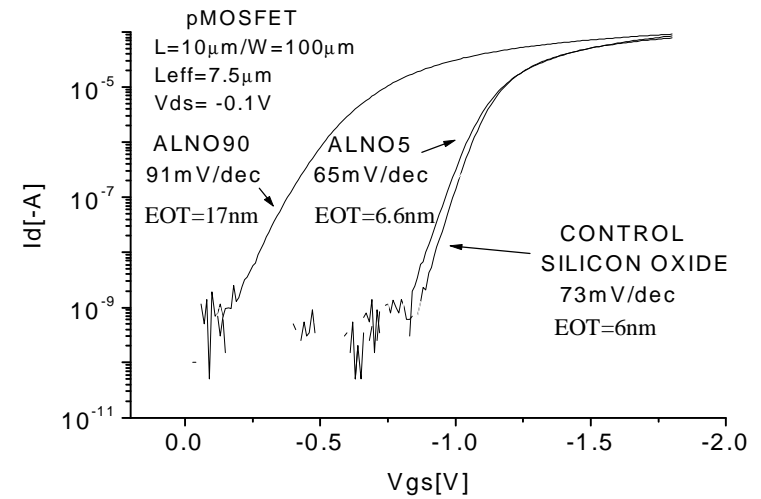
Thin Dielectrics – AlN_xO_y

AlN sputtering deposition + rapid thermal oxidation

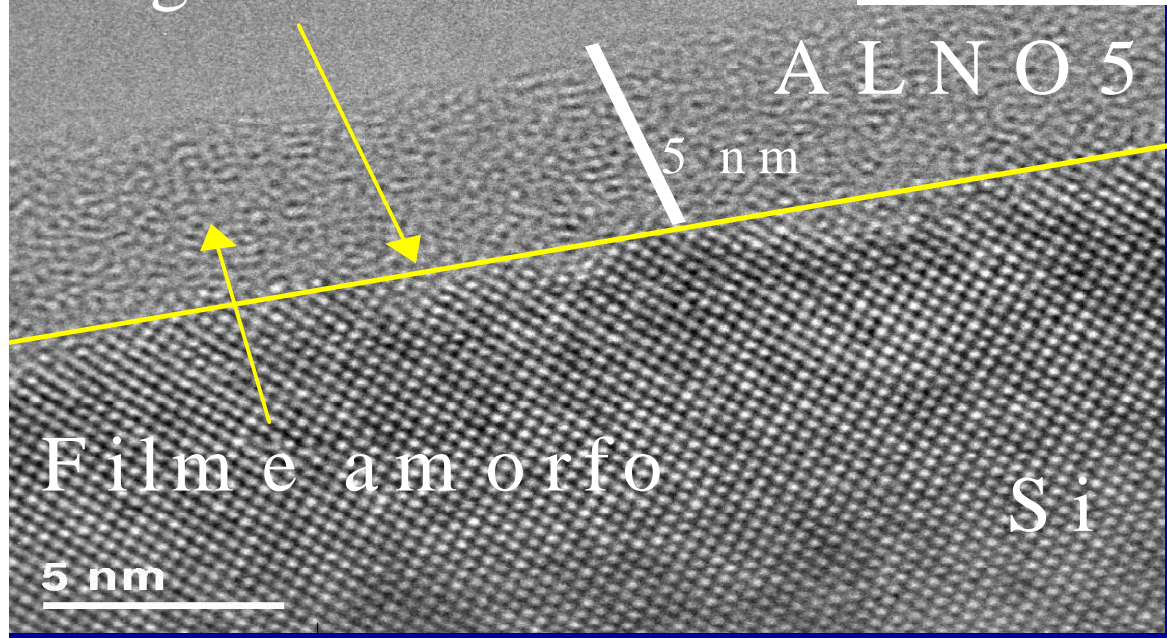


High k dielectrics

Ultra thin AlO_xN_y films



Rugosidade baixa



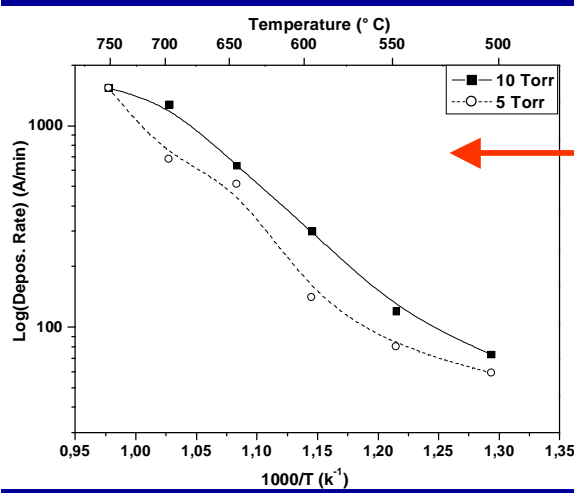
A.2 Poly-crystalline SiGe layers

- Lower thermal budget
- Lower sheet resistance
- Allow workfunction engineering
 - No channel implantation required
- Etches in Hydrogen peroxide and is resistant to HF etch.

Poly-SiGe Technology – LPCVD:

Deposition Range: 5 – 10 torr / 500 – 750 ° C

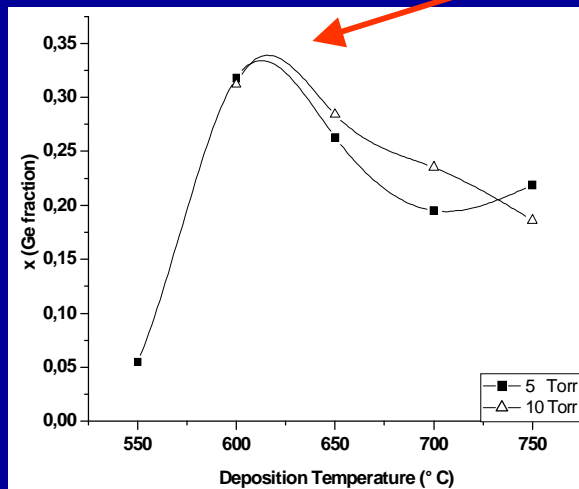
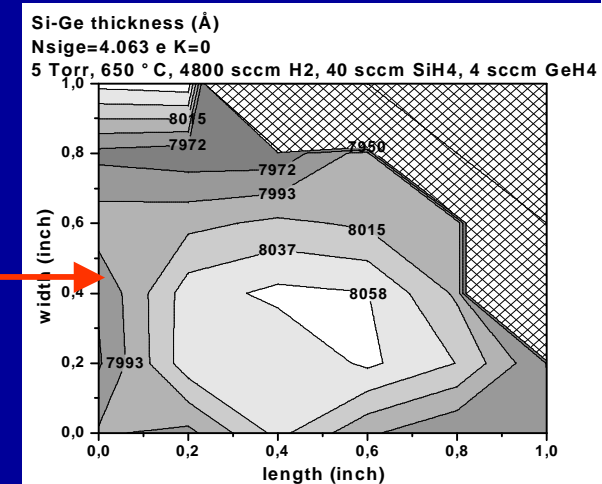
GeH₄ = 4 sccm; SiH₄ = 40 sccm; H₂ = 4800 sccm



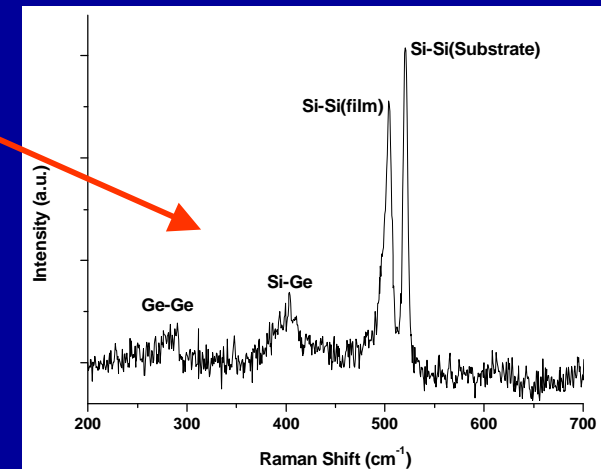
Depos. Rate: 130 nm/min

Uniformity: below 2%

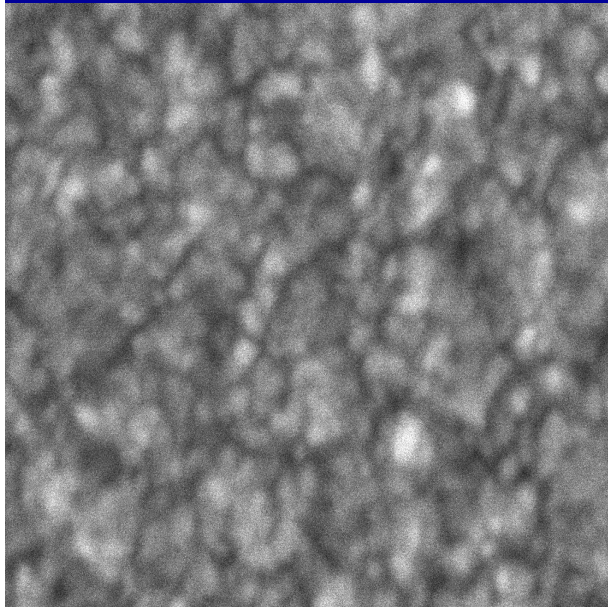
Ge fraction up to 32%



Raman

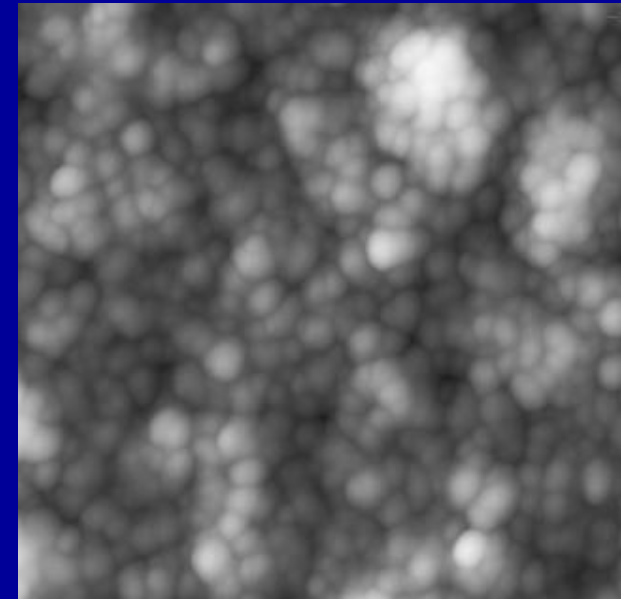


Poly-SiGe Technology



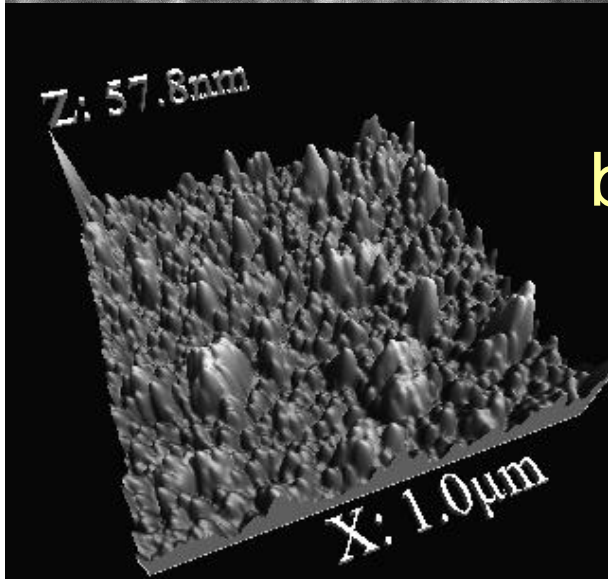
SEM and AFM

Grain size
50 nm

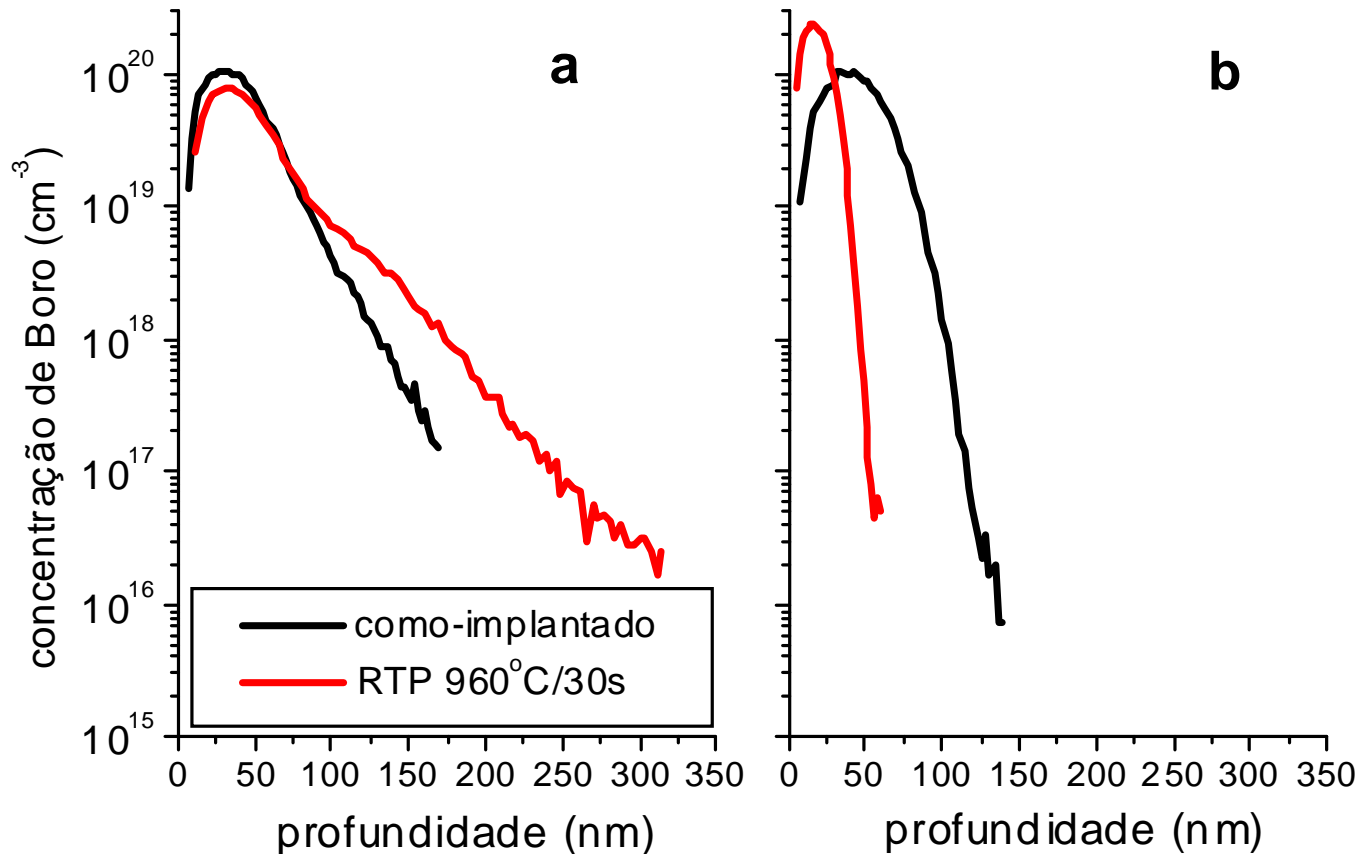


Roughness
between 6 and 17 nm

(For Poly-Si: between 4 and 80 nm)



A.3 Shallow junctions: I/I of F + B



a) I/I direta de B⁺ em Si

b) I/I de B⁺ em Si pré-amorfidado com F⁺

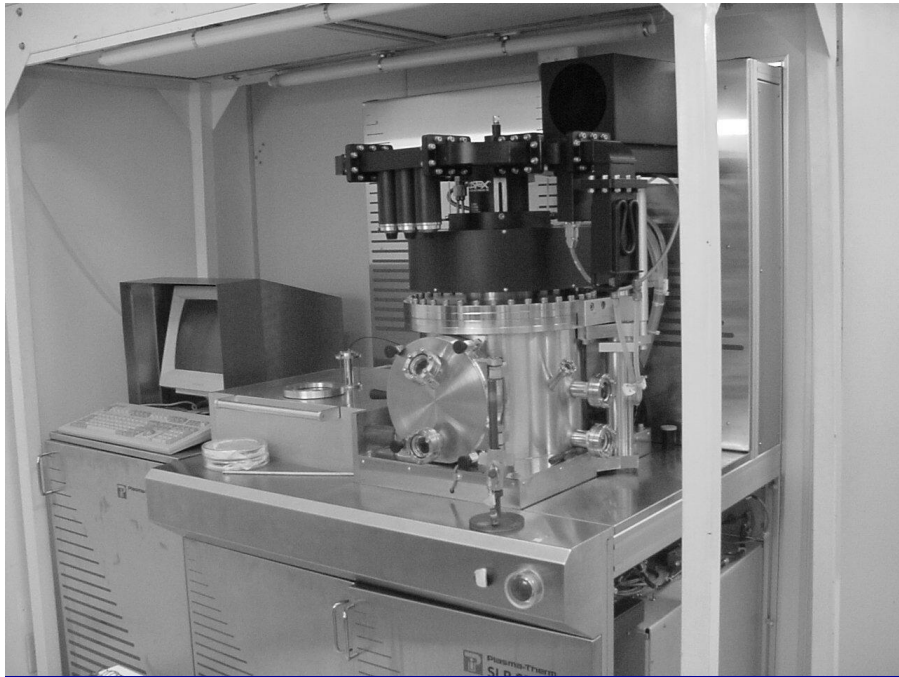
⇒ *defect engineering* p/ reduzir profundidade da junção (*uphill diffusion*)

A.4 Plasma Etching for CMOS & MEMS

- RIE (three systems)
- ECR
- ICP – in construction

- Gases: SF_6 , CF_4 , CHF_3 , Cl_2 , HBr , SiCl_4 , CH_4 , O_2 , H_2 , N_2 , Ar

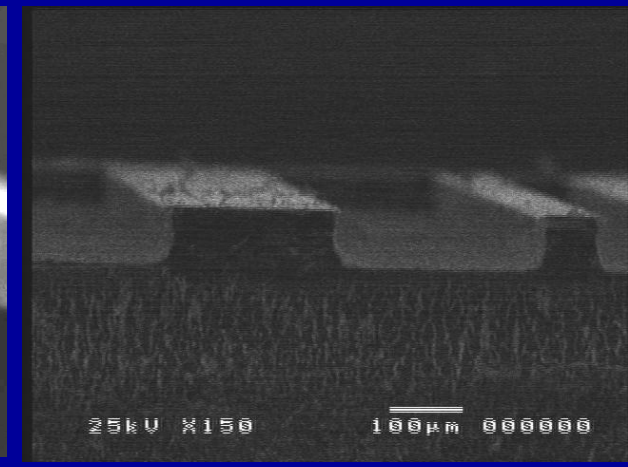
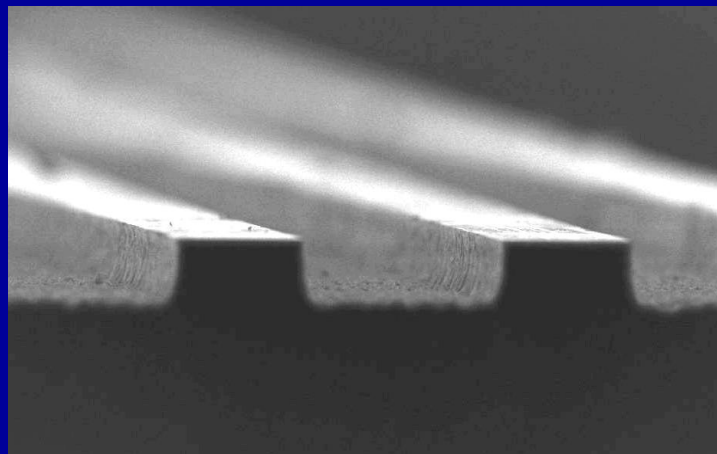
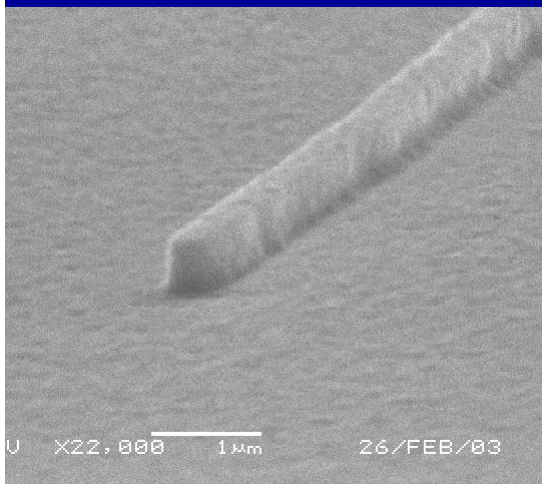
- Materials: Si , Poly-Si, SiO_2 , Si_3N_4 , BCB, W , Pt , III-V



Si-poli $\sim 0,25 \mu\text{m}$

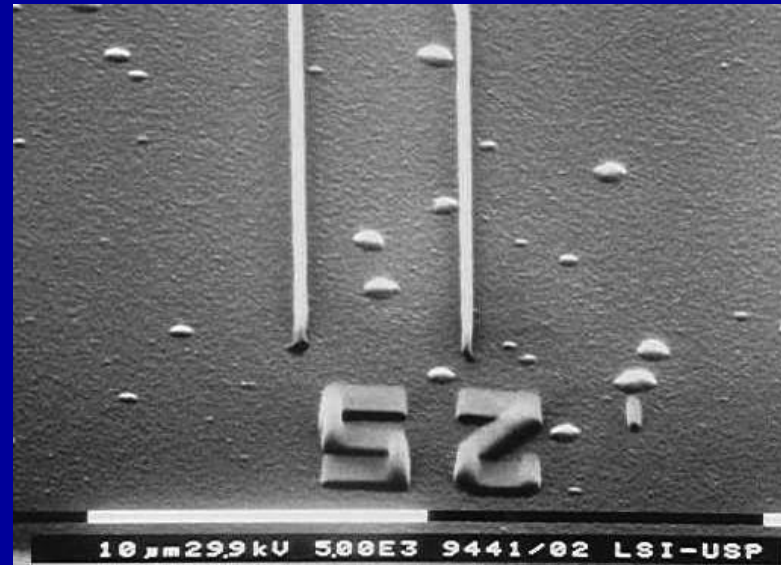
RIE: $\text{SF}_6/\text{CF}_4/\text{O}_2/\text{Ar}$,
 $0.7 \mu/\text{min}$, $A \sim 0.95$

“Bosch” (SF_6/CHF_3) RIE
convencional $\sim 100 \mu\text{m}$

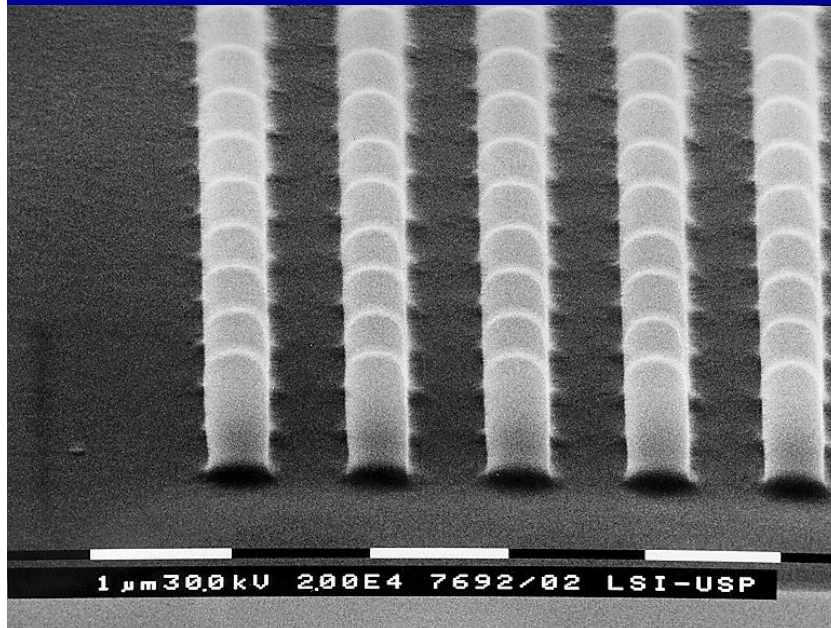


- Fabrication of submicron structures (e-beam @ LSI/USP)

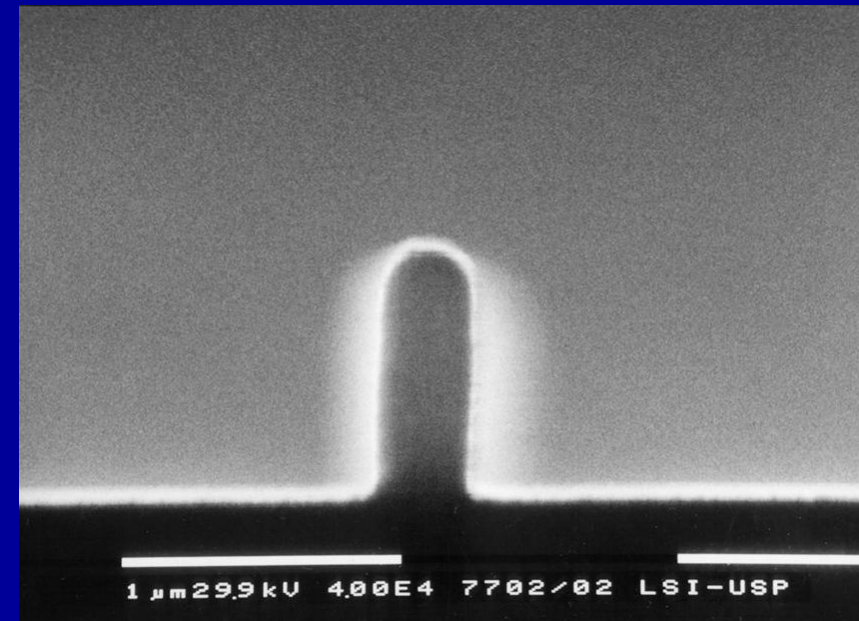
Lines - 0,25 μ m



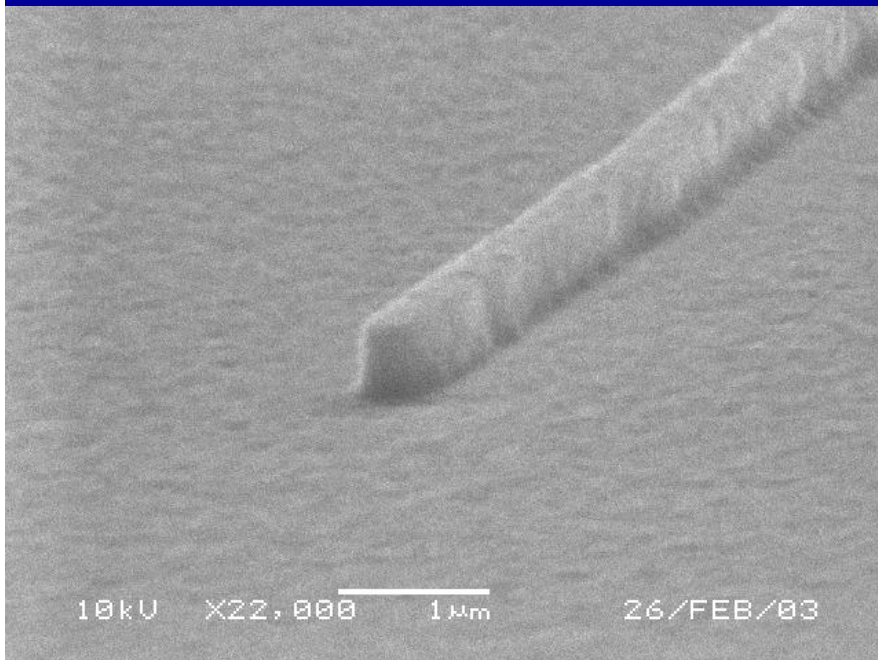
Pilars of 0,5 μ m



Isolated lines - 200nm



Poly-Si Plasma Etch

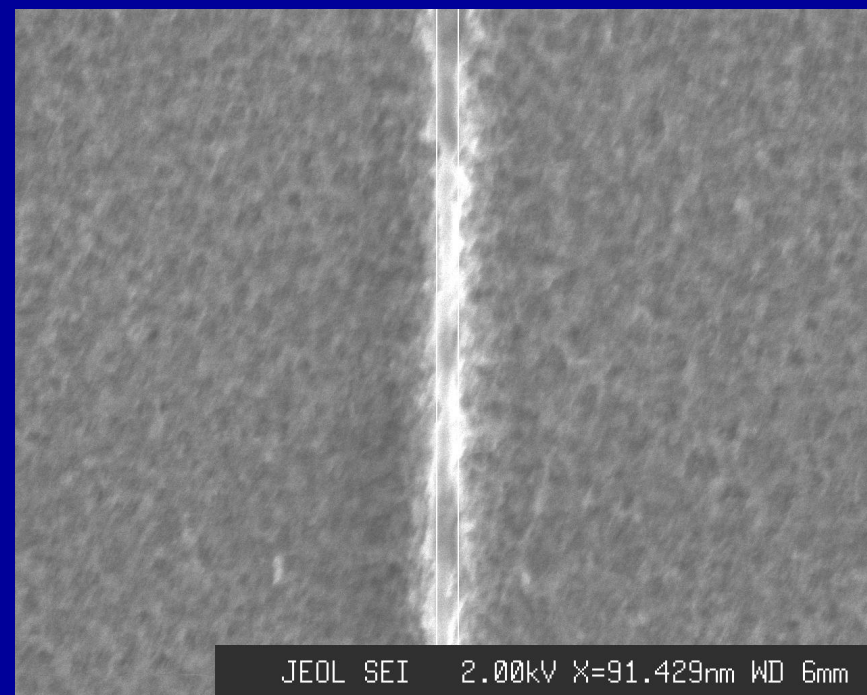
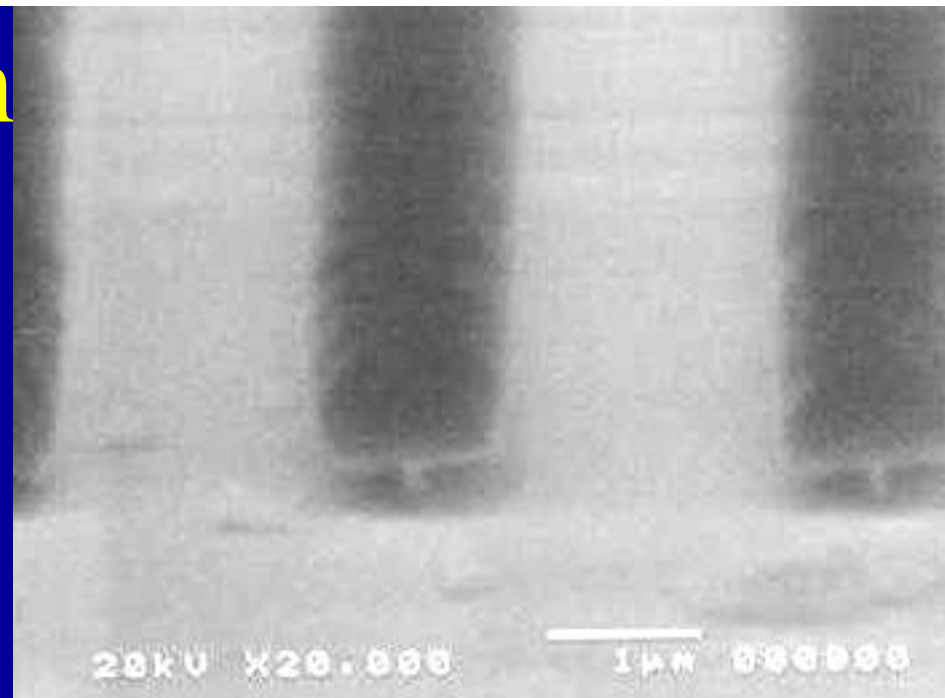


250 nm



$\text{SF}_6/\text{CF}_4/\text{CHF}_3 = 3/10/10$ sccm
50 W, 80 mTorr, 190V.

90 nm



Plasma Etching Processes for CMOS

1. SiN_x

Reactor	Gas mixtures	Power, pressure	Etch rate, nm/min	Selectivity SiN _x /SiO ₂	Selectivity SiN _x /Si
RIE	5SF ₆ /20CH ₄ / 20N ₂	50 W, 150 mTorr	47	5,8	0,07
RIE	5SF ₆ /20CH ₄ / 20N ₂ /9O ₂	50 W, 150 mTorr	25	4,1	2,7
ECR	5SF ₆ /50O ₂ / 10N ₂ , $N_s + NO_g \rightarrow N_2\uparrow + O_s$	750 W (ECR), 0 W (RF), 50 mTorr,	17	>17 (~ 30-50)	2,1

Plasma Etching Processes for CMOS

2. SiO₂

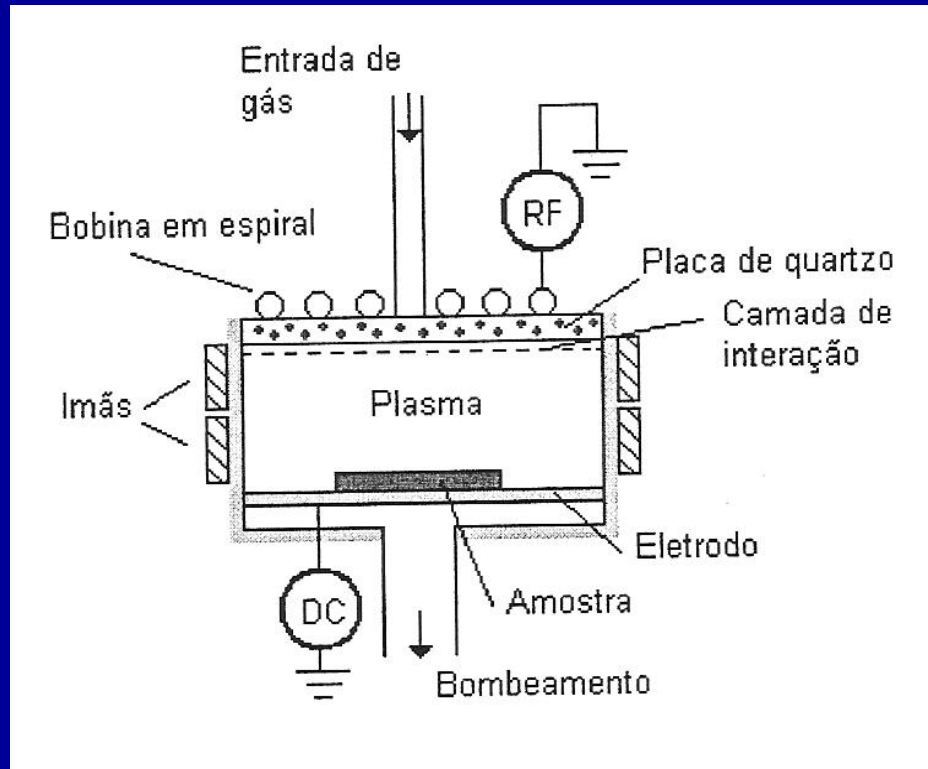
Reactor	Gas mixtures	Power, pressure	Etch rate, nm/min	Selectivity SiO ₂ /Si
RIE (1a fase)	15SF ₆ /30Ar	80 W, 50 mTorr	57	0,3
RIE (2a fase)	15CF ₄ /6H ₂ /5Ar	75 W, 40 mTorr	30	>30

Plasma Etching Processes for CMOS

3. Si-poli

Reactor (mechanism)	Gas mixture	Power, pressure	Etch rate, nm/min	Selectivity Si/SiO ₂	Anisotropy Factor
RIE (thinning/ controlled lateral etch)	15SiCl ₄ / 10CF ₄	50 W, 150 mTorr	30	6	~0,9
RIE (inhibition of lateral etch)	3SF ₆ /10CF ₄ / 10CHF ₃	80 W, 50 mTorr	50	2,4	0,95

LAM RESEARCH Reactor, being re-engineered to ICP-P



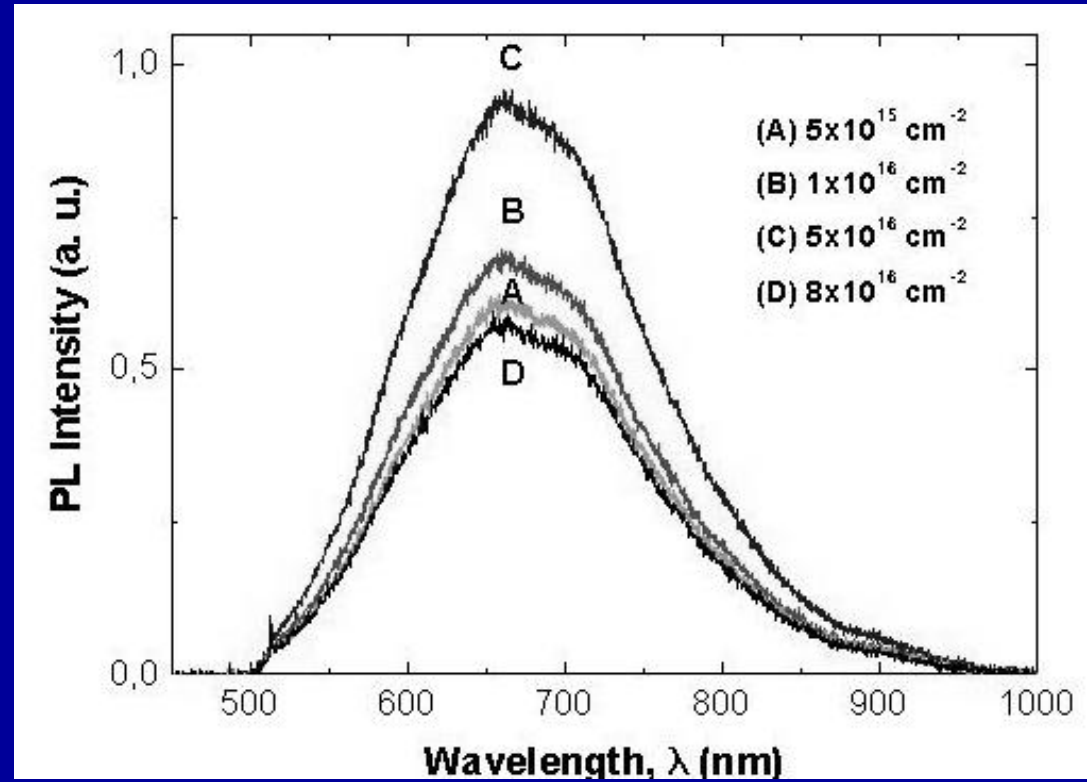
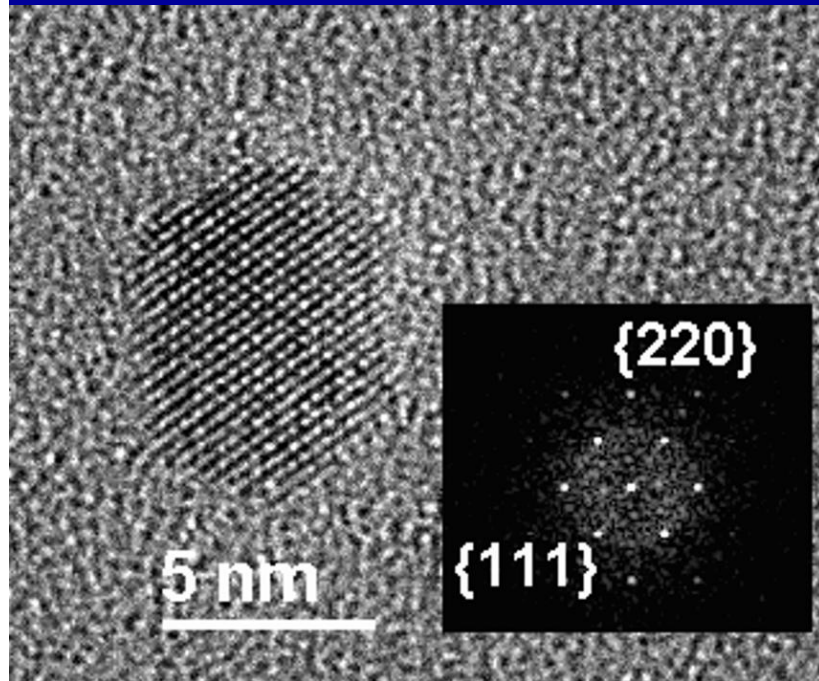
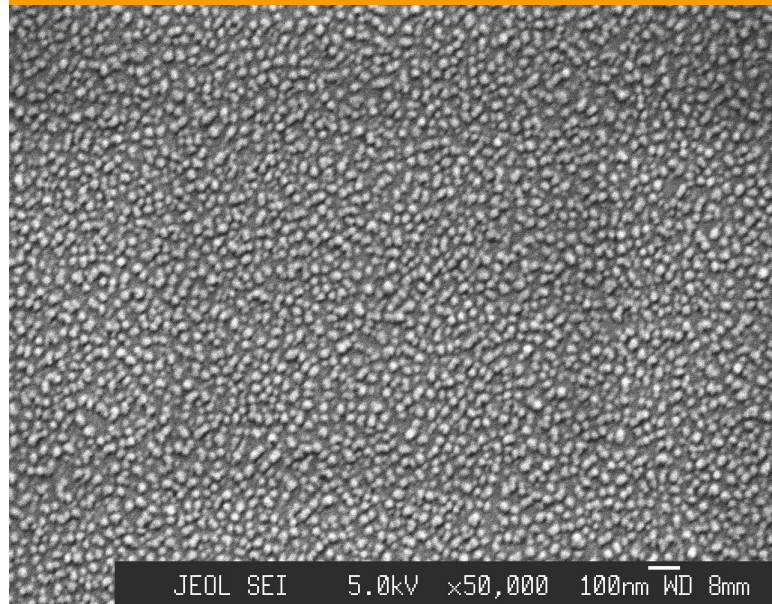
Prototype (Ar plasma):

$$n_e \sim 10^{12} \text{ cm}^{-3}, T_e \sim 2 \text{ eV}$$

A.5 & A.6 Other Nano-structures

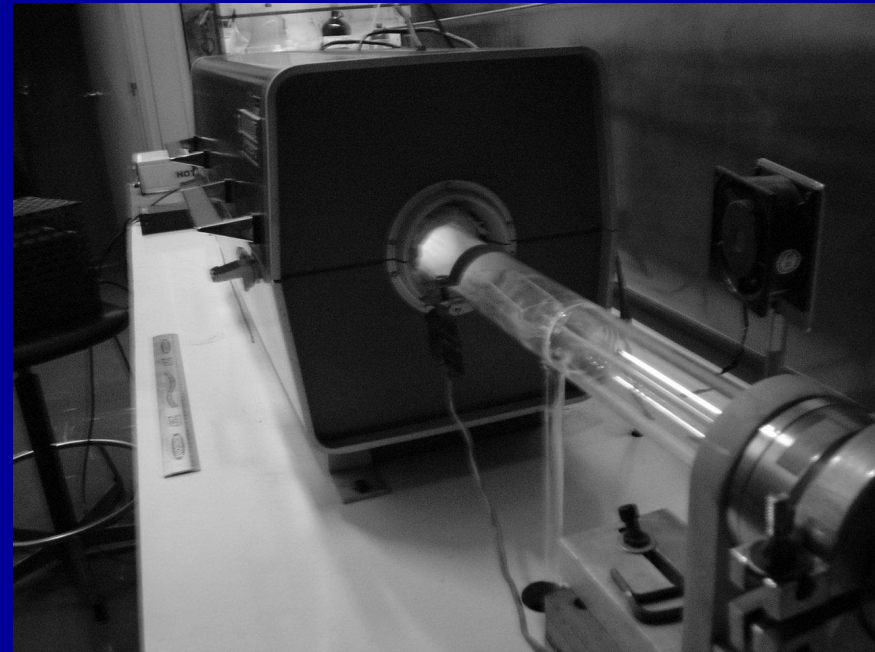
- 3.5 Nano-clusters of Si in SiO₂ films:
 - “Flash” Memory
 - Light Emission
- 3.6 Carbon Nanotubes:
 - Transistors
 - Sensors

A.5 Nano-crystalline Si clusters in SiO₂: I/I of Si + annealing



A.6 CNT's

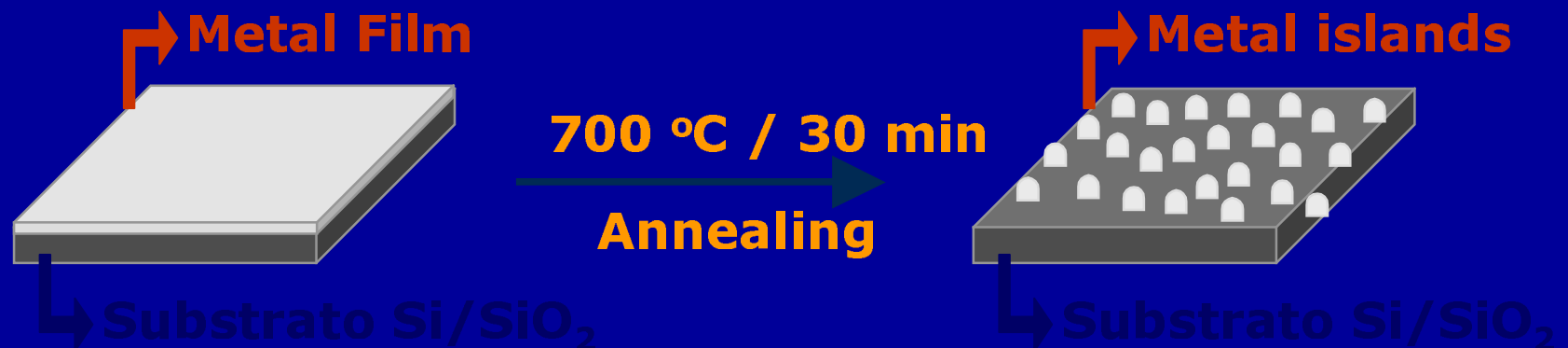
- PECVD – microwave 650 W; 1 Torr; C_2H_2/N_2 ; 500 - 700C.
- APCVD – CH_4/H_2 , CH_4/N_2 or CH_4/NH_3 ; 700 - 950C.
- Catalyst – Ni, Co, Cu, Fe (1 a 60 nm) + agglomeration at 700C

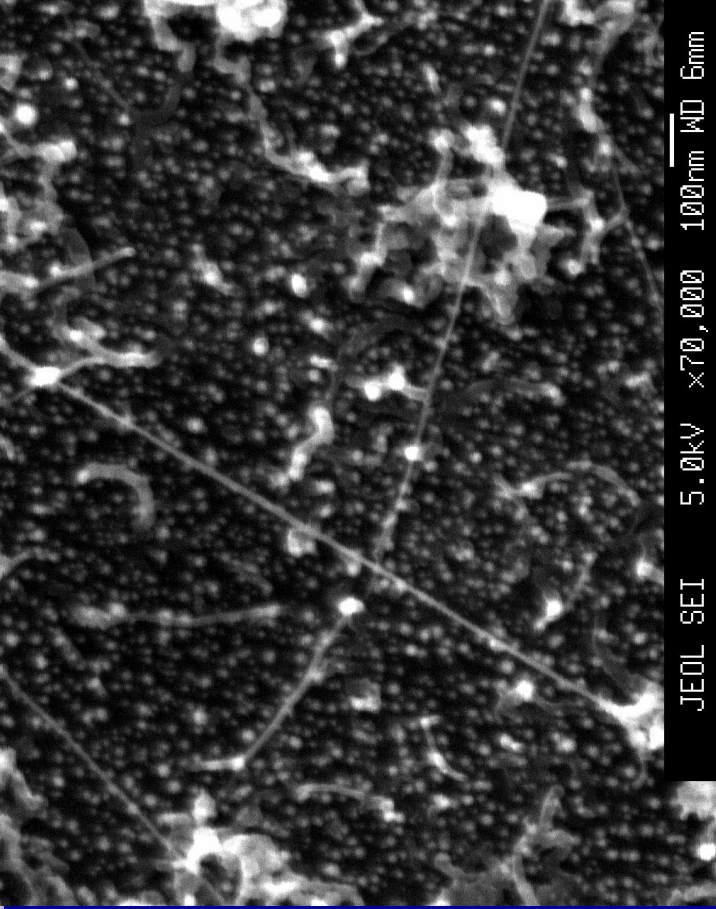
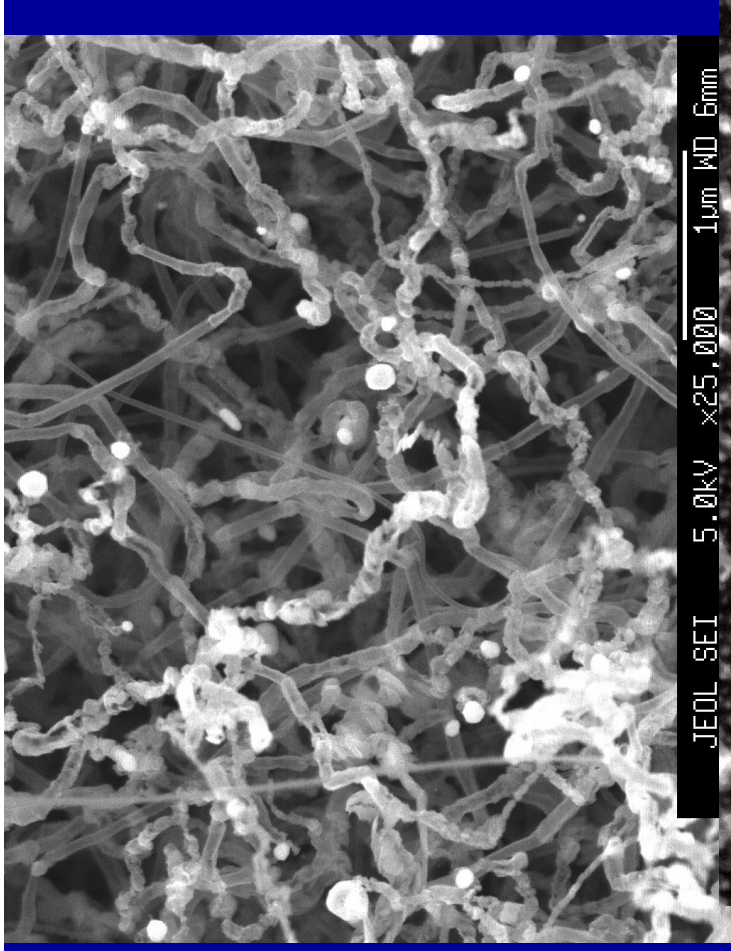
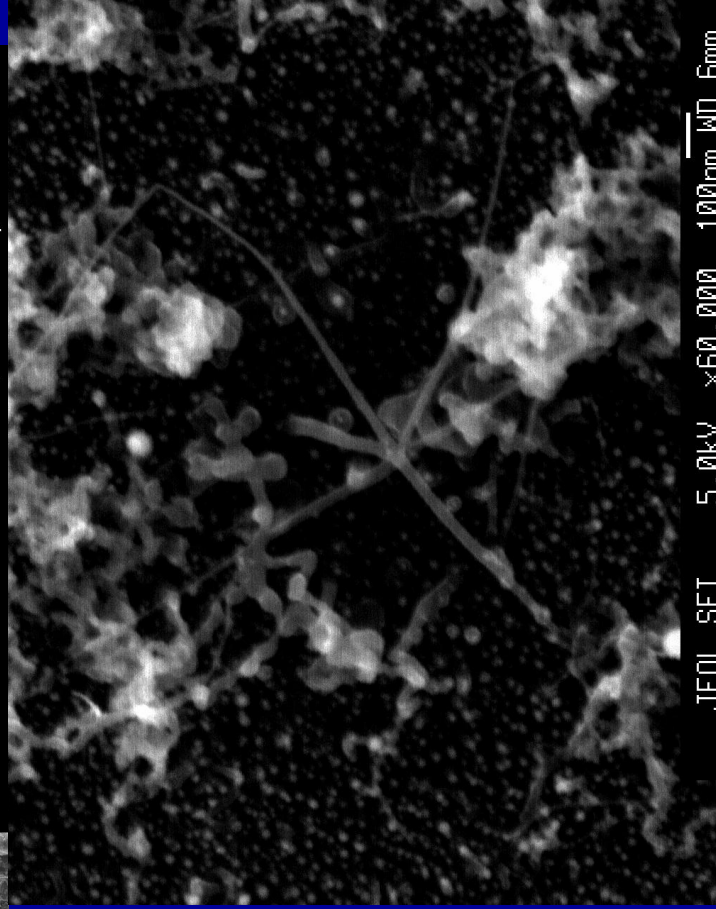
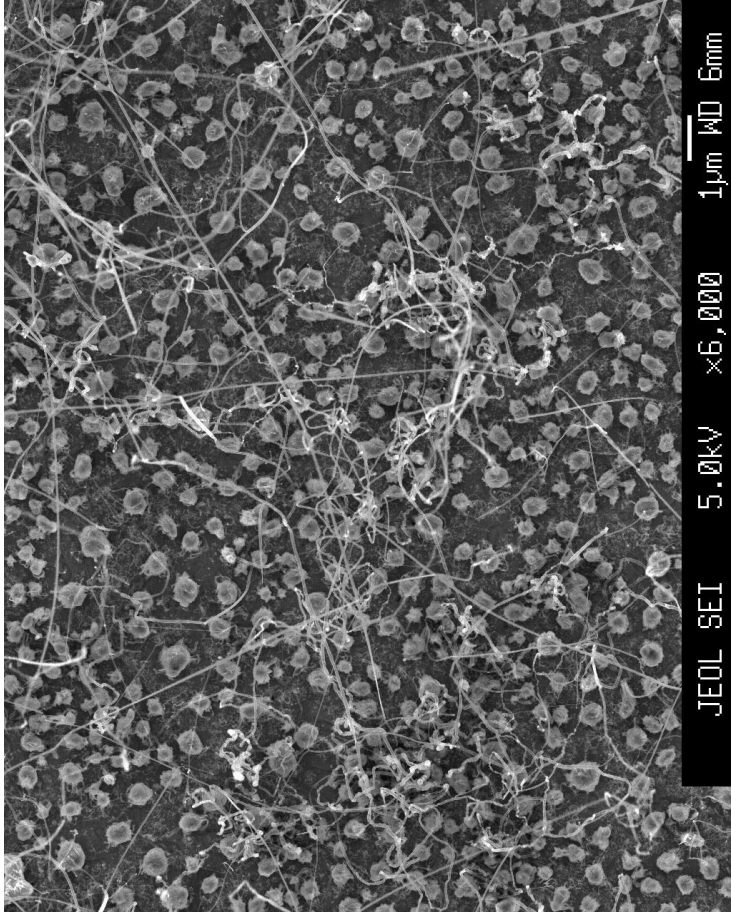


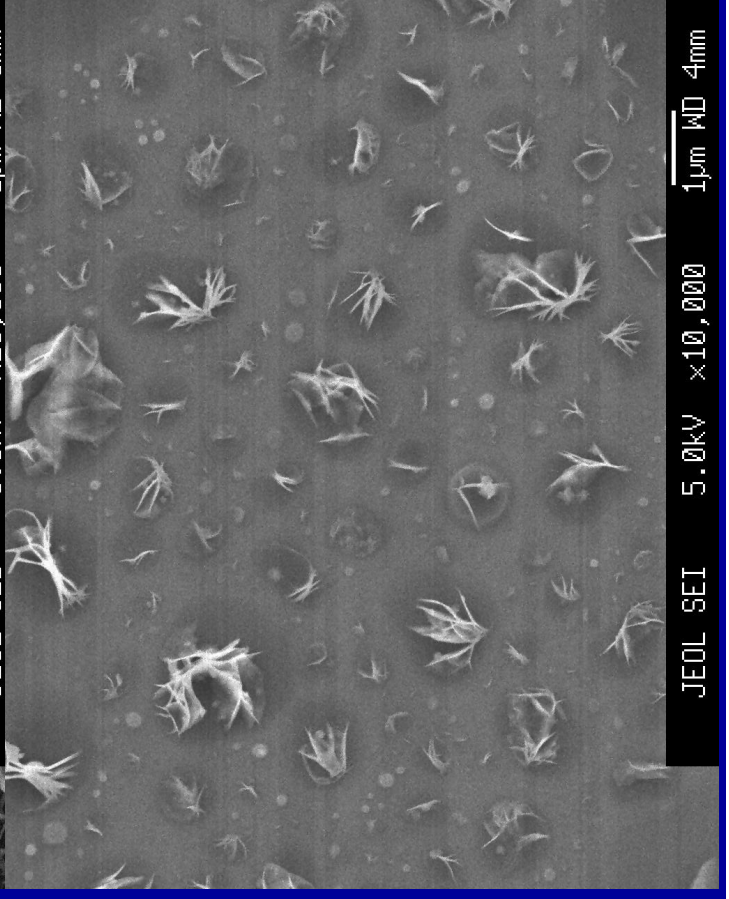
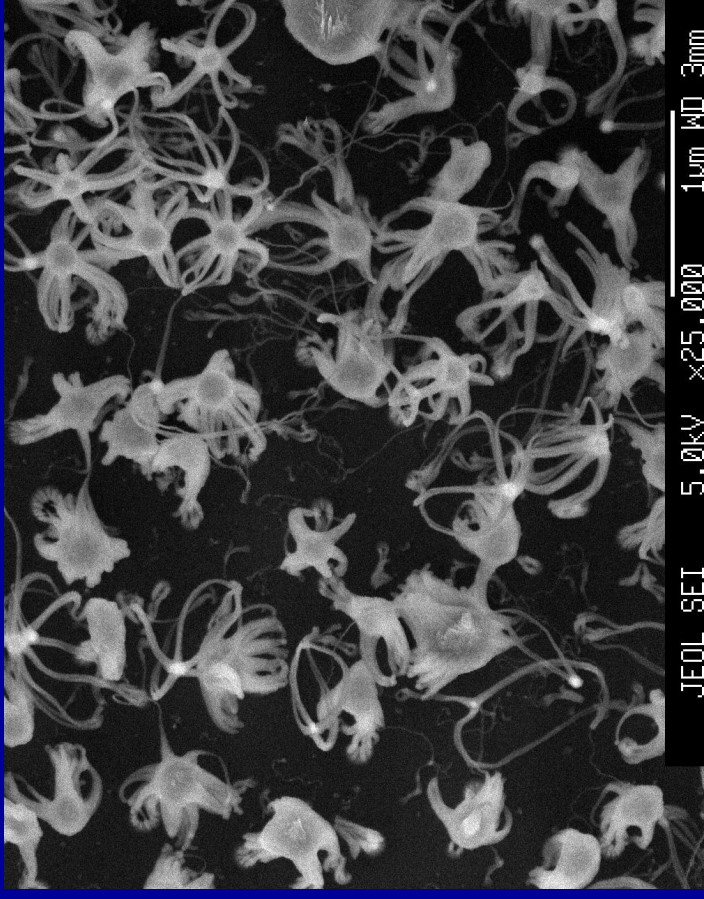
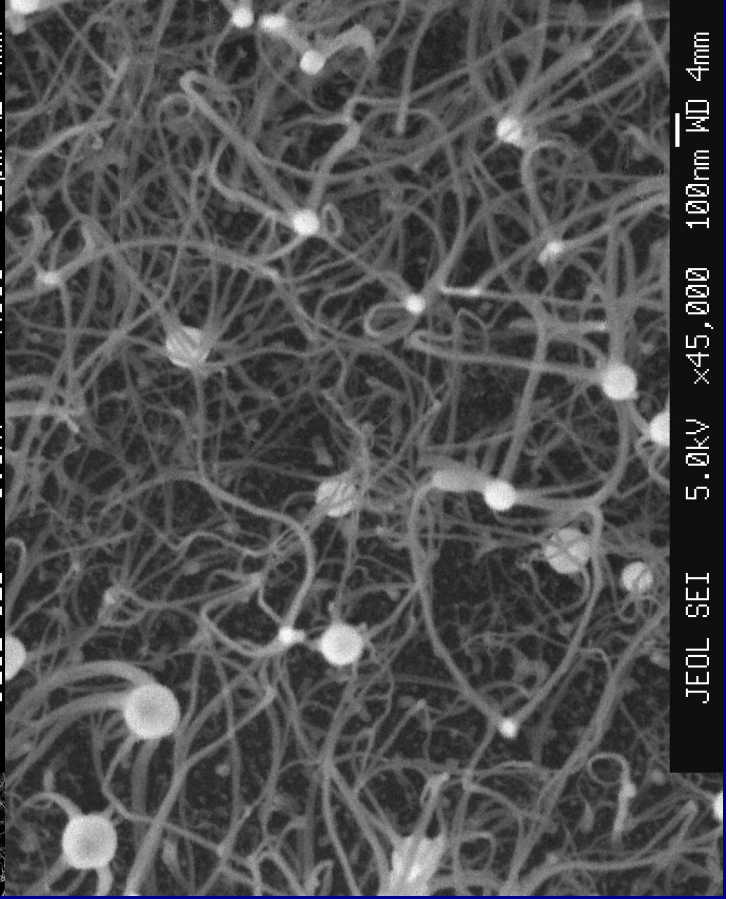
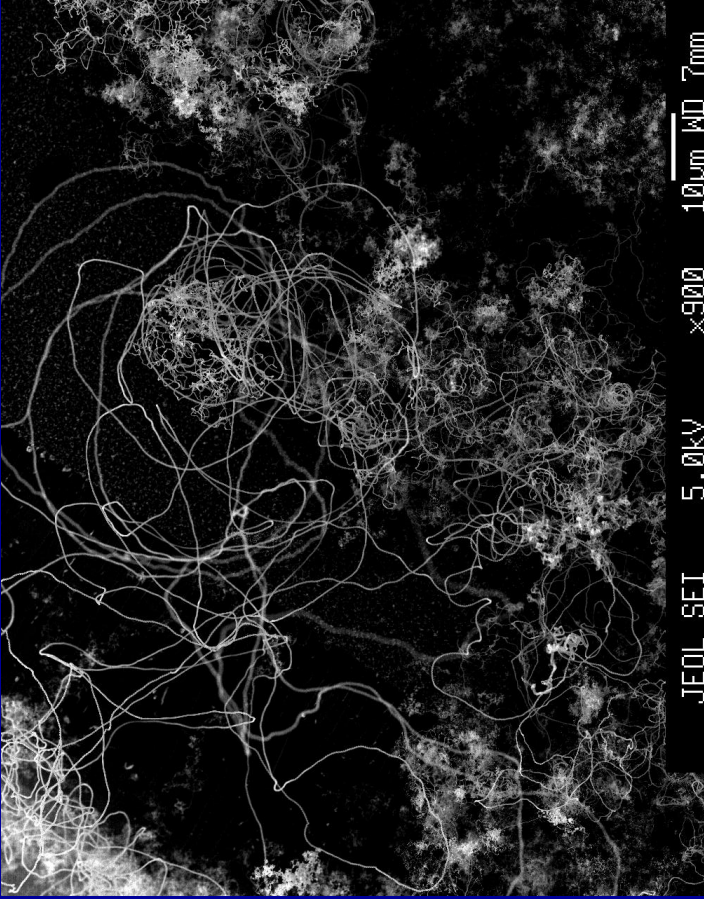
Preparing the catalyst

- Ni thin film (1 to 6 nm thick): by e-beam evaporation
- Fe thin film (5 nm thick): by *sputtering*;
- Fe or Co nano particles (~ 8 nm de diâmetro) in suspension:
by spin-coating.

Thermal treatment of thin films: formation of nano-islands:



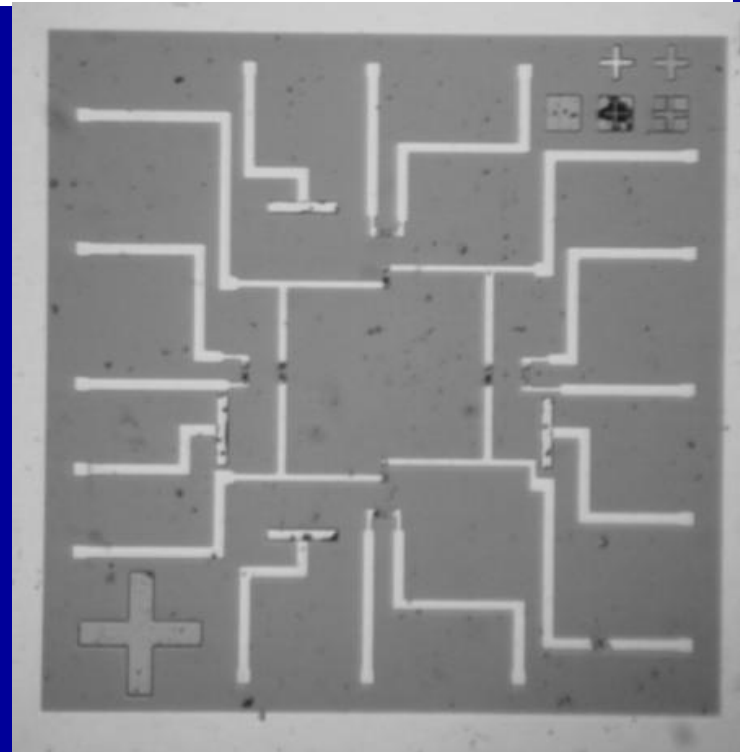
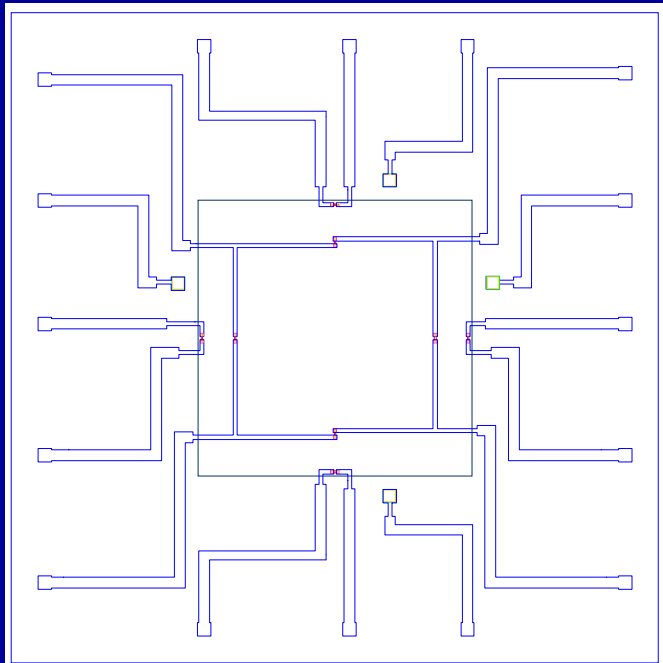
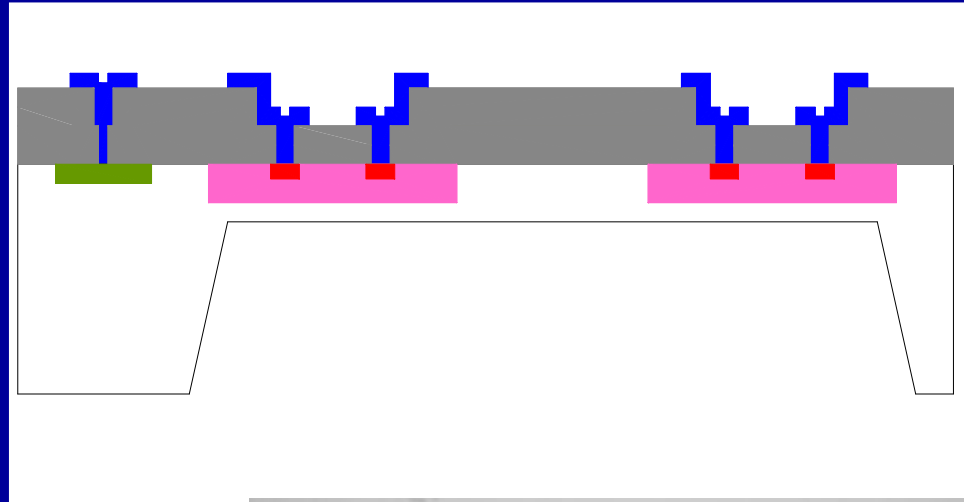
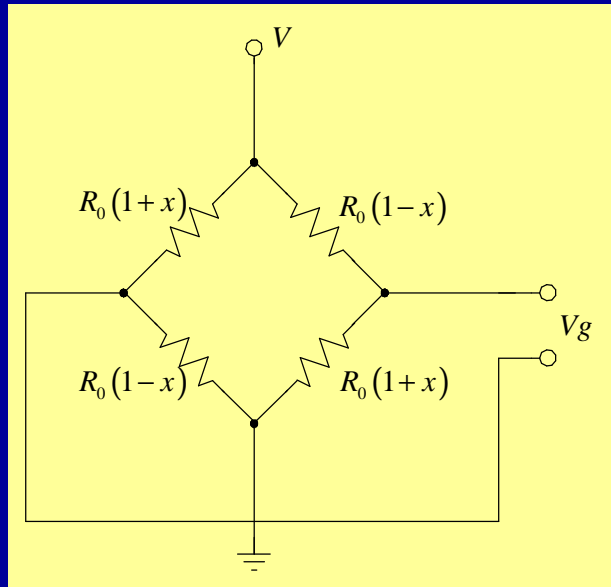




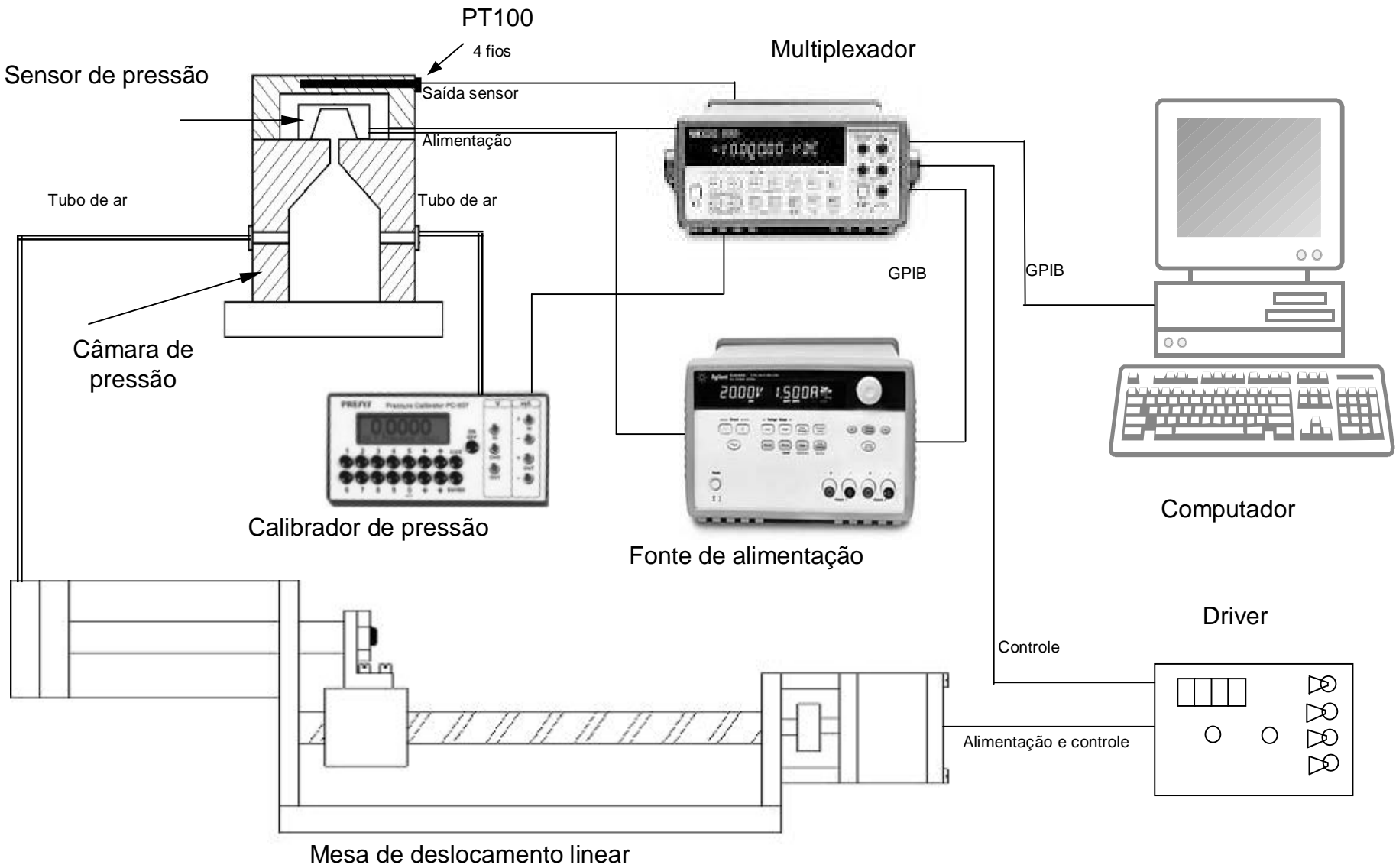
B. Research on Microsystems

1. Pressure sensor
2. Gas flow sensor
3. Bolometer
4. Surface micromachine structures

B.1 Pressure Sensor

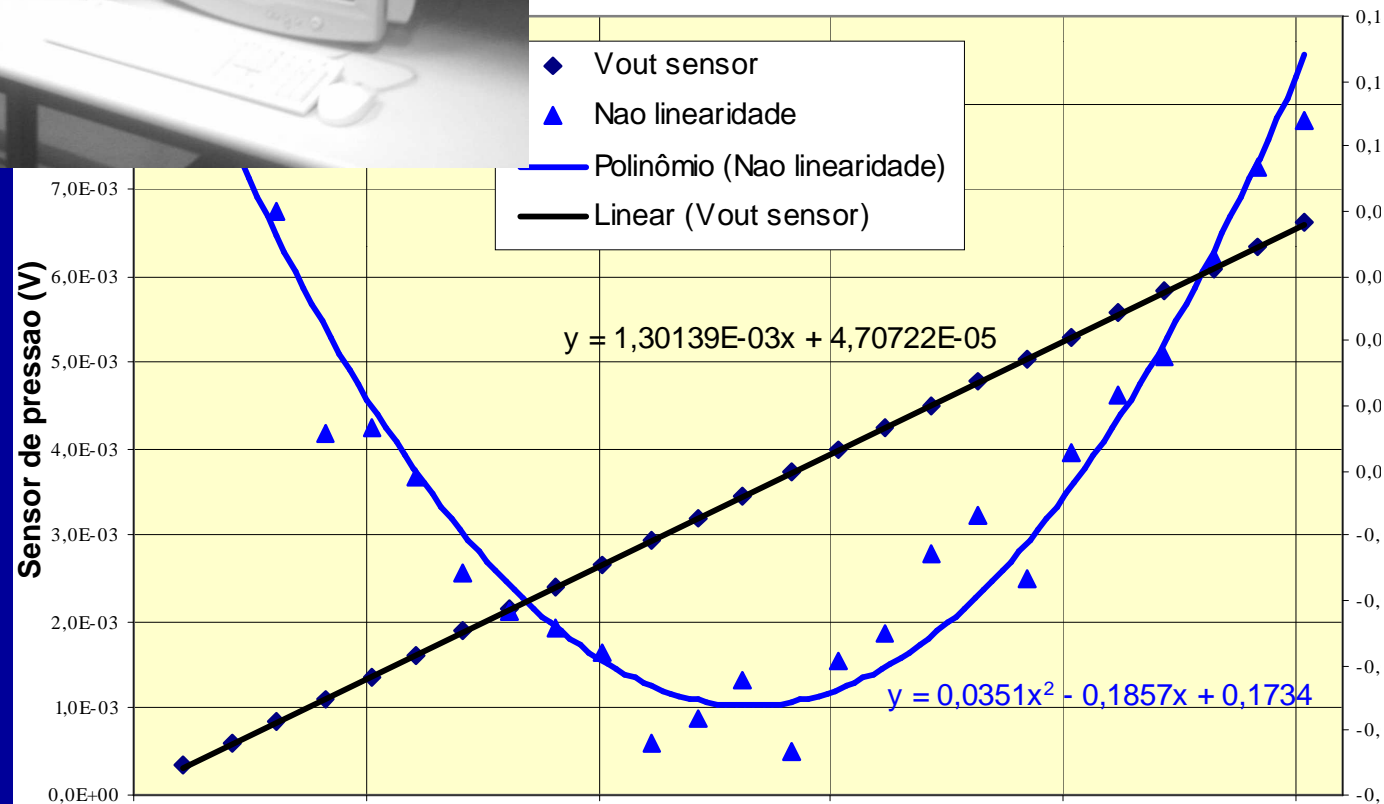


Pressure sensor test set-up

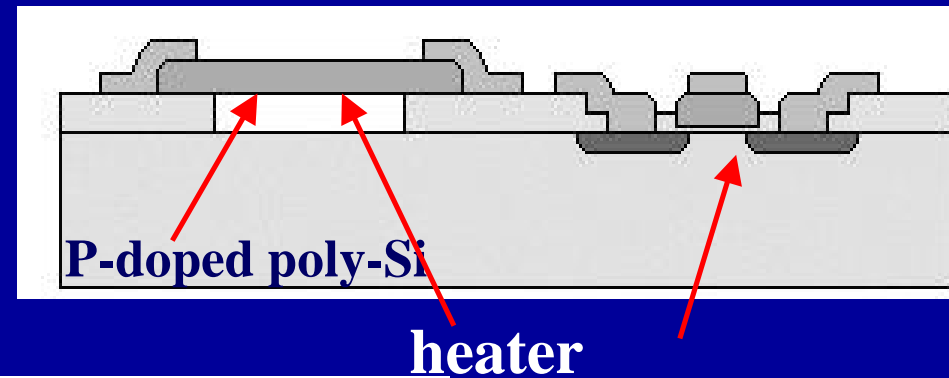
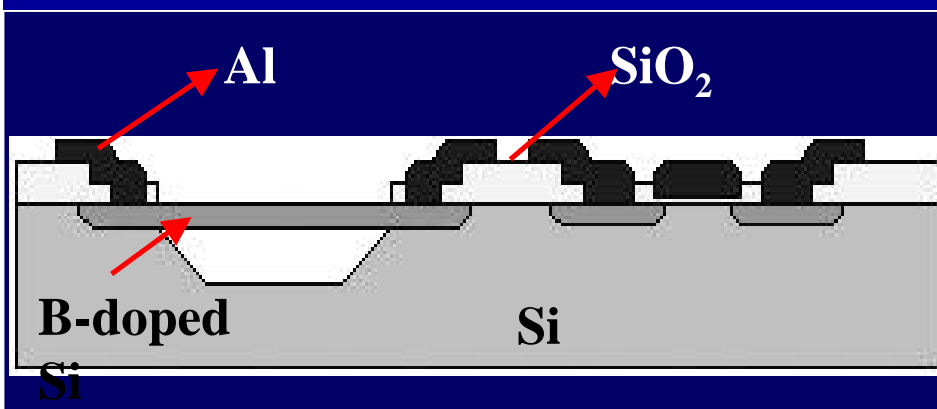
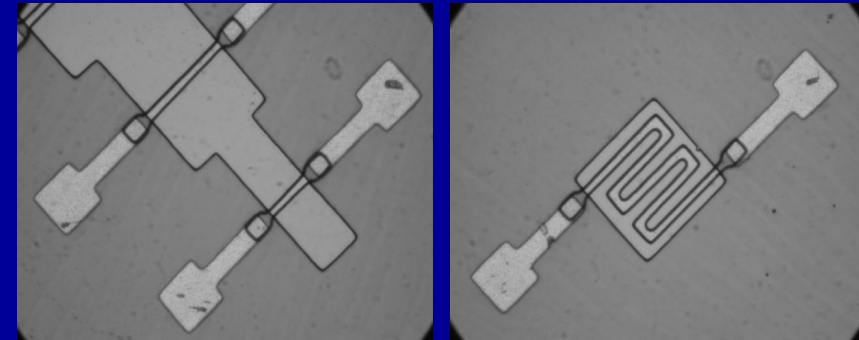
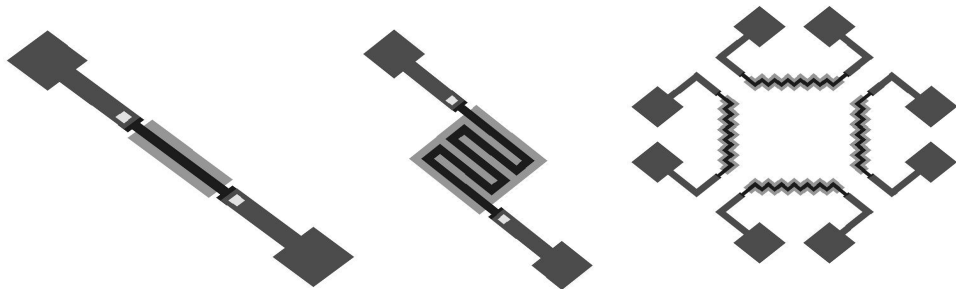




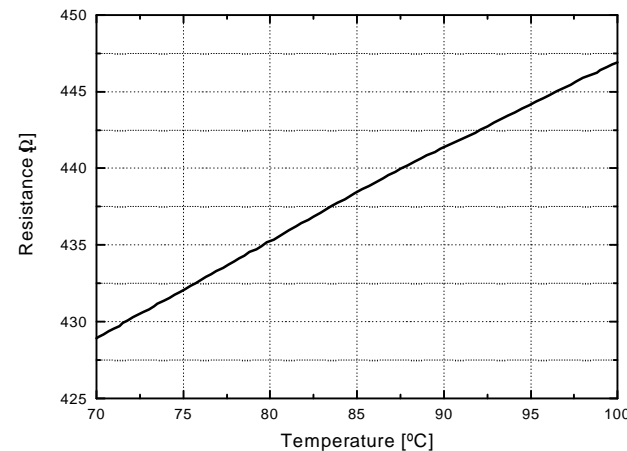
Characterization of a commercial sensor – NPC-100 Nova Sensor



B.2 Gas Flow sensor



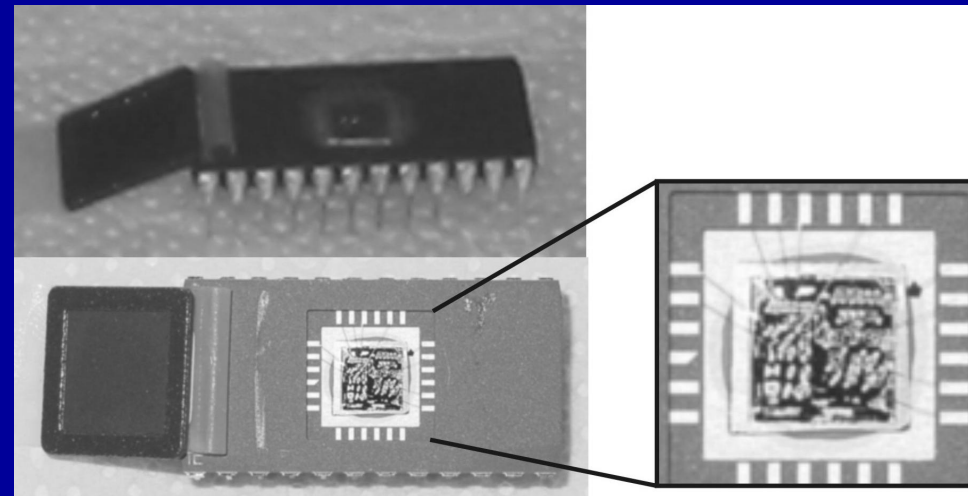
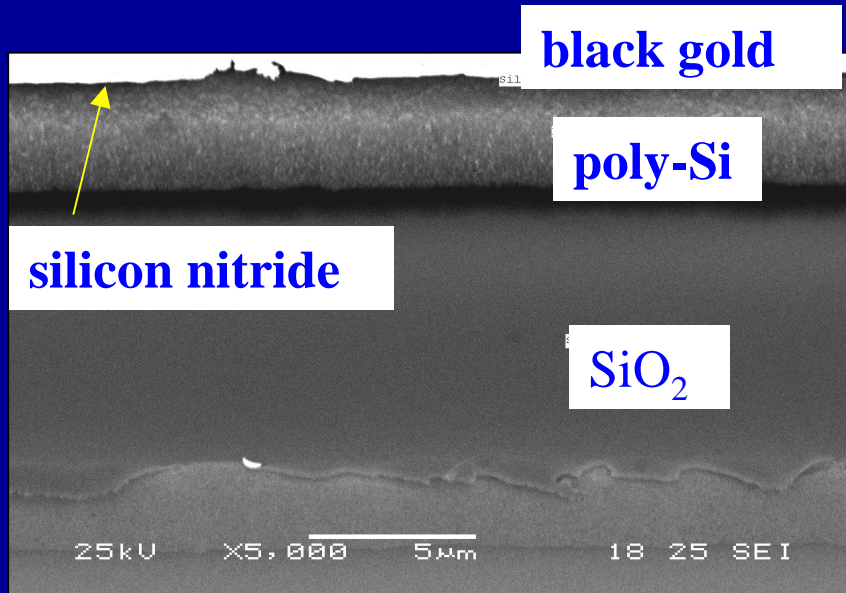
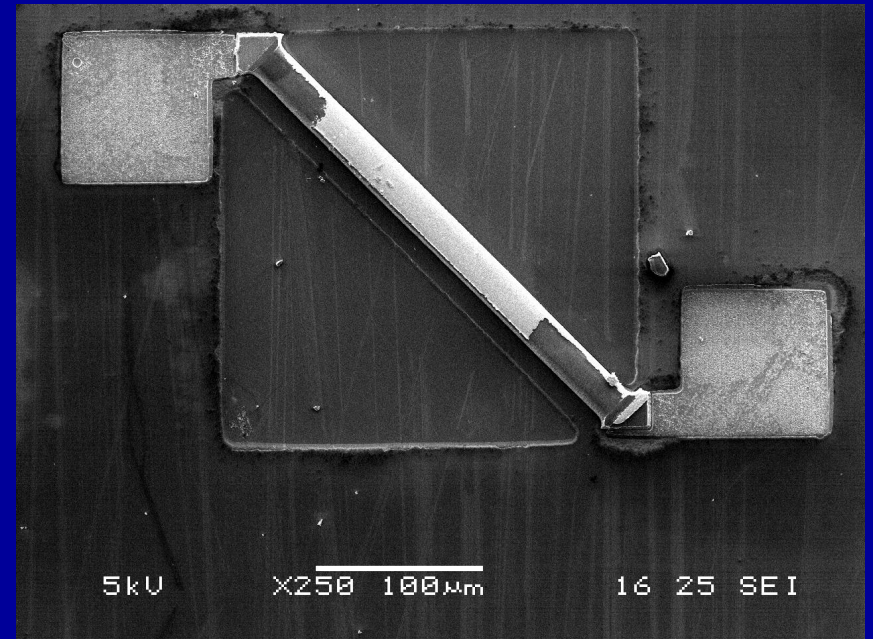
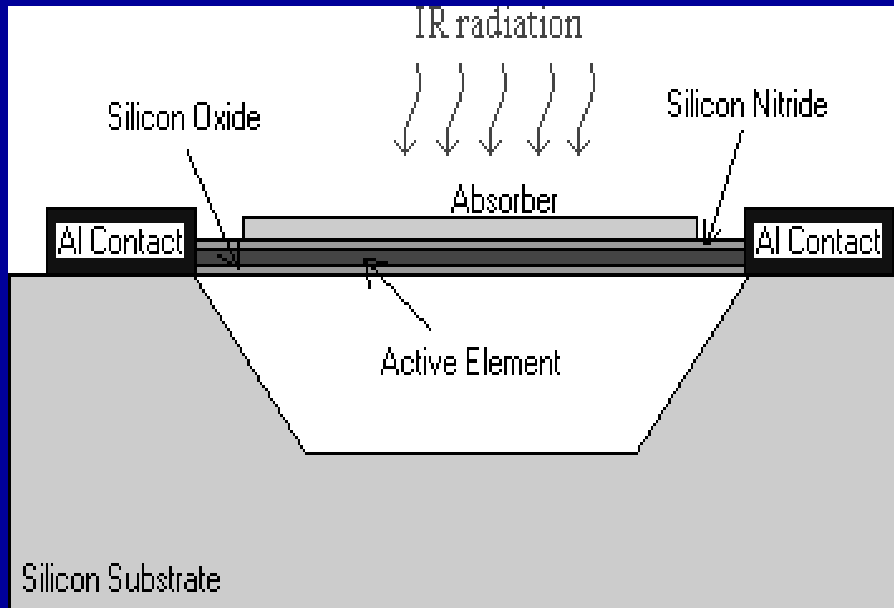
- Microheater : p type poly-si;
- $0.5 \times 20 \times 200 \mu\text{m}$;
- Gas flux w/ controlled temperature
- Circuits: interface and conditioning.



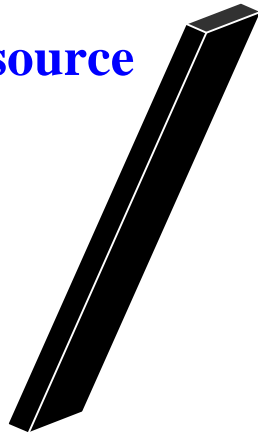
For $T = 27 \text{ }^\circ\text{C}$:

- $R = 401,92 \text{ } \Omega$
- $\text{TCR} = 1.50 \text{ ppm}/^\circ\text{C}$

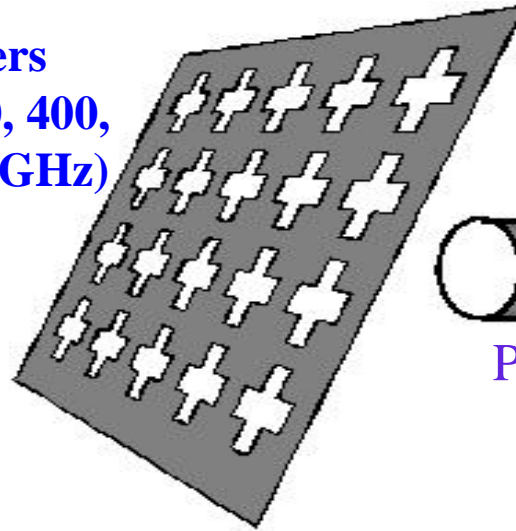
B.3 Bolometer sensor



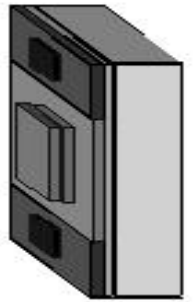
Cold source



Filters
(200, 400,
800 GHz)



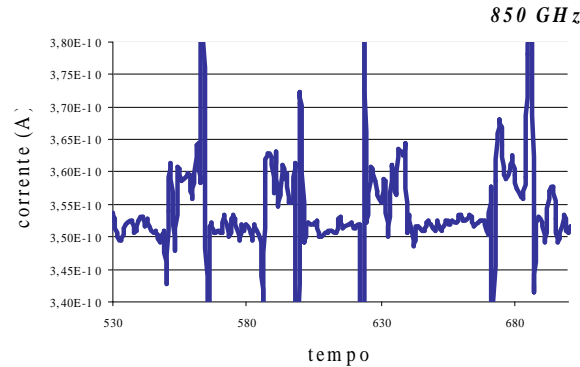
Photon collector



Bolometer

absorber for mm-wave

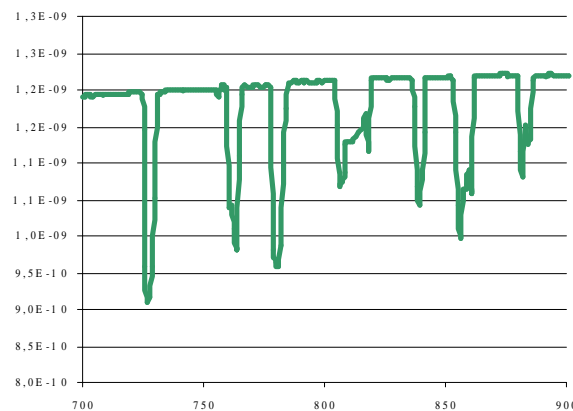
Measurements
with LN



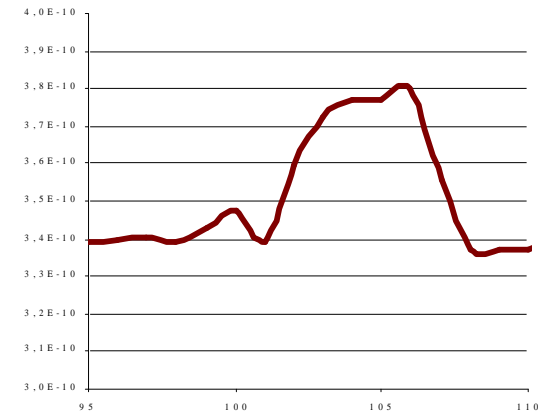
Fast Response

- high and fast responsivity in the desired range of sub-mm IR wavelengths.

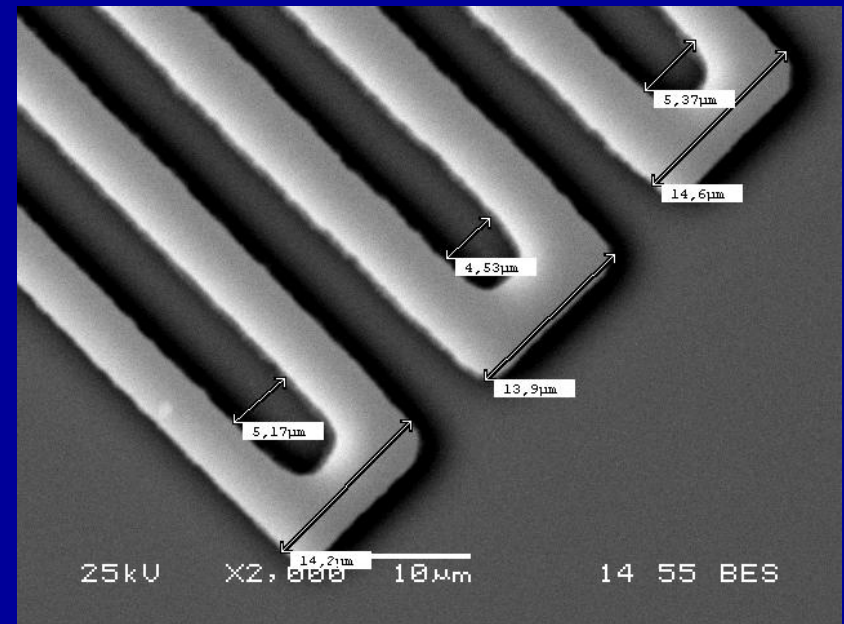
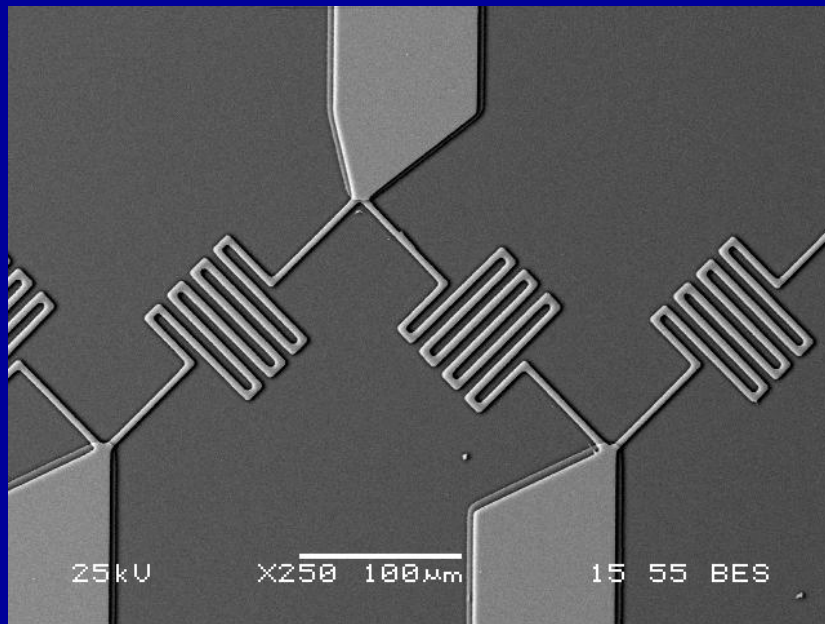
To human
heat



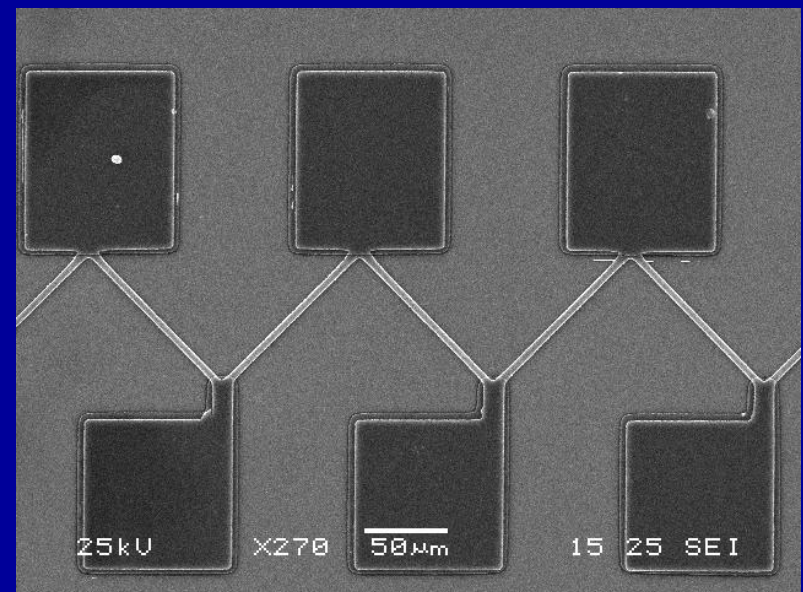
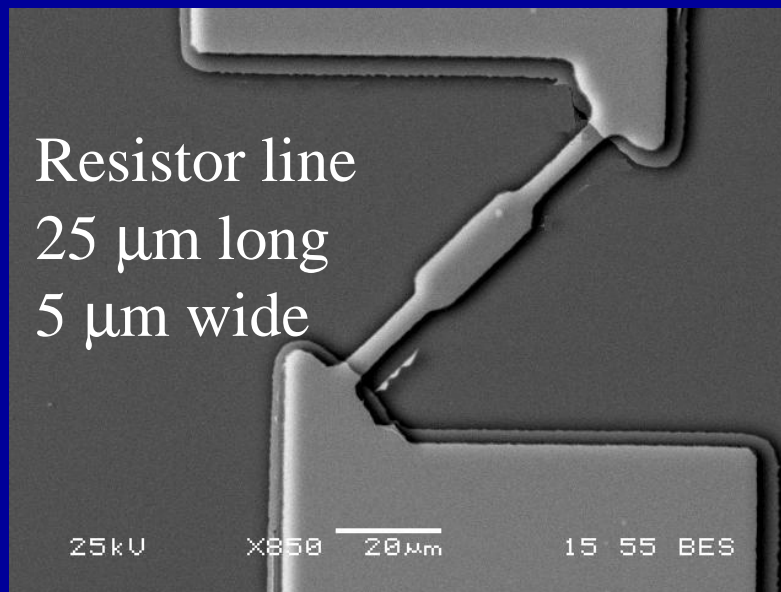
To heated
source
(~300°C)



New structures, different shapes, in progress:

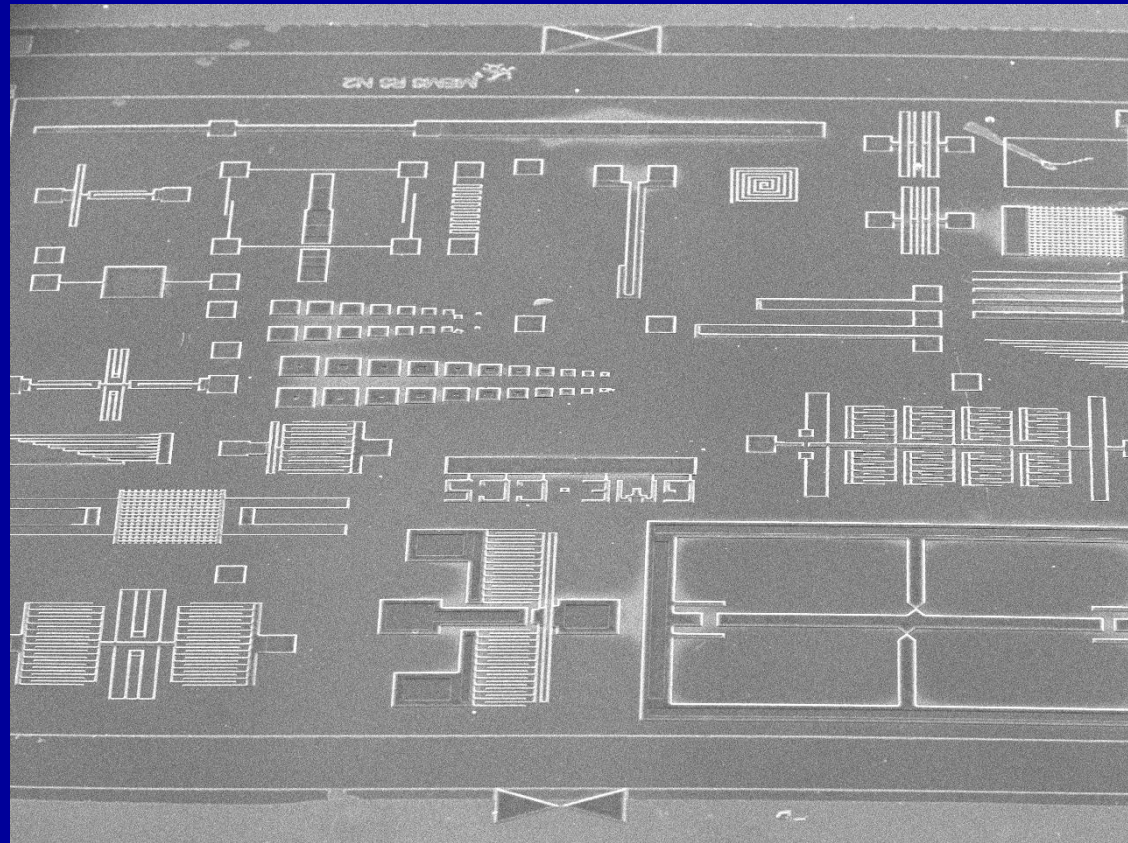


Array of sensors – poly-Si resistor lines of 5 µm wide



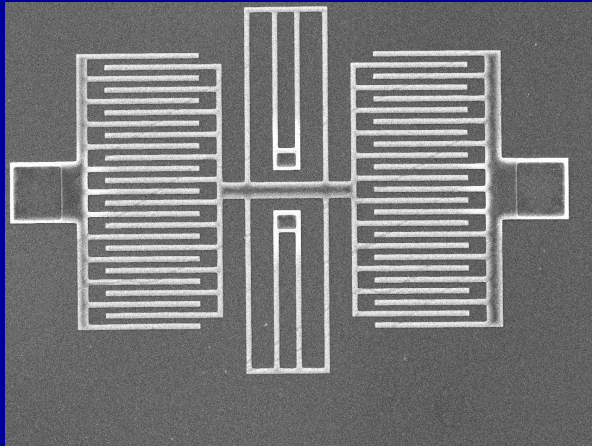
B.4 Surface micromachine structures: comb drive and others

- Fabrication in progress:
- Structures/Devices:
 - ▶ Structure for stress measurements
 - ▶ Comb drive with resonant device
 - ▶ Switches
 - ▶ Cantilevers
 - ▶ Inductor
 - ▶ Structures for process characterization



- **Fabrication Details**

- **Micromechanical resonator**



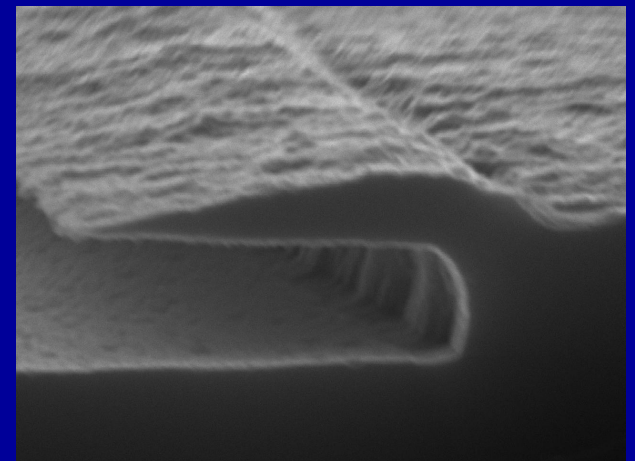
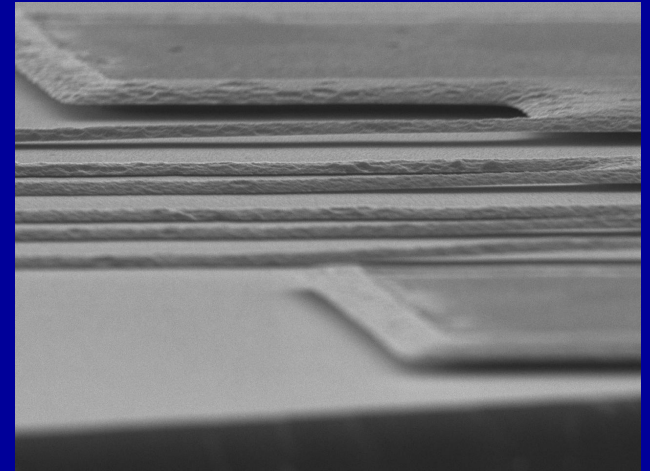
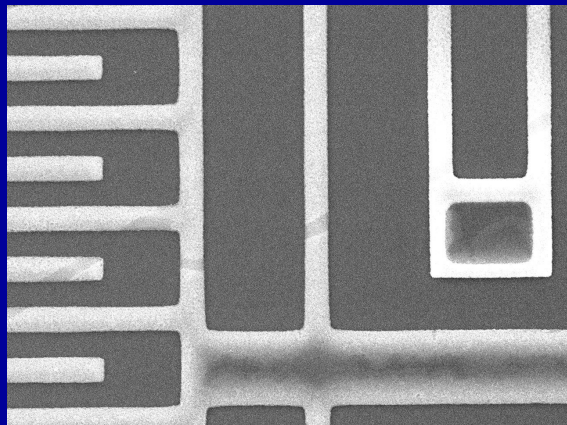
MEMS level

3

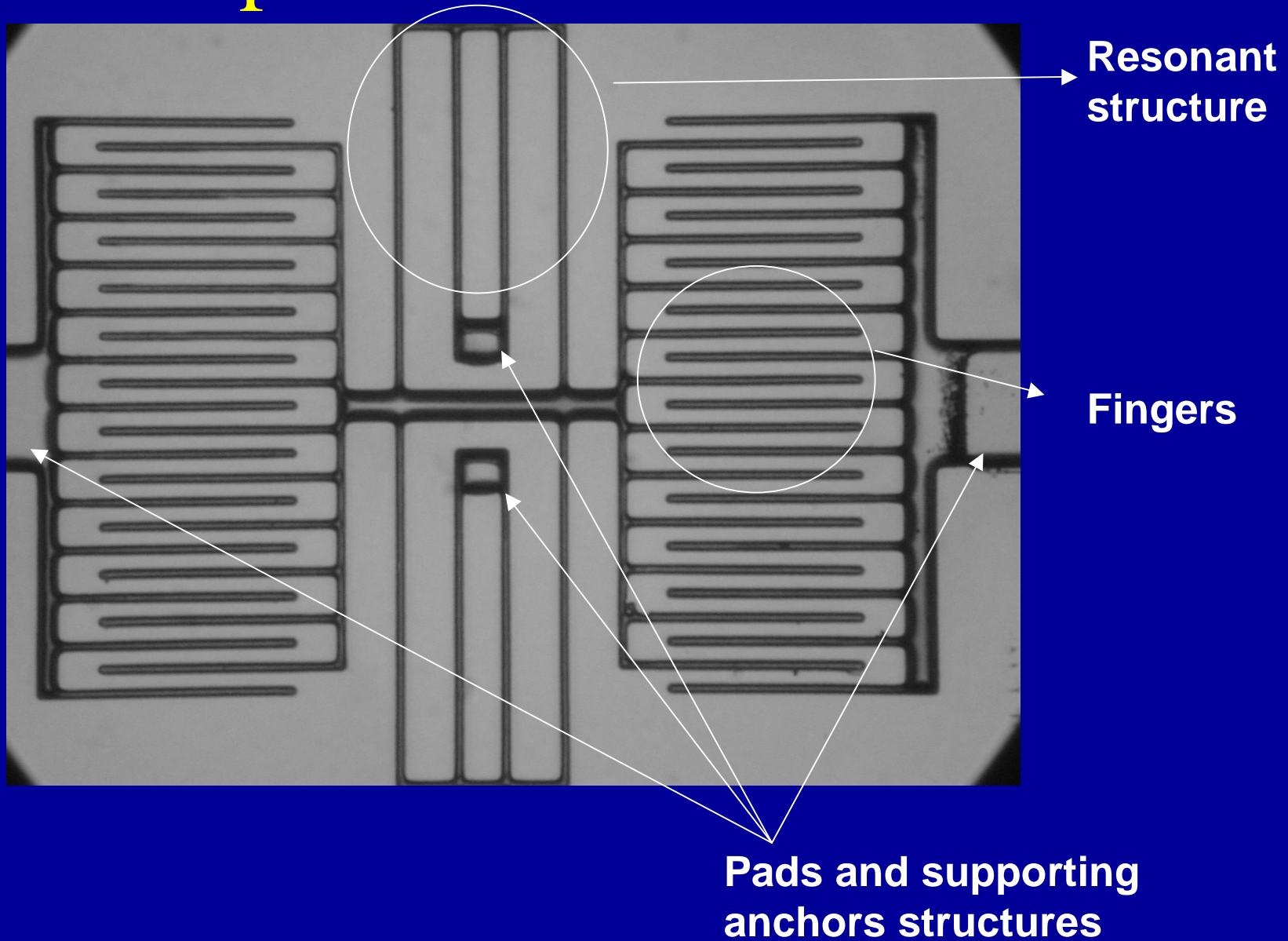
Poly1

onto

mono-Si



- Complete comb-drive structure



Thesis and Dissertations, 1999 - 2004

Year	Master Sc.	PhD.
1999	2	4
2000	2	-
2001	3	2
2002	4	1
2003	6	2
2004	3	-
Total	20	9

Publications, 1998 - 2004

International Journal	34
National Journals	07
International Conferences – Full paper	31
International Conferences - Abstracts	20
National Conferences – Full paper	85
National Conferences – Abstracts	25

<http://www.ccs.unicamp.br>

4. Considerações Finais

Problema: diferentes culturas

- A) Cultura dos especialistas em micro- e nano-fabricação ⇒ **Conhecimento limitado em aplicações em outras áreas.**
- B) Cultura de possíveis usuários, especialistas em biologia, medicina, agricultura, química, outros ⇒ **Conhecimento limitado em tecnologias de micro- e nano-fabricação.**
- ⇒ Existe uma enorme demanda latente ⇒
Necessitamos despertá-la ⇒ eliminar limites entre áreas, enfatizar formação básica e mais ampla.

Some historical curiosities:

- Who was the first to fly?
 - Brothers Wright? No!
 - Santos Dumont (Brazilian, demonstration in Paris)
- Today Brazil is an important player in small and medium aircraft manufacturing - Embraer.

- Who invented wireless telegraph and radio?
 - Marconi? No!
 - Pe. Roberto Landell de Moura (Brazil)

- Pe. Roberto Landell de Moura:

- Lab. in Campinas, SP, 1892 - 1900
- Demonstration of wireless communication – 8 km, 1894.
- 3 patents in USA – filed in 1901, approved 1904.

- Marconi:

- Basic experiments – 1895
- 1st radiogram – 1900.

- Up to now: no large electronics company in Brazil
- Future ????
- Time to do something!

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- Prof. Ioshiaki Doi
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- Dr. André Máscia Daltrini
- Dr. Artem Kostryukov
- Dr. Carla Veríssimo
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- Dr. Marcelo Hayashi
- M.Sc. Ricardo Cotrin
- M.Sc. Adeilton Cavalcanti
- M.Sc. Roberto Neli
- M.Sc. Aline
- M.Sc. Alexandre Gorni
- M.Sc. Gleison Manera
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