On the Design of Very Small Transconductance OTAs with Reduced Input Offset

Alfredo Arnaud
DIE Universidad Católica
8 de Octubre 2738
Montevideo - Uruguay
+598-2 4872717- ext.407
email: aarnaud@ucu.edu.uy

Rafaella Fiorelli
GME-IIE Univ.de la República
Julio Herrera y Reissig 565/IIE
Montevideo - Uruguay
+598-2 7110974 - ext.123
email: fiorelli@fing.edu.uy

Carlos Galup-Montoro
LCI-EEL Univ.Fed. de Santa Catarina
88040-900 Florianópolis - SC
Brazil
+55 48 331 9280
email: carlos@eel.ufsc.br

ABSTRACT

In this paper it will be demonstrated, from the theory and measurements, that series-parallel (SP) mirrors allow building current copiers with copy factors of thousands, without degrading mismatch or noise performance. SP current-division will be then employed to design OTAs ranging from a few pS to a few nS, with up to 1V linear range, consuming in the order of 100nW, and with a reduced area. An integrated 3.3s time-constant integrator will also be presented. One-by-one several design non-idealities will be revised: linearity, offset, noise, leakages; as well as layout techniques. A final analysis concludes that SP-association of transistors allows to build very efficient transconductors, for demanding applications in the field of implantable electronics among others.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Style – *Input/output circuits, VLSI.*

General Terms: Design.

Keywords: Analog design, CMOS, low-power.

1. INTRODUCTION

In recent years there has been considerable research effort in the development of integrated transconductance amplifiers (OTAs), with very small transconductance and improved linear range due mainly to their application in biomedical circuits [1-6]. In a classical symmetrical OTA, voltage to current conversion is carried out in the input differential pair while the other transistors just copy the current to the output. Although bias current can be extremely low [7], thus obtaining an extremely low transconductance, a drawback in this case is the poor linearity as the input transistors operate in weak inversion. Several circuits were reported in the past to overcome the problem but the use of complex OTA architectures also increases noise, mismatch offset, and transistor area, and results in design trade-offs [1]. A rough classification of very low transconductance OTAs may include:

-Those circuits that modify the differential pair performing the voltage-to-current conversion in such a way to reduce the transconductance and increase its linear range (i.e.[4,8]).

-Those circuits that use current cancellation [5], or current division [9,10] to divide the OTA transconductance by a desired factor; but do not increase the input linear range.

-Circuits using voltage division techniques for the extension of the linear range [2,6].

Of course, techniques can be combined. Regarding their limitations: modified-differential pairs increase offset, noise, and are limited to a few nS in their transconductance; a further transconductance reduction requires the use of some kind of division scheme. Current cancellation and voltage division also show in general a large input offset and noise. Meanwhile, simple division of the output current of a differential pair by a high ratio has been widely considered an expensive technique in terms of area [2]. However, the use of series–parallel division of current in an OTA as in Fig.1 [9,10], allows the implementation of an area efficient current divider. In this paper we will examine in detail this circuit and SP current dividers in general. For the NMOS current mirrors in Fig.1, N unitary transistors M_u are placed in-series and in-parallel to achieve an effective output transconductance G_m,

$$G_m = g_{m1} / N^2 \tag{1}$$

g_{m1} is the transconductance of the transistors M_1. To enhance linearity, a modified differential input pair can substitute M_1 in Fig.1, as shown in Fig.2 [8]. The effective transconductance g_{m_eff} of the pair in Fig.2 is calculated by small signal analysis, assuming that transistors M_4 operate in the linear region, each behaving as a resistor of value $2R$. Therefore:

$$g_{m\_eff} = \frac{g_{m1}}{1 + n g_{m1} R} \tag{2}$$

n is the slope factor [11], slightly greater than unity and weakly dependent on the gate voltage. The non-unitary current copiers of Fig.1 are not only area-efficient (their area is proportional to the square root of the copy factor), but are also mismatch-efficient, because they benefit from the improved matching of a large number of equal unitary transistors. With the appropriate placement, the designer can apply the most usual matching rules: common centroid geometry, and same surroundings; while using copy factors as large as thousands if for example N=50 or N=100 are selected. To preserve mismatch benefits while using moderate copy factors, the generic current mirror in Fig.3 can be used.

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SBCCI'05, September 4–7, 2004, Florianópolis, Brazil.

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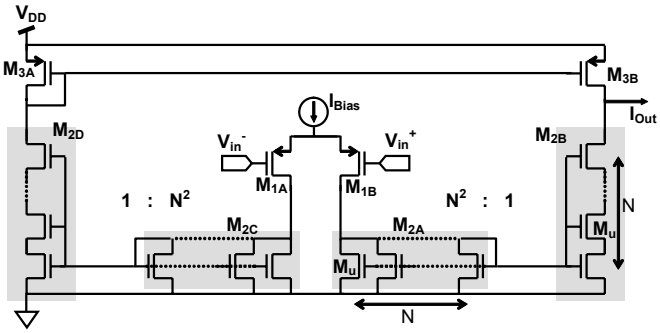

Figure 1: PMOS-input symmetrical OTA with series-parallel current division to reduce transconductance without loss in linear range.

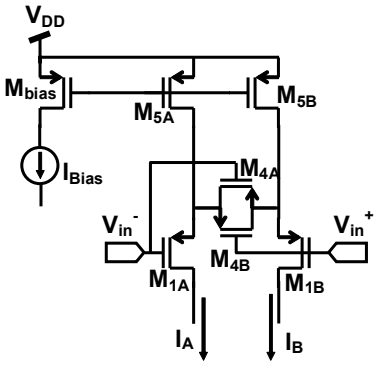

Figure 2: Active linearization of a differential pair to enhance linearity; $I_A - I_B = g_{m\_eff}\left(V_{in}^{+} - V_{in}^{-}\right)$.

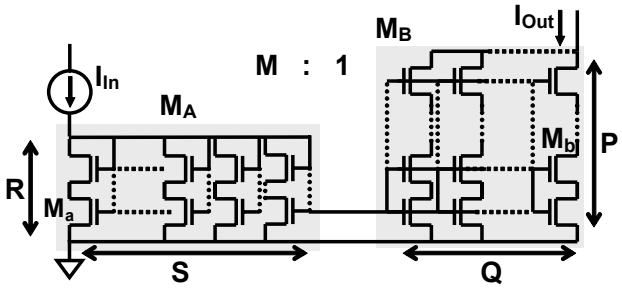

Figure 3: Generic SP current mirror. Unitary transistors are indenticall $M_a \equiv M_b = M_u$.

2. SERIES-PARALLEL CURRENT DIVISION, MULTIPLICATION, AND MISMATCH.

It is widely recognized that the performance of most analog or even digital MOS circuits is limited by random mismatch between transistors. Matching can be modelled by the random variations in geometric, process, and/or device parameters. The approach most employed by designers is to consider only variations in the threshold voltage V_T, and the current factor $\beta = \mu C_{ox}^{'} W/L$ with a normal distribution and a standard deviation (SD) given by [12]:

$$\sigma_{V_T}^2 = \frac{A_{V_T}^2}{2WL}, \qquad \frac{\sigma_\beta^2}{\beta^2} = \frac{A_\beta^2}{2WL} \tag{3}$$

In (3) A_{VT}, A_β, are two technology parameters with typical values of A_{VT}=13-30mV.µm and A_β=2-4%.µm [12]. Series-parallel association of MOS transistors [13] is a useful circuit technique and can be utilized to obtain improved matching between devices. In Fig.4(a) two transistors $M_{S(D)}$, are series connected; the equivalent ratio $(W/L)_{eq}$ of the composite transistor is [13]:

$$\left(\frac{W}{L}\right)_{eq} = \frac{(W/L)_S.(W/L)_D}{(W/L)_S + (W/L)_D} \tag{4}$$

Eq.(4) may be extended to complex combinations of transistors to obtain different equivalent transistor geometries. For example, Fig.4(c) show measured drain current vs. drain voltage for two equivalent transistors: a single unitary sized $(W/L)_u$ =4µm/10µm, and a 10×10 array of the same transistor (Fig.4(b)). The two plots are similar, but note in the upper detail that the drain-source impedance r_{ds} is much higher in the case of the composite transistor. As a rule of thumb, the output conductance of a composite transistor will be inversely proportional to the equivalent channel length [13]. The copy factor *M* in a current mirror is calculated as the ratio between the aspect ratios of transistors, even if M_A,M_B are two arrays as in Fig.3. Using (4) in the mirror of Fig.3:

$$\frac{I_{in}}{I_{Out}} = \frac{S.P}{R.Q} = M \tag{5}$$

where *P*, *R*, *Q*, and *S* are the number of unitary transistors in series or in parallel. Classic current mirrors with a copy factor M>>1 -as in Fig.5(a)- are very sensitive to mismatch offset because at the output there is a single transistor M_B, with a reduced area that according to (3) presents high variations in the threshold voltage and current factor. The composed transistors of Fig.5(b) and Fig.5(c) can be used to implement a current mirror with also a copy factor $M=N^2$, but using the same number of unitary transistors at both input and output branches of the mirror. A better matching and a reduction in random offset are expected if usual layout matching rules are followed, because a large number of unitary transistors have been matched together. In this way, common centroid layout geometry is possible, even when matching transistors with a very different aspect ratio.

2.1 Mismatch calculation in a SP mirror

Even with a careful layout, fluctuations $\Delta\beta_{a(b)ij}$, $\Delta V_{Ta(b)ij}$, of each unitary transistor in Fig.3 produce an output current error term ΔI_{Out}; then $I_{Out} = (I_{in}/M) + \Delta I_{Out}$. The designer requires a formula to estimate the SD of I_{Out}. In Fig.7, a composed transistor M_X (with a transconductance g_{mX}) formed by a large number of series-stacked unit transistors M_{ui} is shown. ΔV_{Ti}, $\Delta\beta_i$ fluctuations on unitary transistors affect the drain current I_{Di} and node voltages of each M_u. For each one is possible to write:

$$\Delta I_{Di} = -g_{m_i}\Delta V_{Ti} + \frac{I_D}{\beta_i}\Delta\beta_i - g_{ms_i}\Delta V_{Si} + g_{md_i}\Delta V_{S(i-1)} \tag{6}$$

where $g_{m_i}, g_{ms_i}, g_{md_i}$ are gate, source, and drain transconductances of M_{ui}, respectively. (6) has been derived for a generic transistor but $\Delta I_{Di} = \Delta I_D$ is constant, because the transistors are series connected; also their channel charge densities at source and drain $Q_{ID_i}^{'} = Q_{IS_{(i-1)}}^{'}$. Thus $g_{ms_{(i-1)}} = g_{md_i}$ [11]. Summing (6) for all the *P* series transistors

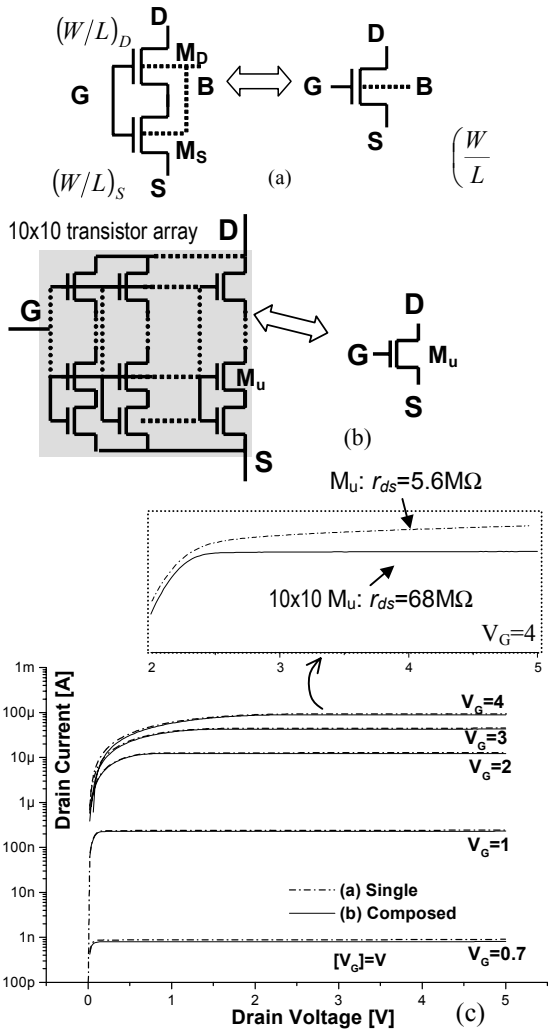

Figure 4: (a) Two series transistors and their equivalent transistor. (b) A single M_u transistor is equivalent to a 10×10 M_u array. (c) Measured I_D-V_D curves at different gate voltages V_G for single M_u sized $(W/L)_u$ =4µm/12µm, and a 10×10 M_u array. At the top, saturation region is magnified for V_G=4V to observe the change in r_{ds}.

and assuming as usual that $\Delta V_{Ti}, \Delta\beta_i$ are non-correlated, and $\sigma^2_{\beta_i}, \sigma^2_{V_T i}$ do not depend on -*i*- we obtain:

$$\sigma^2_{\Delta I_D} = \frac{I_D^2}{P}\cdot\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{\left(\sigma^2_{V_T}\right)_u}{P^2}\cdot\sum_{i=1}^{P} g^2_{m_i} \approx \frac{I_D^2}{P}\cdot\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mX}}{P}\left(\sigma^2_{V_T}\right)_u \tag{7}$$

If now a P×Q transistor array like the M_B of Fig.3 is introduced, fluctuations are calculated summing (7) for the parallel branches; $g_{mB} = Q.g_{mX}$ and drain current is also Q times larger:

$$\sigma^2_{I_D} = \frac{I_D^2}{PQ}\cdot\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{PQ}\left(\sigma^2_{V_T}\right)_u \tag{8}$$

Drain current is fixed in M_A of Fig.3, so eq.(8) should be better expressed in this case, as a fluctuation in its gate voltage V_G:

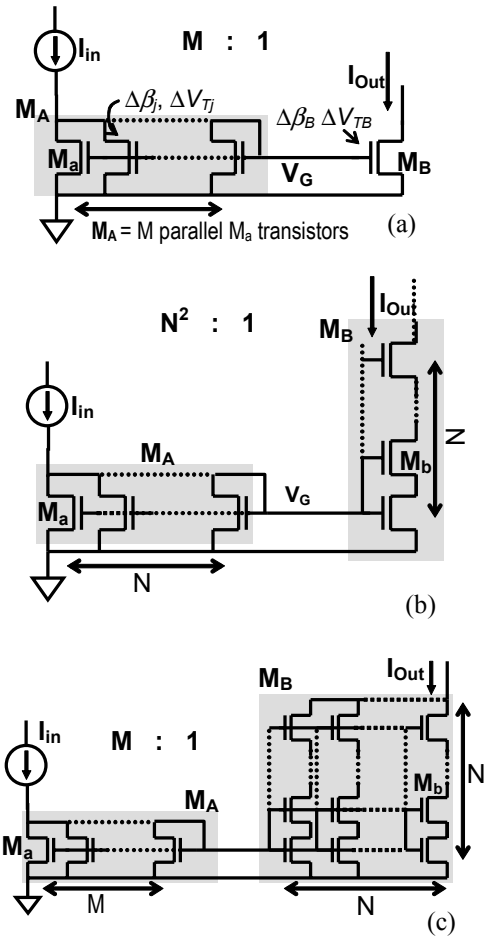

Figure 5: Three *M*:1 current copiers. (a) Classic. (b) $N = \sqrt{M}$ parallel transistors, copy to *N* series-stacked ones. (c) *M* parallel unitary transistors, copy to a $N \times N$ array.

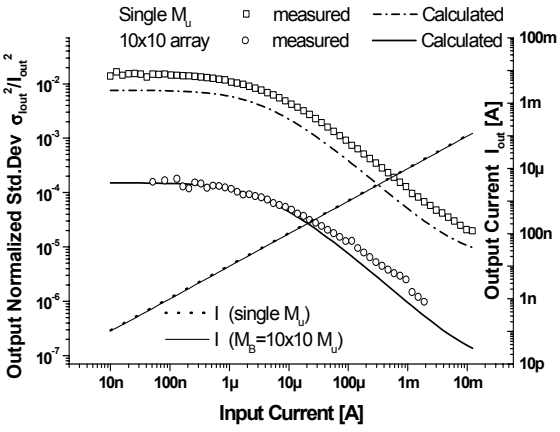

Figure 6: Calculated and measured I_{out}, $\sigma^2_{Iout}/I^2_{out}$ in terms of the input current are shown for a 100:1 NMOS current mirror with the topologies of Fig.5(a) (*M*=100) and Fig.5(c) (*M*=100, *N*=10). σ^2_{Iout} value was obtained from 10 samples of the circuit of the same batch.

$$\sigma^2_{V_G} = \frac{I^2_{in}}{g^2_{mA}.RS}.\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{1}{RS}\left(\sigma^2_{V_T}\right)_u \quad (9)$$

V_G fluctuation is propagated to the output through M_B. Also (8) is summed to calculate total I_{Out} SD in Fig.3 ($g_{mA'}/I_{in} = g_{mB'}/I_{out}$ because M_A,M_B have the same i_f [11]) :

$$\left(\frac{\sigma^2_{I_{Out}}}{I^2_{Out}}\right) = \left(\frac{1}{RS} + \frac{1}{PQ}\right).\left[\left(\frac{\sigma^2_\beta}{\beta^2}\right)_u + \frac{g^2_{mB}}{I^2_{Out}}.\left(\sigma^2_{V_T}\right)_u\right] \quad (10)$$

$\left(\sigma^2_\beta/\beta^2\right)_u$, $\left(\sigma^2_{V_T}\right)_u$, are the SD of the threshold voltage and the current factor for unitary transistors respectively. In Fig.5, three different topologies for a current mirror to perform a M:1 current copy are shown. For a 100:1 copy, the circuit in Fig.5(a) requires 101 unitary transistors, the one in Fig.5(b) only 20, and Fig.5(c) 200. Meanwhile, the SD (10) in output current fluctuation is $\left(\sigma^2_{Iout}/I^2_{Out}\right)_{(a)} \approx 5\left(\sigma^2_{Iout}/I^2_{Out}\right)_{(b)} \approx 50\left(\sigma^2_{Iout}/I^2_{Out}\right)_{(c)}$. In Fig.6 calculated and measured I_{out}, $\sigma^2_{Iout}/I^2_{out}$ in terms of the input current are shown for a 100:1 NMOS current mirror with the scheme of Fig.5(a) and Fig.5(c) (N=10). σ^2_{Iout} value was obtained from 10 samples of the circuit in a 0.8μm technology. $(W/L)_u$=4μm/12μm, and A_{VT}=.03Vμm, A_β=.02μm values, were used for theoretical offset calculation with (3),(10). Note that $\sigma^2_{Iout}/I^2_{Out}$ has been substantially reduced in SP mirrors.

3. DESIGN OF SP VERY LOW TRANSCONDUCTORS

Some other circuit properties should be studied. Linearity can be calculated in terms of the inversion level i_{f1} [11] of the input differential pair (Fig.1). The expression is $V_{Lin} \approx 3n\phi_t\sqrt{\alpha(1+i_f)}$ where V_{Lin} is the input linear range [10]. Linearity is further extended in the topology in Fig.2 [8].

3.1 Offset in the OTA

The input pair M_1, PMOS current mirror transistors M_3, and SP current dividers, contribute to offset in the OTA of Fig.1. Summing their input referred contribution:

$$\sigma^2_{V_{off}} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{I^2_{D1}}{g^2_{m1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1\right] + \frac{4I^2_{D1}}{N.g^2_{m1}}\left[\frac{g^2_{m2B}}{I^2_{D2B}}\left(\sigma^2_{V_T}\right)_u + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u\right] +$$
$$+ \frac{2I^2_{D1}}{g^2_{m1}}\left[\frac{g^2_{m3}}{I^2_{D3}}\left(\sigma^2_{V_T}\right)_3 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_3\right] \quad (11)$$

In Fig.2, transistors M_4 do not introduce offset. But an extra offset is introduced by M_5 while the effect of fluctuations in $M_{1A(B)}$ is slightly different. With a small signal analysis

$$\sigma^2_{V_{in}} = 2\left[\left(\sigma^2_{V_T}\right)_1 + \frac{I^2_{D1}}{g^2_{m1}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_1\right] + \frac{4I^2_{D1}}{N.g^2_{m\_eff}}\left[\frac{g^2_{m2B}}{I^2_{D2B}}\left(\sigma^2_{V_T}\right)_u + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_u\right] +$$
$$2\frac{I^2_{D1}}{g^2_{m\_eff}}\left[\frac{g^2_{m3}}{I^2_{D3}}\left(\sigma^2_{V_T}\right)_3 + \left(\frac{\sigma^2_\beta}{\beta^2}\right)_3\right] + 2\left[\frac{g^2_{m5}}{g^2_{m\_eff}}\left(\sigma^2_{V_T}\right)_5 + \frac{I^2_{D5}}{g^2_{m\_eff}}\left(\frac{\sigma^2_\beta}{\beta^2}\right)_5\right] \quad (12)$$

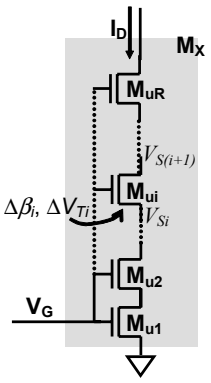

Figure 7: *P* series-stacked unitary transistors.

Expressions (11,12), can be extended to generic SP current division of Fig.3 changing N by $\sqrt{PQ/RS}$.

3.2 Noise Analysis

SP mirror noise is calculated in Fig.3, with the aid of consistent thermal and flicker noise models[14]:

$$\frac{S_{I_{Out}th}}{I^2_{Out}} \approx 2nk_BT\left(\frac{g_{mB}}{I_{Out}}\right)\left(\frac{1}{I_{in}} + \frac{1}{I_{out}}\right)$$
$$\frac{S_{I_{Out}\frac{1}{f}}}{I^2_{Out}} = \frac{q^2N_{otN}}{nC'^2_{OX}(WL)_u}\left(\frac{1}{RS} + \frac{1}{PQ}\right).\frac{g^2_{mB}}{I^2_{out}}.\frac{1}{f} \quad (13)$$

$S_{I_{Out}th}, S_{I_{Out}\frac{1}{f}}$, are thermal and flicker noise PSD, k_B is the Boltzman's constant, T is the absolute temperature, $N_{otN(P)}$ are technology parameters for the flicker noise, q is the electron charge. Note that the output noise (like offset) do not significantly increase when using large SP current dividers. The input referred noise can be calculated for the OTA in Fig.1 (M>>1) using (13). Thermal - $v^2_{input\_th}$ -, and flicker - $v^2_{input\frac{1}{f}}$ - noise are:

$$v^2_{input\_th}(f) \approx \frac{4nk_BT}{G_m}\eta \quad (14)$$

$$v^2_{input\_f}(f) \approx \frac{2nk_BT}{N^*C'_{ox}}\left[\frac{N_{otP}}{(WL)_1} + \eta^2\left(\frac{2N_{otN}}{N(WL)_u} + \frac{N_{otP}}{(WL)_3}\right)\right].\frac{1}{f}$$

The factor $\eta = \left(\sqrt{1+i_{f1}} + 1\right)$, and $(WL)_{1(u)(3)}$, are the gate area of M_1, M_u, and M_3, respectively. Expressions (14) are very similar to that obtained for a simple symmetrical OTA, but a price is paid in noise for the linearization represented by the factor η.

3.3 What is the minimum effective G_m possible with this technique?

M_2, M_3 in Fig.1 may be biased with few pA or less; the only limitation being the sum of the leakage current at the source (drain) of each series transistor in $M_{2B(D)}$. In the target technology leakages in p-doped diffusions are much higher than those in an n-doped ones. For this reason, the presented OTAs include a PMOS differential pair, and NMOS SP current mirrors. From manufacturer's data, estimated leakage current in a single source(drain) was I_{leak}=3fA for a 4μm x 2μm n+ diffusion. The selected design criterion is that the leakages should be at least 10 times smaller than the bias current in the output branch:

$\sum I_{leak} = N.I_{leak} < I_{D1}/10N^2$, which imposes a limit on the minimum achievable transconductance. A minimum 15pS OTA was estimated for N=100, and $(g_m/I_D)_1$ = 5 at the input pair, that is -although reasonable- an arbitrary worst case condition.

4. DESIGNED OTAs.

Several low, and very low transconductance OTAs named G_{m1} to G_{m4} were fabricated for test purpose. The design methodology is the one proposed in [10] while non idealities -noise, offset- are addressed using (11) to (14). G_{m1} is a 35pS OTA. It uses a g_{m1}=170nS differential input pair in the configuration of Fig.1, with a N^2=4900 division factor. G_{m2}=2.35nS OTA uses the differential pair of G_{m1} with a 9:1 division factor obtained with the topology of Fig.3 with P=8, Q=2, R=1, S=18. G_{m3}, G_{m4} are both 500mV linear range OTAs with a transconductance of 2.5nS, and 90pS respectively. The differential pair in Fig.2 with g_{m_eff} =69nS is employed with 28:1, and 784:1 division factors. In G_{m3}, P,Q,R,S = 28,1,5,5 and G_{m4} employs 28 parallel transistors copying to 28 series ones in the current divider. A careful layout plays a central role in obtaining a reduced mismatch. In all cases SP mirrors, as well as $M_{1,3,4,5}$ are built with a large row of unitary transistors interconnected according to the desired topology. Unitary transistors of each composed one are alternated, and usual dummy structures at the row ends and same surroundings rules are respected. It should be pointed that SP OTAS allow a very efficient reutilization of layout blocks. In effect, widely different current mirrors and differential pairs are obtained just by changing SP connections at metal layer as indicated in Table I.

4.1 Measurement results.

Several measured characteristics of G_{m1} to G_{m4} are summarized in Table 2, while in Fig.8 the measured transfer functions of G_{m3},and G_{m4} are shown. It should be highlighted the reduced input offset of the OTAs, obtained with a moderate area and nano-power consumption. Ten circuit samples from the same batch were used to calculate σ_{Voff} in Table 2. Noise figures correspond to the input referred rms voltage integrated in the band from .3 to 10Hz where OTAs are intended to operate. A 3.3s time constant integrator, using G_{m4} and a 50pF capacitor has also been fabricated. The integrator occupies a 0.2mm^2 area. The plot in Fig.9(a) shows the frequency response of a low pass filter based in the integrator. The measured 3dB frequency was 0.3 Hz. The plot of Fig.9(b) shows the measured transient response of the circuit to a large $1V_{pp}$ square wave at the input of 0.3Hz frequency.

5. A COMPARATIVE SURVEY

As pointed in the introduction, several very low transconductors and large time constant G_m-C filters have been reported. In [4], Sharpeskar et al. combine at the input gate degeneration, bulk driven transistors, and the so called bump transistor technique, to achieve a transconductor of 10nS with a linear range of ±1.7V, around 20mV input offset and 1μW power consumption. In [1] several 10nS, sub-μW OTAs, using different input pair linearization techniques are compared; unfortunately no offset measurements are presented. These OTAs require the addition of some kind of division technique –like the one here presented- to achieve few Hz or sub-Hz range G_m-C filters. Techniques may include voltage attenuation [2,6], capacitor scaling[15], or

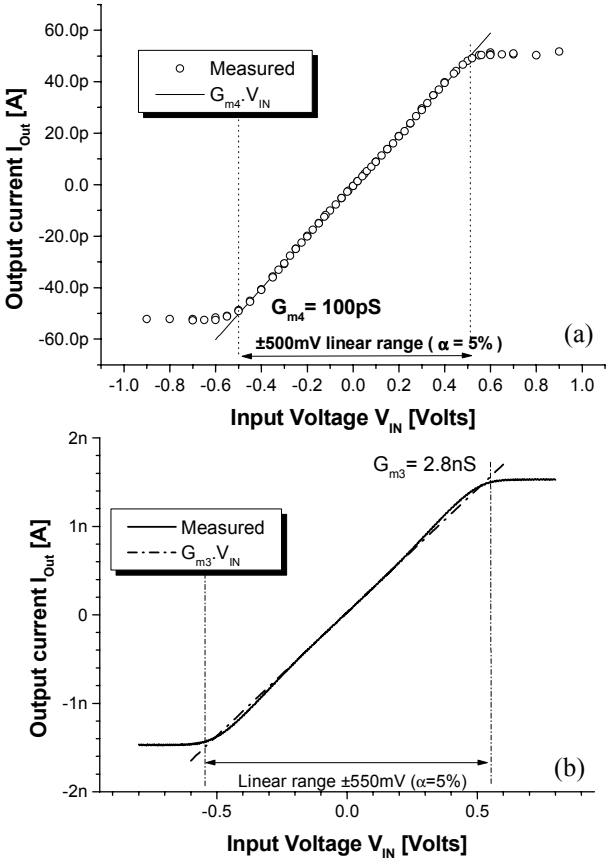

Figure 8: Measured transference of (a) G_{m4} (b) G_{m3}.

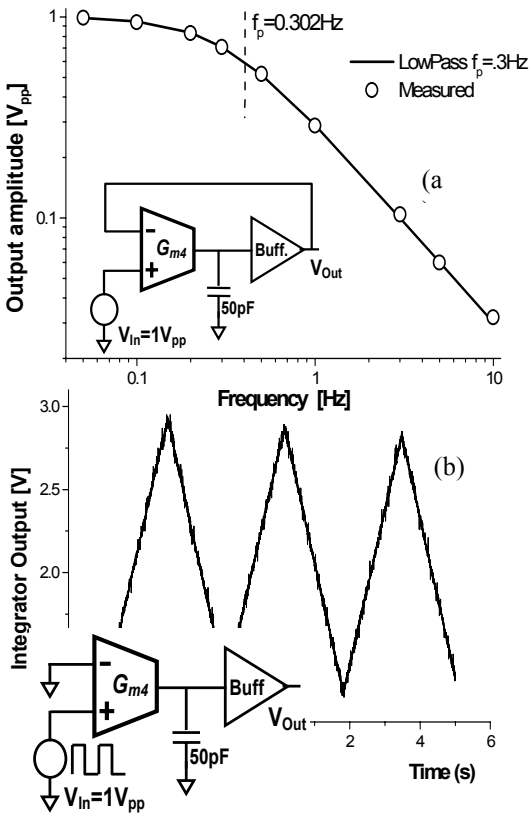

Figure 9: Measured (a) frequency response (b) transient response of the integrator.

current division/cancellation [3,10]. Table 3 puts together some previously reported large time constant integrators and filters. Although the comparative study is difficult because linearity, noise, and particularly offset, are not always measured in the same way, it is possible to conclude that the technique here presented is very efficient regarding mismatch, power consumption, and noise, without a significant overhead in silicon area.

6. CONCLUSIONS

A general expression was introduced, to estimate mismatch offset in series-parallel current mirrors. Extremely large current multiplication (division) factors can be obtained by means of SP mirrors, without a significant loss in terms of area, offset, or noise. Series-parallel division of current in symmetrical OTAs was applied to achieve very low transconductances with extended linear range. Sample OTAs and 3.3s G_m-C integrator were designed, fabricated, and tested. The designed circuits present a very good trade-off in terms of occupied area, consumption, linearity, noise, and input offset.

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Table 1: Several design characteristics of fabricated SP OTAs: input pair transconductance,division factor, unitary transistor size at the divider, area, and power consumption.

OTA	G_{m_pair} [nS]	M (P-Q-R-S)	W_u/L_u [μm/μm]	Area [mm^2]	Power [nW]
G_{m1}	174	72 (2-8-1-18)	4/4	0.04	116
G_{m2}	174	4900 (70-1-1-70)	4/8	0.09	113
G_{m3}	69	28 (5-5-1-28)	4/12	0.15	118
G_{m4}	69	784 (28-1-1-28)	4/12	0.15	113

Table 2: Several characteristics of OTAs: transconductance predicted-measured, measured linearity, predicted-measured input offset SD, maximum measured offset (10 samples), predicted–measured input noise in the band from .3 – 10Hz.

OTA	Transc.	$V_{Lin.}$[mV]	Off.[mV]	$Off._{max}$ [mV]	Noise [μV_{rms}]
G_{m1}	2.4-2.6 nS	±160	8.0 – 4.4	8.3	48 – 89
G_{m2}	35-33pS	±160	5.4 – 2.1	4.0	193 –160
G_{m3}	2.4–2.8 nS	±550	8.8 – 9.1	21	56 – 108
G_{m4}	89–100pS	±500	9.0 – 6.8	12	190 – na

Table 3: A comparative table of several reported division schemes used in OTAs, and large time constant G_m-C filters.

Technique	Ref.	Division Factor & Time const.	Offset	Comments
SP Current Division	This work	70 to 4900 3.3s	2-9mV (SD)	Low noise, good linearity, nW power.
Voltage Division	[2]	Up to 10000 10s	Very large.	Poor linearity, small silicon area, nW power.
SP Current Division	[3]	2200 0.7s	130mV	Large offset probably due to non-symmetrical SP copy.
Capacitive Scaling & Others.	[15]	1.2s	~20mV	4^{th} order, .1-5Hz tunnable band-pass filter. ~25μW power.
Current Div./Canc.	[5]	1000 100ms	40mV*	Uses 10pF capacitors. *random offset + 80mV systematic.