Characterization of MOS Transistor Current Mismatch

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ABSTRACT
Electron device matching has been a key factor on the performance of today's analog or even digital electronic circuits. This paper presents a study of drain current matching in MOS transistors. CMOS test structures were designed and fabricated as a way to develop an extensive experimental work, where current mismatch was measured under a wide range of bias conditions. A model for MOS transistor mismatch was also developed, using the carrier number fluctuation theory to account for the effects of local doping fluctuations. This model shows a good fitting with measurements over a wide range of operation conditions, from weak to strong inversion, from linear to saturation region, and allows the assessment of mismatch from process and geometric parameters.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design Aids – *simulation.*

General Terms
Measurement, Performance, Design, Experimentation.

Keywords
MOSFET, analog design, matching, mismatch, compact models.

1. INTRODUCTION
Integrated circuit design is fundamentally based on the concept of behavior similarity of identically designed electronic devices, thus the capability of fabricating matched devices is a factor of strong impact in the performance of analog or even digital circuits [1]-[3]. Progressive shirinkage of MOSFET dimensions and reduction of supply voltage increase this impact to such an extent that several new studies about MOS transistor mismatch have been published in recent years [4], [5]. Although some fundamental aspects of mismatch are known, the complete process is too complex, being not yet well understood. Matching devices was treated for years as an empirical art, lacking of a systematic analysis and modeling.

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Nowadays, although a great progress have been done in mismatch understanding, existing models preserve some historical limitations from the past, being restricted to some operation region or based on unadequate parameters.

Mismatch is the time-independent variation of device parameters observed between two or more identically designed devices. It occurs because every phase necessary to fabricate integrated circuits present several uncontrolable variations, related to the discrete nature of matter, temperature fluctuation, mechanical stress, etc. Mismatch is generally classified as presenting a *global* and a *local* aspect. *Global* aspect is the result of process gradients, i. e., quantities that change progressively across the waffer or through the batch. They are caused by equipament variations and spatial drifts, e. g., photo-mask distortion, lens aberration, photo-resist thickness variation, mechanical strain and oxide thickness variation. *Global* variations produce systematic mismatch for a identically designed group of devices. Thus, it can be minimized by the use of some design "tricks", like the common-centroid technique, placement of "matched" devices as close as possible, keeping the same current orientation, etc. *Local* aspect of mismatch is related to variations that occur in short-distance range when compared to device dimensions, being related to the discrete nature of matter. Some causes are dopant difusion and clustering, interface states and fixed charges, edge roughness and poly-Silicon grain effects. *Local* variations produce random mismatch that depends on the process parameters, device dimensions and bias. It must be well-understood by designers as a way to deal with the limitations imposed to the design.

2. MISMATCH MODELING
Existing mismatch models use either simple drain current models limited to a specific operating region [1], [2], [5], or too complex expressions [4] like that of BSIM. In general, however, it is widely accepted that matching can be modeled by the random variations in geometric, process and/or device parameters, and the effect of these parameters on the drain current can be quantified using the dc model of the transistor. As pointed out in [5] and [6], there is a fundamental flaw in the current use of dc models for mismatch analysis that results in inconsistent formulas. Mismatch models implicitly assume that the actual values of the lumped model parameters can be obtained by integration of the position-dependent distributed parameters over the area of the channel region of the device. As analyzed in [5], the application of this concept to series or parallel association of transistors leads to an inconsistent result owing to the nonlinear nature of MOSFETs. Consequently, the simple use of fluctuations in the lumped parameters of the dc model (V_T, β etc) is not appropriate to

develop matching models and new formulas must be derived from basic principles.

A better approach for matching modeling can be attained when mismatch causes are computed across the MOSFET gradual channel, rather than through lumped parameters. In this way the MOS transistor is splitted into 3 series elements (an upper transistor, a lower transistor, and a small channel element of length Δx and area $\Delta A = W\Delta x$, where W is the channel width). Small-signal analysis allows one to calculate the effect of the local current fluctuation of the small channel element ($i_{\Delta A}$) on the total drain current deviation (ΔI_d) [7], [8]. Since local current fluctuations along the channel are uncorrelated, the square of the total drain current fluctuation is given by

$$\overline{\Delta I_D{}^2} = \sum(\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left(\frac{\Delta x}{L} i_{\Delta A} \right)^2 = \frac{1}{L^2} \int_0^L \Delta x \left(i_{\Delta A} \right)^2 dx \qquad (1)$$

where L is the channel lenght and x is the distance from the channel element to the source.

To obtain general results for all bias regions of the transistor we have used the Advanced Compact MOSFET (ACM) model, a physics-based one-equation all-regions model [9], [10]. With the help of ACM model, it is easy to relate the local current fluctuation ($i_{\Delta A}$) to the inversion charge density fluctuation ($\Delta Q'_I$) along the channel, and it to the fluctuation in the concentration of ionized impurities ($\Delta Q'_{IMP}$) under the gate, as a result of charge conservation. Integrating (1) from drain to source, a compact expression for current mismatch can be derived [7], [8]

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{q^2 N_{oi} \mu}{L^2 n C'_{ox} I_D} \ln \left(\frac{n C'_{ox} \phi_t - Q'_{IS}}{n C'_{ox} \phi_t - Q'_{ID}} \right) \qquad (2)$$

where q is the electron charge, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, μ is the effective mobility, ϕ_t is the thermal voltage, Q'_{IS} and Q'_{ID} are the inversion charge densities in the source and drain ends of the channel, respectively, and N_{oi} represents the average number of impurities per unit area, in the depletion region, which is the only additional parameter needed for our mismatch model.

In the ACM model [9], [10], the drain current (I_D) is expressed as the difference between the forward (I_F) and reverse (I_R) components, $I_D = I_F - I_R = I_S (i_f - i_r)$, where $I_S = \frac{1}{2}\mu C'_{ox} n \phi_t^2 (W/L)$ is the specific current and i_f and i_r are the forward and reverse inversion levels. Using the relationship between inversion charge density and current ($-Q'_{IS(D)} / nC'_{ox}\phi_t = \sqrt{1 + i_{f(r)}} - 1$) [9], [10], expression (2) can be rewritten as

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{i_f - i_r} \ln \left(\frac{1 + i_f}{1 + i_r} \right) \qquad (3)$$

where $N^* = -Q'_{IP} / q = nC'_{ox} / q$ as in [10], being Q'_{IP} the channel charge density at pinch-off.

Expression (3) can be simplified under specific conditions as shown in Table 1. A complete description of this mismatch model can be found in [7] and [8].

Table 1. Expression (3) simplified under specific conditions.

$\sigma^2_{I_D} / I_D^2$	weak inversion ($i_f << 1$)	strong inversion ($i_f >> 1$)
linear ($i_f \cong i_r$)	$\frac{N_{oi}}{WLN^{*2}}$	$\frac{N_{oi}}{WLN^{*2}} \frac{1}{1 + i_f}$
saturation ($i_r \to 0$)		$\frac{N_{oi}}{WLN^{*2}} \frac{\ln(1 + i_f)}{i_f}$

3. TEST CIRCUIT

A mismatch test circuit was designed and fabricated in the TSMC 0.35µm 3.3V CMOS n-well process, through the MOSIS Education Program (MEP). It is composed of a set of NMOS and PMOS transistors disposed in arrays of 20 identical functional devices, surrounded by dummy ones to ensure uniform boudary conditions for all active transistors, improving matching properties. Transistor dimensions (WxL) of each array are 12µm x 8µm (*large*), 3µm x 2µm (*medium*), 0.75µm x 8µm (*narrow* - minimum width), 12µm x 0.5µm (*short* - minimum length) and 0.75µm x 0.5µm (*small* - minimum size), and they are disposed side by side in rows. Wide metal conections and multiple contact windows were designed to lower ohmic drops [11]. Devices of each array have identical design and current orientation. Figure 1 shows a schematic diagram of two arrays (being the lower NMOS and the upper PMOS) of our test circuit. Five pairs of arrays composed by 20 NMOS and 20 PMOS transistors having the same dimensions are connected with drain, source and bulk in parallel, being the selection made by individual gate terminals for each array. Using this multiplexing strategy, it was possible to access 200 transistors in a 40 pin DIP package.

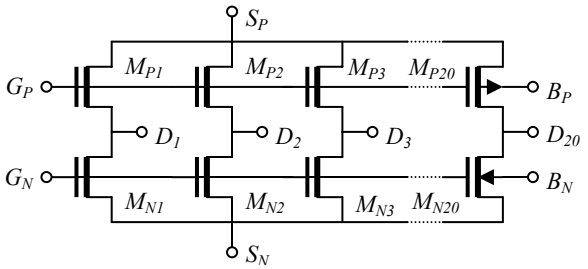

Figure 1. Schematic diagram of each pair of arrays with the same dimensions.

4. MEASUREMENTS

Intradie current mismatch was measured from ten packaged dies of an amount of forty, all of them presenting the same mismatch behavior. The circuit shown in Figure 2 was used for measuring current mismatch. $V_D = V'_D$ and V_B are voltage sources and I_B is the bias current for the reference transistor M_{REF}. The source V_S = 0V for all mismatch measurements. Source/monitor units (SMU) of the semiconductor parameter analyzer HP4145B were employed in the test setup. The same M_{REF} was used for all measurements while the remaining 19 transistors were measured in pairs of adjacent devices, M_i and M_{i+1} ($i=1, \ldots, 18$), for data acquisition. Transistor pairs M_i and M_{i+1} were sequentially characterized, with the currents of both transistors (I_1 and I_2) being measured simultaneously for each bias condition with the switches in either position 1 or 2. The dc current flowing in each device, $I_{D(i)}$ or $I_{D(i+1)}$, was taken as the average value of the two

currents measured for each transistor. This procedure minimizes any error that may result from mismatch between the two SMUs.

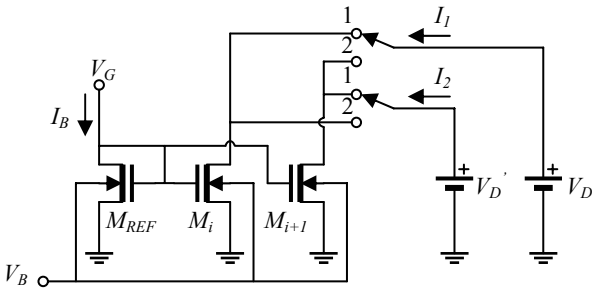

Figure 2. Test setup: M_{REF} is the reference transistor while M_i and M_{i+1} are the transistors under test. I_B (V_B, V_D'=V_D) is a current (voltage) source. I_1 and I_2 are the measured currents.

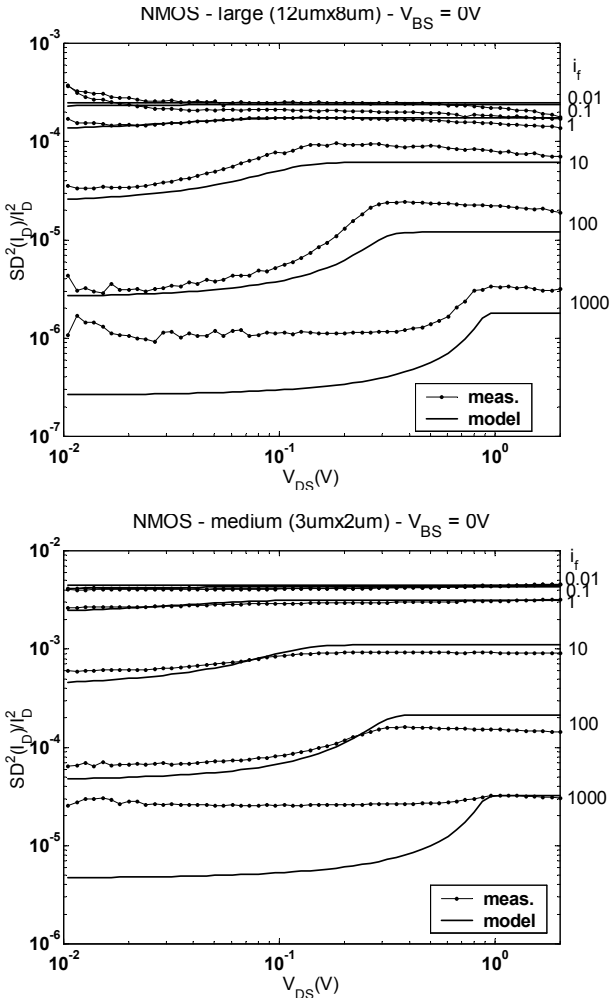

Figure 3. Normalized current mismatch for the NMOS transistor arrays. *Large* (12µm x 8µm) and *medium* (3µm x 2µm) size arrays are shown. Inversion level (i_f) ranges from 0.01 to 1000. Bulk was kept at zero volt.

Normalized differencial mismatch [12] for each array is then calculated using the following expression

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{SD^2(I_D)}{I_D^2} = \frac{1}{2(N-1)\overline{I_D}^2}\sum_{i=1}^{N}\left(I_{D(i)} - I_{D(i+1)}\right)^2 \qquad (4)$$

where N is the total number of pairs in each group of identical transistors (N=18 for our test structures). The factor *2* in the denominator of (4) was necessary to convert the variance of a differentially measured parameter into the variance of a single parameter.

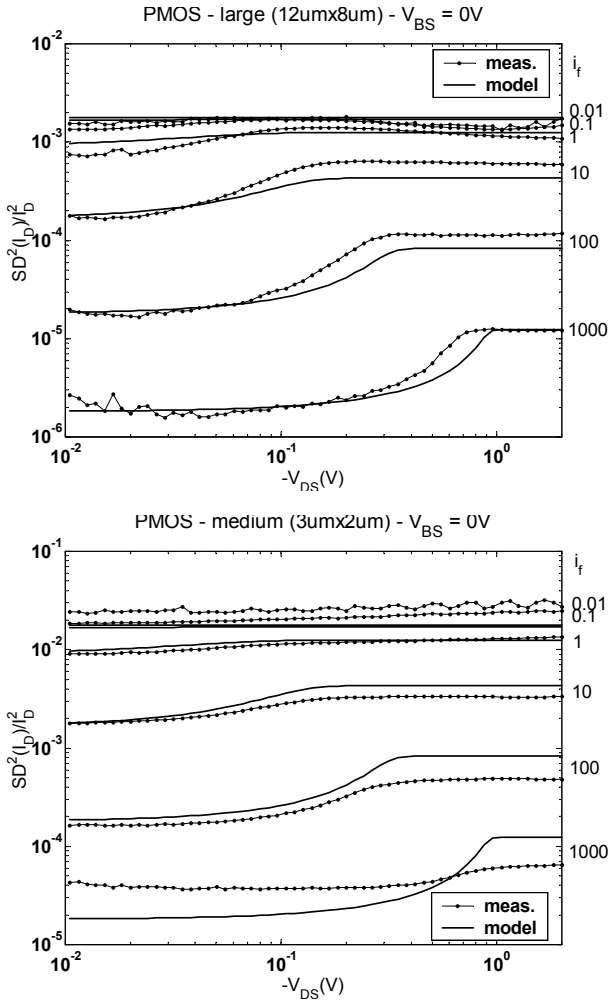

Figure 4. Normalized current mismatch for the PMOS transistor arrays. *Large* (12µm x 8µm) and *medium* (3µm x 2µm) size arrays are shown. Inversion level (i_f) ranges from 0.01 to 1000. Bulk was kept at zero volt.

Figures 3 and 4 present the mismatch power normalized to the dc power ($SD^2(I_D)/I_D^2$) for drain-to-source voltage ranging from +(-)10mV (linear region) to +(-)2V (saturation) for the NMOS (PMOS) devices. Mismatch was measured (dotted lines) for six different inversion levels (0.01, 0.1, 1, 10, 100, and 1000), for the *large* and *medium* device arrays. The bulk terminal was kept at zero volt. Simulated curves (solid lines) were determined from

expression (3), with i_r calculated through the long-channel ACM model [9], [10].

In weak inversion (i_f = 0.01 and 0.1), mismatch is almost constant from the linear to saturation regions and independent of the inversion level, as predicted by (3). Measured and simulated curves for weak inversion are almost coincident, being hardly distinguishable in some cases.

From moderate (i_f = 1 and 10) to strong (i_f = 100) inversion, both the simulated and measured curves present similar behavior, increasing from the linear region to saturation, where a plateau is reached. Differences between measured and simulated curves at saturation, may be associated with statistical spatial-nonuniformity concentration of dopant atoms [13].

Parameter N_{oi} was estimated from measurements in weak inversion, using equation (3). Effective transistor width and length (W_{eff} and L_{eff}) were calculated [14] with the help of BSIM parameters *WINT* and *LINT* (0.065µm and 0.075µm, respectively). *N** was calculated based on parameters provided by MOSIS. The same value of N_{oi}, $1.8\text{x}10^{12}$ cm^{-2}, for the NMOS devices, and $7\text{x}10^{12}$ cm^{-2} for the PMOS devices was obtained for both the *large* and *medium* transistors. It should be noted that N_{oi} includes both the acceptor and donor impurities. As a consequence, N_{oi} is usually higher than the product of the net ion concentration and the depletion layer depth.

Some authors [4] suggest that PMOS devices show better matching than NMOS devices, or vice-versa [3]. Our results, however, indicate that matching depends on process details, such as doping patterns (halo implant, twin-well, surface implant adjustment, retrograde implant etc). As can be seen from the results, for NMOS and PMOS devices with the same geometry, inversion level, and drain voltage, PMOS (in compensated N well) present higher mismatch than NMOS transistors. Other authors have found that PMOS show greater mismatch than NMOS devices [15], while some have found the contrary [6]. We conclude that there is not a simple "rule of thumb" regarding which type of MOS transistor is better matched. Our model approach states that, in general, mismatch is higher for the device type (N or P) with higher total channel impurity density.

Figure 5 shows the measured and simulated dependence of current matching on inversion level for the linear and saturation regions of NMOS transistors, at two bulk bias voltages (V_{BS}). From these figures, one can see that larger transistors follow the "area rule", as shown in our model. For a particular bulk bias, we used the same N_{oi} for modeling the matching of both the *large* and *medium* transistors, in the linear and saturation regions. The *small* transistors do not follow this rule, presenting a mismatch 55% lower than the model estimates (at zero volt bulk bias) using the same N_{oi}. At V_{BS}= –3V, the mismatch measured for the *small* transistors is in good agreement with the value estimated by our model. However, values of N_{oi} for the *small* transistors different from those measured for the *large* transistors were chosen in order to obtain better fitting of the curves.

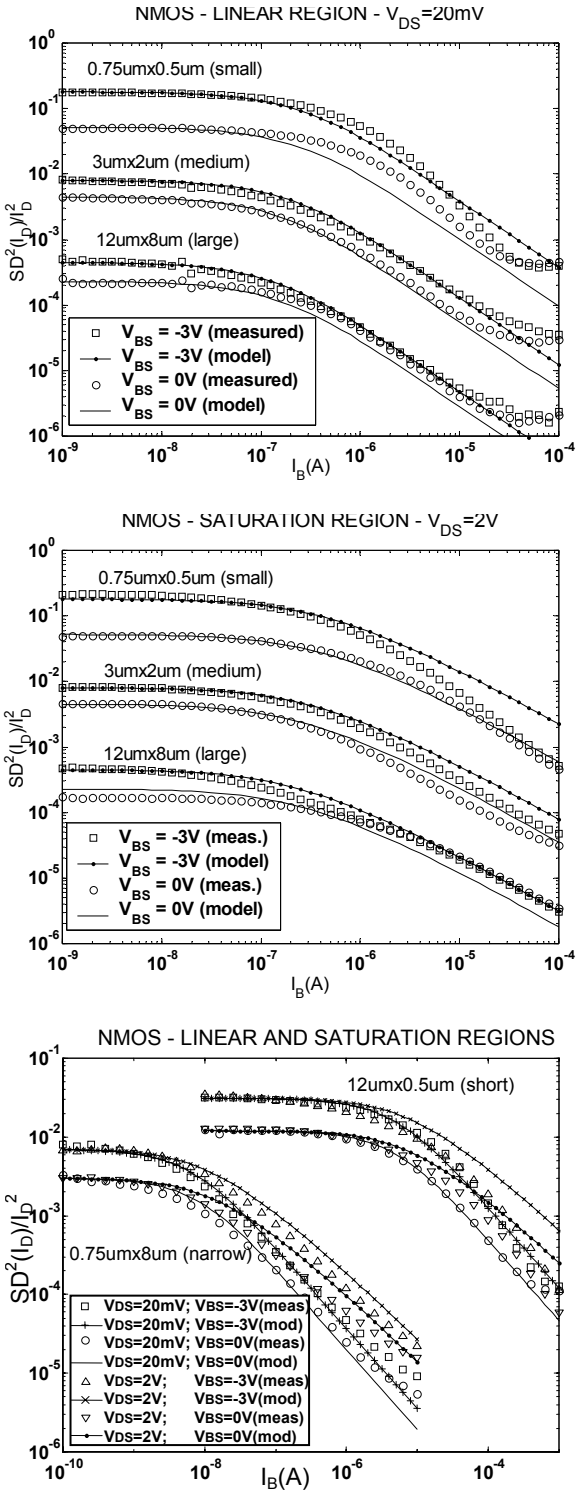

Figure 5. Current matching vs. inversion level for linear and saturation regions for the NMOS *large*, *medium*, *small*, *short* and *narrow* transistor arrays under two bulk bias voltages.

For the dies we characterized, *small* transistors presented an unpredictable N_{oi}, as previously observed in reference [16]. Indeed, electrical characteristics of short-channel devices are very sensitive to fluctuations due to a greater dependence on edge effects. This high sensitivity of short-channel devices is one of the main reasons for the difficulties found in modeling mismatch, mainly in today's very complex submicron technologies. Also, for minimum length devices, drain and source doped regions are very close to each other, affecting strongly the shape of the depletion layer below the channel. As experimental data demonstrated, the model we developed for mismatch can also be used for short-channel transistors, even though fitting of N_{oi} is required. A good approach for modeling mismatch in short-channel transistors would be to define a range of "maximum-minimum" values for N_{oi}. In a conservative design, the maximum value of N_{oi} would be chosen to predict the worst-case mismatch. Also in the case of minimum length (*short*) and minimum width (*narrow*) devices, our mismatch model is applicable to both showing good agreement with measured data.

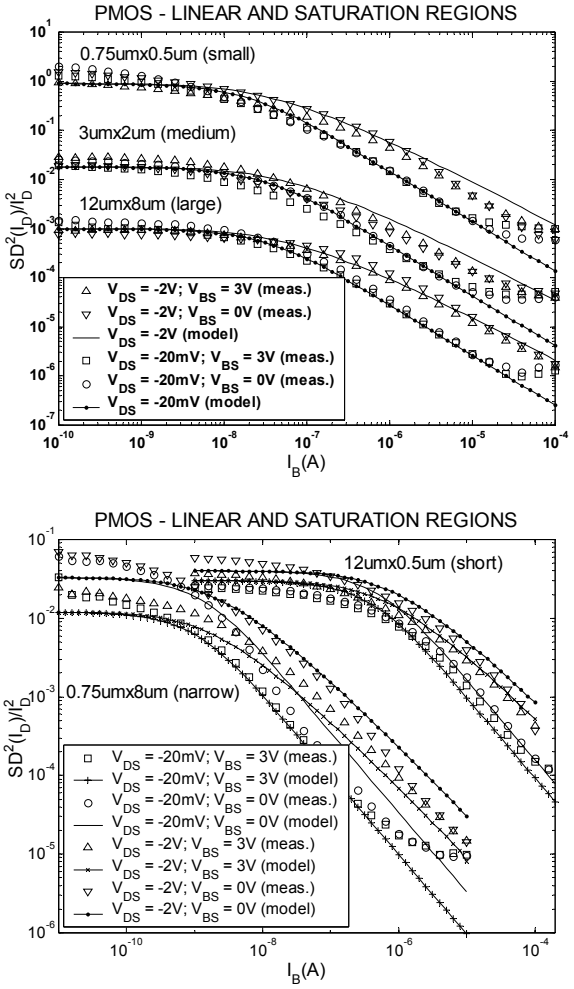

Figure 6. Current matching vs. inversion level for linear and saturation regions for the PMOS *large*, *medium*, *small*, *short* and *narrow* transistor arrays under two bulk bias voltages.

Figure 6 presents the results from the measurements and the modeling for PMOS devices. For these devices, bulk bias has a lesser impact on mismatch than for NMOS devices. The measured data show good agreement with the "area rule", except, again, for the *small* devices. The N_{oi} used for the fitting of the curve for *small* devices is 80% higher than the value estimated for larger PMOS devices. From the measurements taken on devices fabricated in the 0.35µm technology we can observe that, for equivalent size and bias, PMOS exhibit higher mismatch than NMOS devices.

Besides fluctuation of dopant atoms in the channel, gate dopant fluctuation and geometrical variations are also relevant mismatch factors [2], [17]. Many authors have shown from experiments that the first factor is the dominant factor for threshold voltage (V_T) mismatch (resulting in current mismatch), the second being also very relevant for sub-micron processes, and the third being the least relevant in general. Gate dopant fluctuation results from the inherent poly-silicon clustering process, and doping implant concentration, therefore, changes along the oxide interface. As a result, the gate depletion layer is not uniform over the gate area, affecting transistor behavior as if oxide thickness were not uniform (changing the charge density locally). As can be seen, other sources of mismatch can be included in our model to improve its accuracy but, for the moment, we have tried to keep it as simple as possible.

5. CONCLUSIONS

In this paper, we characterized current mismatch for the MOS transistor operating under a wide range of bias conditions. A set of arrays of identical transistors was manufactured in a 0.35 µm CMOS technology from TSMC to assess the influence of bias and geometry on current mismatch. Careful measurement process was done to provide differencial mismatch data from pairs of transistors. A previously developed mismatch model, continuous in all operating regions was used for comparision. The approach that was used for mismatch modeling is based on the integration of the random number of carriers along the channel, resulting in a compact easy-to-use formula for mismatch that covers all operating regions. The results we obtained for mismatch are closely related to those derived in [18] for *1/f* noise, since the physical mechanisms at the origin of both phenomena are similar. We conclude that fluctuations in lumped parameters such as the threshold voltage are not appropriate for describing mismatch owing to the nonlinear distribution of carriers along the transistor channel. Experimental results confirmed the accuracy of our model under a wide range of geometries and bias conditions, including different bulk bias voltages. For the technology under analysis, we concluded that the dominant factor in mismatch characterization is N_{oi}, the average number of dopants per unit area in the depletion layer below the channel. We expect this work could help circuit designers to predict transistor mismatch accurately from a single parameter (N_{oi}).

6. ACKNOWLEDGMENTS

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