An Accurate Zero-Current-Switching Circuit for Ultra-Low-Voltage Boost Converters

Rafael L. Radin, *Student Member, IEEE,* Mohamad Sawan*, Fellow, IEEE*, and Márcio Cherem Schneider*, Senior Member, IEEE*

***Abstract*— The use of digital schemes to indirectly detect the zero-current crossing and perform the zero-current switching in ultra-low-voltage inductive boost converters has been prevalent in recent developments. However, design guidelines for such digital schemes are still lacking. In this paper, an efficient zero-current switching scheme for ultra-low-voltage boost converters is proposed and implemented in standard CMOS 130 nm technology. Instrumental to our design was the introduction of the proper time delay for sensing the direction of the inductor current on the opening of the high-side switch. The correct delay time as a function of the circuit parameters keeps the switching as close as possible to the zero-current crossing. Owing to an efficient zero-current-switching scheme, the fabricated prototype provides end-to-end efficiency of 76% for a voltage converter having an input voltage as low as 20 mV.**

***Index Terms*— Boost converter, energy harvesting, ultra-low power, ultra-low voltage, zero-current switching**

I. Introduction

RECENT developments in thermal energy harvesting have been focused on low-voltage operation using the inductive boost converter (Fig. 1(a)) in discontinuous conduction mode (DCM) to provide DC-DC conversion of ultra-low input voltages (V_{IN}) to output voltage (V_{OUT}) levels suitable for powering electronic devices. For the efficient operation of the converter in DCM (Fig. 1(b)), the high-side switch (HSS) should be opened when the inductor current is very close to zero. The opening of the HSS when the current is positive impedes the energy stored in the inductor from being fully transferred to the output. On the other hand, a negative current leads to a reverse energy flow that partially discharges the output capacitor [1], [2]. A possible candidate for the HSS implementation is the diode [3]. However, this solution is not efficient for low power applications due to both the diode reverse leakage current and the forward voltage drop.

This work was supported in part by the Brazilian government agencies Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (CAPES), Finance Code 001, and the National Council for Scientific and Technological Development – CNPq.

R. L. Radin and M. C. Schneider are with the Electrical Engineering Department, Federal University of Santa Catarina (UFSC), 88040-900, Florianopolis, SC, Brazil.(e-mail: rafaelradin@gmail.com).

M. Sawan is with Polystim Neurotech Lab, Polytechnique Montreal, Canada, and CenBRAIN Lab, Westlake University, Hangzhou, China.

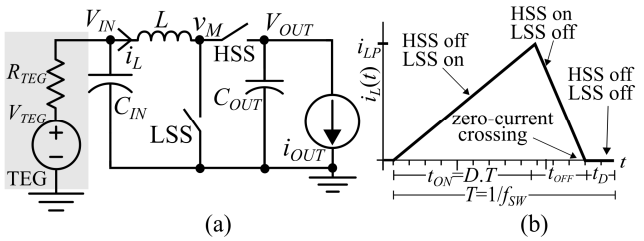

Fig. 1. (a) Simplified inductive boost converter topology and (b) inductor current in DCM.

In order to improve the efficiency, a MOS switch controlled by a zero-current-switching (ZCS) scheme is usually employed as the HSS. ZCS schemes are used for the opening of the HSS of the boost converter at the instant close to the zero crossing of the inductor current (Fig. 1(b)), at the end of the inductor discharging time (t_{OFF}). Some designs use voltage comparators to sense the voltage drop through the HSS to detect the zero-current crossing [1], [4]-[6]. Since the HSS resistance is low during the on state, detecting the very low voltage drop across the HSS when the current is close to zero is unavoidably prone to error.

Another approach to perform the ZCS involves the use of digital schemes to detect the zero-current crossing through an indirect variable [2], [7]-[11], which is the voltage v_M (Fig. 1(a)). This is the most commonly used approach, since the power consumption of the ZCS scheme is reduced due to the adoption of digital circuits. In this solution, v_M is sensed after the opening of the HSS, and quantized using a 2-level logic, where logic low is associated with early opening of the HSS while logic high is associated with its late opening. The sensed and quantized signal is sent to a control circuit that selects a pulse width that sets the state of the HSS for switching near the zero-current crossing. However, this approach is associated with two fundamental problems: firstly, the appropriate time for sensing the voltage v_M, referred to herein as the measurement delay (Δt_M) [2], [8], has not yet been addressed; and secondly, the linear scaling used to modulate the width of the pulse that controls the HSS state is inefficient at low V_{IN}, leading to low accuracy in the zero-current crossing detection in this range. To perform the synchronization of the measurement delay, most authors report the adjustment of Δt_M by simulation, although they do not provide any hints on how to properly set the value of Δt_M as a function of the circuit parameters. To address the problem related to the detection accuracy at low V_{IN}, in [10] the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2020.3040501, IEEE Transactions on Circuits and Systems II: Express Briefs

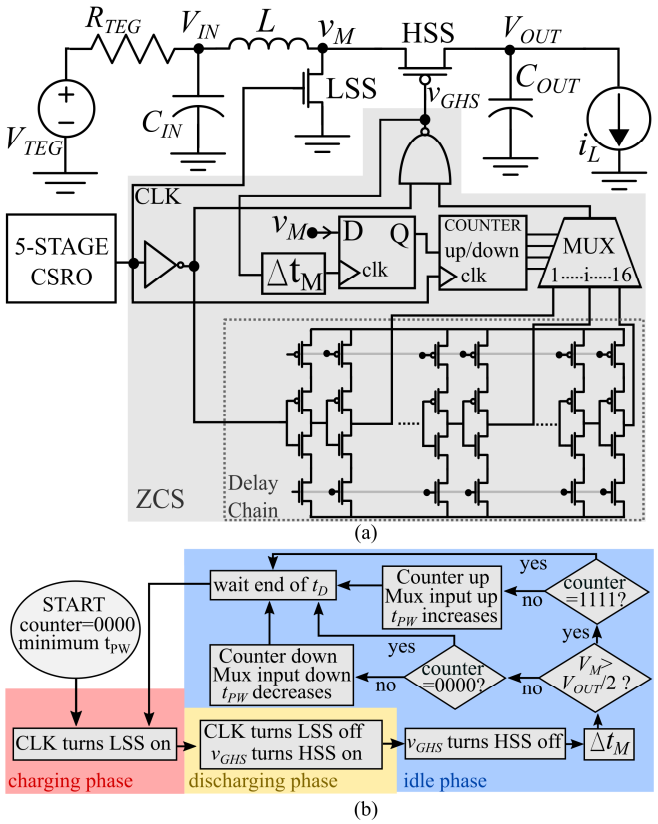

Fig. 2. (a) Proposed circuit architecture of the boost converter. The shaded area represents the schematic of the control circuit of the HSS and (b) a flowchart detailing the operation principle of the ZCS circuit.

resolution is increased with the use of coarse and fine delay stages, which set the width of the pulse that opens the HSS. However, the ZCS circuit in [10] uses an external 0.6 V power supply to reduce the power consumption and operates only in a narrow input range (20-50 mV). Also, to increase the resolution in [11] the authors use a 6-bit resolution, which increases the circuit complexity and power consumption.

In this brief, we analyze and implement a digital ZCS scheme for the improvement of the overall boost efficiency. The proper setting of the measurement delay Δt_M employed in this work allows the correct discrimination between early and late opening of the HSS. The value of Δt_M has a direct influence on the conversion efficiency and a criterion for its setting has not yet been established in the literature. The proper choice of the Δt_M value along with the pulse-width geometric scaling adopted here allows the HSS to perform switching very close to the zero crossing of the current over the whole operational range of the converter.

II. Proposed ZCS Circuit

To open the HSS close to the zero-crossing of the inductor current, we implemented the ZCS circuit shown in Fig. 2(a), which shares some of the operation principles of the circuits reported in [2], [7]-[11]. However, important modifications were introduced to improve the detection accuracy and minimize synchronization errors, especially at low V_{IN}. The

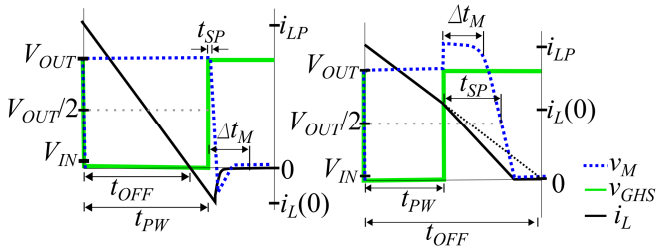

Fig. 3. Representation of the inductor current, v_{GHS} and v_M for the case of late opening (left) and early opening (right).

power consumption of the ZCS circuit is mainly due to the switching losses of the logic circuits. In post-layout simulations, the power dissipation of the ZCS circuit self-supplied by V_{OUT}=1 V was 348 nW for f_{SW}=40 kHz.

Ideally, the ZCS circuit shown in Fig. 2(a) generates a pulse signal (v_{GHS}) that keeps the HSS closed during t_{OFF} and open during the inductor idle (t_D) and charging (t_{ON}) times (see Fig. 1(b)). In our application, t_{ON} (17 µs) and T (25 µs) are fixed parameters provided by the clock signal shown in Fig. 2(a), which is generated by a five-stage current-starved ring oscillator (CSRO). The pulse generated by the ZCS circuit (v_{GHS}), applied to the gate of the HSS, has a variable width (t_{PW}) that should be as close as possible to t_{OFF}, which is an almost linear function of V_{IN}, especially at high voltage conversion ratios (M) [12]. At each cycle of operation, the ZCS circuit needs to detect the early or late opening of the HSS and select the value of t_{PW} during which the HSS is closed. For the 4-bit system adopted in this research, 16 different values for the pulse width (t_{PW}) are generated to accommodate the range of t_{OFF} or, equivalently, the range of V_{IN}. To implement these functionalities, the ZCS circuit is comprised of a delay chain with 16 stages of current-starved inverters (Fig. 2(a)) that generate a sequence of increasing pulse widths, the sensing flip-flop, the measurement delay (Δt_M) circuit and a pulse selection mechanism (multiplexer and a 4-bit counter).

A. Circuit operation

The operation principle of the proposed ZCS circuit is represented in the flowchart of Fig. 2(b). Using a D-type flip-flop, the circuit senses the voltage v_M at a time slot equal to Δt_M after the opening of the HSS. If the HSS opens after the zero-current crossing, the initial condition for the inductor current at the opening of HSS is negative ($i_L(0)<0$) and v_M will shift rapidly from V_{OUT} to zero. Therefore, if v_M is lower than the flip-flop switching point ($V_{OUT}/2$), logic low is detected by the sensing flip-flop, which is interpreted as late opening. On the other hand, if the HSS opens before the zero-current crossing ($i_L(0)>0$), the inductor current discharges through the high off-resistance of the HSS, causing an overshoot at v_M (Fig. 3), which lasts until the inductor completely discharges. Thus, if v_M is still higher than the switching point a short time (Δt_M) after the opening of the HSS, logic high is detected by the flip-flop, which is interpreted as early opening.

Depending on the logic level detected, the counter is then incremented, for logic high (early opening), or decremented, for logic low (late opening), in order to make the current pulse

width applied to the gate of the HSS as close as possible to t_{OFF}. The 4-bit counter controls a multiplexer, which connects one of the outputs of the 16-stage delay chain to the pulse generator circuit, thus setting the pulse width. In steady state, the pulse width generated by the ZCS circuit (t_{PW}) will alternate between two values around t_{OFF}. In one cycle of operation, t_{PW} will be slightly narrower than t_{OFF}; thus, early opening is detected and a control signal is sent to the counter in order to increase t_{PW}. In the next cycle, t_{PW}, which was increased in the previous cycle, is now slightly wider than t_{OFF}, and late opening is detected by the flip-flop. Similarly, the counter decreases the pulse width, returning to the previous condition where t_{PW} is slightly narrower than t_{OFF}; thus keeping t_{PW} oscillating around t_{OFF}.

III. The Measurement Delay

The time (Δt_M) after the opening of the HSS at which v_M is sensed by the flip-flop is set by the measurement delay block, comprised of two inverters calibrated for the required delay (Δt_M). Although in previous works the measurement of v_M has been used to discriminate between early or late opening of the HSS, no specific criterion for determining the value of Δt_M has been proposed.

Let us now define t_{SP} as the time interval between the opening of the HSS and the crossing of v_M through the switching point (V_{OUT}/2) of the sensing flip-flop, as shown in Fig. 3. The value of t_{SP} is a function of certain circuit parameters and initial conditions at the opening of the HSS. If Δt_M is set too short, compared to t_{SP}, late opening can be interpreted as early opening. Conversely, if Δt_M is set too long, early opening can be interpreted as late opening. Therefore, the accuracy in detecting late or early opening for this type of ZCS scheme is strongly related to the synchronization of the sensing circuit, which is set by Δt_M.

In order to evaluate the dependence of t_{SP} on the inductor current at the opening of the HSS ($i_L(0)$), post-layout transient simulation was performed, where the initial condition for the inductor current was swept and t_{SP} was measured for different values of L and V_{OUT}. The results are shown in Fig. 4 for the normalized $i_L(0)$, in order to provide a curve which is independent of the boost inductance value and output voltage. As can be seen in Fig. 4, t_{SP} is a monotonic function of $i_L(0)$. Therefore, the measurement delay Δt_M should be set at a value higher than the values of t_{SP} for negative $i_L(0)$, allowing v_M to cross the switching point and, thus, late opening to be correctly detected. Similarly, Δt_M should be lower than the values of t_{SP} for positive $i_L(0)$, preventing v_M from crossing the switching point and, thus, allowing early opening to be correctly detected. Hence, setting Δt_M equal to the value of t_{SP0}, which is the value of t_{SP} for $i_L(0)$=0, allows both the early and late opening of the HSS to be correctly discriminated. For L=220 µH and V_{OUT}=1 V, the post-layout simulation indicated a value of t_{SP0} equal to 33 ns, which was the value chosen for Δt_M.

In the appendix, we analyze the time response of v_M after the opening of the HSS. For the second-order system

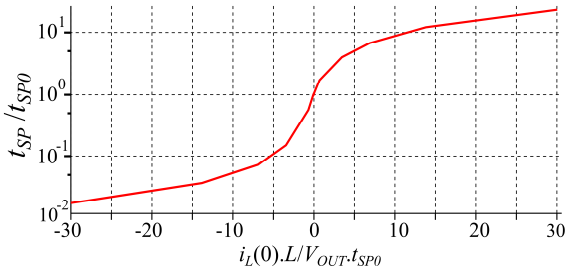

Fig. 4. Post-layout results for normalized t_{SP} vs $i_L(0)$.

comprised of the capacitance at node v_M (C_{MP}), the inductance (L) and the parasitic resistance of the switches (Fig. 8(a)), t_{SP0} is given by

$$t_{SP0} = \sqrt{LC_{MP}}\arccos(0.5) \approx 1.05\sqrt{LC_{MP}}\,. \quad (1)$$

Hence, setting Δt_M equal to t_{SP0} given by expression (1) minimizes the synchronization error. The result obtained with (1) is in close agreement with the post-layout simulations.

In steady-state, the circuit is designed to alternate between two consecutive pulse width values that cause alternating logic level readings. If Δt_M is equal to t_{SP0}, these pulse widths also generate alternating late and early opening, as represented in Fig. 3, keeping $i_L(0)$ as close as possible to zero. However, inappropriate values of Δt_M can lead to an alternation around a value of $i_L(0)$ different from zero. In this case, the pulse width values could generate only either early or late opening.

IV. Synchronization Error and Losses

The values of t_{PW} provided by the delay chain should cover the whole range of t_{OFF}, which is dependent on the specified range of V_{IN}. The accuracy of the ZCS scheme can be increased by increasing the bit resolution, but the power consumption of the ZCS block increases roughly by a factor of two for each additional bit of resolution. If the range of t_{OFF} is linearly divided, the relative synchronization error is higher for lower V_{IN}, owing to a relative step size of t_{PW} which is greater than at high values of V_{IN}, or t_{OFF}. To overcome this problem, the use of the geometric scaling of t_{PW} has been proposed [9] to decrease the step size in t_{PW} for low values of t_{OFF} (or V_{IN}).

The synchronization errors are translated into synchronization losses ($\mathcal{L}_{SYNC}$), which are defined with the aid of Fig. 3. $\mathcal{L}_{SYNC}$ can be expressed in terms of the energy transferred to the load for a given t_{PW} (E_{TPW}) and the energy transferred to the load for the case of ideal ZCS (E_{ZCS}), obtained when t_{PW}= t_{OFF}, leading to

$$\mathcal{L}_{SYNC} = \frac{E_{ZCS} - E_{TPW}}{E_{ZCS}} = \frac{k_L\left(t_{OFF} - t_{PW}\right)^2}{t_{OFF}^{\ 2}} \quad (2)$$

For the case of $i_L(0)$<0 (late opening), all of the energy which is drained from the output capacitor after the zero-current crossing is lost; thus, k_L is equal to 1. For the case of $i_L(0)$>0 (early opening), the energy stored in the inductor at the opening of the HSS is partially delivered to the load and partially lost in the HSS in the form of conduction losses. Therefore, k_L represents the fraction of the energy that is lost in the HSS and is a function of the HSS off-resistance and also

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2020.3040501, IEEE Transactions on Circuits and Systems II: Express Briefs

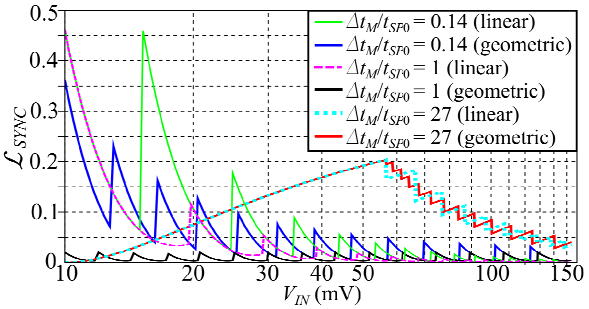

Fig. 5. Calculated $\mathcal{L}_{SYNC}$ vs V_{IN} for different Δt_M values (4 bits, k_L =0.3, L =220 µH).

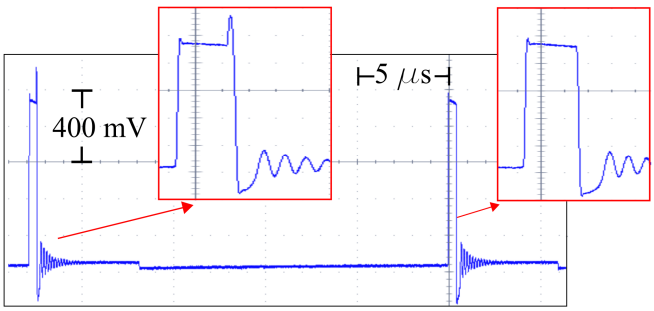

Fig. 6. Measured v_M waveform during steady-state operation. V_{IN}=20 mV.

slightly dependent on $i_L(0)$ and V_{IN}. An approximate value for k_L can be empirically estimated by simulation once the size of the HSS is defined. In our design, the value of k_L was around 0.3. Since in steady state the system alternates between two t_{PW} values, one slightly narrower and one slightly wider than t_{OFF}, the overall $\mathcal{L}_{SYNC}$ for a given t_{OFF} is the average of the $\mathcal{L}_{SYNC}$ values for the two alternating t_{PW} values.

To calculate (2) for any given set of Δt_M and V_{IN}, we need to determine t_{OFF}, which is easily obtained using the boost converter expressions [12], and the two alternating values of t_{PW}, which are calculated as follows: firstly, it should be noted that each Δt_M matches the t_{SP} of a specific $i_L(0)$, through the relation given in Fig. 4. This value of $i_L(0)$ should be compared to $i_L(t=t_{ON}+t_{PW})$ calculated from the time domain expression of i_L during t_{OFF} [12]. For each V_{IN} and Δt_M, the lowest value of t_{PW} generated by the ZCS circuit that makes $i_L(t=t_{ON}+t_{PW})<i_L(0)$ needs to be found. This is also the lowest value of t_{PW} that generates logic low for the given set of V_{IN} and Δt_M. In steady-state, the system alternates between this value of t_{PW} and its immediate lower value, which in turn generates logic high. Under these considerations, $\mathcal{L}_{SYNC}$ is calculated and plotted against V_{IN} for different values of Δt_M in Fig. 5, for both geometric and linear pulse scaling. As can be observed, using the geometric pulse scaling and setting Δt_M according to (1) minimizes the synchronization losses, which can become significant as Δt_M deviates from t_{SP0}. Values of Δt_M much lower than t_{SP0} have a stronger influence on $\mathcal{L}_{SYNC}$, especially at low V_{IN}.

V. Experimental Results

The inductive boost converter using the proposed ZCS circuit was designed and fabricated in a standard 130 nm CMOS process. The circuit is also comprised of startup and

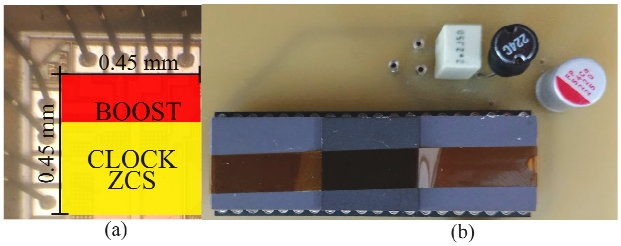

Fig. 7. (a) The micrograph of the fabricated chip and (b) the complete prototype used for measurements.

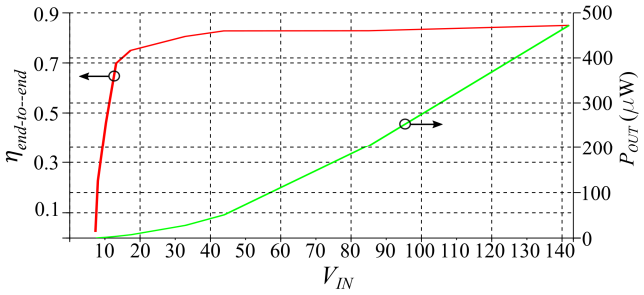

Fig. 8. Measurement results of the maximum $\eta_{end\text{-}to\text{-}end}$ and P_{OUT} vs V_{IN}.

TABLE I
Comparison of This Work with Other ZCS Approaches

Work	[5]	[8]	[10]	[11]	[4]	This work
Technology	130 nm	180 nm	65 nm	65 nm	180 nm	130 nm
Year	2015	2016	2017	2018	2020	
Minimum V_{IN}	10 mV	15 mV	20 mV *	40 mV*	60 mV*	7.3 mV
$\eta_{Peak\ end\ to\ end}$	83%	86.6 %	81%	75%	83.9%	85%
$\eta_{end\text{-}to\text{-}end}$ @ ≈ 20 mV	53%	22.2 %	58 % *	-	-	76%
ZCS approach	Compa-rator	4-bit digital	coarse and fine delays	6-bit digital	Compa-rator	geometric scaling $\Delta t_M = t_{SP0}$
Silicon area (mm^2)	0.12**	0.3**	0.04**	1.0	0.94**	0.2**

* - Expressed as a function of the TEG open circuit voltage (V_{TEG})
** - Only active area (not including the pads)

maximum power point tracking blocks, but those are beyond the scope of this brief. A micrograph of the fabricated chip is shown in Fig. 7(a). The complete prototype includes the off-chip components L=220 µH, C_{IN}=22 µF and C_{OUT} =2.2 µF, as shown in Fig. 7(b). The input source was emulated with a variable power supply and a 40 Ω series resistor.

Fig. 6 shows the waveform of v_M, where it is possible to see the alternation between early and late opening of the HSS. As can be noted, early opening of the HSS generates a glitch in the waveform of v_M, whereas late opening does not. The alternation between late and early opening occurs, as expected for a properly designed Δt_M, thus keeping $i_L(0)$ around zero. The damping of the system after the opening of the HSS is dependent on the off-resistance of the switches, the values for which are functions of v_M. Based on the results given in the appendix, one can conclude that the resistance of the switches has values that will lead to an underdamped system for v_M ranging from close to zero to one volt. This conclusion was confirmed by the underdamped oscillatory nature of the

transient signal observed in the experimental waveforms of Fig. 6, for both early and late opening.

Using a variable resistive load at the output, the end-to-end efficiency ($\eta_{end\text{-}to\text{-}end}$), which is the ratio of the output power to the available power, and P_{OUT} were measured for different input voltages, as shown in Fig. 8. The minimum V_{IN} capable of achieving voltage conversion was 7.3 mV for a 10 MΩ load (oscilloscope load). For V_{IN}=20 mV, $\eta_{end\text{-}to\text{-}end}$ is 76%, and for voltages higher than 40 mV, the efficiency remains between 82 and 85%. Table I summarizes the performance achieved with previously reported state-of-the-art ZCS approaches.

VI. Conclusion

A fully digital ZCS scheme that minimizes the synchronization error and losses has been proposed herein. An analytical expression for choosing the optimum measurement delay is provided, which gives values in close agreement with simulation results. The impact of the measurement delay on the synchronization losses was investigated, revealing an improvement in the efficiency of ZCS circuits through the choice of an appropriate measurement delay. The proposed circuit was implemented in 130 nm standard CMOS technology, confirming circuit feasibility for efficient conversion of ultra-low input voltages provided by energy harvesters, delivering peak end-to-end efficiency of 85% and allowing operation for input voltages below 10 mV.

Appendix

The time response of the voltage v_M after the opening of the HSS is analyzed using the equivalent circuit shown in Fig. 9(a) for $i_L(0)$=0. Applying Kirchhoff's current law at node v_M yields

$$\frac{d^2 v_M(t)}{dt^2} + \frac{dv_M(t)}{dt}\left[\frac{1}{C\left(R_{LS}//R_{HS}\right)}\right] + \frac{1}{LC_{MP}}\left(v_M(t)\right) = \frac{V_{IN}}{LC_{MP}}. \quad (3)$$

To evaluate the type of damping that occurs after the opening of the HSS, we measured the values of the resistances (R_{HS} and R_{LS}) of the switches and the parasitic capacitance at node v_M (C_{MP}). For the switches resistance, the DC transfer simulation was performed, sweeping v_M from -0.3 to 1.3 V, as shown in Fig. 9(b). When v_M shifts from V_{OUT} to $V_{OUT}/2$, the parallel combination of R_{HS} and R_{LS} ranges from 55 kΩ to 100 kΩ.

To evaluate C_{MP}, we performed a post-layout simulation of the step response of v_M through the application of a pulse signal source with a known series resistance. On analyzing the time constant of the rising signal, we obtained the value of C_{MP}=4.6 pF.

For the parallel equivalent resistance of the switches resistance and C_{MP} obtained with our design, along with the boost inductance (L=220 µH), the system is highly underdamped. Thus, using (3), the time response of v_M right after the opening of the HSS [13] is

$$v_M(t) = V_{IN} + \left(B_1\cos(\omega_D t) + B_2\sin(\omega_D t)\right)e^{-\alpha t}, \quad (4)$$

where $\omega_D \approx (LC_{MP})^{-1/2}$ and $\alpha = [2(R_{LS}//R_{HS})C_{MP}]^{-1}$. Furthermore, since $V_{IN} << V_{OUT}$, $\omega_D >> \alpha$ and $v_M(t=0) = V_{OUT}$, we approximate (4) for the time interval $0 \le t \le t_{SP}$ and for $i_L(0)$=0

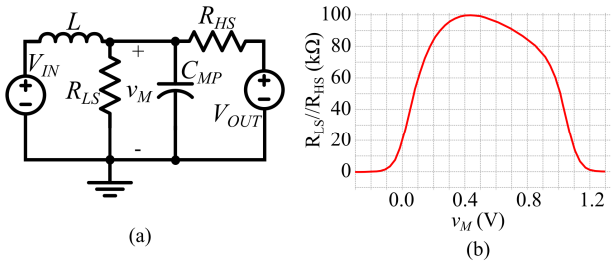

Fig. 9. (a) Equivalent circuit of the boost converter after opening of the HSS and (b) the off-resistance of the HSS and LSS in parallel.

as

$$v_M(t) = V_{OUT}\cos(\omega_D t). \quad (5)$$

Considering that at the switching point (t=t_{SP0}) v_M is equal to $V_{OUT}/2$, we use (5) to obtain (1).

Acknowledgment

CMC Microsystems is acknowledged for chip fabrication.

References

[1] Z. Luo, L. Zeng, B. Lau, Y. Lian and C. Heng, "A sub-10 mV power converter with fully integrated self-start, MPPT, and ZCS control for thermoelectric energy harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 5, pp. 1744-1757, May 2018.

[2] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mV startup voltage," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 333– 341, Jan. 2011.

[3] Y. K. Teh, P. K. T. Mok, "Design of transformer-based boost converter for high internal resistance energy harvesting sources with 21 mV self-startup voltage and 74% power efficiency," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2694–2704, Nov. 2014.

[4] Z. Shang, Y. Zhao, W. Gou, L. Geng and Y. Lian, "83.9% efficiency 100-mV self-startup boost converter for thermoelectric energy harvester in IoT applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 9, pp. 1654-1658, Sept. 2020.

[5] A. Shrivastava, N. E. Roberts, O. U. Khan, D. D. Wentzloff, B. H. Calhoun, "A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric and solar energy harvesting with 220 mV cold-start and 14.5 dBm, 915 MHz RF kick-start," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 8, 2015.

[6] J. Mu and L. Liu, "A 12 mV input, 90.8% peak efficiency CRM boost converter with a sub-threshold startup voltage for TEG energy harvesting," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2631-2640, Aug. 2018.

[7] A. K. Sinha and M. C. Schneider, "Short startup, batteryless, self-starting thermal energy harvesting chip working in full clock cycle," *IET Circuits, Devices & Systems*, vol. 11, no. 6, pp. 521-528, 11 2017.

[8] J. Katic, S. Rodriguez and A. Rusu, "A dual-output thermoelectric energy harvesting interface with 86.6% peak efficiency at 30 µW and total control power of 160 nW," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1928-1937, Aug. 2016.

[9] R. L. Radin, M. Sawan, C. Galup-Montoro and M. C. Schneider, "A 7.5 mV-input boost converter for thermal energy harvesting with 11 mV self-startup," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 8, pp. 1379-1383, Aug. 2020.

[10] M. Alhawari, B. Mohammad, H. Saleh and M. Ismail, "An efficient zero current switching control for L-based DC–DC converters in TEG applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 3, pp. 294-298, March 2017.

[11] B. Lim, J. Seo and S. Lee, "A colpitts oscillator-based self-starting boost converter for thermoelectric energy harvesting with 40-mV startup voltage and 75% maximum efficiency," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3293-3302, Nov. 2018.

[12] R. Erickson and D. Maksimovic, "Fundamentals of Power Electronics," Springer, 2001.

[13] C. Alexander and M. Sadiku, "Fundamentals of Electric Circuits (4th. ed.)," McGraw Hill Higher Education, USA, 2008