profile of 1557. Modelling of the quantum well subband energy levels was carried out using the envelope function approximation in which the energy states are described using a three-band Kane $\boldsymbol{k.p}$ approximation that takes into account the effect of band nonparabolicity and strain. We used this model to design structures each with an $n = 1$ to $n = 2$ transition at about 3.6 μm and to ascertain that all the samples have the same number of states in the well (three).

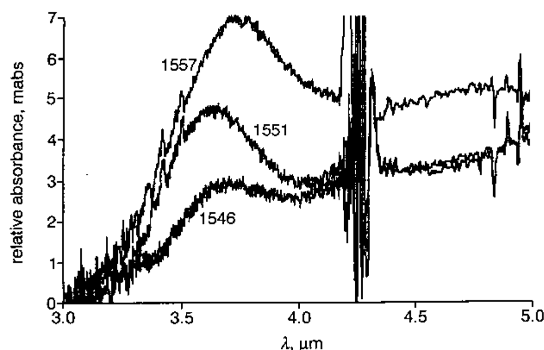

Fig. 2 *Room temperature FTIR absorption spectrum of samples 1546, 1551, and 1557 at Brewster angle using p-polarised light*

Curves are offset for clarity. Dip at 4.25 μm is due to CO_2 absorption in infrared beam path

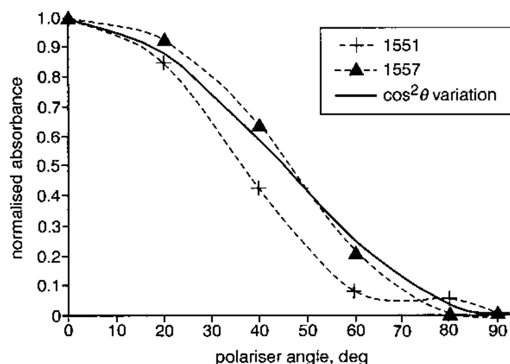

Fig. 3 *Normalised $n = 1$ to $n = 2$ peak intensity against polariser angle, θ, for samples 1551 and 1557*

Results: The room temperature intersubband absorption was measured in a Bio-Rad FT-3000 Fourier transform infrared spectrometer with a ZnSe wire grid polariser. Since the polarisation selection rule allows only radiation with its electric field vector perpendicular to the plane of the QW to stimulate an intersubband transition [1], the samples were oriented at the Brewster angle. The absorption spectrum was then measured using light p-polarised with respect to the plane of incidence. Fig. 2 shows the $n = 1$ to $n = 2$ intersubband absorption for the three samples studied. As expected there is an increase in the magnitude of absorption with carrier concentration for the two GaAs well samples (1546 and 1551). Significantly increased absorption is observed for the stepped well sample (1557) compared to 1551, even though it has a lower sheet carrier density (see Table 1). To investigate further the increased absorption in the stepped DBQW, the angle of the polariser was varied from $\theta = 0$ to 90° thus varying the fraction of p-polarised light in the incident beam. The normalised peak intensities for the stepped well (1557) and the higher-doped GaAs well (1551) are shown in Fig. 3. According to the selection rule for light induced intersubband transitions in QWs the absorption should decrease as $\cos^2\theta$ under these conditions. The solid line in Fig. 3 indicates this theoretical curve. The stepped well shows a greater than $\cos^2\theta$ dependence of the peak intensity whereas the square well peak intensity drops off much more rapidly with polariser angle. The enhanced absorption in the stepped well and the persistence of the absorption to greater polariser angles indicates a degree of relaxation of the selection rule forbidding normal incidence absorption. Since all the samples have three levels in the well and incorporation of the step is known to increase the oscillator strength of the normally forbidden $n = 1$ to $n = 3$ transition [6], the increase in the $n = 1$ to $n = 2$ transition in sample 1557 cannot be due to an increase in oscillator strength for this transition. It has previously been proposed that reduction in the well bandgap partially relaxes the electric field vector selection rule [8]. Alternatively the step itself may have a similar effect due to the contribution to the energy states from two different materials. Relaxation of the selection rule in a conventional stepped well has been theoretically analysed in [9]. (It is interesting to note that here we observe absorption enhancement despite the $n = 1$ level not being confined with the InGaAs alone.)

Conclusion: We have demonstrated an enhancement in the strength of the $n = 1$ to $n = 2$ intersubband absorption in GaAs DBQWs by introduction of an InGaAs layer. This occurs despite an expected reduction in the oscillator strength for this transition due to other normally forbidden transitions becoming allowed. The enhanced absorption is attributed to relaxation of the electric field vector selection rule.

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K.T. Lai, S.K. Haywood and R. Gupta (*Department of Engineering, University of Hull, Cottingham Road, Hull HU6 7RX, United Kingdom*)

E-mail: s.k.haywood@hull.ac.uk

M. Missous (*Department of Electrical Engineering and Electronics, UMIST, P.O. Box 88, Manchester M60 1QD, United Kingdom*)

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Well-driven floating gate transistors

A.F. Mondragón-Torres, M.C. Schneider and E. Sánchez-Sinencio

A new layout structure for floating gate MOS devices on top of an isolating n-well is proposed. The well provides the floating device with noise isolation from the substrate and can also be used as an additional input for threshold voltage control or signal modulation.

Introduction: Floating gate (FG) transistors are used in both digital and analogue circuits. In digital circuits they are the core of flash memories [1, 2]. For analogue circuits, multiple input (MI) FGMOS devices are used in low voltage applications [3], as analogue memories [4] or as translinear computing elements [5].

Traditionally, FG structures are laid out on top of the substrate. However, it is a common practice to lay out capacitors on top of a well to isolate the capacitor from substrate noise. Using this principle, we designed a MI-FGMOS transistor with a floating gate on top of an n-well.

Floating gate device: The FG element consists of an electrode surrounded by an insulator, with no direct electrical connection to any other conductor. The FG electrode acts as the gate of a MOSFET, which serves as the sensor transistor. The potential on the floating gate can be modified either by capacitive coupling with other conductors or by changing the charge stored on the floating gate [1].

In Fig. 1*a*, we show the symbol representing an MI-FGMOS transistor, which is a generalisation of a FG device with only one controlling gate. One of the most interesting characteristics of FG devices for analogue circuit design is that the drain current is a function of the weighted sum of voltages at the N controlling inputs.

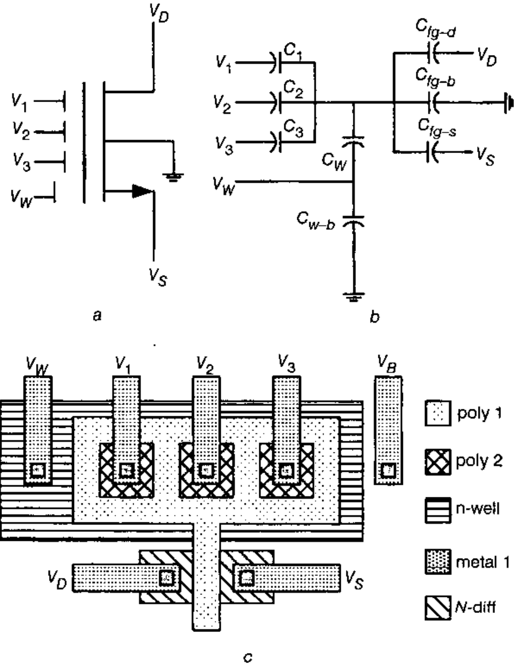

Fig. 1 *MI-FGMOS transistor*
a Symbol
b Equivalent capacitive model
c Layout
V_W is additional well input

In Fig. 1*c*, we show the MI-FGMOS layout, including a well beneath the floating gate. In Fig. 1*b*, we show its capacitive equivalent model. The voltage at the floating gate can be expressed as

$$V_{FG} = \sum_{i=1}^{N} \alpha_i V_i + \alpha_W V_W + V_{EQ} \quad (1)$$

where $\alpha_i = C_i/C_T$ is the ith coupling coefficient, C_i represents the capacitance from the ith controlling input V_i to the floating gate and C_T is the total capacitance of the floating gate. Similarly, $\alpha_W = C_W/C_T$ is the coupling coefficient from the well input V_W to the floating gate. V_{EQ} is an equivalent voltage due to both the charges stored on the floating gate and to DC voltages at the source and drain that are capacitively coupled to the floating gate.

In weak inversion, the current in the drain terminal is

$$I_D = I_0 \exp\left\{\frac{1}{n\phi_t}\left(\sum_{i=1}^{N} \alpha_i V_n + \alpha_W V_W + V_{EQ}\right)\right\} \quad (2)$$

where n is the subthreshold slope factor, ϕ_t is the thermal voltage, and I_0 is a constant dependent of technology and geometry [5]. The weak inversion region is more convenient to extract the subthreshold factor and thus the coupling coefficients, but the extraction methods are not limited to this level of operation.

Measurement results: All the measurements were performed on three-input FGMOS devices fabricated in a 0.35 µm technology with MOSFET channel dimensions W = 1.8 µm and L = 0.8 µm. Each controlling input capacitor was laid out with an area of 3.2 µm × 3.2 µm resulting in C_i = 8.8 fF. The drawn area of the n-well is 12.8 µm × 5.2 µm.

For measurement purposes we connected all controlling inputs together. From now on, V_{CG} is referred to as the controlling input and $\alpha_{CG} = \sum_{i=1}^{N} C_i/C_T$, as the total coupling coefficient associated with the controlling input.

The determination of the coupling coefficients is based on comparison of measurements taken on both the FG element and a 'dummy cell', which is a reference NMOS transistor with the same channel geometry as the FG device. To estimate α_{CG} and α_W we measure the equivalent subthreshold slope factors n, n^{CG} and n^W directly from the linear portion of the drain current against voltage plots shown in Fig. 2. Referring to (2), we observe that $n^x = n/\alpha_x$, where x represents CG or W.

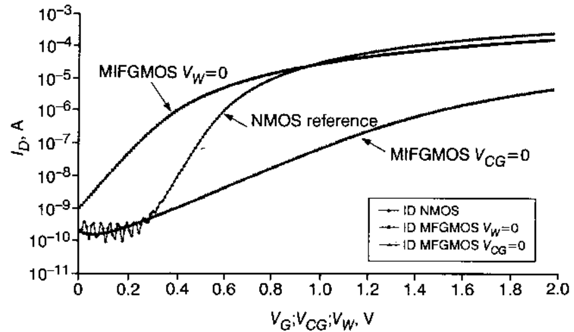

Fig. 2 *I_D against V_G (MOSFET), I_D against V_{CG} (V_W = 0 MI-FGMOS), and I_D against V_W (V_{CG} = 0 MI-FGMOS)*

To extract the subthreshold slope factors from Fig. 2, we find the regions with an exponential characteristic and we obtain the values from the definition $1/n = \phi_t d\ln(I_D)/dV_{GS}$. The measured subthreshold slope factors obtained are $n = 1.45$, $n^{CG} = 2.11$ and $n^W = 5.68$, and the corresponding coupling coefficients are $\alpha_{CG} = 0.69$ and $\alpha_W = 0.26$.

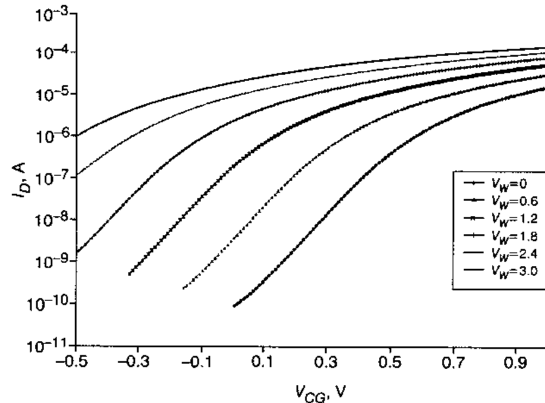

Fig. 3 *I_D against V_{CG}*

In Fig. 3, we show I_D against V_{CG} plots for well voltages V_W from 0 V to 3.3 V in 0.6 V steps. The I_D against V_{CG} curve shifts to the left as V_W is increased; the result is equivalent to a modification of the effective threshold voltage V_T^{CG} seen from the controlling gate, according to

$$V_T^{CG} = \frac{1}{\alpha_{CG}}(V_T - \alpha_W V_W - V_{EQ}) \quad (3)$$

where V_T is the threshold voltage at the floating gate. We can also express the variation of the threshold voltage by

$$\Delta V_T^{CG} = -\frac{\alpha_W}{\alpha_{CG}} \Delta V_W \quad (4)$$

where

$$\frac{\alpha_W}{\alpha_{CG}} = \frac{C_W}{C_{CG}} \quad (5)$$

C_W is the poly_1 to n-well thick oxide capacitance.

Fig. 3 shows that the threshold (horizontal) shift of the curves is approximately proportional to the well voltage. Therefore, one can conclude from (4) that the ratio given by (5) is almost constant over the whole range of well voltages. Since C_{CG} is a linear capacitor, one can conclude that C_W is also linear. This result is the expected one because in our FG device the well operates in the accumulation region for the whole range of allowable well voltages.

The remaining capacitance C_R ($C_{fg\text{-}d} + C_{fg\text{-}b} + C_{fg\text{-}s}$) at the floating gate is

$$C_R = \frac{(1 - \alpha_{CG} - \alpha_W)}{\alpha_{CG}} C_{CG} \quad (6)$$

The total input capacitance of the controlling gate estimated by the layout and from manufacturer's specifications is $C_{CG} = 26$ fF. Then, by using (5), the resulting poly_1-to-well capacitance is $C_W = 10$ fF and using (6), the remaining capacitance is $C_R = 2$fF. Note that the capacitor C_W from well to bulk represents a very important contribution to the total capacitance at the floating gate.

Conclusion: The new well-driven MI-FGMOS device can be used in applications where the controlling inputs require isolation from the substrate, where the additional n-well input can be used to program the equivalent threshold voltage without altering the behaviour of the controlling inputs or where modulation of the controlling inputs is required.

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A.F. Mondragón-Torres and E. Sánchez-Sinencio (*Department of Electrical Engineering, Texas A&M University, College Station, TX, 77840, USA*)

E-mail: antoniofmondragon@ieee.org

M.C. Schneider (*LCI-Departamento de Engenharia Elètrica, Universidade Federal de Santa Catarina, CP 476, 88 040 900, Florianópolis, SC, Brasil*)

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Window-gate for echo canceller of DMT ADSL

S.-W. Wei and H.-Y. Wang

A window-gate for the echo-canceller of a discrete multi-tone asymmetric digital subscriber line system is presented. This modification can significantly improve the convergence of the echo-canceller in the startup training procedure as well as the re-synchronisation in splitterless operation.

Introduction: Multicarrier modulation (MCM) has been proved to be one of the optimum modulation techniques for severe distortion channels [1, 2]. Since the 1980s a digital implementation of MCM using the discrete Fourier transform (DFT) or fast Fourier transform (FFT) technique has been developed, and is referred to as the discrete multi-tone (DMT) modulation. Owing to its high transmission efficiency, DMT has been adopted as the standard modulation for the asymmetric digital subscriber line (ADSL) system. ADSL is a new transmission technology that may provide a 1.5 to 8 Mbit/s data rate over existing local loops. Both the frequency division multiplexing (FDM) scheme and the echo-canceller (EC) scheme are allowed in DMT ADSL [3]. The EC-based structure can have a larger transmission capacity than that of the FDM structure, however, an EC is required. Data driven EC is the most popularly employed architecture for DSL because of its easy implementation [4]. A traditional EC model is shown in Fig. 1, without the window-gate circuit. The detailed theory of EC for ADSL is covered in [4] in detail. ADSL EC is generally composed of one frequency-domain EC and a time-domain tail canceller. The frequency-domain EC consists of N adaptive one-tap FIR filters in parallel, where N is the number of subchannels. The tap-coefficients of the frequency-domain EC can be represented by an N-tuple vector, denoted by $\hat{H}$. To maintain a less complex circuit, the least mean square (LMS) algorithm is always employed to update the tap-coefficients. As $\hat{H}$ is determined, the time-domain echo response $\hat{h}$ can be quickly estimated by an IFFT, denoted by EC-IFFT here. Assuming $\hat{H}$ and $\hat{h}$ are both known, the time-domain echo tail can be precisely estimated by performing a short-time convolution.

Fig. 1 *Modified ADSL data driven echo-canceller*

Splitterless operation: Integrating plain old telephone services (POTS) with data services is a necessary requirement in the ADSL system. In the splitterless ADSL operation environment, the equivalent loop impedance seen from the remote-side varies when the telephone sets 'hook' on or off. In fact, the pulse response of the channel will suddenly change at the instant the telephone hooks on/off. Therefore, a fast re-synchronisation operation is necessary when a telephone hooks on/off. In this simulation, the in-home loop model recommended in the G.test standard is employed [5]. Initially, we suppose the ADSL is working in a normal state and all telephones are hooked on. Then, based on reasonable operation, we assume four different operation modes (On/On; Off/On; Off/Off; On/Off) occur for phone A and phone B. Fig. 2 shows the corresponding echo channel responses for the four possible different modes where the impedance modelling of telephone hooking on/off follows the models presented in the G.test [5]. In the simulation results shown in Fig. 2, a test loop T1.601#7 is used as the outdoor loop [3].

Modified EC: For the EC simulation with traditional structure, i.e. without the window-gate in Fig. 1, we observed that the frequency domain EC could not immediately locate the exact solution $\hat{h}$ at the beginning due to the use of the LMS algorithm (an example of the learning curve is shown in Fig. 3). This is because the vector $\hat{H}$ cannot be immediately determined and will vary for a short time during the initial period of the training operation. Obviously, the time-domain echo response $\hat{h}$ will also vary so that the echo tail cannot be estimated correctly. This error will be passed back to the estimation of $\hat{H}$ via the FFT path in the receiver. This joint convergence between $\hat{H}$ and $\hat{h}$ makes the convergence rate slower.

Since the tail of the echo response should be very small and nearly zero due to the operation of the time-domain (TEQ) equaliser [6], we can force part of the echo tail to be zero during the initial training period, i.e. only use the main part of $\hat{h}$ and discard the tail since it is