Zero-Threshold-Voltage MOSFETs: A Survey

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***Abstract*—In this paper, we report an overview concerning zero-threshold-voltage MOS transistors and analyze the usefulness of this kind of transistor for low-voltage and low-power applications. Firstly, we compare the zero-V_T transistors to other two types os MOSFETs from the IBM 130-μm CMOS technology. Then simulation results and measured data are used to derive design insight into the use of zero-V_T devices, which in fact present a better overall performance for ultra-low supply voltages in comparison with low-threshold-voltage and standard MOSFETs in the same technology.**

I. Introduction

The threshold voltage is one of the most important parameters in MOS integrated circuits. The subject has been extensively studied and V_T-extraction methods have been proposed [1], [2]. The idea behind zero-V_T transistors has been introduced in the 90's [3], but their use is not so popular nowadays. Also the zero-threshold transistor has not received much attention from the scientific community and studies on this issue are quite scarse.

When the leakage contribution power in an active device equals the order of magnitude of the dynamic switching contribution power, the optimum power dissipation is achieved [4], which can be accomplished by the use of zero-V_T transistors. ALD110800 from Advanced Linear Devices is one example of low-cost zero-threshold transistor and has been used to implement ultra-low-voltage circuits, such as a Colpitts oscillator operating at a 20-mV supply voltage [5].

This paper aims to demystify the concepts related to zero-threshold MOS transistors, giving theoretical and practical insight for integrated circuit designers, who must be aware of the advantages of zero-V_T devices, which are very attractive for low-power and low-voltage applications. As the supply votage decreases down to levels below 300 mV, the performance of low-threshold and standard transistors is dramatically degraded, which does not occur for zero-threshold MOS transistors. As a consequence, the latter has a g_m/C_{ox} ratio higher than the others for ultra-low supply voltages.

This paper is organized as follows. In section II, the performance of three different types os transistors in the same technology is evaluated is a function of the supply voltage, showing the benefits and drawbacks for the use of zero-V_T MOSFETs. Finally, section III presents the main technological parameters of zero-threshold transistors, comparing simulated and measured data for IBM 0.13-μm CMOS devices.

II. Performance Comparison

It is well known that reduction in supply voltage is one of the most used strategies to lower power consumption, since the dynamic power consumption is proportional to V_{DD}^2 and the static power consumption is proportional to V_{DD} [6], [3].

However, lowering V_{DD} reduces the performance as well if standard devices are used. Therefore, a device that has a higher current drive capability at ultra-low-voltages is desired. Fig. 1 shows a comparison between the standard, low-V_T and zero-V_T transistors available in the 130-μm CMOS technology, with nominal threshold voltages of 340, 245 and 5 mV, respectively, for the minimum channel length in each case. Considering a gate voltage V_G eguals zero, the behavior of the drain current I_D as a function of the drain-to-source voltage V_{DS} indicates that the zero-V_T transistor presents a current level three orders of magnitude higher than the standard transistor under the same condition.

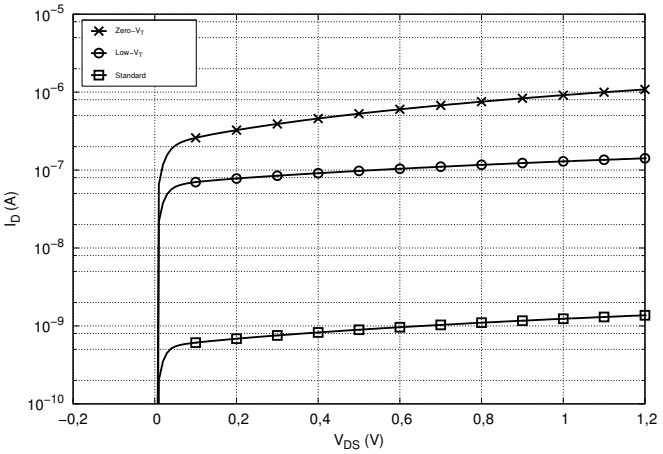

Fig. 1. I_D vs. V_{DS} for the standard, low-V_T and zero-V_T transistors with ($W/L = 3\mu m/0.42\mu m$).

In order to make a fair comparison by considering the minimum channel length available for each transistor, we have plotted the transconductance-to-gate capacitance ratio g_m/C_{ox}, which is also a measure of the device speed. Fig. 2 shows the large advantage of the zero-V_T over the low-V_T and standard transistors for supply voltages below 300 mV, in applications where a current drive capability or a higher frequency is necessary.

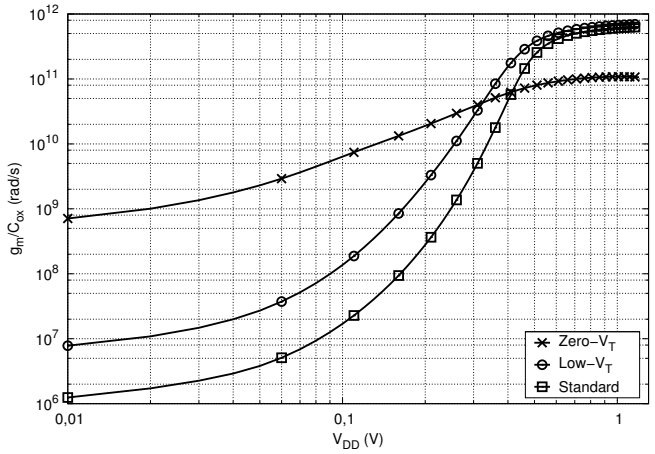

Fig. 2. Transconductance-to-capacitance ratio of the standard ($W/L = 0.84\mu$m $/0.12\mu$m), low-V_T ($W/L = 0.84\mu$m $/0.12\mu$m) and zero-VT ($W/L = 3\mu$m $/0.42\mu$m) transistors. The transconductance g_m was simulated for $V_S = V_B = 0$, and $V_D = V_G = V_{DD}$.

On the other hand, due to the second-order effects related to the fabrication process, the leakage current represents an important drawback of the zero-V_T transistor. However, for some applications, this constraint can be minimized by using back biasing in reverse mode [3].

III. Zero-V_T Parameter Extraction

This section introduces the simulations and measured results achieved to characterize the zero-V_T transistor. Simulations were performed using Cadence Design Kit for IBM 0.13-μm technology. The experimental set up was carried through the semiconductor parameter analyzer HP 4156C and using a device composed of 500 n-channel parallel-transistors (W=5μm and L=0.42μm).

Before extracting the zero-V_T parameters, simulations were performed to show I_D vs V_G for V_G ranging from -200 mV to 1.2 V, considering V_S=0 and V_D=13 mV, in order to find the specific current I_S and the equilibrium threshold voltage V_{T0} from transconductance-to-current ratio g_m/I_D. The circuit used to perform this simulation is presented in Fig. 3, where V_G and V_D are the gate and drain voltage, respectively.

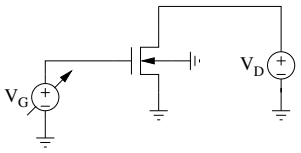

Fig. 3. Circuit used to perform zero-V_T parameter extraction.

Simulation results depicted in Fig. 4 were perfomed after parasitic extraction and one can observe that the flat level tends to take place for a value of current I_D approximately equal to 1 mA. As can be seen, simulation and experimental results agree quite well. From the g_m/I_D characteristic, V_{T0} can be taken as the value of V_G corresponding to the point where $g_m/I_D \cong 0.531 \times (g_m/I_D)_{max}$ [7] [1].

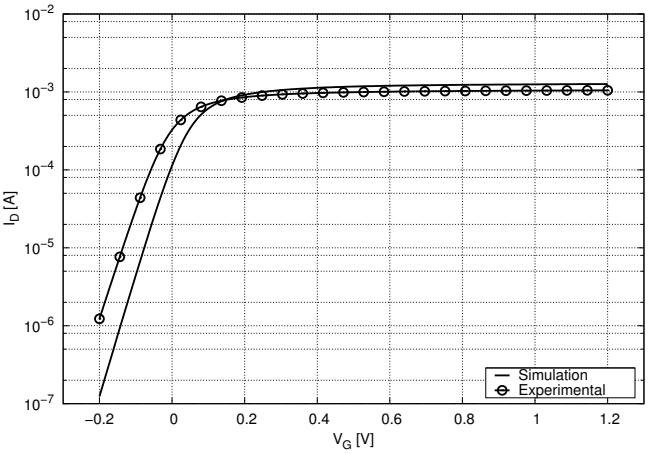

Fig. 4. I_D vs V_G performance for V_G = -200 mV to 1.2 V and V_D = 13mV.

Simulation results have shown a $0.531 \times (g_m/I_D)_{max} = 19.13V^{-1}$, which gives a value for the equilibrium threshold voltage of $V_{T0} = 73.1\ mV$.

The specific current I_S is the corresponding value of drain current for a gate voltage equal to the equilibrium threshold voltage V_{T0}. Again, from the I_D versus V_G characteristic, one can find a value of $I_S = 798\ \mu A$.

Experimental results have shown values for V_{T0} and I_S equal to -16 mV and 286 μA, respectively. Simulation and experimental results presented some deviation from each other probably because simulation did not take into account some parasitic effects such as series resistance.

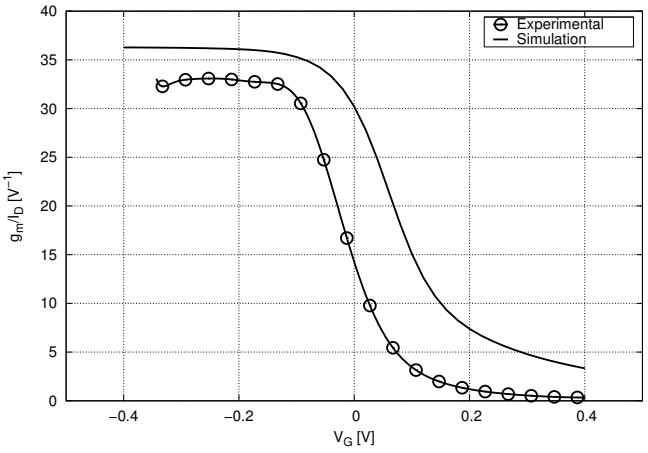

Fig. 5. g_m over I_D.

Following the parameter extraction, we have simulated I_D vs V_{DS} for V_G ranging from -100 mV to 100 mV in 25 mV steps and for $V_S = 0$ in order to better show weak inversion region.

Fig. 6 presents points for values of V_{DS} for which the ratio of the inversion charge density per unit area at the drain (q'_{ID}) to that at the source (q'_{IS}) (herein denoted by $\xi = q'_{ID}/q'_{IS}$

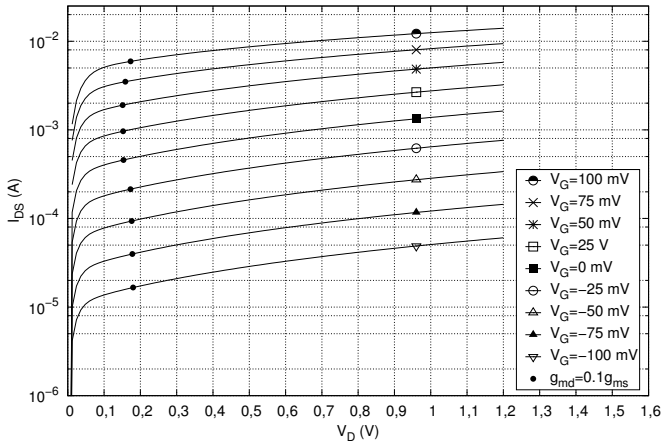

Fig. 6. I_D vs V_{DS} for V_G = -100 mV to 100 mV.

[7], which can also be defined as the g_{md}/g_{ms} ratio) is a value stipulated at 0.1 in order to set up a pratical criterion to determine the saturation condition.

This relation denotes that for values of $\xi \rightarrow 0$ the inversion charge per unit area at the drain is much lower than at the source, which means the current tends to saturate or, in other words, the saturation level tends to be maximum [7]. Moreover, we can notice that the zero-V_T transistor presents small values for ξ even for low values of V_{DS}, which indicates that this transistor may be useful in low-power applications.

A particular feature we have identified for negative values of gate voltage in our simulation results is that q'_{ID} characteristic has shown a gradual increase as V_{DS} becomes higher from a particular value.

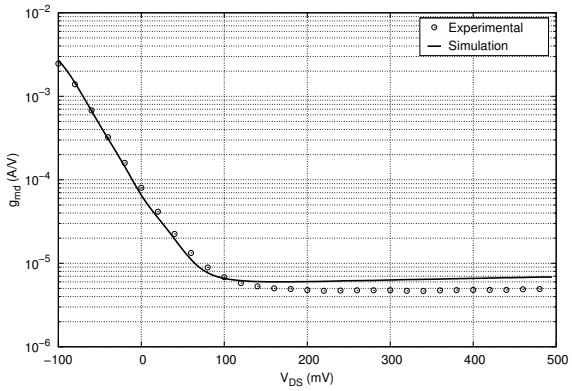

Fig. 7. Simulated and measured g_{md} as a function of V_{DS}.

This specific behavior has instigated the authors to perform a minute investigation on negative values of gate voltage and compare it with measured data. This comparison is depicted in Fig. 7. The gate voltage was -200 mV for the experimental curve and -125 mV for the simulation. The difference is due to fitting purposes. One can observe that the measured data denote that the specific behavior shown in simulation does not correspond to what actually happens.

As zero-V_T has become a fastidious device to model because of its undesirable features due to fabrication process (there is no halo- or pocket- implantation, so leakage currents and short-channel effects become more pronounced), the authors believe this atypical behavior is pronounced in simulation results due to a not perfect modeling of this device for the design kit.

Simulations for I_D vs V_{DS} for V_G ranging from 0V to 1.2 V in 100 mV steps and for $V_S = 0$ are presented in Fig. 8, in order to better show the strong inversion region.

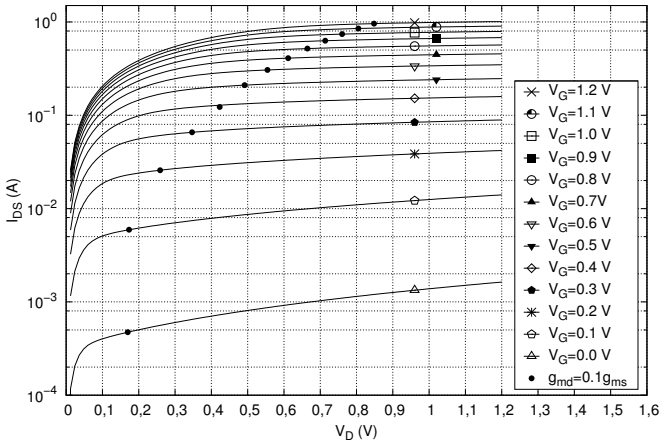

Fig. 8. I_D vs V_{DS} for V_G = 0 V to 1.2 V.

Another important figure of merit to obtaind in parameter extraction is the intrinsic transition frequency f_T, which is defined as the frequency at which the short-circuit current gain in the common-source configuration drops to 1 [7]. This parameter can be taken from the g_m/C_{gg} curve, where $C_{gg} = C_{gs} + C_{gb} + C_{gd}$. Fig. 9 presents the f_T versus the gate voltage.

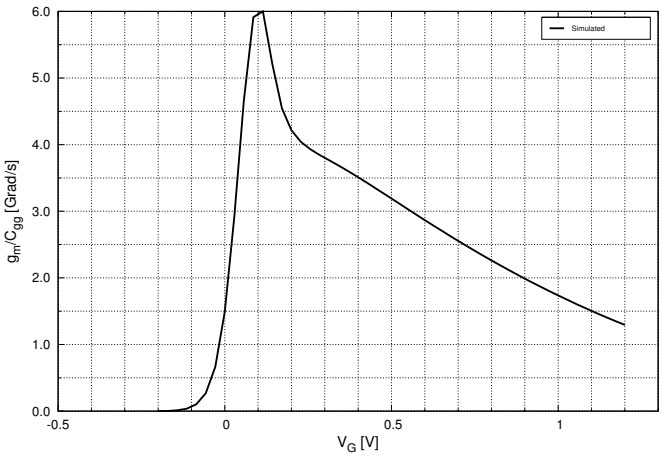

Fig. 9. The intrinsic transition frequency f_T.

A maximum intrinsic transition frequency (approximately 6 Grad/s) can be observed for V_G=100 mV, which again indicates that the zero-V_T transistor may be useful in low-power

and low-voltage applications. Finally, we present simulation results for V_S variation in terms of V_G for the circuit depicted in Fig. 10, in order to find the slope factor $n = (dV_S/dV_G)^{-1}$.

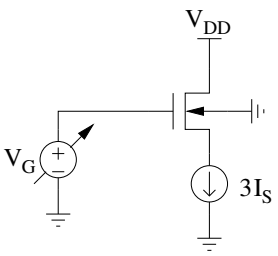

Fig. 10. Circuit used to extract the slope factor.

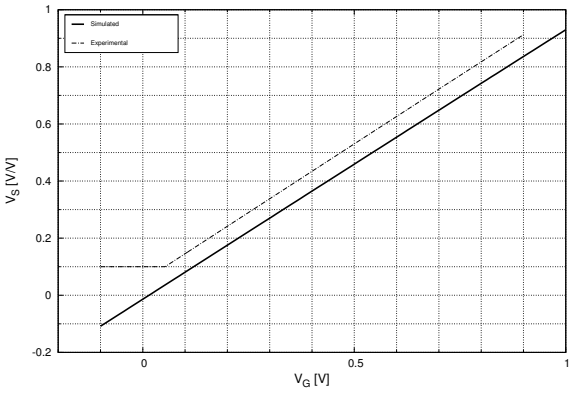

Fig. 11. Simulated and experimental V_S versus V_G.

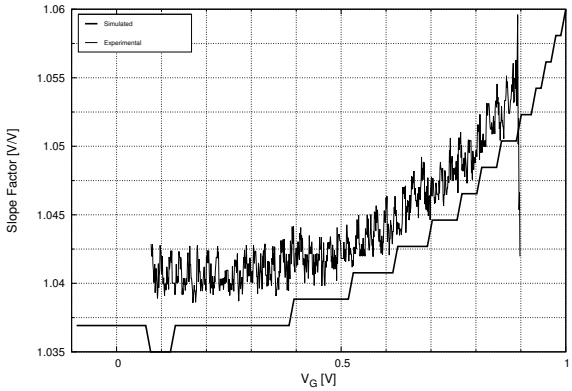

Fig. 12. Simulated and experimental slope factor results.

From the curves presented in Fig. 11 and 12, one can notice that the simulated results and experimental data have shown the same trend. Furthermore, both slope factors have shown a slightly variation around the unit value. This result can be observed in practice, since the zero-V_T is poorly doped, which makes this parameter not so much dependent on V_G variations. It should also be noted that the increasing behavior of the slope factor with V_G is probably due to short-channel effects.

IV. Conclusion

This paper presented a study about zero-threshold-voltage transistors, analyzing the different aspects on the capabilities of this type of transistor. The main goal of the analysis was to extract the main technological parameters of zero-V_T MOSFETs and show which applications are suitable for them. Simulation results and experimental measurements using IBM 0.13-μm CMOS technology indicate that this transistor presents a g_m/C_{ox} ratio higher than standard and low-threshold-voltage transistors for supply voltages below 300 mV, which means that zero-V_T MOS transistors are an excelent choice for analog and RF circuits in low-voltage and low-power applications.

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